NEW SAR ADC family

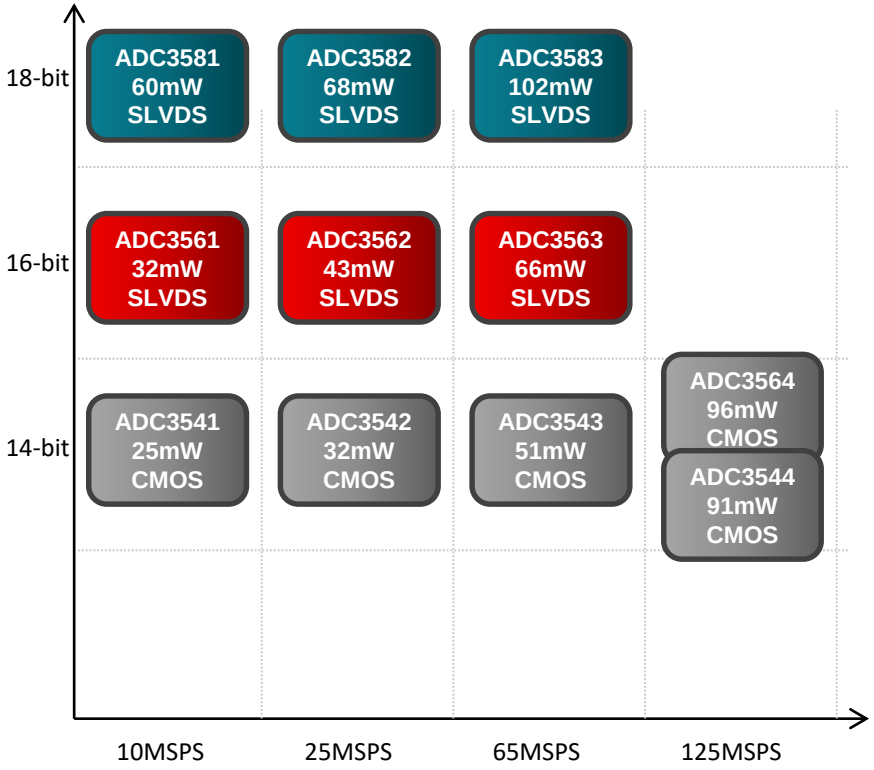
Single/Dual 14 bit 0.5 to 65 M/125MSPS
Single/Dual 16 bit 0.5 to 65 MSPS
Single/Dual 18 bit 0.5 to 65 MSPS

Worlds Highest Speed SAR ADCs

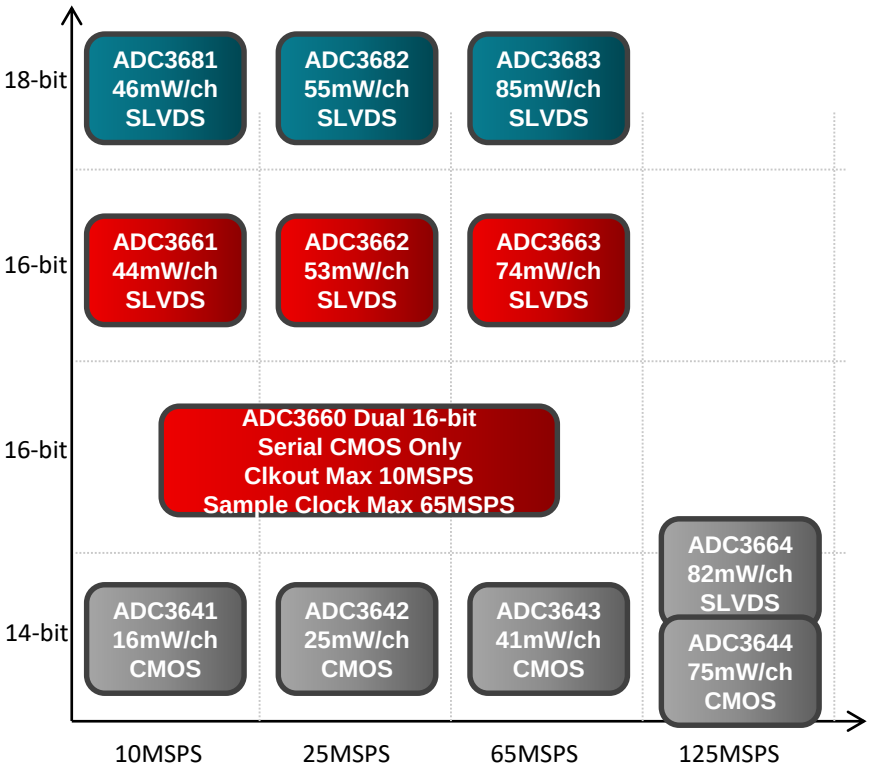
18 – bit 65MSPS (>4x faster than competition)
Industry leading SNR, SFDR, INL, DNL & Power Consumption
Integrated DDC (Digital Filter & Programmable NCO)

Q1 2021

Complete Family



ADC35XX – 1 CHANNEL ADCS



ADC36XX – 2 CHANNEL ADCS

ADC35/36 Single/Dual 14/16/18 Bit, 0.5MSPS to 125 MSPS

Features

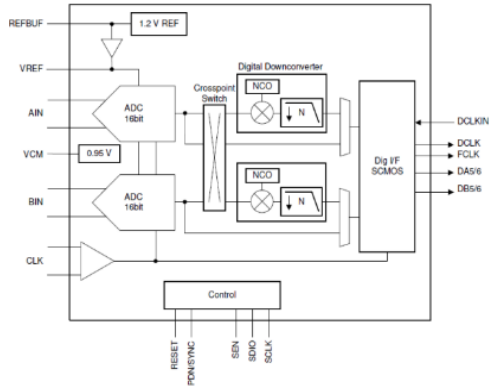
• Sample range:	0.5 – 65/125 MSPS (14 bit)
	0.5 – 65 MSPS (16/18 bit)
• Low Latency:	1 – 2 clock cycles
• Low Power:	29mW to 100mW per channel
• No missing codes	
• Input Bandwidth	900 MHz (up to 65MSPS)
	1400 MHz (125MSPS)
• Wake Up time	14 us
• INL/DNL	0.5/0.2, 2.0/0.2, 7/0.7 LSB
	(14/16/18bit typ)
• Reference options	Int and Ext 1.2/1.6V
• SNR	79/82/85 dB (14/16/18 bit)
• SFDR/THD	95dB at 1 MHz
• DDC	Decimation by 2, 4, 8, 16, 32
	32-bit NCO
• Digital Interface:	SDR/DDR CMOS & SLVDS
• Power supply:	1.8V (14/16/18 bit)
• Package:	40QFN (5x5mm)
• Low cost Sitara based reference design available in Q1 2021	

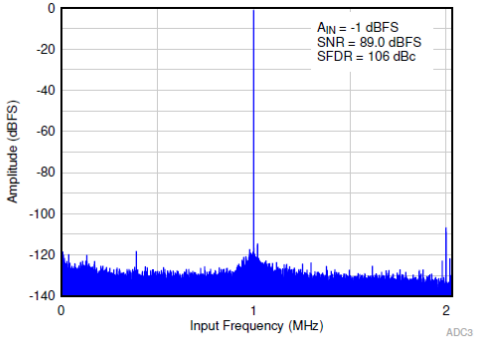
Applications

- Data Acquisition
- Power Quality Analyzer / meter
- Imaging (Thermal, MRI, PET)
- Ultrasonic Flow Metering
- Motor diagnostics & monitoring
- Sonar & Radar
- High-speed Control Loops
- OTDR
- Wireless Communicaitons

Key features

High dynamic range (85dB SNR, 95dB SFDR)
>90dB SNR, > 100dB SFDR (on chip 32x decimation)
Low power consumption 29mW to 100mW/ch
Excellent Linearity 0.2 LSB DNL, 0.5 LSB INL
Internal or external reference options
Programmable decimation and NCO
900MHz / 1400MHz (65/125MSPS) input bandwidth
1 – 2 clock cycle latency
CMOS or SLVDS interface
Single 1.8V power supply





FS = 65 MSPS, F_{in} = 1 MHz, 16x Decimation, real

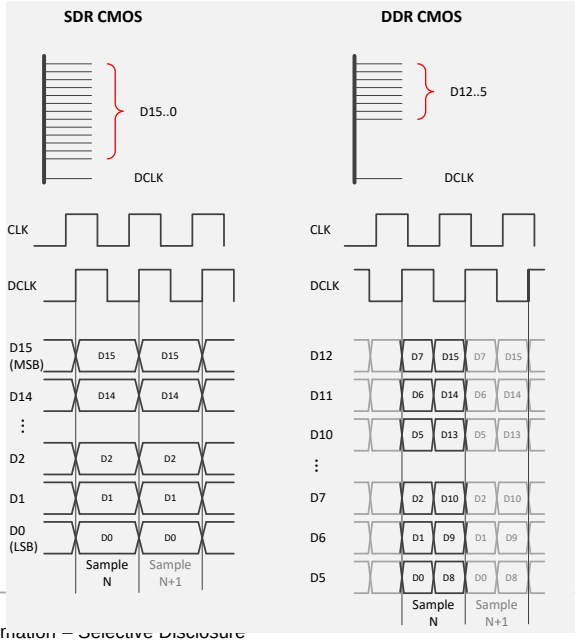
Complete Family – Key specs

Device	Resolution (bits)	Min Sample rate (MSPS)	Max Sample rate (MSPS)	Output Data rate (MSPS)	No. Of Channels	Input Bandwidth (MHz)	Interface	Power Consumption (mW)	NSD (dBFS/Hz)	SNR (dBFS)	SFDR (dBc)	INL (LSB)	DNL (LSB)	Latency (clock cycles)	Digital Filter	Input Range (Vp-p)	Voltage Reference	Supply Voltage (V)	Operating Temp Range	Package	Pin Compatibility	Status	Release Date
ADC3541	14	0.5	10	10	1	900	CMOS	36	-146	79	93	0,6	0,1	1	2, 4, 8, 16, 32X decimation. 32 bit NCO	2,25	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	March 21
ADC3641	14	0.5	10	10	2	900	CMOS	29/ch	-146	79	93	0,6	0,2	1	2, 4, 8, 16, 32X decimation. 32 bit NCO	2,25	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	March 21
ADC3542	14	0.5	25	25	1	900	CMOS	45	-151	79	93	0,6	0,1	1	2, 4, 8, 16, 32X decimation. 32 bit NCO	2,25	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	March 21
ADC3642	14	0.5	25	25	2	900	CMOS	35/ch	-151	79	93	0,6	0,2	1	2, 4, 8, 16, 32X decimation. 32 bit NCO	2,25	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	March 21
ADC3543	14	0.5	65	65	1	900	CMOS	79	-155	79	93	0,5	0,2	1	2, 4, 8, 16, 32X decimation. 32 bit NCO	2,25	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	March 21
ADC3643	14	0.5	65	65	2	900	CMOS	72/ch	-155	79	93	0,6	0,2	1	2, 4, 8, 16, 32X decimation. 32 bit NCO	2,25	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	Released
ADC3544	14	0.5	125	125	1	1400	CMOS	91	-153	74	90	1,5	0,5	1	2, 4, 8, 16, 32X decimation. 32 bit NCO	2,25	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	May 21
ADC3644	14	0.5	125	125	2	1400	CMOS	80/ch	-153	74	90	1,5	0,5	1	2, 4, 8, 16, 32X decimation. 32 bit NCO	2,25	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	May 21
ADC3564	14	0.5	125	125	1	1400	SLVDS	137	-156	77.5	85	1,5	0,5	1	2, 4, 8, 16, 32X decimation. 32 bit NCO	3,2	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	March 21
ADC3664	14	0.5	125	125	2	1400	SLVDS	100/ch	-156	77.5	85	1,5	0,5	1	2, 4, 8, 16, 32X decimation. 32 bit NCO	3,2	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	Released
ADC3561	16	0.5	10	10	1	900	SLVDS	76	-150	82	90	2	0,2	2	2, 4, 8, 16, 32X decimation. 32 bit NCO	3,2	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	May 21
ADC3661	16	0.5	10	10	2	900	SLVDS	50/ch	-150	82	90	2	0,2	2	2, 4, 8, 16, 32X decimation. 32 bit NCO	3,2	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	May 21
ADC3562	16	0.5	25	25	1	900	SLVDS	83	-154	82	90	2	0,2	2	2, 4, 8, 16, 32X decimation. 32 bit NCO	3,2	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	May 21
ADC3662	16	0.5	25	25	2	900	SLVDS	60/ch	-154	82	90	2	0,2	2	2, 4, 8, 16, 32X decimation. 32 bit NCO	3,2	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	Mar 21
ADC3563	16	0.5	65	65	1	900	SLVDS	119	-158	82	90	2	0,2	2	2, 4, 8, 16, 32X decimation. 32 bit NCO	3,2	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	Mar 21
ADC3663	16	0.5	65	65	2	900	SLVDS	95/ch	-158	82	90	2	0,2	2	2, 4, 8, 16, 32X decimation. 32 bit NCO	3,2	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	Released
ADC3660	16	0.5	65	31	2	900	CMOS	71/ch	-159	82	90	2	0,2	1	2, 4, 8, 16, 32X decimation. 32 bit NCO	3,2	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Released	Released
ADC3581	18	0.5	10	10	1	900	SLVDS	76	-153	85	95	7	0,7	2	2, 4, 8, 16, 32X decimation. 32 bit NCO	3,2	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	May 21
ADC3681	18	0.5	10	10	2	900	SLVDS	50/ch	-153	85	95	7	0,7	2	2, 4, 8, 16, 32X decimation. 32 bit NCO	3,2	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	Mar 21
ADC3582	18	0.5	25	25	1	900	SLVDS	83	-157	85	95	7	0,7	2	2, 4, 8, 16, 32X decimation. 32 bit NCO	3,2	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	May 21
ADC3682	18	0.5	25	25	2	900	SLVDS	60/ch	-157	85	95	7	0,7	2	2, 4, 8, 16, 32X decimation. 32 bit NCO	3,2	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	March 21
ADC3583	18	0.5	65	65	1	900	SLVDS	119	-161	85	95	7	0,7	2	2, 4, 8, 16, 32X decimation. 32 bit NCO	3,2	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	Released
ADC3683	18	0.5	65	65	2	900	SLVDS	95/ch	-161	85	95	7	0,7	2	2, 4, 8, 16, 32X decimation. 32 bit NCO	3,2	INT & EXT 1,2 & 1,6V	1,80	–40 to +105ºC	40-pin WQFN package (5 x 5mm)	✓	Sampling	Released

Digital Interface Options

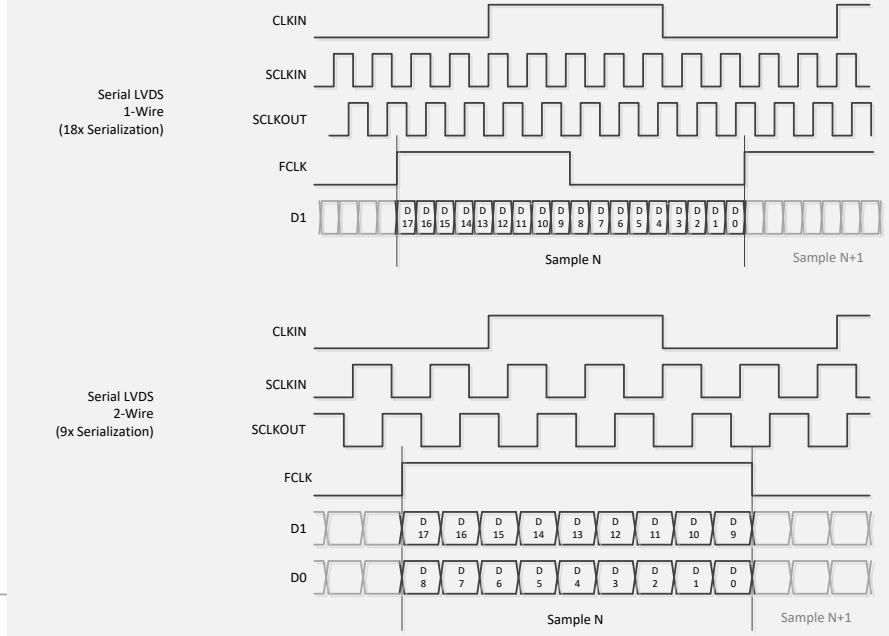
Single ended CMOS (example)

CMOS Interface	ADC Sampling Rate	DCLK	FCLK	Dout
SDR CMOS	65Msps	65Msps	-	65Msps
DDR CMOS	65Msps	65Msps	-	130Msps



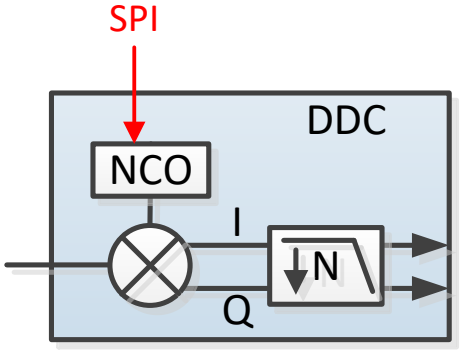
Serial LVDS (example)

CMOS Interface	ADC Sampling Rate	FCLK Rate	SCLKIN	SCLKOUT	D0/D1
1 wire SLVDS	32.5Msps	32.5Msps	292.5Msps	292.5Msps	585Msps
2 wire SLVDS	65Msps	32.5Msps	292.5Msps	292.5Msps	585Msps

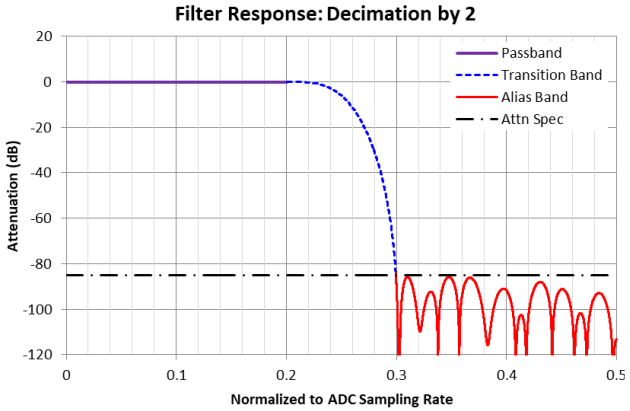


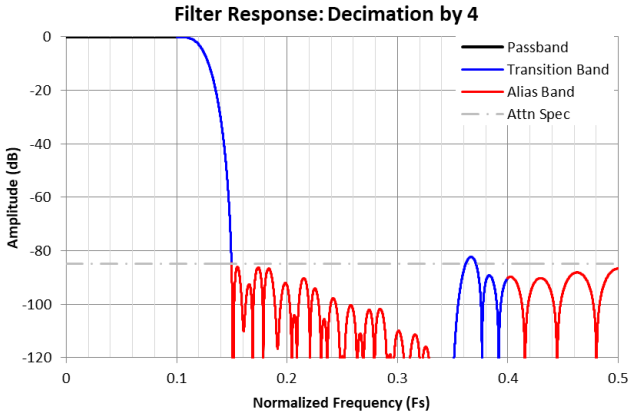
Internal Decimation Filter

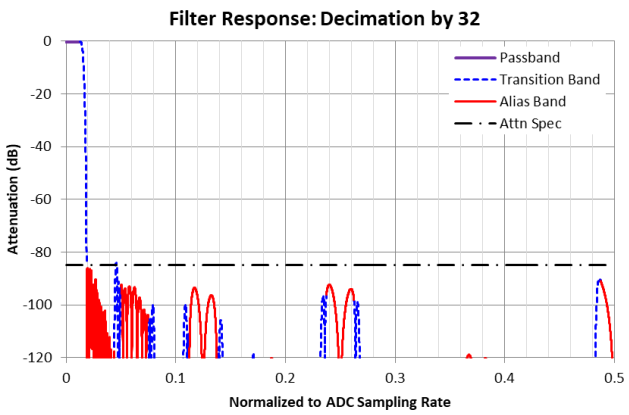
- Complex Decimation by 2, 4, 8, 16 and 32
- 32-bit NCO: Frequency Resolution
- Supports real output decimation w/o NCO
  - 2, 4, 8, 16, 32 decimation
- Passband: ~42%
- Stopband attenuation ~ 85dB min

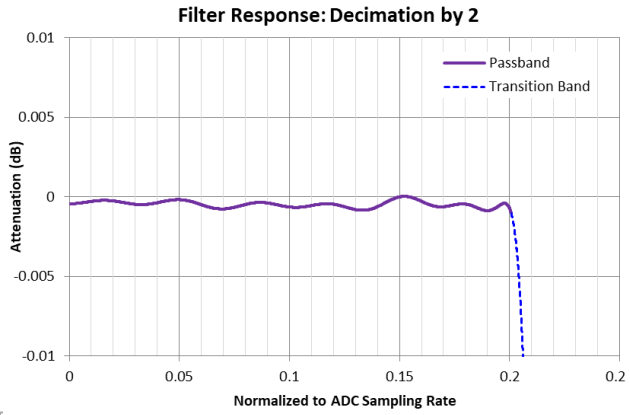


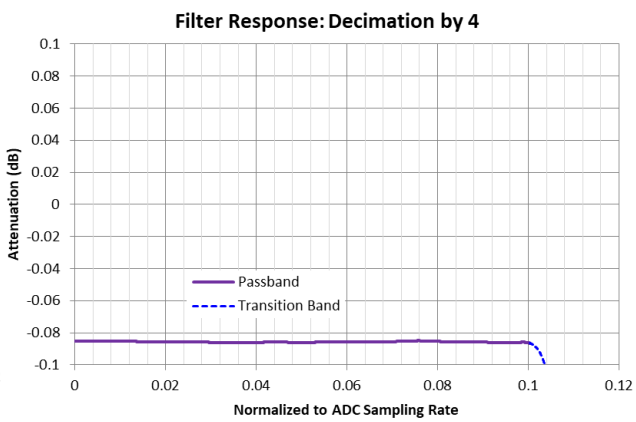
Decimation Filter Response (/2, /4 and /32 examples)

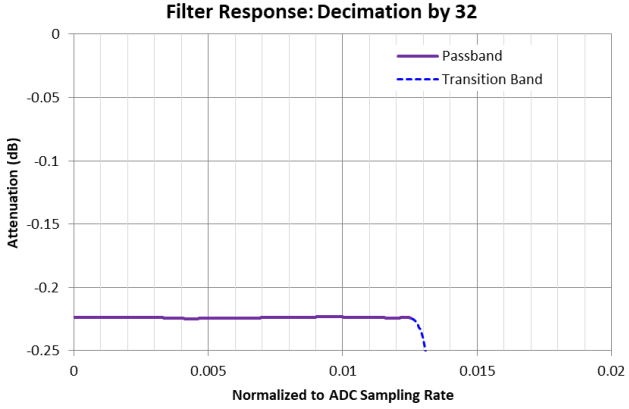








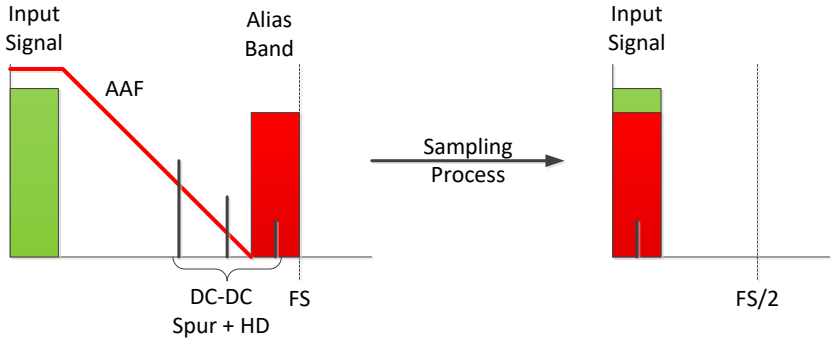


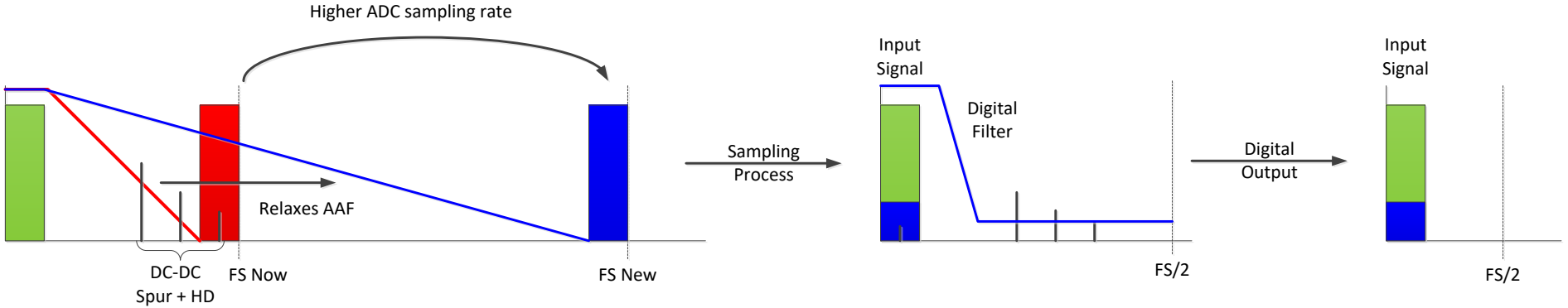


Faster SAR ADC Sampling Rate

Faster ADC sampling rate:

- Relaxes AAF filter requirements
- Reduces susceptibility to power supply spurs/noise inside ADC



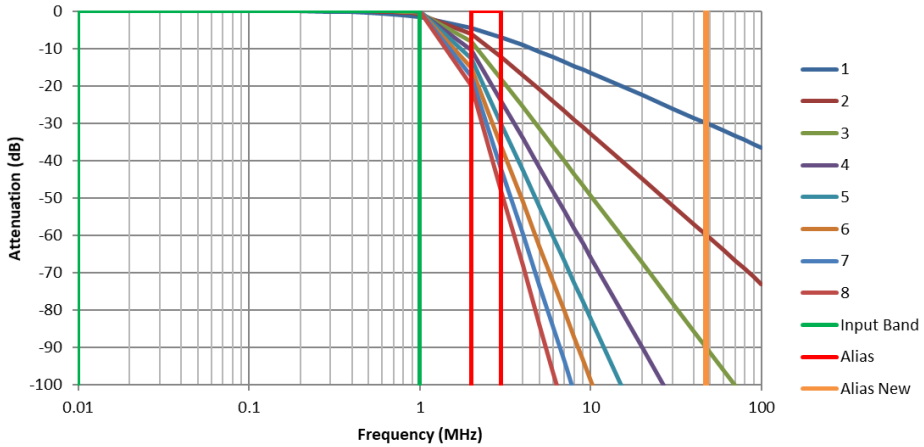


Oversample + Decimate Configuration

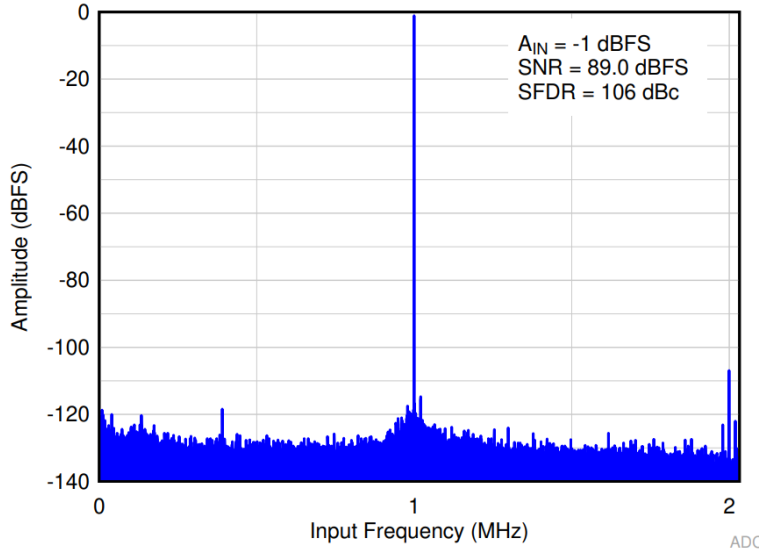
Operate ADC at a faster clock rate and use internal digital decimation

- Relaxes external anti alias filter
- Improves SNR (3dB/2x decimation)
- Reduces output data rate

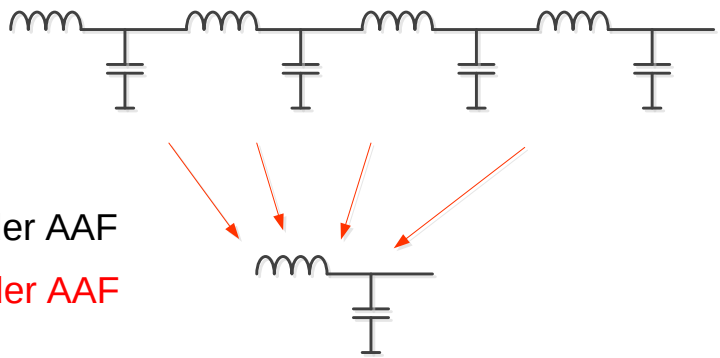
$F_{S,old}$ = 3 MSPS: Alias at 2-3MHz => heavy filter
$F_{S,new}$ = 24 or 48 MSPS: Alias at 23/47MHz => relaxed filter



FS = 65 MSPS, FIN = 1.0 MHz, 16x Decimation



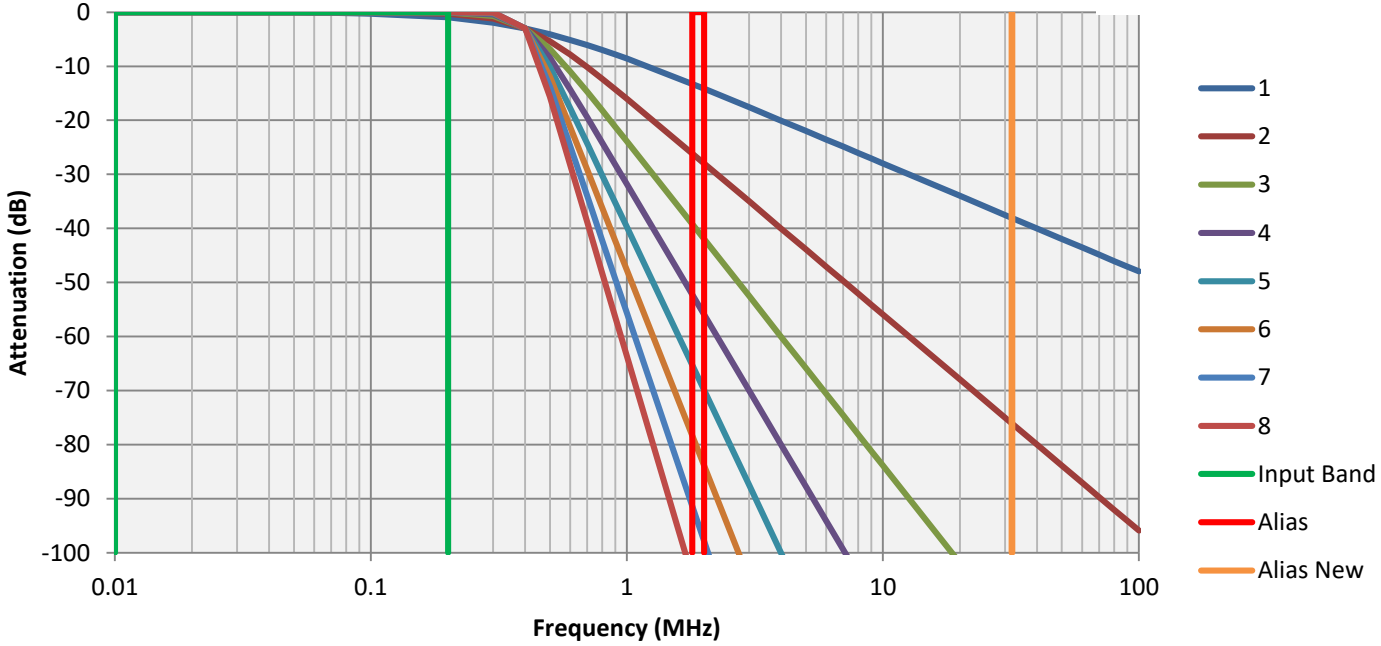
AAF Filter relaxation



Fin = 0-200kHz

Fs = 2Msps => Alias = 1.8-2MHz => requires 8th order AAF

Fs_{New} = 32Msps => Alias = 31.8-32MHz => requires 3rd order AAF



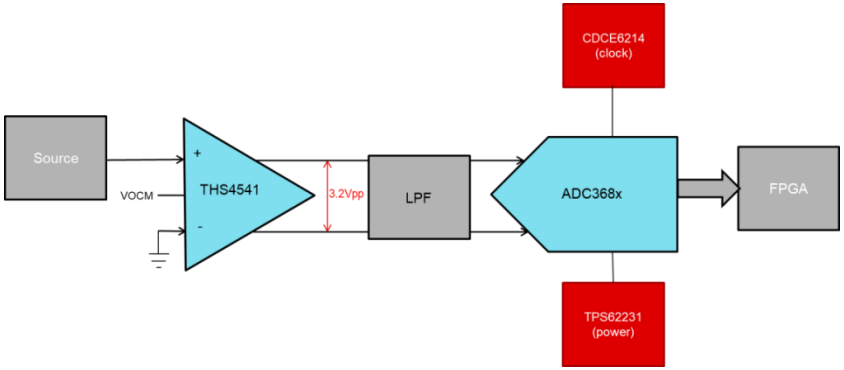
Evaluation tools (EVMs)

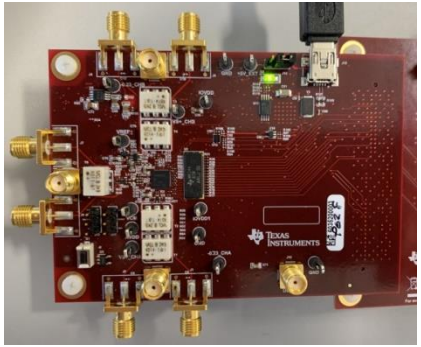
ADC3683EVM - Industries Fastest 18-bit Digitizer – Dual 18 bit 65MSPS

Exceptional SNR & SFDR at Ultra Low Power Consumption

Features

- **Sample range:** **0.5 – 65 MSPS (18 bit)**
- Input driver options: AC coupled through ADT1-6T+ (125MHz BW)
  - Supports SE to DIFF or DIFF to DIFF conversion
  - DC coupled through THS4541 (20 MHz BW)
  - Supports SE to DIFF or DIFF to DIFF conversion
  - 0V to 3.2V p-p input range
- **ADC Voltage Reference options:** **Internal 1.2/1.6V (lowest cost)**
  - **External 1.2/1.6V (highest performance)**
- Time doman applications: DC coupled FDA input (0Hz to 20MHz)
- Freq domain applications: AC coupled transformer input (30kHz to 125MHz)
- **Clocking options** **On board clock (350fs jitter typical)**
  - **Option to connect external clock (<350fs clock jitter)**
- Low Power consumption: 95mW/ch (ADC)
  - 800mW (Complete Digitizer)
- **Low Latency for control loop applications:** **2 clock cycles (30.77ns at 65MSPS)**
- Signal Chain SNR @ 1MHz fin: 85 dB (Nyquist) – transformer/FDA input
  - Includes input driver, onboard clock & INT voltage reference: 9x dB (32x decimation) – transformer/FDA
- **Signal Chain SFDR @ 1MHz fin** **95 dB (transformer/FDA)**
  - Includes input driver, onboard clock & INT voltage reference: **10x dB (32x decimation) – transformer)/FDA**
- ADC INL, DNL: 7 LSB, 0.7 LSB (typ)
- **Digital Interface:** **SLVDS (ADC)**
  - **FMC connector (Digitizer)**
- Power supply ADC/Board: 1.8V/5V
- **Operating Temperature:** **-40 to +105degC**
- Design files: Schematics & gerber files available on ti.com





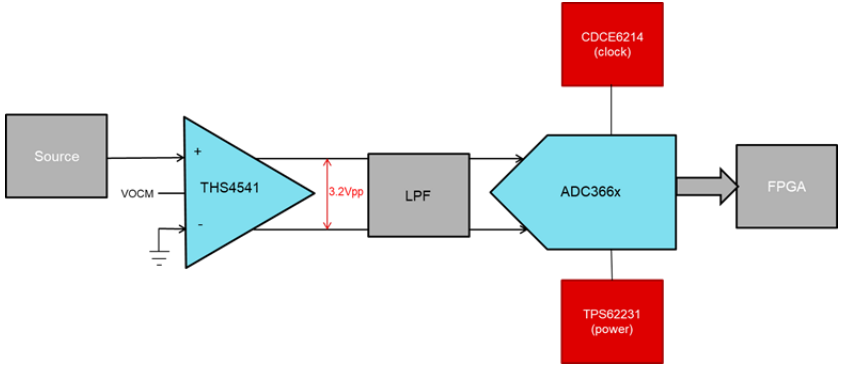
Target Applications
Data Acquisition
Power Analyzer
Sonar
Radar
Optical Encoders
Control Loops
Imaging (MRI, Xray, PET)
Flow Metering (Ultrasonic)

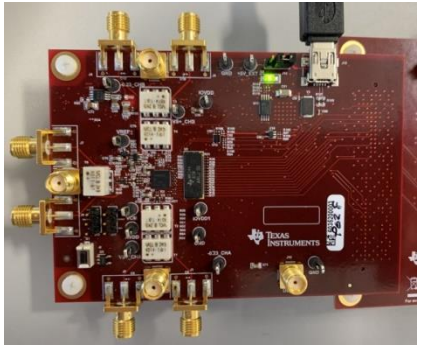
High dynamic range, low power, 16-bit Dual channel 65MSPS Digitizer

>90db SNR, 108dB SFDR @ 95mW/Ch (ADC3660/61/62/63EVM)

Features

• **Sample range:**	**0.5 – 65 MSPS (16 bit)**
• Input driver options:	AC coupled through ADT1-6T+ (125MHz BW)
	Supports SE to DIFF or DIFF to DIFF conversion
	DC coupled through THS4541 (20 MHz BW)
	Supports SE to DIFF or DIFF to DIFF conversion
	0V to 3.2V p-p input range
• **ADC Voltage Reference options:**	**Internal 1.2/1.6V (lowest cost)**
	External 1.2/1.6V (highest performance)
• Time doman applications	DC coupled FDA input (0Hz to 20MHz)
• Freq domain applications	AC coupled transformer input (30kHz to 125MHz)
• **Clocking options**	**On board clock (350fs jitter typical)**
	Option to connect external clock (<350fs clock jitter)
• Low Power consumption:	95mW/ch (ADC)
	800mW (Complete Digitizer)
• **Low Latency for control loop applications:**	**2 clock cycles (32ns at 62.5MSPS)**
• Signal Chain SNR @ 1MHz fin	82 dB (Nyquist) – transformer/FDA input
Includes input driver, onboard clock & INT voltage reference	90.7 dB (32x decimation) – transformer/FDA
• **Signal Chain SFDR @ 1MHz fin**	**90 dB (transformer/FDA)**
Includes input driver, onboard clock & INT voltage reference	**108 dB (32x decimation) – transformer)/FDA**
• ADC INL, DNL	2 LSB, 0.2 LSB (typ)
• **Digital Interface:**	**CMOS, SLVDS (ADC)**
	FMC connector (Digitizer)
• Power supply ADC/Board:	1.8V/5V
• **Operating Temperature:**	**-40 to +105degC**
• Design files:	Schematics & gerber files available on ti.com





Target Applications
Data Acquisition
Power Analyzer
Sonar
Radar
Optical Encoders
Control Loops
Imaging (Xray, Thermal, MRI)
Flow Metering (Ultrasonic)

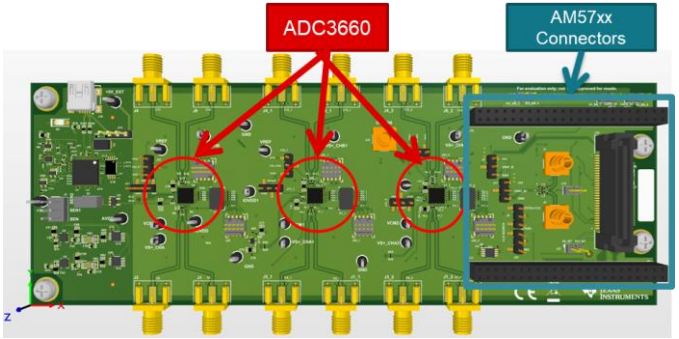
High dynamic range, 16-bit 6 - CH Digitizer interfaces to TI Sitara Processor

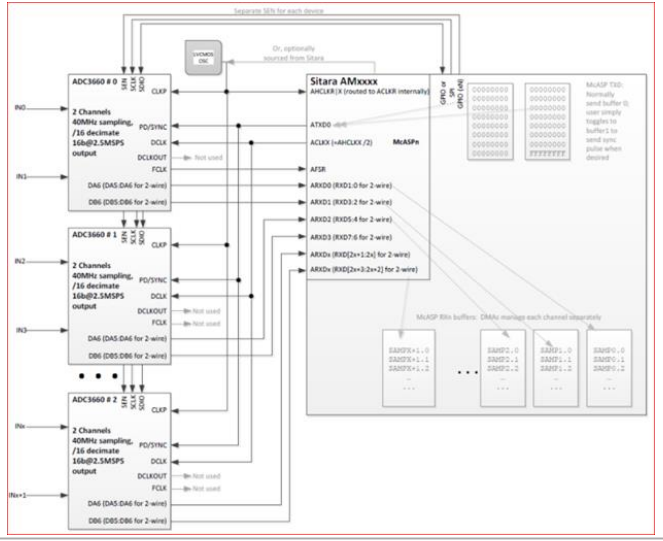
Exceptional SNR & SFDR @ 71mW/Ch (ADC3660)

Features

- ADC3660 paired with the AM57xx (Beagle Bone AI) utilizing McASP interface.
- Can support 3 synchronized ADC3660s with max data rate of 50 Mbps.
- Expected release in Q1 2021.

Sample range:	0.5 – 10 MSPS (16 bit) Max data rate of 50Mbps
Input driver options:	DC coupled through THS4541 (20 MHz BW) Supports SE to DIFF or DIFF to DIFF conversion 0V to 3.2V p-p input range
ADC Voltage Reference options:	Internal 1.2/1.6V (lowest cost) External 1.2/1.6V (highest performance)
Time doman applications	DC coupled FDA input (0Hz to 20MHz)
Clocking options	On board clock (350fs jitter typical) Option to connect external clock (<350fs clock jitter)
Low Power consumption:	71mW/ch (ADC) 800mW (Complete Digitizer)
Low Latency:	2 clock cycles
Signal Chain SNR @ 1MHz fin Includes input driver, onboard clock & INT voltage reference	82 dB (Nyquist) – transformer/FDA input X? dB (32x decimation) – transformer/FDA
Signal Chain SFDR @ 1MHz fin Includes input driver, onboard clock & INT voltage reference	90 dB X? dB (32x decimation)
ADC INL, DNL	2 LSB, 0.2 LSB (typ)
Digital Interface:	CMOS (ADC) connector (Digitizer)
Power supply ADC/Board:	1.8V/5V
Operating Temperature:	-40 to +105degC
Design files:	Schematics & gerber files available (Q1 2021) on ti.com



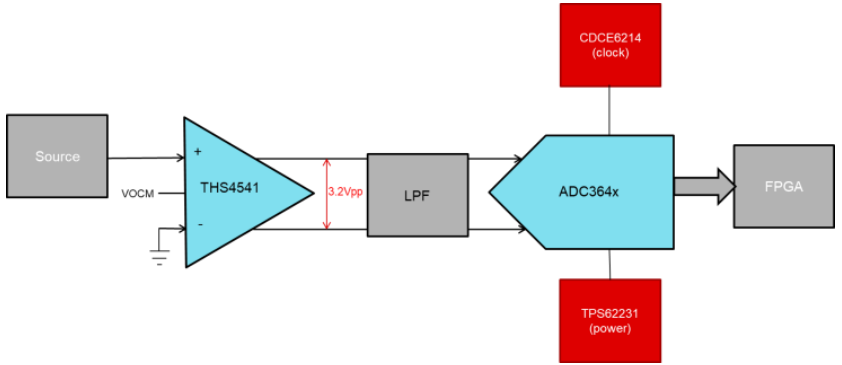


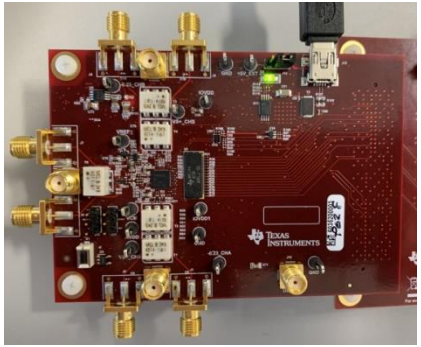
14-bit Digitizer with industry leading INL, DNL and SNR

Dual channel 14-bit 0.5 to 125MSPS (ADC3641/2/3/4EVM)

Features

- **Sample range:** **0.5 – 125 MSPS (14 bit)**
- Input driver options: AC coupled through ADT1-6T+ (125MHz BW)
  - Supports SE to DIFF or DIFF to DIFF conversion
  - DC coupled through THS4541 (20 MHz BW)
  - Supports SE to DIFF or DIFF to DIFF conversion
  - 0V to 2.25V p-p input range
- **ADC Voltage Reference options:** **Internal 1.2/1.6V (lowest cost)**
  - **External 1.2/1.6V (highest performance)**
- Time doman applications: DC coupled FDA input (0Hz to 20MHz)
- Freq domain applications: AC coupled transformer input (30kHz to 125MHz)
- **Clocking options** **On board clock (350fs jitter typical)**
  - **Option to connect external clock (<350fs clock jitter)**
- Low Power consumption: 80mW/Ch (ADC @ 125MSPS)
  - 800mW (Complete Digitizer)
- **Low Latency for control loop applications:** **1 clock cycle (8ns at 125MSPS)**
- Signal Chain SNR @ 1MHz fin: 79 dB (Nyquist) – transformer/FDA input
  - Includes input driver, onboard clock & INT voltage reference: 9x? dB (32x decimation) – transformer/FDA
- **Signal Chain SFDR @ 1MHz fin** **93 dB (transformer/FDA)**
  - **Includes input driver, onboard clock & INT voltage reference** **10x? dB (32x decimation) – transformer)/FDA**
- ADC INL, DNL: 0.6 LSB, 0.2 LSB (typ @ 65MSPS)
- **Digital Interface:** **CMOS (ADC)**
  - **FMC connector (Digitizer)**
- Power supply ADC/Board: 1.8V/5V
- **Operating Temperature:** **-40 to +105degC**
- Design files: Schematics & gerber files available on ti.com



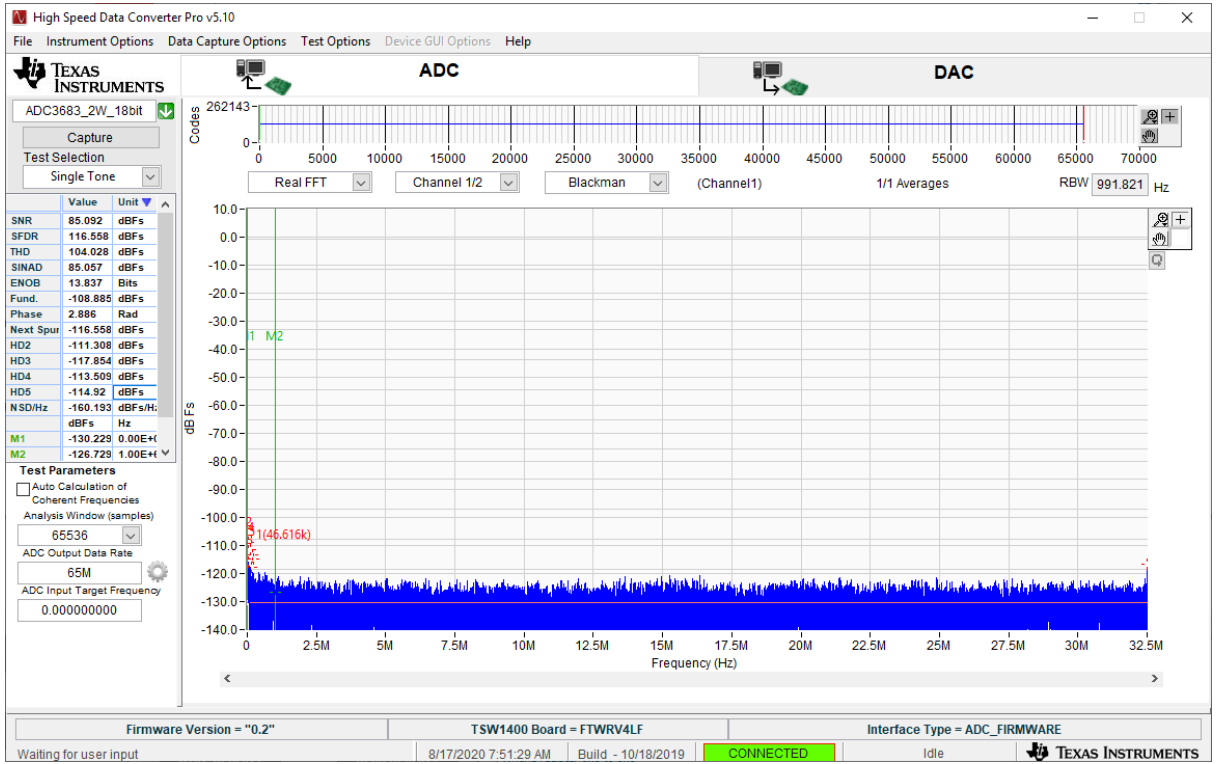


Target Applications
Thermal Imaging
Data Acquisition
Flow Metering (Ultrasonic)
Control Loops
Imaging (MRI, Xray, PET)
Sonar
Radar
Communications

EVM measurements

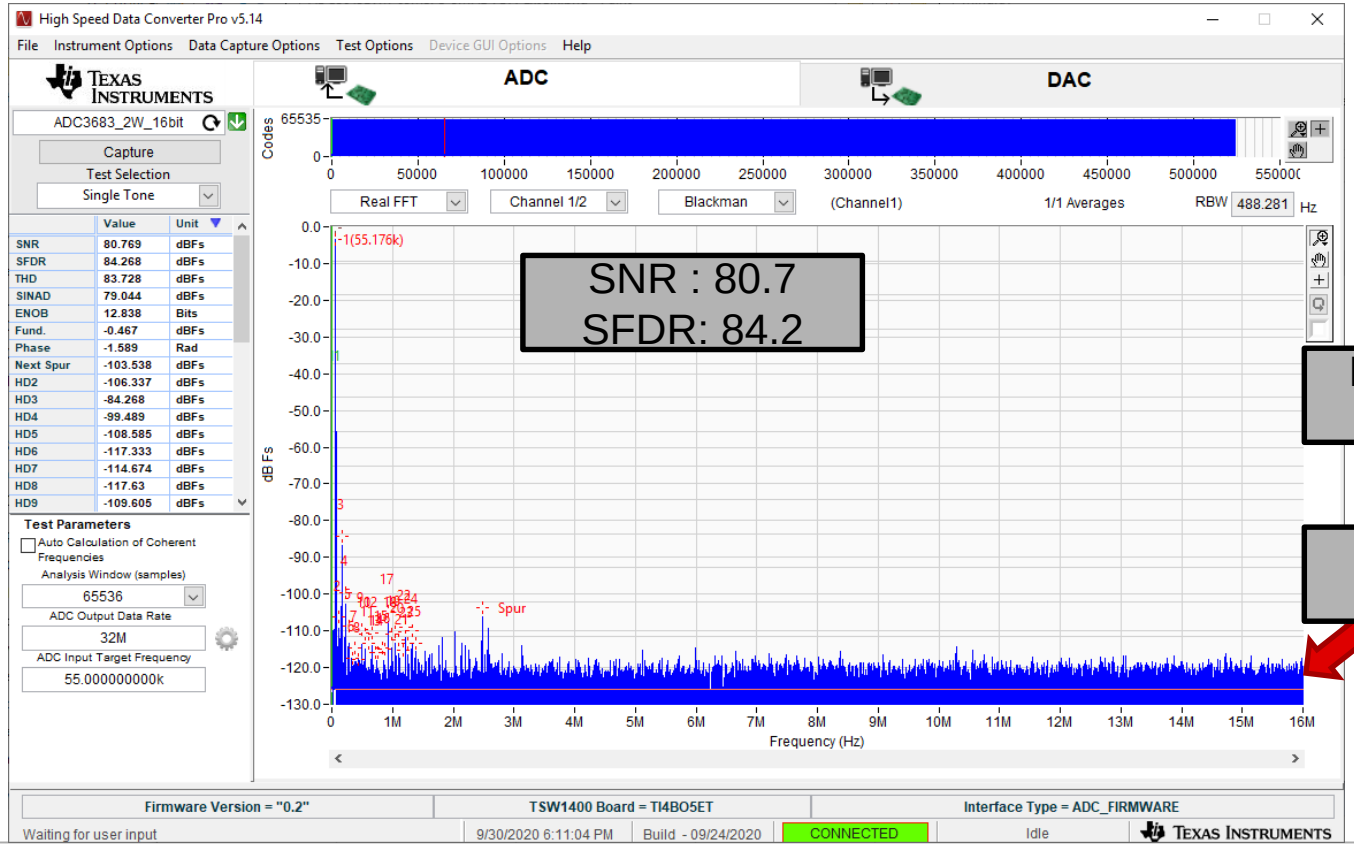
ADC3583

- 18-bit noise floor of -160dBFS

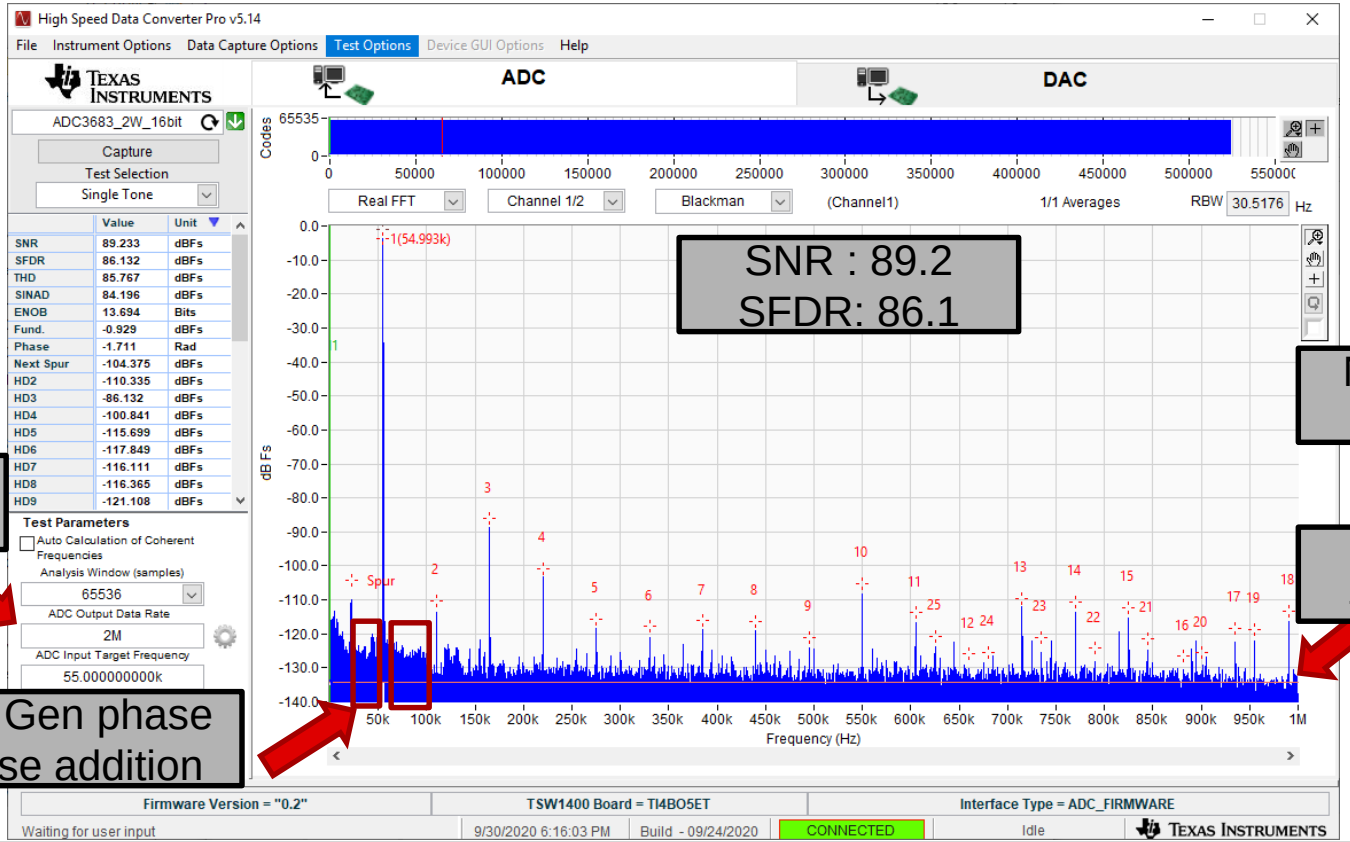


SNR: 85 dBFS
SFDR: 116 dBFS
NSD better than 160dbFS/Hz!

ADC3683EVM 32 MSPS: Bypass, 55KHz Fin



ADC3683EVM 32 MSPS: Decimation by 16, 55KHz Fin



Lower data rate

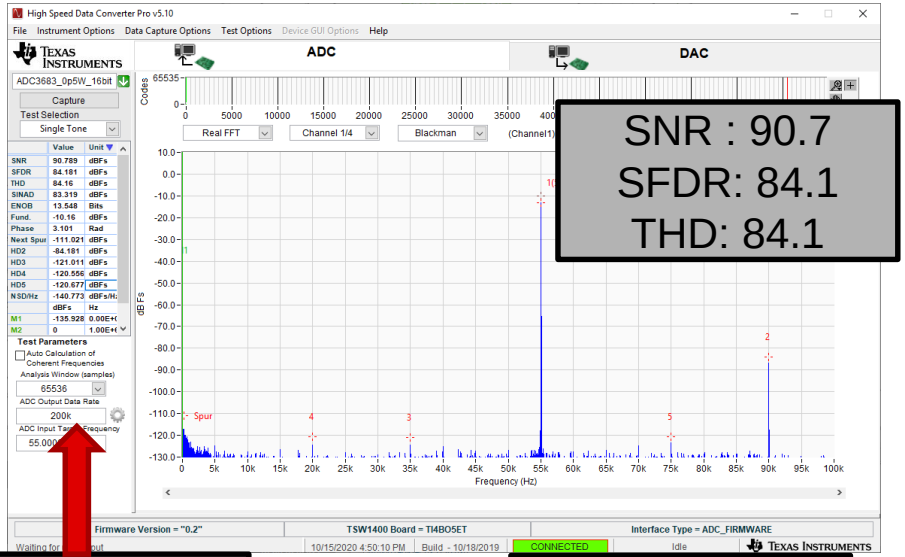
Sig Gen phase noise addition

Nyquist Zone 1 MHz

Noise Floor ~ -130 dBFS

ADC3683EVM 6.4 MSPS, 32x Decimation, 55KHz Fin

No Filter

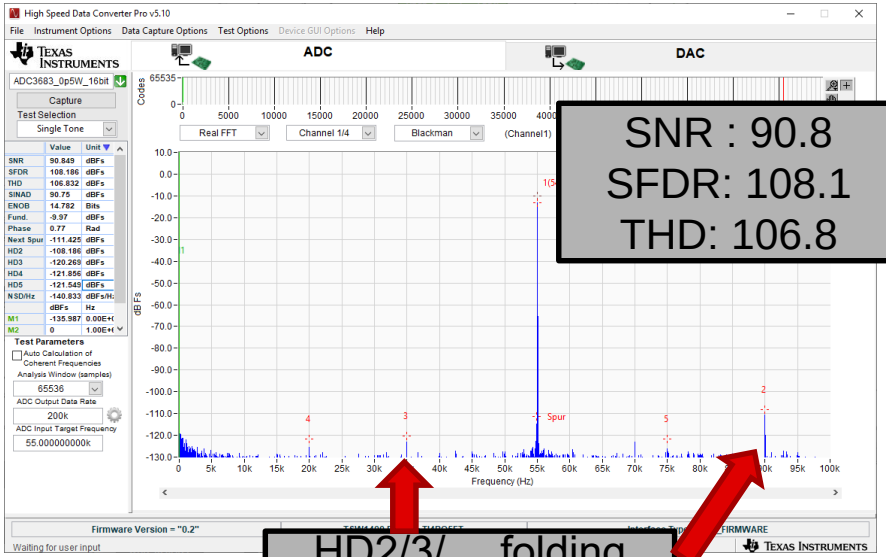


SNR : 90.7
SFDR: 84.1
THD: 84.1

Much lower data rate

Nyquist Zone 100 kHz

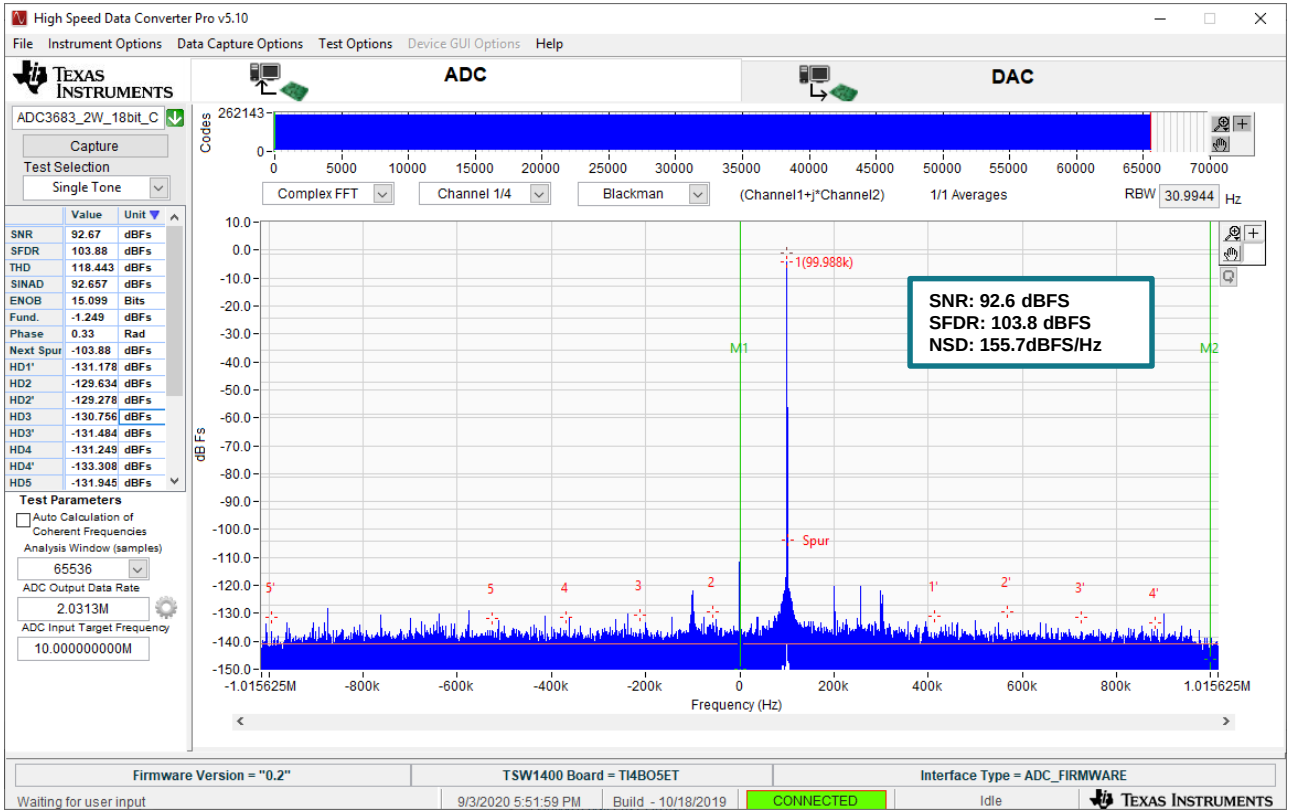
100 kHz LPF



SNR : 90.8
SFDR: 108.1
THD: 106.8

HD2/3/… folding back into Nyquist Zone

ADC3683EVM – 18bit, 65MSPS, 32x Decimation, 10 MHz, Ain = -1.25dBFS



ADC3683EVM – 18bit, 65MSPS, 32x, Idle Channel