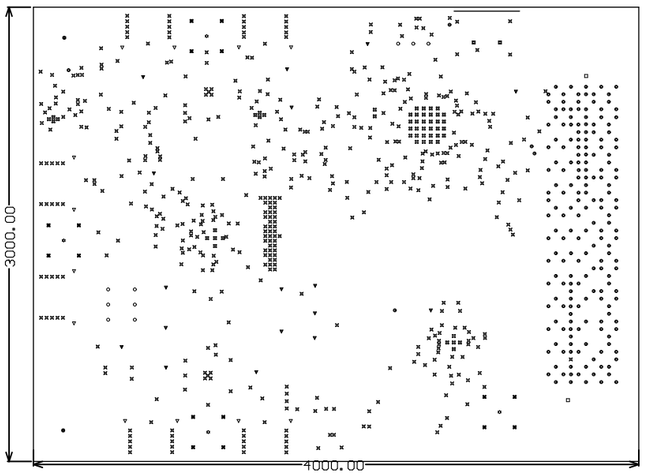
NOTE:

1. 17 MIL TRACES ON L1 AND L6 LAYER ARE 50 OHMS +/- 10%
2. ALL VIA HOLES NEED TO BE TENTED ON TOP AND BOTTOM SIDE.
3. VIA HOLES UNDER IC U2 NEED TO BE FILLED WITH SOLDER MASK TO PREVENT SOLDER PASTE FLOW INTO VIAS.
4. 4.4 MIL WIDTH DIFFERENTIAL TRACES ON LAYER 3 100 OHMs +/- 10%.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.50mil	3.5	
1	L1_Top Layer		1.40mil		
	Dielectric 1		8.50mil	4.7	
2	L2_GND1		1.40mil		
	Dielectric 2		14.00mil	4.7	
3	L3_Signal		1.40mil		
	Dielectric 3		8.50mil	4.7	
4	L4_Plane		1.40mil		
	Dielectric 4		14.00mil	4.7	
5	L5_GND2		1.40mil		
	Dielectric 5		8.50mil	4.7	
6	L6_Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.50mil	3.5	
	Bottom Overlay				



Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Routed Path Length	Hole Length	Drill Layer Pair	Tolerance
	2	35.43mil (0.900mm)	NPTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
	2	50.00mil (1.270mm)	NPTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
	52	7.87mil (0.200mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	+/- 3 mil
	513	8.00mil (0.203mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
	191	10.00mil (0.254mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	+/- 3 mil
	12	18.00mil (0.457mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
	9	35.00mil (0.889mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
	4	59.06mil (1.500mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
	17	63.00mil (1.600mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	+/- 3 mil
	16	66.93mil (1.700mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
	2	125.98mil (3.200mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
	820 Total							

1000.00mil

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 5 mil
MIN. VIA PAD SIZE: 18 MIL
MINIMUM ANNULAR RING IPC Class 2 specifications
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☐ FR-4 High Tg ☒ OTHER 370HR
THICKNESS: ☒ 62 MIL +/-10% ☐ OTHER
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER
SOLDER RESIST COLOR: ☐ GREEN ☒ OTHER RED
☐ MATTE ☒ SEMI-GLOSS
SURFACE FINISH: ☐ IMMERSION GOLD (ENIG) ☒ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER
ARRAY/PANEL: ☒ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☐ V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: ADC3644 EVM
DESIGNED FOR: Public Release
FILE NAME: DC104F_PCB.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: DC104F	REV: F	SVN REV: Not in version control
LAYER NAME = [illegible]	TID #: N/A		
PLOT NAME = DC104F	GENERATED : 4/1/2022 3:36:46 PM	TEXAS INSTRUMENTS	

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ENGINEER: Daniel Brock	LAYOUT BY: Daniel Brock
SCALE: 1.00	ALTIUM DESIGNER VERSION: 21.2.2.38