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RF Sampling Training Workshop

Version 1p0

Abstract:

This is a one-day, hands-on training course that introduces the RF sampling concepts and its use in high end communication systems. The lab component of the workshop utilizes the DAC38RF80 RF DAC and the ADC32RF80 RF ADC device. The lab component will exercise most of the key features within the devices to give the user an intuitive understanding of how to manipulate the components in a real system. The lab component is self-contained and does not require any external test equipment.

Agenda:

Time		Topics
8:30 AM - 9:00 AM	Introductions/Set-up	
9:00 AM - 9:30 AM	Lecture #1	Introduction to RF Sampling
9:30 AM - 10:00 AM	Lecture #2	Introduction to ADC32RFxx RF ADC
10:00 AM - 10:30 AM	Lab Session #1	ADC32RF45 Initialization
10:30 AM - 10:45 AM	Break	
10:45 AM - 11:15 AM	Lecture #3	Introduction to DAC38RF8x RF DAC
11:15 AM - 11:45 AM	Lab Session #2	DAC38RF80 Initialization
11:45 AM - 1:00 PM	Lunch	
1:00 PM - 1:30 PM	Lecture #4	DAC38RF8x DUC Features
1:30 PM - 2:00 PM	Lab Session #3	Exercise RF DAC DUC Features
2:00 PM - 2:30 PM	Lecture #5	ADC38RFxx DDC Features
2:30 PM - 3:00 PM	Lab Session #4	Exercise RF ADC DDC Features
3:00 PM - 3:15 PM	Break	
3:15 PM - 4:00 PM	Lecture #6	RF Sampling Clocking
4:00 PM - 4:30 PM	Lab Session #5	Examine Wideband Signals
4:30 PM - 5:00 PM	Wrap-up	

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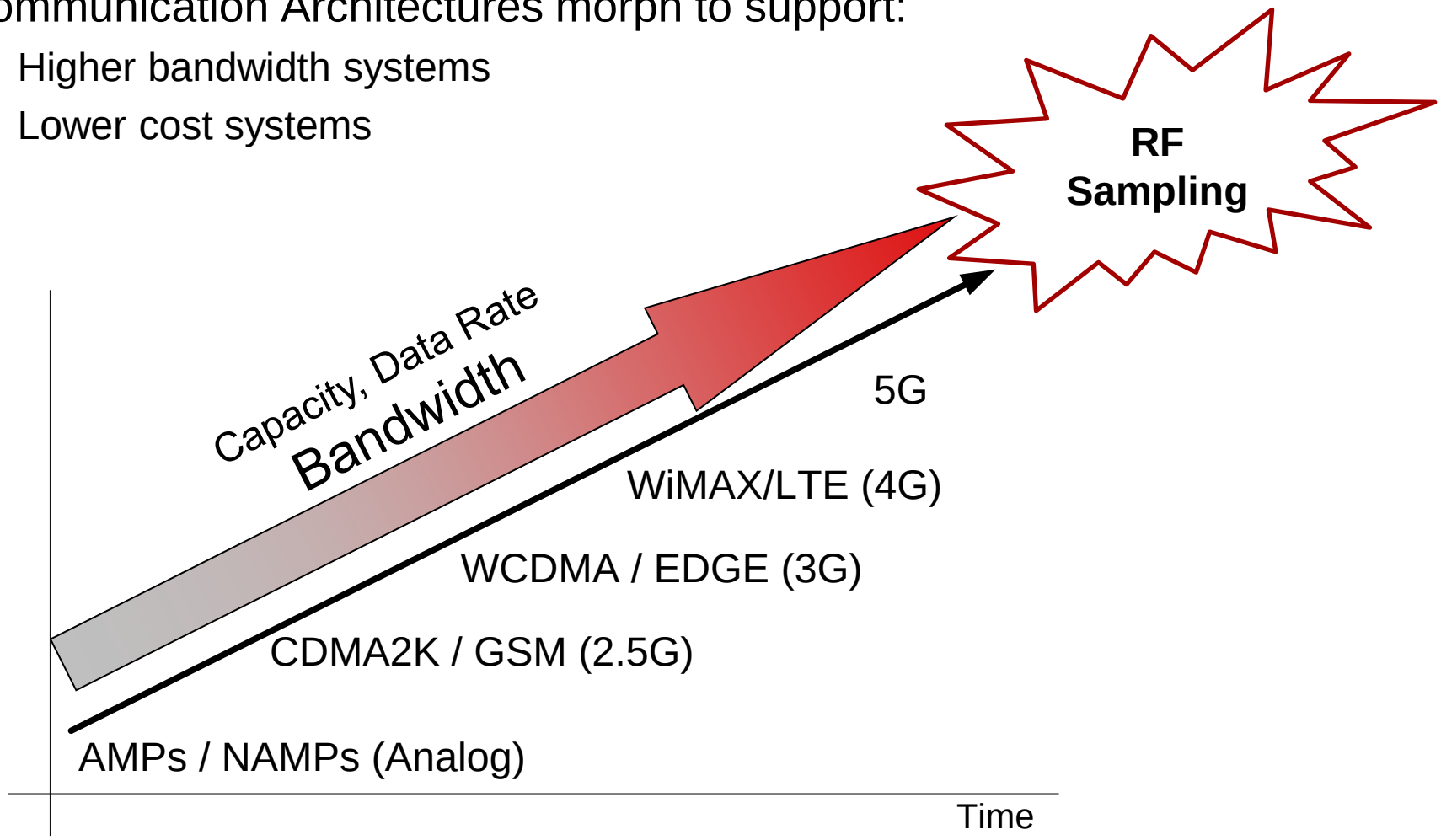
Introduction to Direct RF Sampling

Lecture 1

Communication Trend
(e.g. Wireless Infrastructure)

- Communication Architectures morph to support:
  - Higher bandwidth systems
  - Lower cost systems

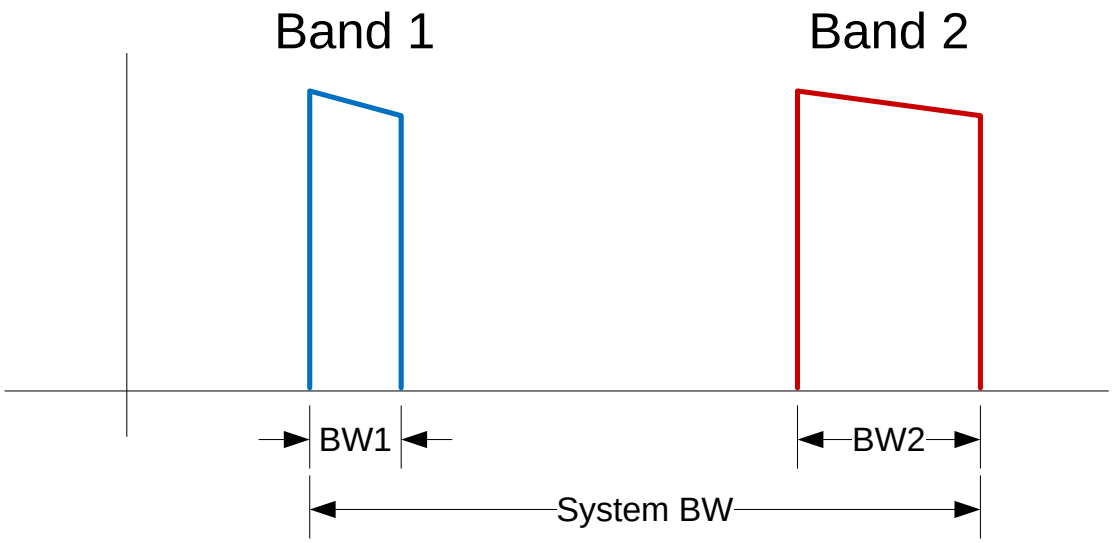


Bandwidth Consideration

- Large BW signals support large data throughput and high capacity
  - How to support?
- Traditional architectures were limited by data converter sampling rate
  - Per Sampling Theorem, minimum sampling rate is at least 2x desired BW
  - Only alternative was to chop-up signal into smaller chunks for sampling
- RF Converters drastically increase sampling rate and thus can support much higher signal bandwidths
  - Very large signal bandwidths can be directly sampled
  - High frequency signals under-sampled to the first Nyquist zone
- Example:
  - 1 GHz of Spectrum requires minimum of 2 GHz sampling rate
  - For practical consideration, additional guard band is required

High Bandwidth - Multi-band Operation

- Signal BW does not need to be contiguous
  - i.e. Two smaller BW signal separated in frequency can be considered as one larger signal BW
- RF Sampling solution provides a mechanism to support multiple bands, each with arbitrary signal bandwidth and with variable spacing



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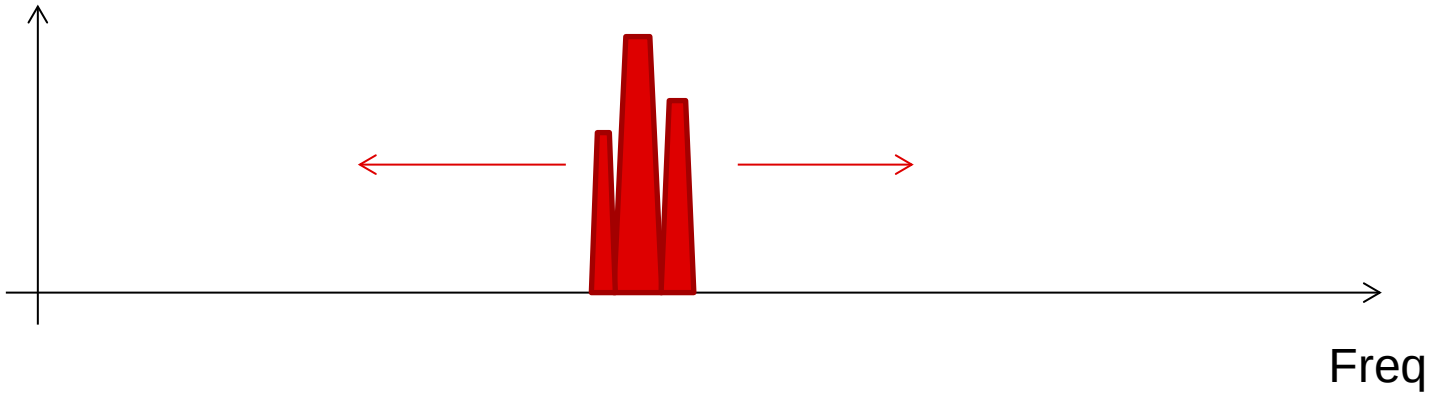
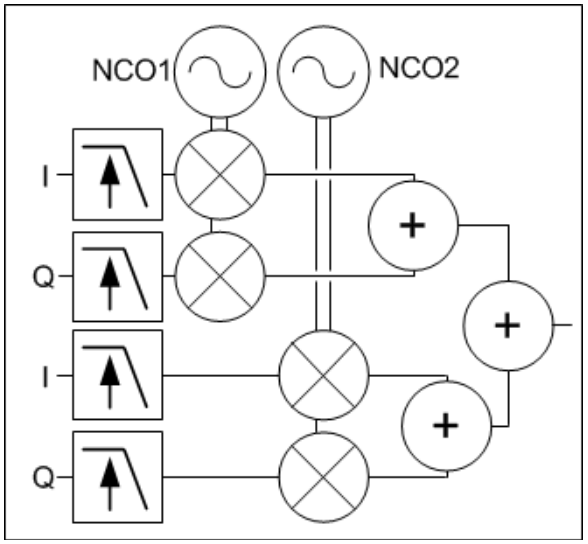
High Bandwidth - Tunable

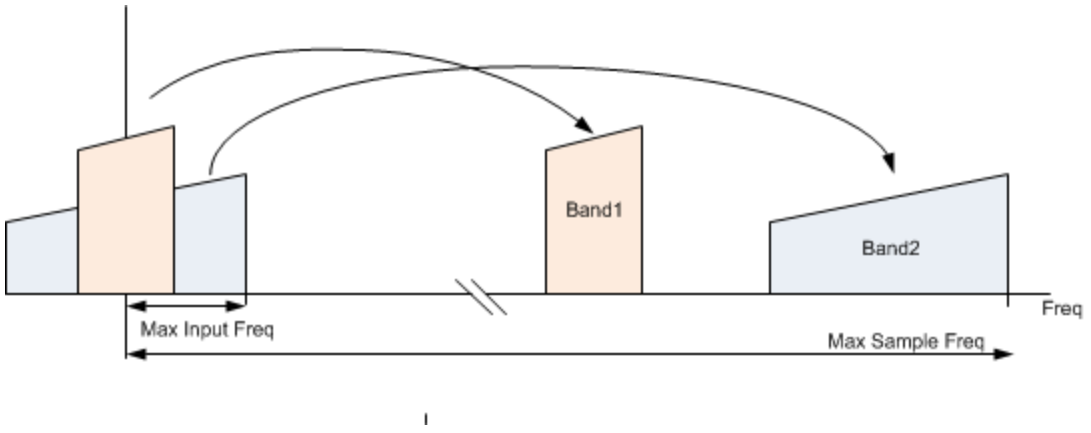
- Allocated RF Frequency Band is pre-defined
  - i.e. defined from standards requirement, regulatory requirements, or from system specifications
- Within the allocated band, desired signal can be assigned to specific (narrow band) channel
- RF Sampling Solution provide mechanism to easily place/capture desired signal at any arbitrary channel.



Multiple NCO – Multi-Band

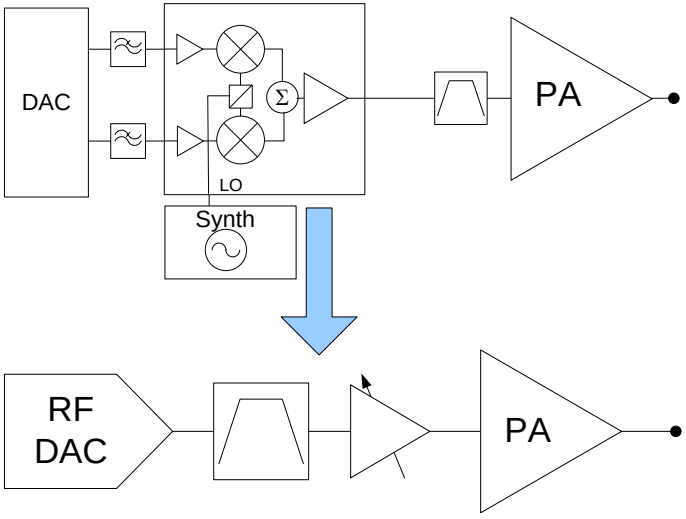
- Include multiple NCOs to tune separate channels to arbitrary RF frequency location
  - Supports non-contiguous multi-carrier operation
  - Supports multi-band or multi-mode operation
- Keeps input data rates low; sufficient to meet bandwidth requirements of each signal
- Supports very wide effective output bandwidth

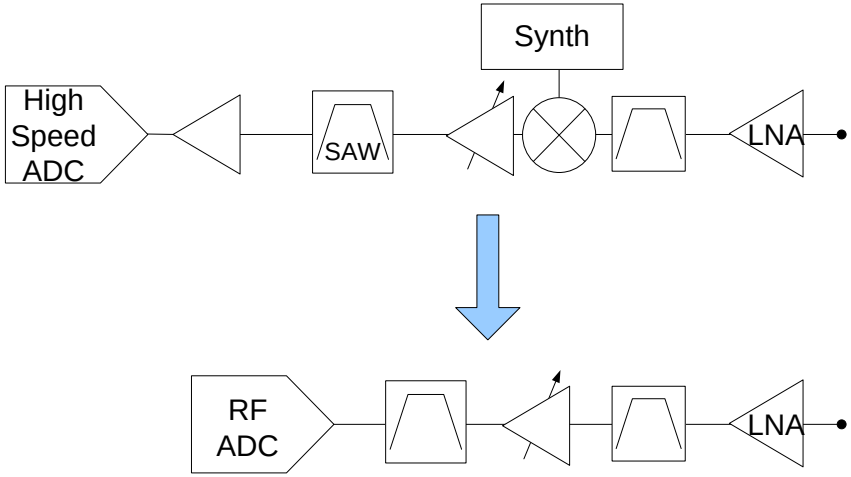




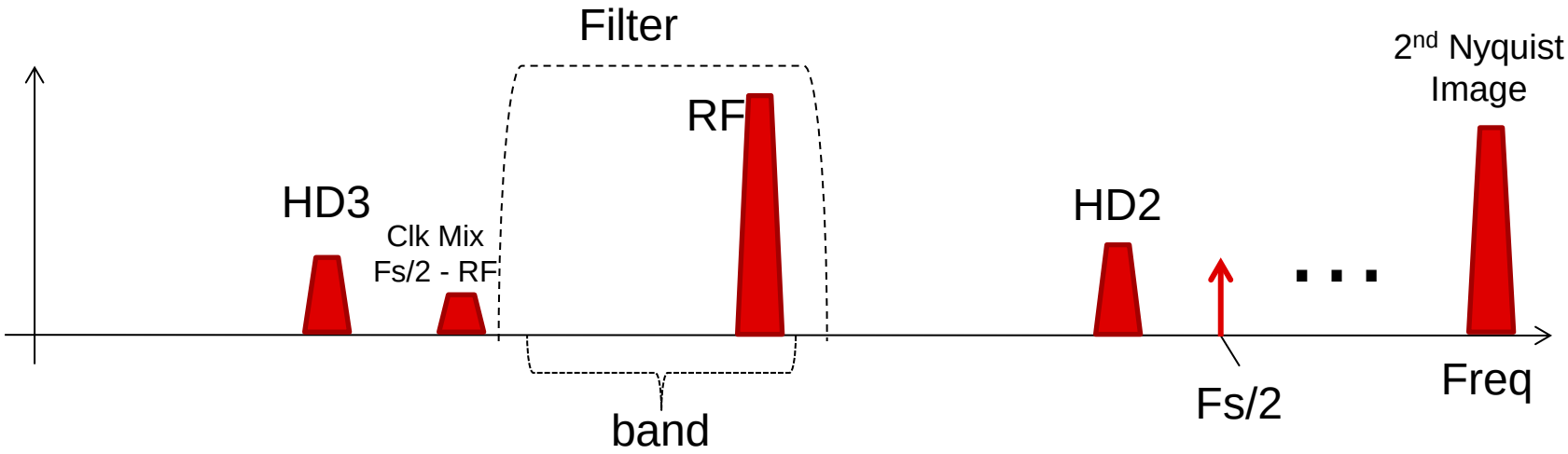
Transformation to RF Sampling Architecture

- Transmitter
  - Eliminate IQ Modulator
  - Eliminate RF Synthesizer
- Receiver
  - Eliminate RF mixer
  - Eliminate RF Synthesizer
  - Eliminate IF channel filter
  - Transform IF VGA to RF VGA



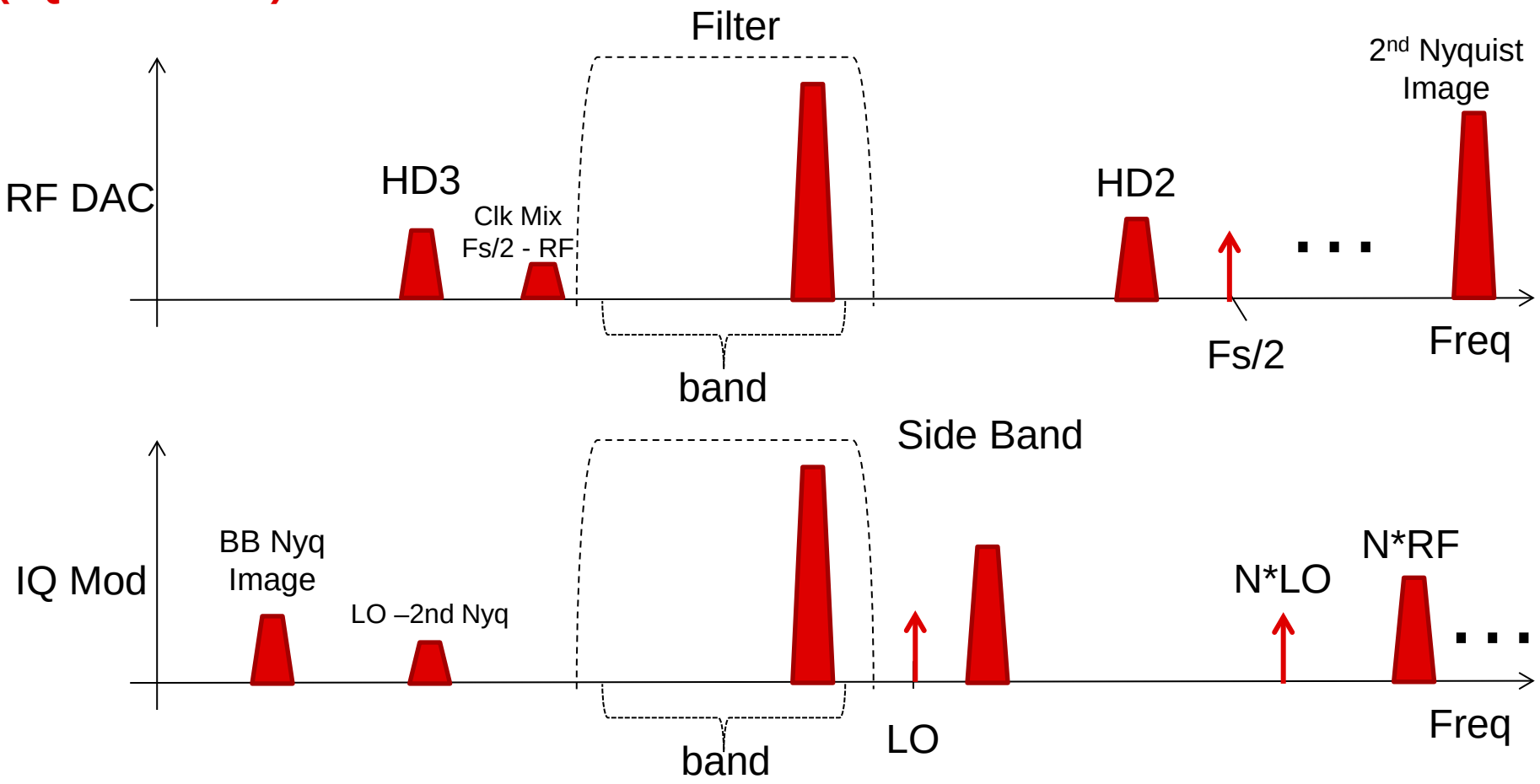


Reality of RF Sampling Transmitter



- Ideal Transmitter: Fundamental signal at the frequency of interest
- Real World Impairments:
  - HD2 Component
  - HD3 Component (aliased)
  - Clock Mixing Spurious
  - Fs/2 Spur
  - Image Frequency in 2nd (and higher) Nyquist zone
- Analog filter added to minimize/eliminate spurious outputs

Comparison w/ Direct Conversion Architecture
(I/Q Modulator)



- Comparable analog filter needed to remove spurious/images

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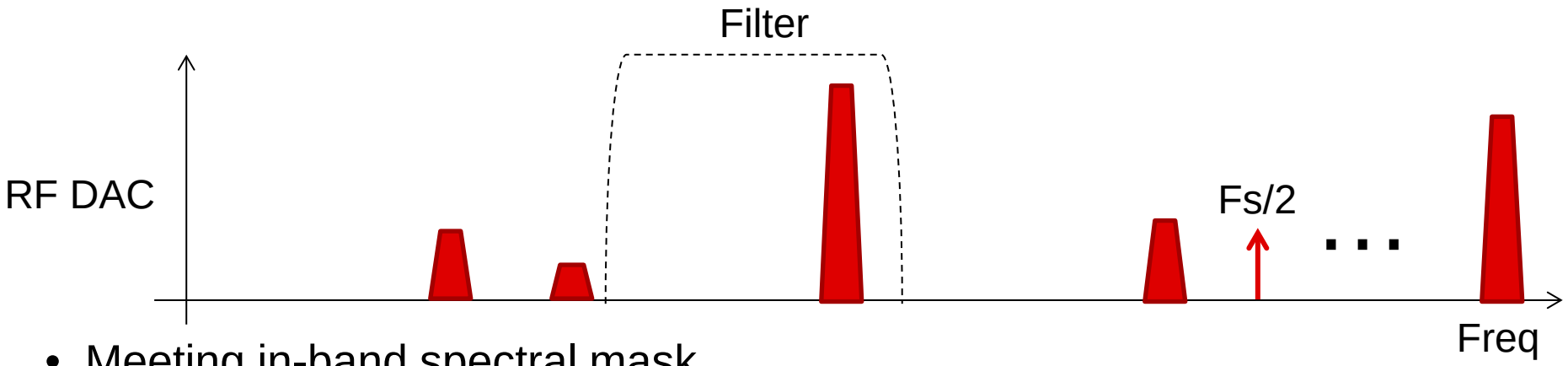
Strategy for Spectral Mask with RF DAC

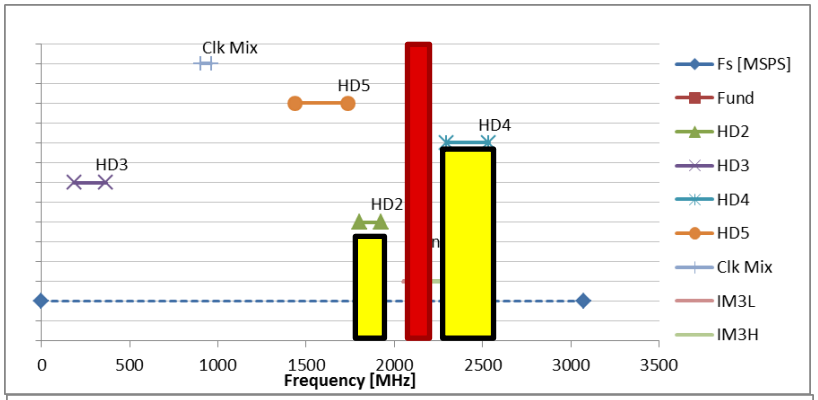


- Meeting in-band spectral mask
  - No filtering is possible; inherent performance must meet mask
  - Frequency plan to move known spurious product outside of band
- Meeting out-of-band spectral mask
  - Optimize sampling rate to move spurious far away from desired band
  - Incorporate filtering to suppress out-of-band spurious from being transmitted
  - Farther the separation of spurious products, the easier to filter
  - With proper planning, filtering can be eliminated or relaxed compared to other architectures

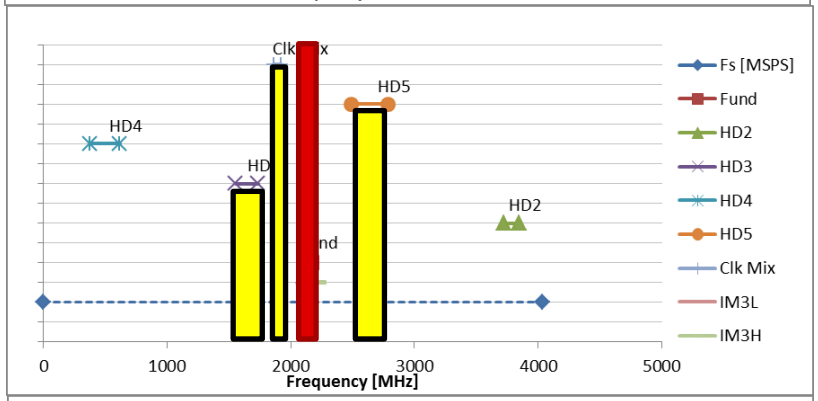
TX Frequency Planning Example

RF = 2140 MHz; BW = 60 MHz

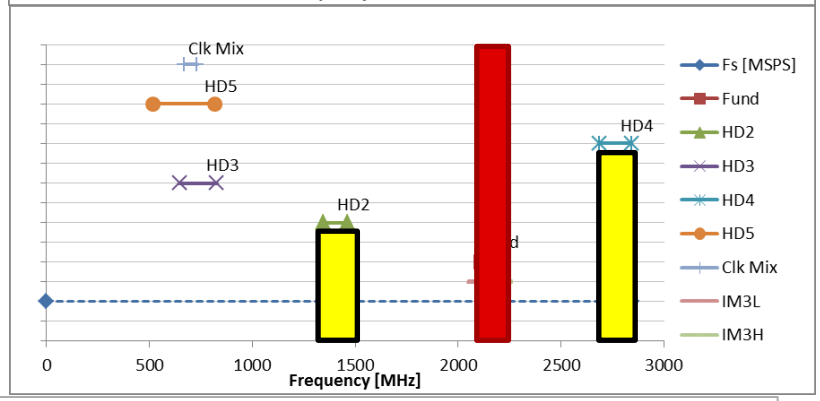
- Fs = 6144 MHz
- In-band is clear but HD2 and HD4 are close and hard to filter



- Increase sampling rate:
  - Fs = 8024 MHz
- In band still clear but HD3, HD5, and Clock mixing spur hard to filter



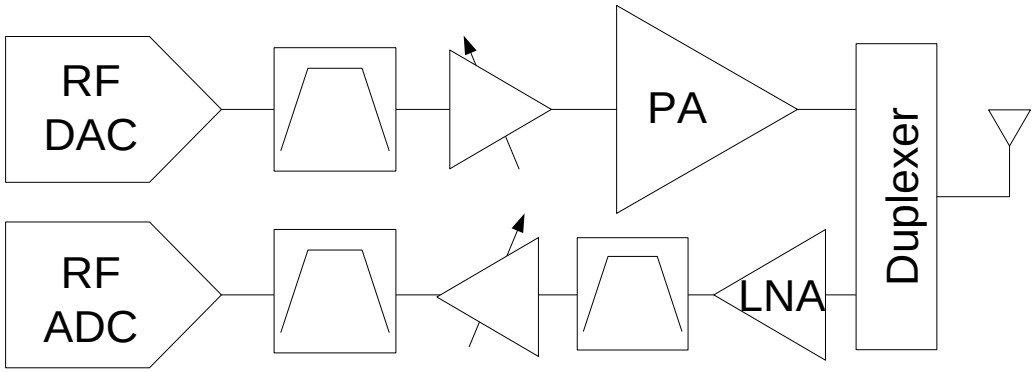
- Decrease sampling rate:
  - Fs = 5683.2 MHz
- In-band clear and lots of spacing to other spurious ➔ easy filtering



RF Sampling Transmitter Advantages

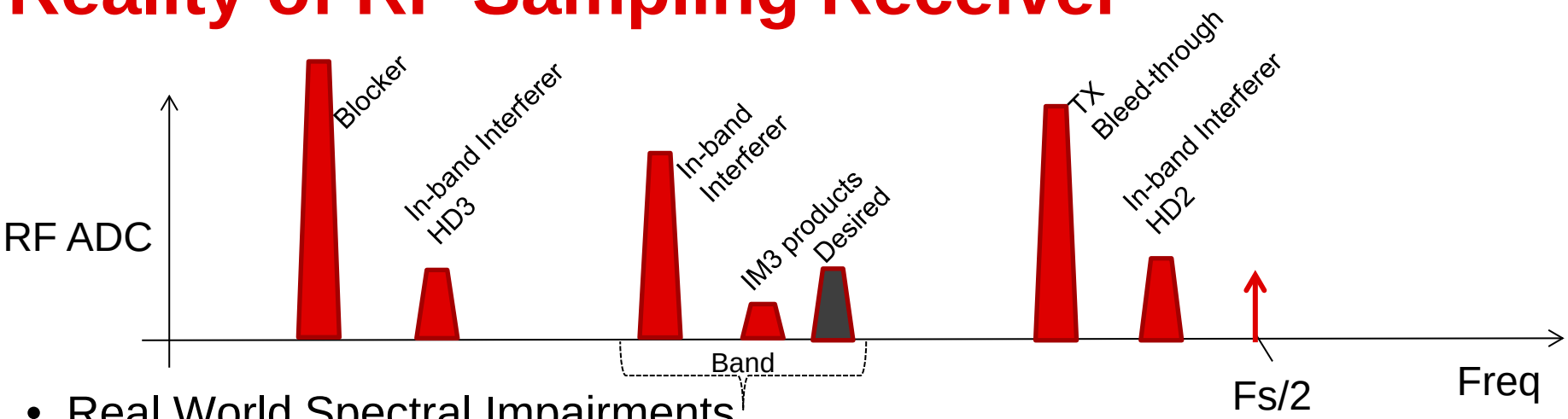
- In-band Impairments: Better for wider bandwidth
  - Digital quadrature modulation eliminates sideband correction.
    - Higher BW signals yield more frequency dependent phase/gain mismatch
    - More difficult to correct in traditional architecture
  - More consistent Gain/Phase vs. Frequency than with analog BB or IF filter
- Power dissipation
  - Potential for improvement over discrete approach depending on implemented features and sampling rate.
- Size (PCB Real Estate)
  - 80% size reduction over discrete IF solution
  - 50% size reduction vs. MCM IF solution
- Better for…
  - Wide bandwidth signals and Multi-band applications
  - Higher density systems (MIMO, beam-forming)
  - Easier implementation for new markets, requirements and frequency bands

RF Sampling Receiver



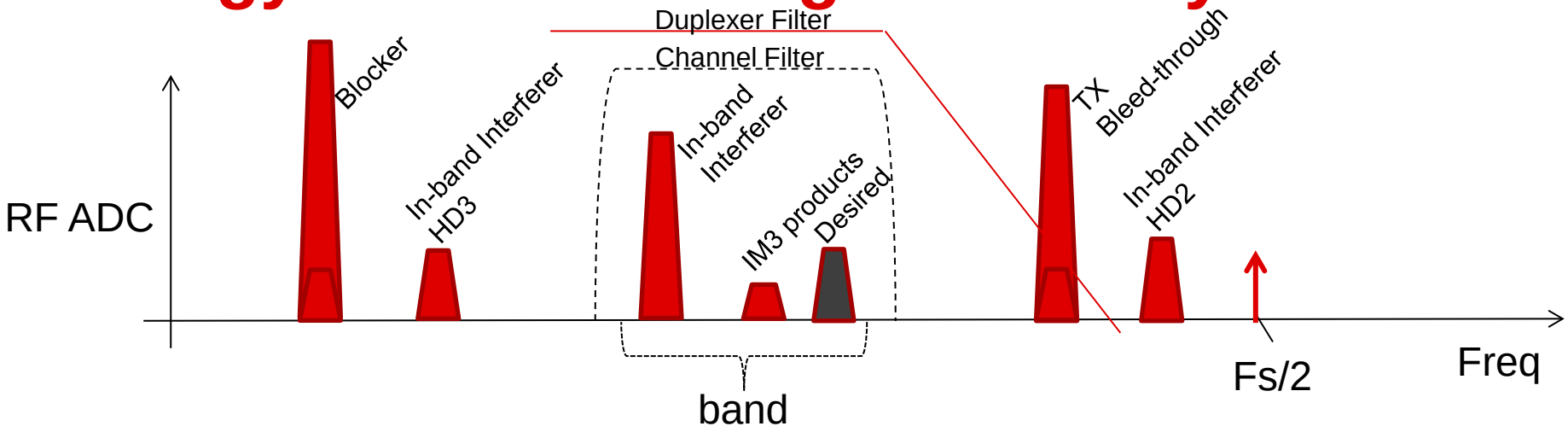
- All signals alias down into the first Nyquist zone
- Ideal RF Sampling ADC directly captures desired band
- ADC must balance dynamic range
  - Need low noise floor (good SNR) to capture desired low power received signal
    - Maintain Sensitivity requirements
  - Need to handle high amplitude level from blocker or TX bleed-through so that ADC is not overdriven and distorted.
    - Maintain blocker/jammer requirements

Reality of RF Sampling Receiver



- Real World Spectral Impairments
  - Spurious signals (i.e. IM3, HD2, HD3 etc.) from in-band interferers generated in analog chain (i.e. LNA, VGA)
  - Out-of-band Interferers from Blockers/Jammers
  - TX signal bleed-through to the RX path
  - IM3 Mixing products between Jammers and TX bleed-thorough
- Real World Overdrive Impairments
  - TX Bleed-through
  - Blockers/Jammers
- Broadband Noise folding into 1st Nyquist Zone

Strategy for Maintaining Sensitivity w/ RX



- Duplexer Filter
  - Suppresses TX Bleed-through into receiver
  - Eliminates IM3 Spurious generation
- Channel Filter
  - Suppress out-of-band spurious generated from in-band interferers
  - Suppress Blocker signals
  - Suppress harmonic/mixing spurs from blocker(s)
- Anti-aliasing filter to eliminate broadband noise

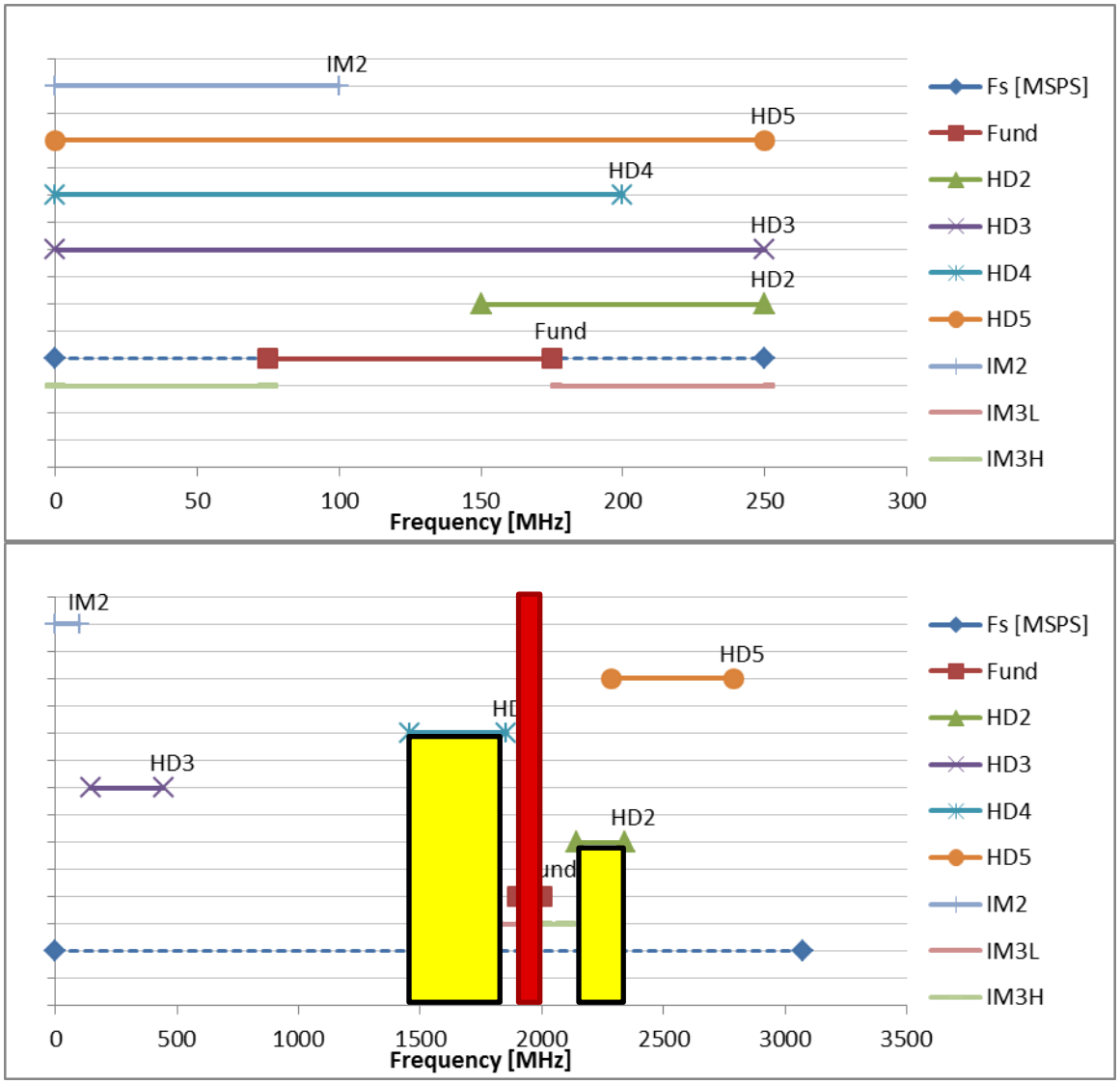
RF Sampling ADC - Frequency Planning

- Spurs from out-of-band interferers or TX bleed-through
  - Proper filtering can minimize or eliminate these threats
- Spurs from in-band interferers
  - Can not filter these signal out
  - Need to frequency plan around

- Higher sampling rate affords flexibility in frequency planning around troublesome harmonic and spurious products
- Frequency planning in High IF systems
  - Choose available sampling rate converter
  - Optimize IF location for best results
- Frequency Planning in RF Sampling
  - Can not choose location of RF signal; this is fixed
  - Optimize sampling rate to achieve best results

Frequency Planning Example

- Case 1: High IF Sampling
  - Fs = 500 MHz
  - IF = 375 MHz
  - BW = 100 MHz
- *Can not escape from aliased HD2 and higher harmonics*
- Case 2: RF Sampling
  - Fs = 6144 MHz
  - BW = 100 MHz
  - RF = 1950 MHz
- *Higher order harmonics do not fall in band*



RF Sampling Receiver Advantages

- Spectral Performance
  - Support wide bandwidth signals (or multi-mode)
  - Frequency agile
  - Digital features like decimation can minimize filter requirements
- Power dissipation
  - Power dissipation improvement possible by eliminating mixer and RF synthesizer components (depending on digital features/sampling rate).
- Size (PCB Real Estate)
  - Size reduction over discrete IF solution
- Better for…
  - Wide bandwidth signals, Multi-band applications, and DPD feedback
  - Higher density systems (MIMO, beam-forming)
  - Easier implementation for multiple standards

Input Data Rates

- Higher sampling rates required for sampling at RF and for frequency planning around spurious
- Data rates can not operate at those speeds
  - Limited by processor or FPGA rate
  - Limited by available I/O on the device
- Implement
  - Interpolation/Decimation in order to keep data rates reasonable
  - NCO (Numerically Controlled Oscillator) to move desired signal to any required band
- Rule of thumb:
  - Select data rate to support bandwidth of the signal
  - Select sampling rate to support output frequency band and spectral purity

System Challenges for RF Sampling

- **Digital Interface**
  - High data rates needed to support high bandwidth signals
  - Incorporate interpolation/decimation filters to maintain reasonable rates
- **Clocking**
  - Requires high frequency, low phase noise sampling clock
    - Challenging to generate and route across board
    - Challenging for multi-device synchronization
  - Incorporate an optional internal PLL/VCO to generate required clock on-chip
- **Spectral Performance**
  - Low order harmonics
    - Frequency plan around troublesome spurious when possible
    - Maintain low spurious generation where frequency planning not possible
  - High order harmonics
    - Cannot frequency plan around these
    - Must rely on design to meet requirement

Overall System Benefits for RF Sampling

- Support higher bandwidth signals that were previously not possible
- Support for a frequency agile architecture
  - One design can service many bands, standards, etc.
- Digital features allow for additional flexibility in controlling the signals and manipulating the channel
- Filtering schemes can be relaxed in many cases and potentially eliminated
- Multiple devices/line-ups can be more easily synchronized together to build more complex systems
  - Large Radar Arrays
  - Beam-forming Antennas
  - Massive MIMO

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End of Lecture 1

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Introduction to ADC32RFxx RF ADC

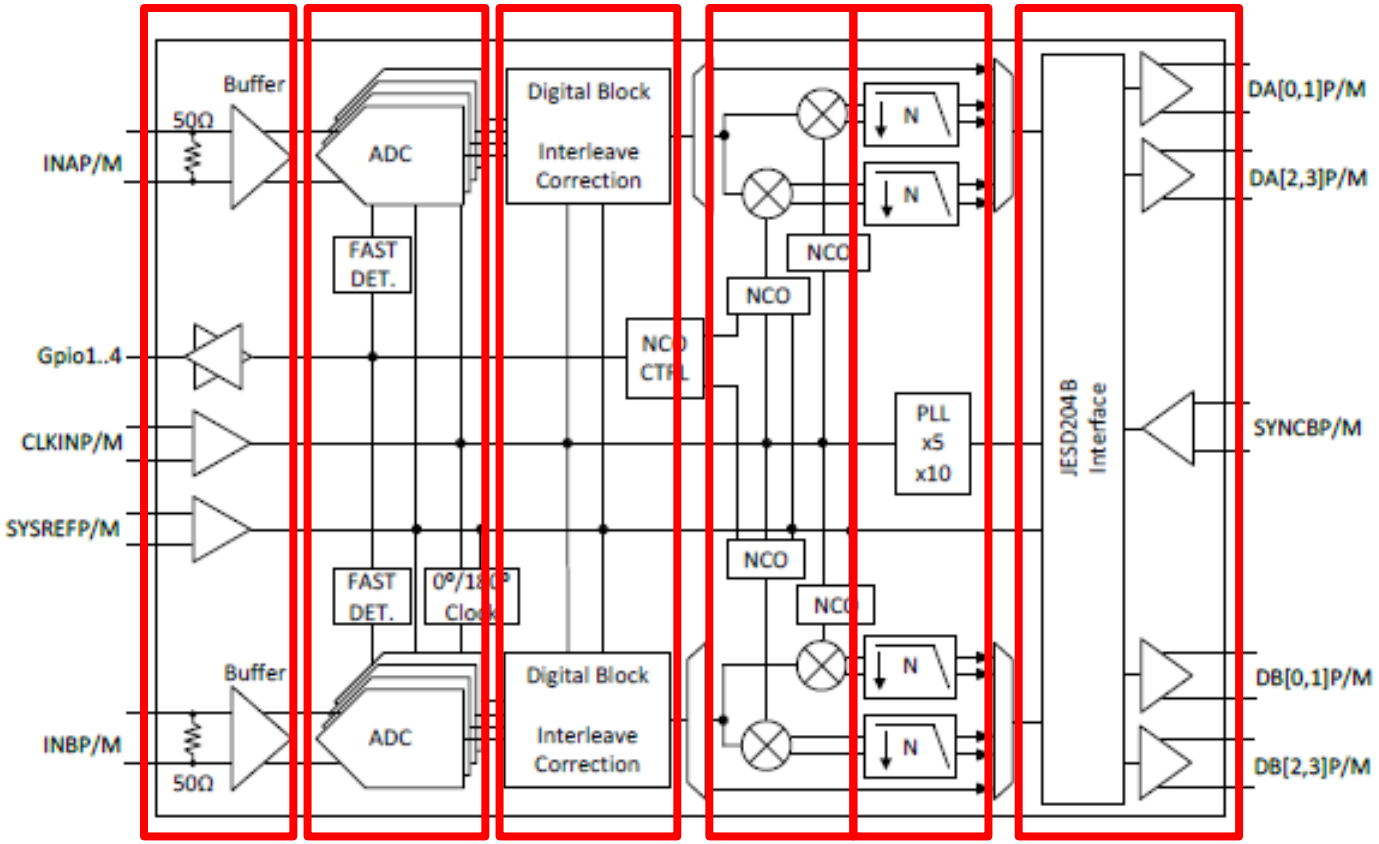
Lecture 2

ADC32RFxx Product Overview

- Two main families
  - ADC32RF45 Dual-channel, 14-bit, 3GSPS
    - Supports Bypass mode (operation with full Nyquist bandwidth)
    - Supports full DDC (Digital Down Converter) modes
  - ADC32RF80 Dual-channel, 14-bit, 3 GSPS
    - Supports only DDC modes (decimation /4 to /32)

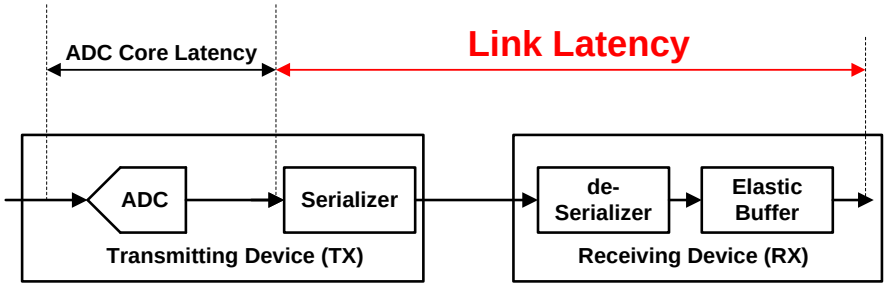
ADC32RF4x Family		
Device	**# of DDC**	**Speed Grade**
ADC32RF45	2	3.0 GSPS
ADC32RF44	2	2.5 GSPS
ADC32RF43	2	2.0 GSPS
ADC32RF42	2	1.5 GSPS
ADC32RF41	2	1.0 GSPS
ADC32RF8x Family		
Device	**# of DDC**	**Speed Grade**
ADC32RF80	2	3.0 GSPS
ADC32RF83	1	3.0 GSPS

ADC32RFxx Block Diagram



JESD204B Interface

- JESD204B SerDes (Serializer/De-serializer) standard provides a widely adopted interface for transferring a large amount of data
  - Data is parsed over specified number of lanes
  - Uses 8b/10b encoding for synchronization, clock recovery, and DC balance
  - Standard supports up to 12.5 Gbps lane rates
  - Provisions to support deterministic latency across the serialized link
- Key clocking requirements
  - **Sample clock**: sampling clock and reference for all other system timing
  - **SysRef:**
    - Source synchronous to the sample clock
    - Provides phase reference for SerDes frame clocks



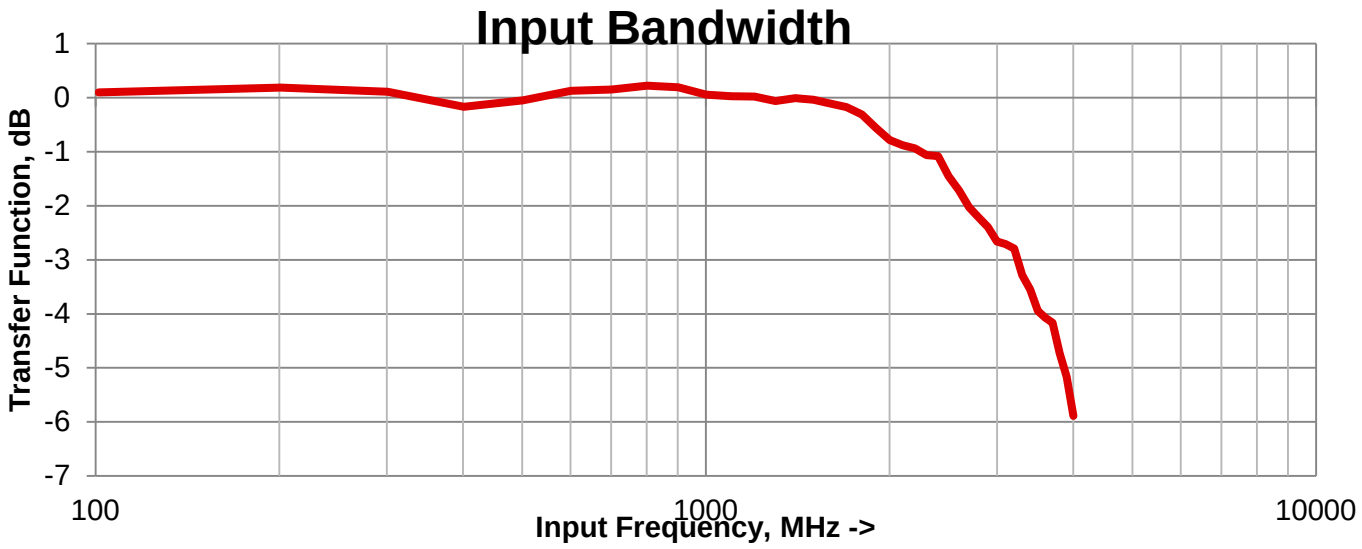
JESD204b Interface – Key Parameters

- Key Data Converter Parameters: LMFS
  - L # of lanes per converter device
  - M # of converters per device
  - F # of octets per frame (per lane)
  - S # of samples per converter per frame clock cycle
- SerDes speeds may vary for each of the LMFS mode
  - Fewer lanes increases lane rate
  - More decimation decreases lane rate
  - FPGA clocking will often be 1/10 to 1/40 the lane rate
- Data Sheet provides lane mapping for desired modes/lanes
  - "L" = up to **8 lanes** at **12 Gbps** max rate
  - "M" = 2, 4, 8 effective converters
    - M= 2 Bypass mode
    - M= 4 Single DDC, complex mixer
    - M= 8 Dual DDC, complex mixer

Decimation Setting (complex)	# of Active DDCs	Output Complex/ Real	L	M	F	S
/ 4		Complex	8	4	1	1
		Complex	4	4	2	1
/ 6		Complex	8	4	1	1
		Complex	4	4	2	1
/ 8		Complex	4	4	2	1
		Complex	2	4	4	1

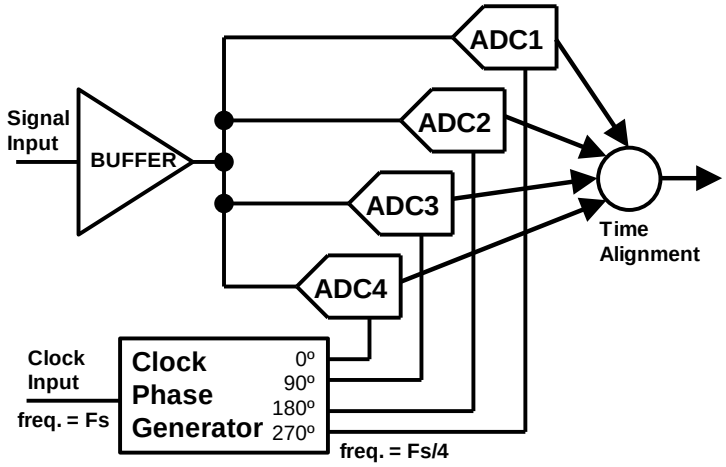
Input Buffer

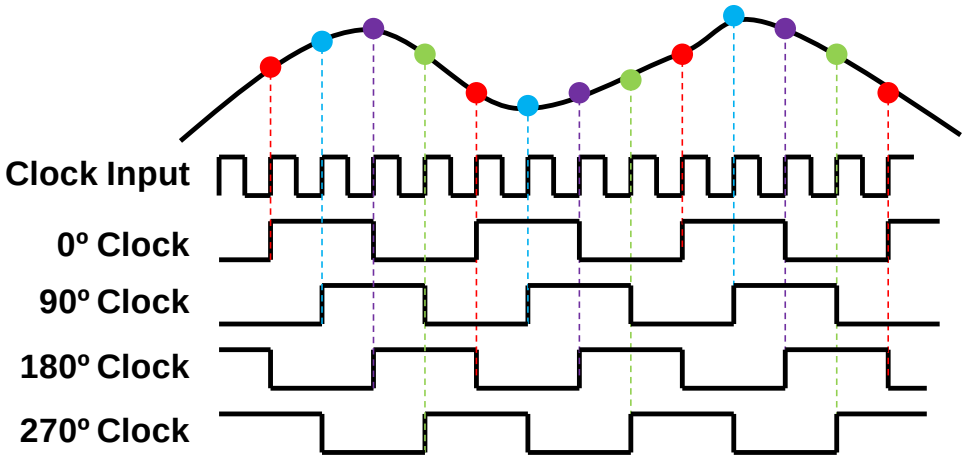
- Differential Input buffer impedance: 50 ohms
- Recommend high frequency 1:1 balun/transformer with good phase balance across the frequency of operation
- Input bandwidth capability: 3 GHz
  - Support 1st and 2nd Nyquist bands directly
  - Support 3rd Nyquist up to 4 GHz with degraded performance



Interleaving

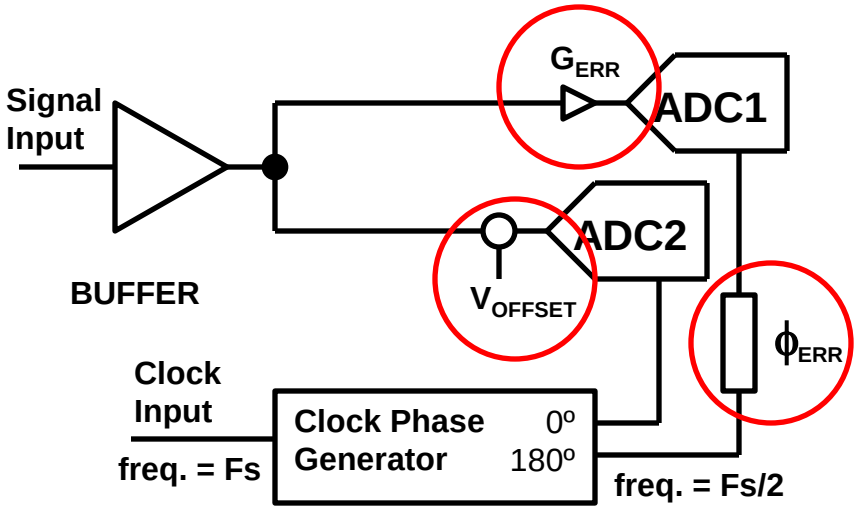
- Interleave four 750 MSPS ADC cores = 3 GSPS
- Clock distribution handled on-chip
  - ADC cores sample at same divided frequency but at different phase offsets
  - Digital outputs are re-aligned in time
- Why Interleave?
  - Utilize ADC core with good SNR/SFDR performance
  - Combine to achieve high sampling rate & high bandwidth capabilities

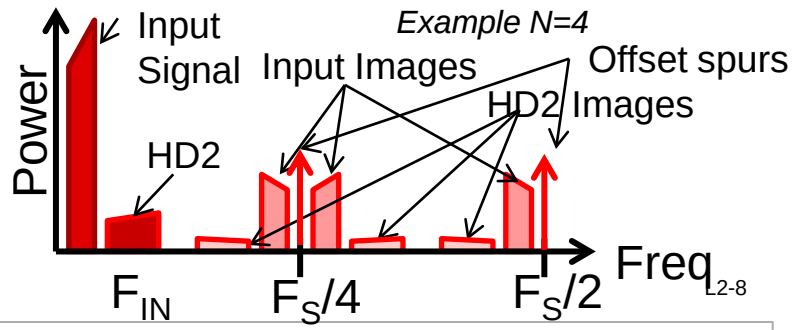




Non-ideal Interleaving

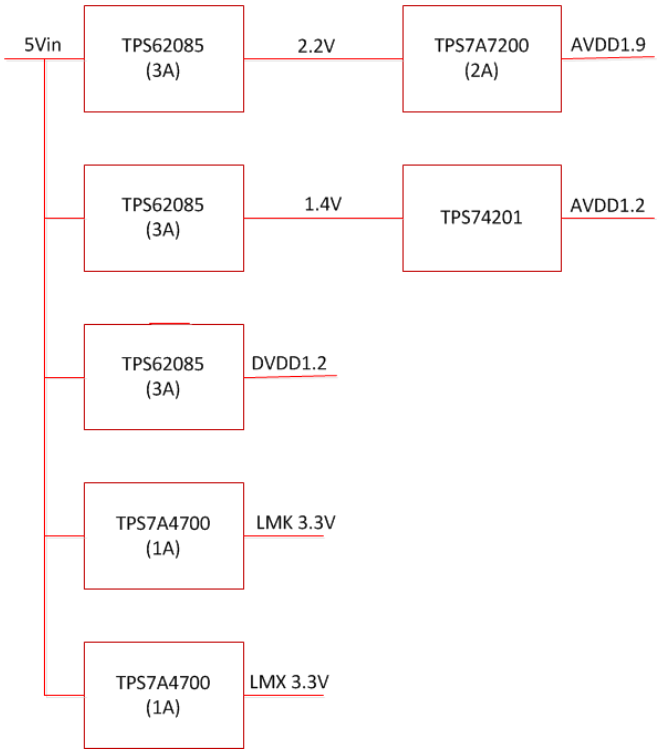
- Offset Errors
  - Mismatched ADC core voltage offset
- Amplitude Errors
  - ADC core gain error
  - ADC reference voltage error
- Phase Errors
  - Input routing delay
  - Input BW difference
  - Clock phase error or imprecise sampling instant
- Interleaving errors create unwanted spurs and images
  - Offset Errors => spurs at Fs/2, Fs/4
  - Amplitude/Phase => images
- Digital Correction Block
  - Continuous digital interleave adjustment
  - Maintain IL spur < 80 dBc at 2.1 GHz





DC Power Considerations

- ADC Power rails
  - Analog: 1.9 V
  - Analog: 1.2 V
  - Digital: 1.15 V
- Power management strategy
  - Option 1: (most conservative)
    - DC-DC convert to intermediate voltage
    - LDO convert to required rail
  - Option 2: (minimum power dissipation/cost)
    - DC-DC convert to required rail
    - Ensure switching spurs/noise do not cause system issues
    - Improve supply filtering as needed
- Power Dissipation: ~6W
  - Dependent of sampling frequency and mode
  - Heat sink recommended



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End of Lecture 2

1.0 **Session #1** Objective: **Acquire an initial ADC capture with an external 1960 MHz tone.**

2.0 Hardware Set-up

2.1 TSW14J56 connections

2.1.1 Connect ADC32RF80 EVM

2.1.2 Connect 5V power jack

2.1.3 Connect USB hub to computer USB port

2.1.4 Connect USB3.0 cable from USB hub to J9

2.2 ADC32RF80 connections

2.2.1 Connect 5V power jack

2.2.2 Connect USB cable

2.2.3 Verify jumper JP3 set to “INTCLK”

2.3 Signal source (TSW3065)

2.3.1 Connect **6V** power jack

2.3.2 Verify “Supply Select” is set to “6V In”

2.3.3 Verify Dip switch (or LED indicator) is set to [D3, D4, D5, D6] = [0100]

2.3.4 Change “Ref Select” to: “Internal” (flip to right)

2.3.5 Cable “Ref Out” to LMK_CLKIN (J7) on ADC32RFxx EVM

2.3.6 Connect “LO HF Bal Out” to bandpass filter

2.3.7 Connect BPF filter output to ADC channel A input at J2

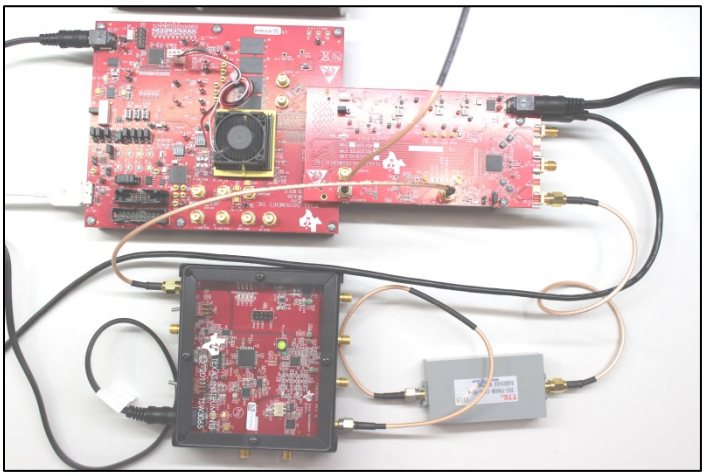

Figure 1.0: Hardware set-up

3.0 Software setup

3.1 ADC32RFxx

3.1.1 Launch ADC32RFxx GUI

3.1.2 Select *LMK04828* tab> *PLL1 Configuration* tab; toggle “RESET” button

3.1.3 Select *Low Level View* tab

a) Select “Open Configuration” folder icon (Figure 1.1)

b) Select “ADC32RF80 DDC” folder

c) Load: “LMK_ADC32RF80_2949MSPS.cfg”
d) Verify LED D4 and D3 illuminates
e) Select “Open Configuration” folder icon again
f) Load: “LMX_2949p12M.cfg”

3.1.4 Press reset button on the ADC32RF80 EVM (SW1)
3.1.5 In the *Low Level View* tab
a) Select “Open Configuration” folder icon once again
b) Select “ADC32RF80_DDC” folder
c) Load: “ADC32RF80_ 8xIQ_lmfs8821.cfg”
d) Select “Read All” icon
3.1.6 Select *ADC32RFxx* tab> *DDC Configuration* tab
a) Set *Sample Clock* to: 2949.12
b) Set *ChA DDC0 NCO 1 freq* to: 1860
c) Click in *ChA DDC0 NCO 1 and* hit <space> then enter; this loads actual NCO frequency
d) Set *ChB DDC0 NCO 1* to: 1860
e) Click in *ChB DDC0 NCO 1 and* hit <space> then enter; this loads actual NCO frequency

3.2 HSDC Pro
3.2.1 Launch HSDC Pro software
3.2.2 Load *ADC32RF80_LMF_8821_isync0* ini file
3.2.3 Change to “Complex FFT”
3.2.4 Change to “Channel 1/8”
3.2.5 Toggle ADC Output Setup icon
a) Click “Enable?”
b) Change ADC Sampling rate to: 2949.12M
c) Change ADC Input Frequency to: 1960M
d) Change NCO to: -1859.985M
e) Change Decimation to: 8

3.3 Press Capture button

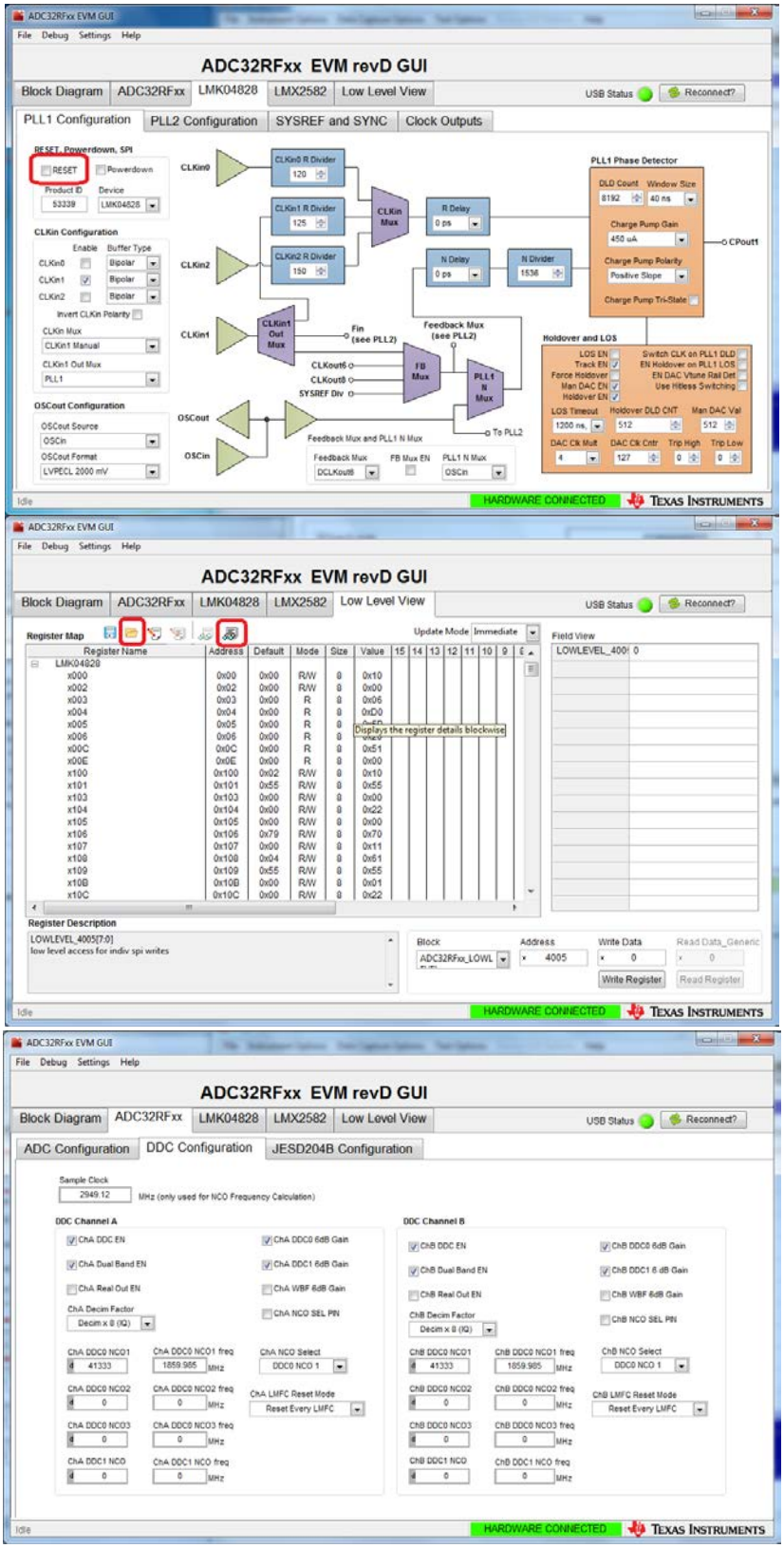

Figure 1.1: ADC32RFxx GUI set-up

4.0 Measurement Result

4.1 Verify that you get a data capture; verify marker location is at the proper place

4.2 What is the value of the highest spur? Is this a real spur? If not, what is it?

4.3 Adjust notching

4.3.1 HSDC Pro>Test Options>Notch Frequency Bins

4.3.2 Change “Number of bins to remove on either side of the fundamental” to: 100

4.3.3 Press “OK”

4.4 Did the location of the highest spur move?

4.5 Change to channel B

4.5.1 Move input cable to J3

4.5.2 Change to Channel 5/8 on HSDC Pro

4.5.3 Press Capture button

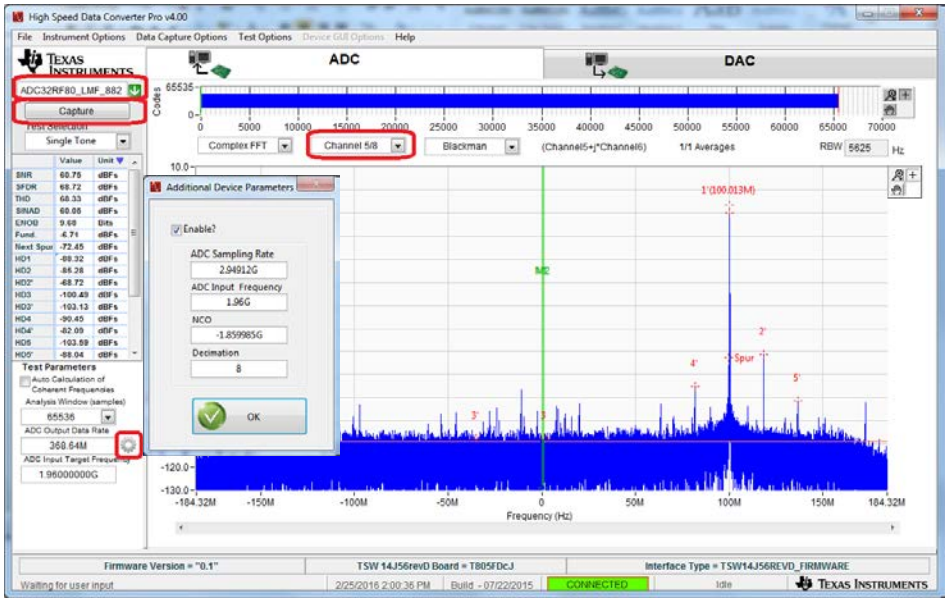

Figure 1.2: HSDC Pro set-up and initial capture

5.0 Additional experiments

5.1 SNR Observations

5.1.1 What is the SNR performance?

5.1.2 Remove the filter from the path and press “Capture”

a) How does SNR performance compare?

b) How does the spectrum compare?

c) Re-insert filter; press “Capture”

d) What does the filter do in this case?

5.2 SFDR observations

5.2.1 What is the SFDR performance?

5.2.2 Which spur is limiting performance?

***** Leave set-up as-is for use in the next session *****

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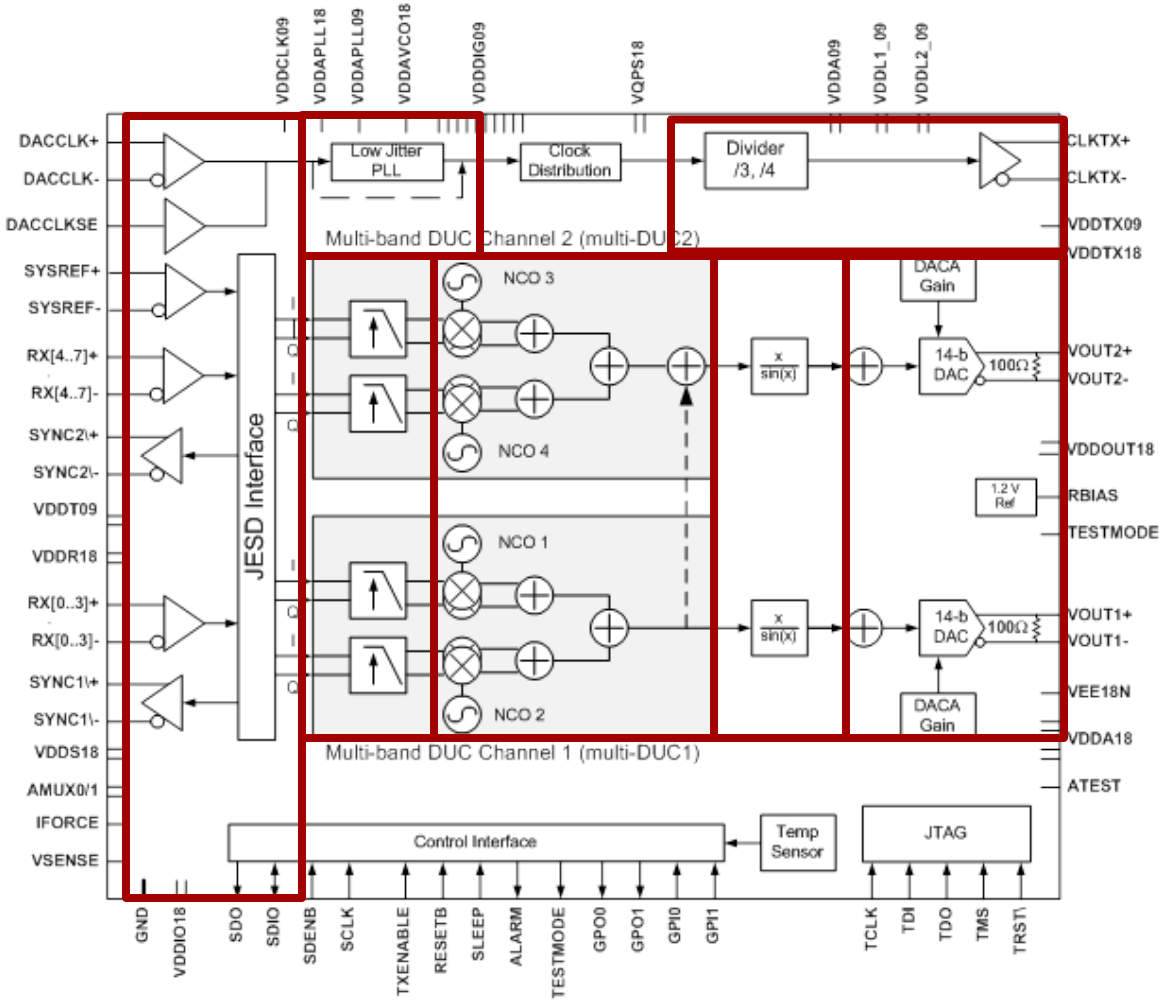
Introduction to DAC38RF8x

Lecture 3

DAC38RF8x Product Overview

	DAC38RF80	DAC38RF82	DAC38RF83
Channels	2	2	2
Output Interface	SE	DIFF	DIFF
Output Frequency Range	700-2700 MHz	100 - 4500 MHz	100 - 4500 MHz
Resolution	16, 12	16, 12, 8	16, 12
Min Interpolation	6x	1x	6x
Max Interpolation	24x	4x	24x
Maximum Signal BW	750 MHz	1600 MHz	750 MHz
Integrated Balun	Yes	No	No
Integrated PLL	Yes	Yes	Yes
Coarse Mixer	Yes	Yes	Yes
48-bit NCO	Yes	Yes	Yes
JESD204B Interface	Yes	Yes	Yes
Max SerDES Rate (Gbps)	12.5	12.5	12.5

Anatomy of RF DAC



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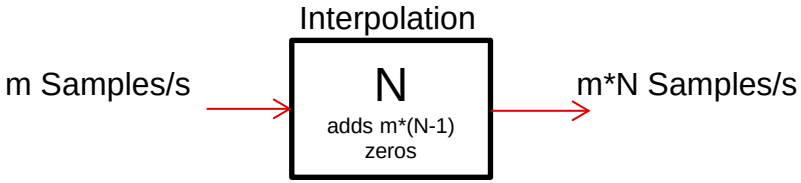
What is Interpolation?

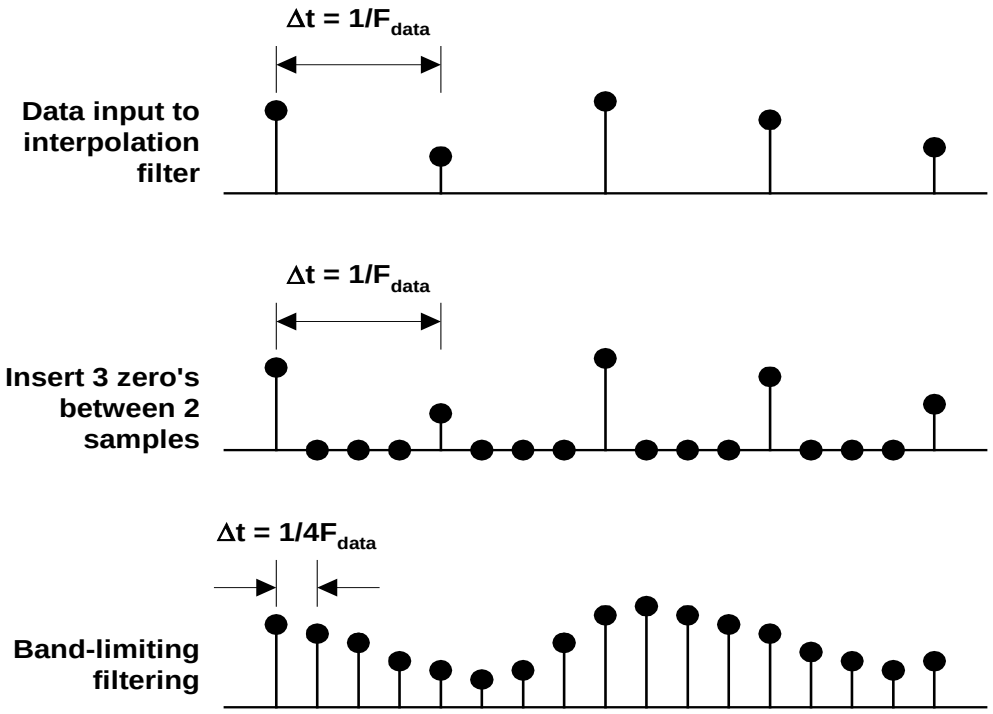
- Interpolation increases the sample rate of a signal without affecting the signal itself
  - Insert a 0 between each sample (zero stuffing / up sampling)
  - Filter the resulting images from the up sample process



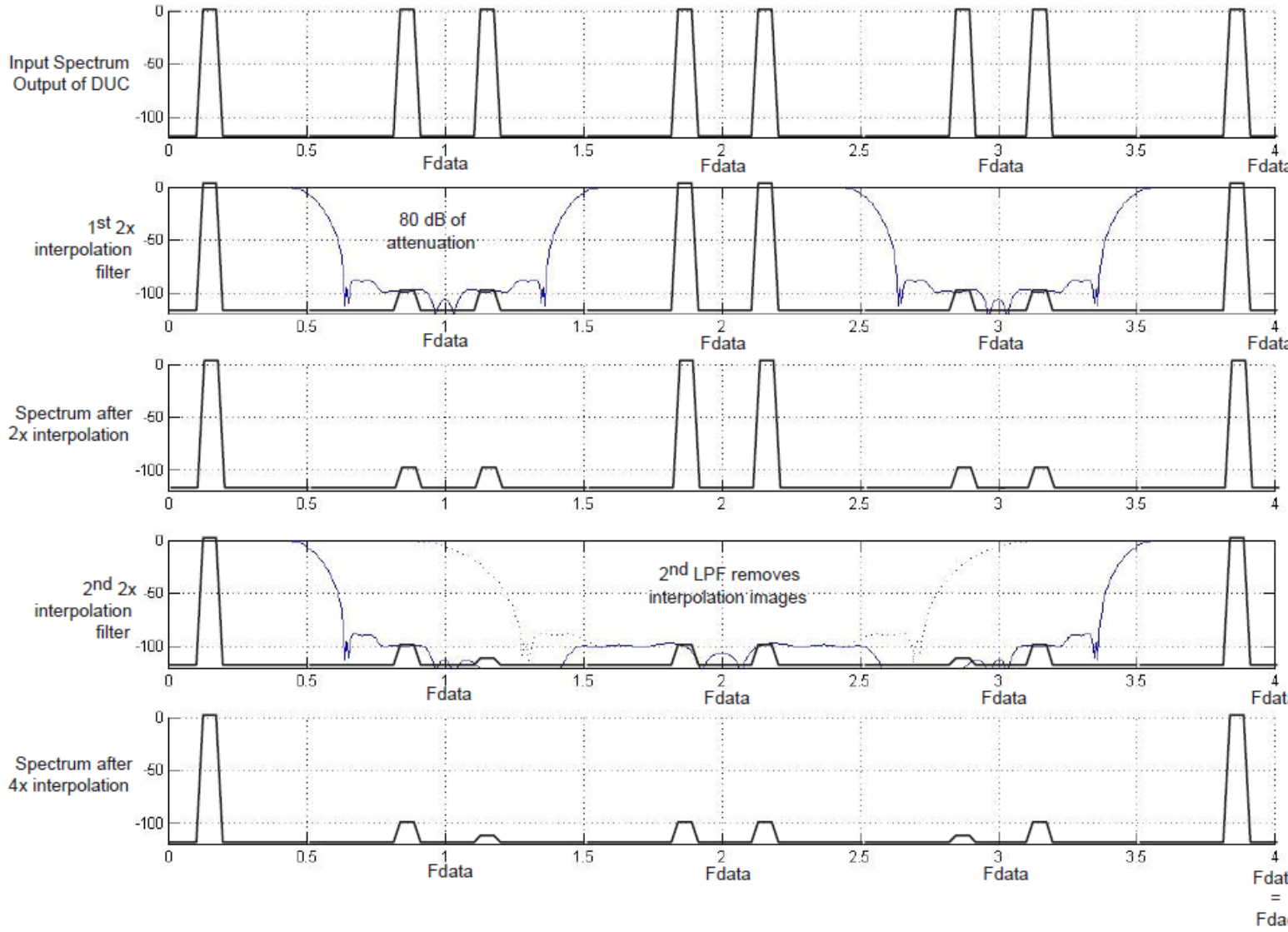
- Interpolation is used to:
  - Maintain reasonable input data rates; achieve higher output frequencies
  - Shift the DAC images further from the band of interest…easier filtering
  - Allow for a wider Nyquist zone for more flexible frequency planning
  - Reduces NSD as quantization noise is spread over a wider Nyquist band
- Input BW limited by interpolation filters
  - BW = 0.4 * F_{data}

Time Domain View of Interpolation

- 0's are inserted between the original samples
  - Adding a 0 does not change the spectral content, just sampling frequency
  - Widens the unique BW of the signal
- Low-pass (band-limiting) filtering fills in the missing levels between the original samples



Frequency Domain View of Interpolation



0 stuff the original signal to get 2 x F_{DATA}

Filter the signal to remove images

0 stuff the new signal to get 4 x F_{DATA}

Filter the signal to remove images

Final DAC output with F_{DAC} = 4 x F_{DATA}

DAC38RF8x Interpolation Options

	Filters Used						
Interpolation Rate	FIR0 (2x)	FIR1 (2x)	LPFIR0_5X	FIR2 (2x)	LPFIR0_3X	FIR3 (2x)	LPFIR1_3X
6	x				x		
8	x	x		x		x	
10	x		x				
12	x	x					x
16	x	x		x		x	
18	x				x		x
20	x	x	x				
24	x	x		x			x

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JESD Interface

- Supports up to 4 input IQ pairs
  - ‘RF80/83
    - Fdata(max) = 1500 MSPS
    - Resolution: 16, 12 bit
    - Int: 1, 2, 4
    - Lanes: 4, 8
  - ‘RF82
    - Fdata(max) = 3333 MSPS
    - Resolution = 16, 12, 8 bit
    - Int: 6, 8, 10, 12, 16, 18, 24
    - Lanes: 1, 2, 4, 8
- Max SerDes Rate
  - 12.5 Gbps

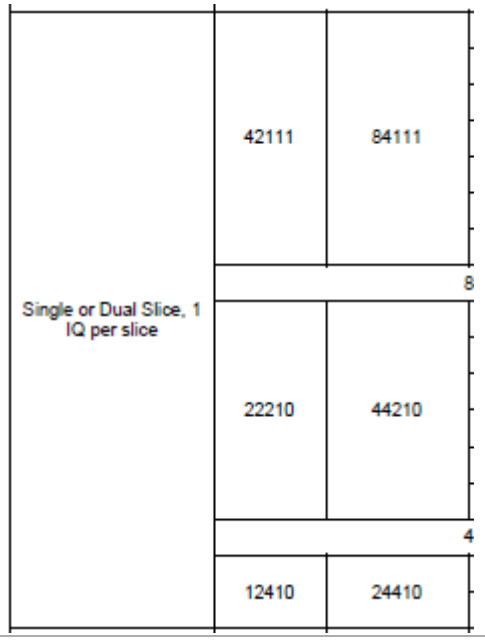
Category	New LMFSHd (1 slice)	New LMFSHd (2 slices)	Input Resolution	Complex	# input IQ's	Interp	Input rate max (MSPS)	Fdac Max (MSPS)
Wideband, Single Slice	81180	N/A	8	N	0	1	9000	9000
Wideband, Dual Slice I and Q in different slices	41380	82380	12	N	0	1	3333	3333
			12	N	0	2	3333	6666
	82380 above is just 41380 programmed in each SLICE							
	41121	82121*	16	N	0	1	2500	2500
			16	N	0	2	2500	5000
			16	N	0	4	2250	9000
	82121 above is 41121 programmed in each SLICE							
Single Slice Only, 1 IQ per slice	82121	N/A	16	Y	1	6	1500	9000
			16	Y	1	8	1125	9000
			16	Y	1	12	750	9000
			16	Y	1	16	562.5	9000
	82121 above is in one SLICE only.							
Single or Dual Slice, 1 IQ per slice	42111	84111	16	Y	1	6	1250	7500
			16	Y	1	8	1125	9000
			16	Y	1	10	900	9000
			16	Y	1	12	750	9000
			16	Y	1	16	562.5	9000
			16	Y	1	18	500	9000
			16	Y	1	24	375	9000
	84111 above is 42111 programmed in both SLICES.							
	22210	44210	16	Y	1	8	625	5000
			16	Y	1	12	625	7500
			16	Y	1	16	562.5	9000
			16	Y	1	18	500	9000
			16	Y	1	20	450	9000
			16	Y	1	24	375	9000
	44210 above is 22210 programmed in both SLICES.							
	12410	24410	16	Y	2	16	312.5	5000
			16	Y	2	24	312.5	7500
Single or Dual Slice, 2 IQ per slice	44210	88210	16	Y	4	8	625	5000
			16	Y	4	12	625	7500
			16	Y	4	16	562.5	9000
			16	Y	4	24	375	9000
	88210 above is 44210 programmed in both SLICES.							
	24410	48410	16	Y	4	16	312.5	5000
			16	Y	4	24	312.5	7500
	24310	48310	12	Y	2	24	375	9000

DAC38RF82

DAC38RF83/80

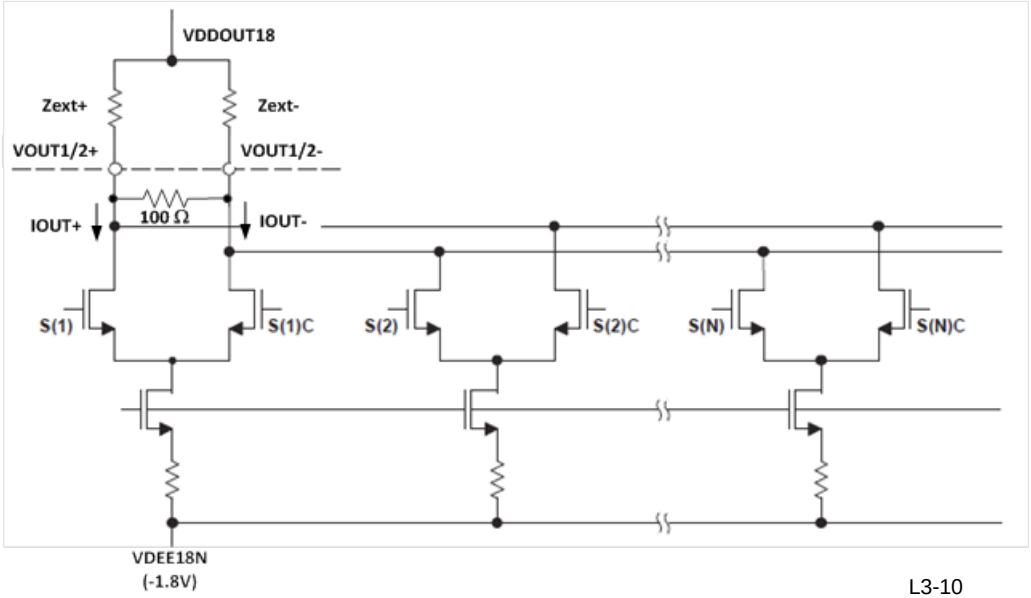
JESD204b Interface – Key Parameters

- Key Data Converter Parameters: LMFS
  - L # of lanes per converter device
  - M # of converters per device
  - F # of octets per frame (per lane)
  - S # of samples per converter per frame clock cycle
- Data Sheet provides lane mapping for desired modes/lanes
  - "L" = up to **8 lanes** at **12.5 Gbps** max rate
  - "M" = 2, 4, 8 effective converters
    - M= 2 Single slice, 1 IQ pair per slice
    - M= 4
      - Single slice, 2 IQ pair per slice
      - Dual slice, 1 IQ pair per slice
    - M= 8 Dual slice, 2 IQ pair per slice



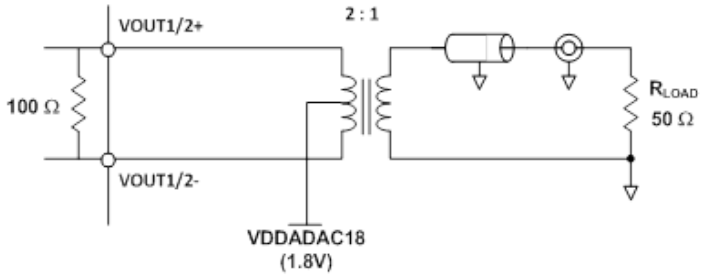
Output Network – Internal Structure

- Output Network
  - DAC38RF82/83 Diff Output Integrated 100 ohm impedance
  - DAC38RF80 SE Output Integrated balun
- Full Scale Current
  - $IOUT_{FS} = I_{RBIAS} + I_{coarsetrim}$
    - $I_{RBIAS} = 32\ mA$
    - $I_{Coarsetrim} = 2 \times (\boldsymbol{DACFS} - 11)$ where ***DACFS****= [0:15] (SPI Programmable)*
  - $IOUT_{FS} = 40$ mA (max)
- Output Current
  - $IOUT_{+} = IOUT_{FS}\left(\frac{Code}{2^{14}}\right)$
  - $IOUT_{-} = IOUT_{FS}\left(\frac{1-Code}{2^{14}}\right)$

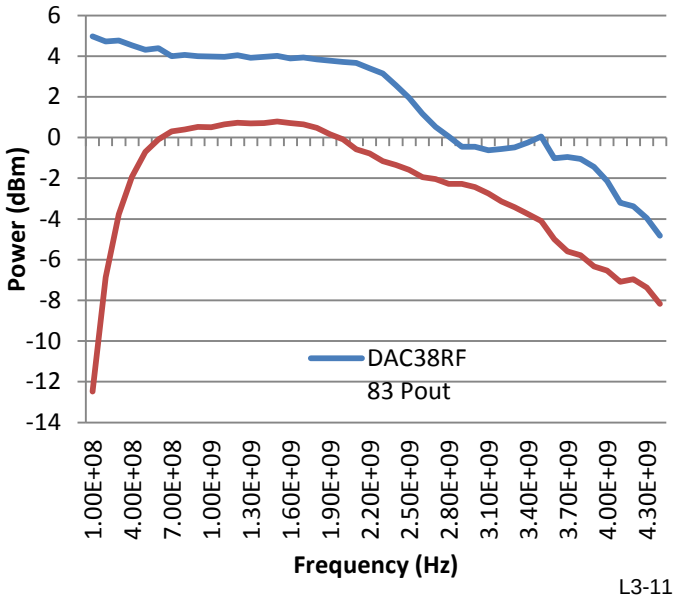


Output Network – External Structure

- DAC38RF83/82
  - Output Load:
    - 100Ω (int) // 100Ω load = 50Ω
    - 1.8V common mode voltage
  - Maximum Signal Swing (per leg): 1 Vpp
  - Max output power: 7 dBm (ideal)

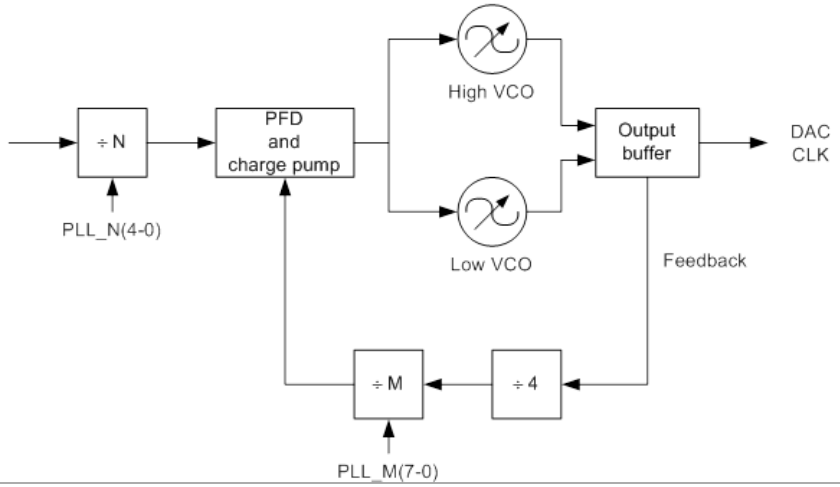


- DAC38RF80
  - Frequency Range: 700 MHz – 3800 MHz
  - Max output power: 4 dBm (target)



Clocking Options/PLL

- Sample Clock
  - Frequency range: 100 MHz to 9 GHz
  - Single ended and differential clocking inputs available
  - Use high clock input power (>6dBm) to reduce low order clock mixing products (Fs/2,Fs/4, Fs/8 and Fs/16):below -78dBc
- On-chip PLL
  - VCO1= 8.16GHz to 9.75GHz (target) 7.7GHz to 8.9GHz (actual)
  - VCO0 = 5.38GHz to 6.42GHz (target) 5.38GHz to 6.42GHz (actual)
    - Modified/corrected in final silicon
  - PFD Frequency <600MHz



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End of Lecture 3

1.0 **Session #2** Objective: **Set-up RF DAC output at 1960 MHz and capture with the RF ADC**

2.0 Initial hardware set-up

2.1 TSW14J56 (#2) EVM connections

2.1.1 Connect DAC38RF80 EVM

2.1.2 Connect 5V power jack

2.1.3 Connect USB3.0 cable from computer to J9

2.2 DAC38RF80 EVM connections

2.2.1 Connect 5V power jack

2.2.2 Connect USB cable

2.2.3 Connect ADC32RF80 EVM Clock output (J13) to DAC38RF80 EVM LMK CLKIN (J4)

2.2.4 Ensure that JP10 is disengaged

2.2.5 Connect RF cable from IOUTA_SE (J7) to filter and then to ADC32RF80 EVM Channel B input.

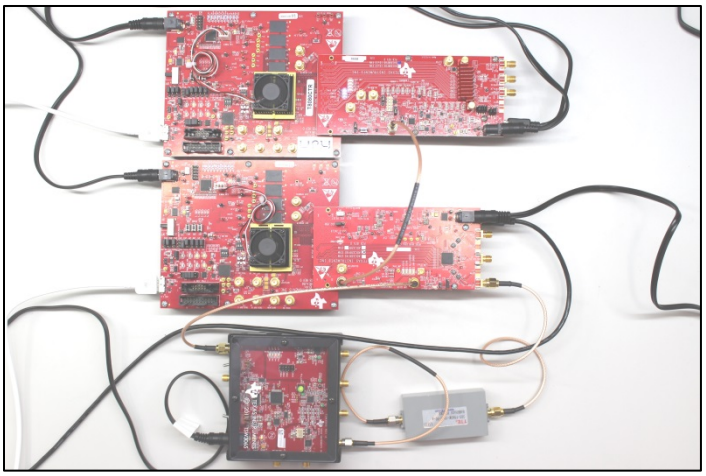


Figure 2.0: Hardware Set-up

3.0 Software setup

3.1 ADC32RFxx GUI> *LMK04828* tab> *Clock Outputs* tab

3.1.1 On CLKout 10 and 11 column de-select “Group Powerdown”

3.1.2 Verify DCLK Divider is set to: 8

3.2 DAC38RF80

3.2.1 Launch DAC38RF8x GUI

3.2.2 Verify USB status is green; if not, select “Reconnect FTDI”

3.2.3 On *QuickStart* tab

a) Toggle “DAC RESETB Pin”

b) Press “Load Default” button

c) Set on-chip PLL Registers for 8847.36 MHz clock

i. Toggle “PLL Enable” button

ii. Change M value to: 6

iii. Change “Ref Freq (MHz)” to 368.64

d) DAC Mode Registers
   i. Change "# of DACs" to "Dual DAC"
   ii. Change "# of Pairs per DAC" to "1 IQ pair"
   iii. Verify "# of serdes lanes per DAC" is set to 4
   iv. Change "Desired Interpolation" to "18x"
e) Press "CONFIGURE DAC"
f) Press "PLL AUTO TUNE"
g) Press "RESET DAC…TRIGGER"

3.2.4 Confirm PLL is locked
a) Select *DAC38RF8x* tab > *Clocking* tab
b) Press "Check Loop Filter Voltage" button
c) Verify *PLL LF Voltage* value changes from 0 to: 3, 4, or 5

3.2.5 Select *DAC38RF8x* tab > *Digital(DACA)* tab
a) Mixer Registers
   i. Toggle Path AB to: on
   ii. Set Mixer Gain to: 6 dB
b) NCO Registers
   i. Toggle Path AB to: on
   ii. Set NCO Frequency to: 1960
   iii. Press "Update NCO"

3.2.6 Select *DAC38RF8x* tab > *Digital(DACB)* tab
a) Mixer Registers
   i. Toggle Path AB to: on
   ii. Set Mixer Gain to: 6 dB
b) NCO Registers
   i. Toggle Path AB to: on
   ii. Set NCO Frequency to: 1940
   iii. Press "Update NCO"
c) Select *Quick Start* tab; Press "RESET DAC…TRIGGER"

3.3 HSDC Pro

3.3.1 Instrument Options>Disconnect from Board
3.3.2 Instrument Options>Connect to Board
3.3.3 Select the serial number of the 'J56 connected to the RF DAC EVM; press "OK".
3.3.4 Select DAC tab
3.3.5 Load "DAC38RF8x_LMF_841_RevD" ini file
3.3.6 Change Data Rate (SPS) field to: 491.52M (Fclk/Int)
3.3.7 Change DAC Option to: 2's Compliment

3.3.8 I/Q Multitone Generator

a) Set Tone BW to: 1

b) Set # to: 1

c) Set Tone Center to: 0

d) Set Tone Selection to: Complex

e) Press “Create Tones” button

3.3.9 Press “Send” button; click “OK” if window pops up

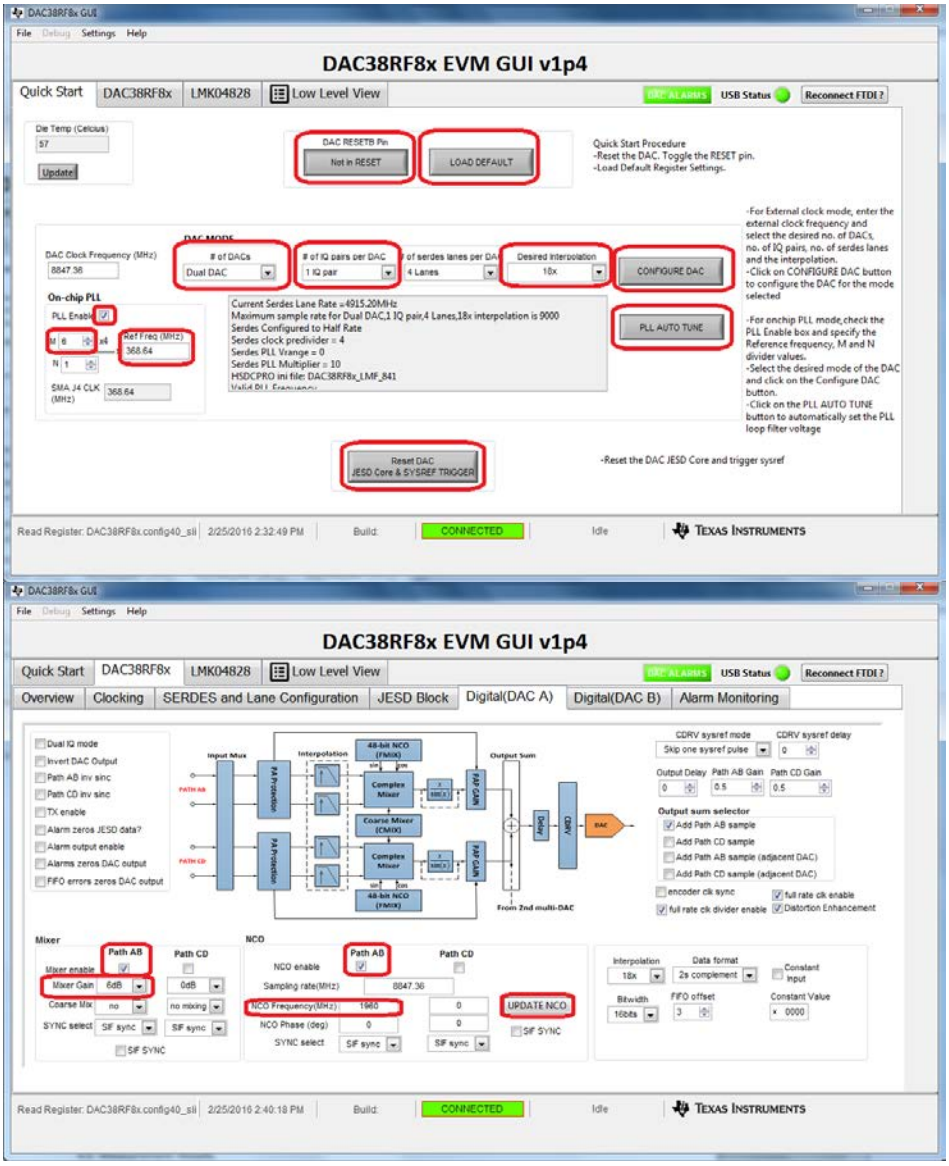


Figure 2.1: ADC32RF8x GUI settings

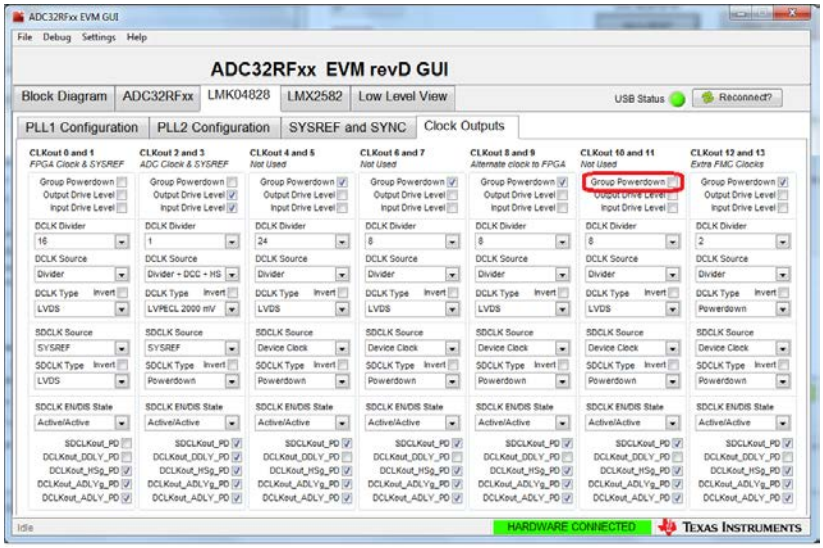


Figure 2.2: ADC32RFxx GUI: set clock divider output

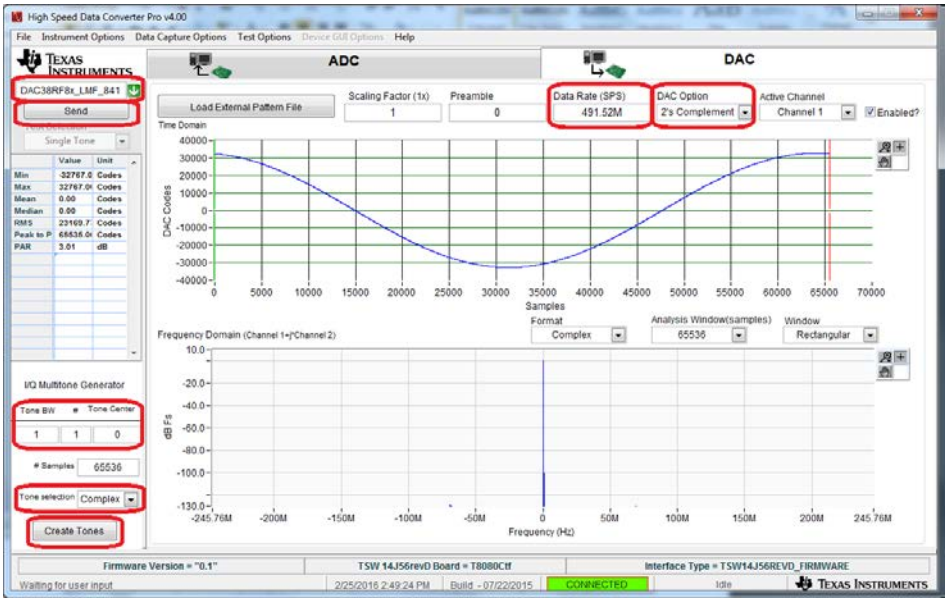


Figure 2.3: HSDC Pro (RF DAC) software settings

4.0 Measurement Results

4.1 Switch HSDC Pro to ADC

4.1.1 Instrument Options>Disconnect from Board

4.1.2 Instrument Options>Connect to Board

4.1.3 Select the serial number of the 'J56 connected to the RF ADC EVM; press "OK".

4.2 Re-set-up ADC Configuration

4.2.1 Change to "Channel 5/8"

4.2.2 Toggle ADC Output Setup icon

a) Click "Enable?"

b) Change ADC Sampling rate to: 2949.12M

c) Change ADC Input Frequency to: 1960M

d) Change NCO to: -1859.985M

e) Change Decimation to: 8

f) Press "OK"; press "OK" on the pop-up window

4.3 Press "Capture" button

4.4 Verify that you get a signal at same frequency as before (100 MHz)

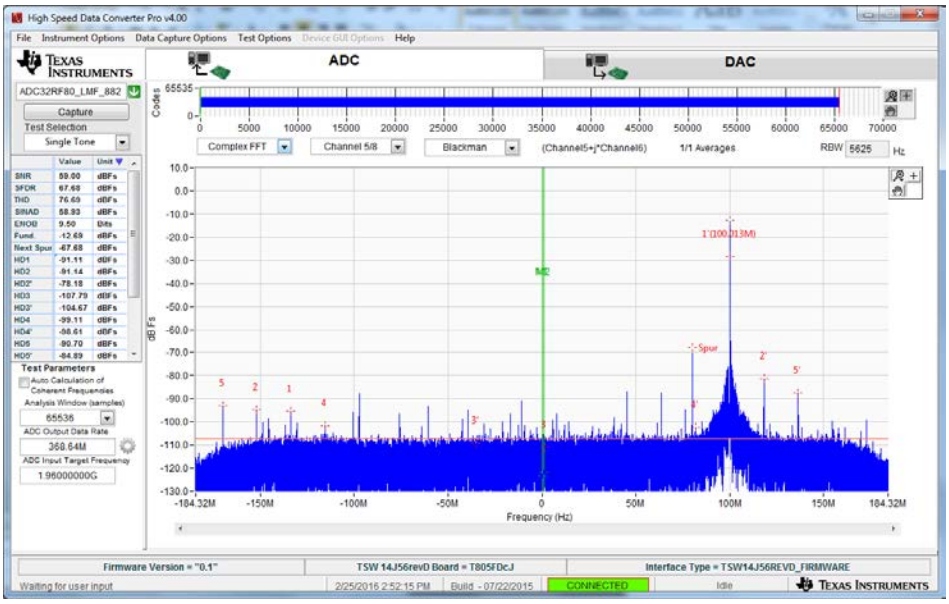


Figure 2.4: Capture Results

5.0 Additional experiments

5.1 Signal Observations

5.1.1 What is the fundamental power level?

5.1.2 Increase DAC output power

a) Go to *DAC38RF8x* tab > *Overview* tab

b) Increase Coarse DAC Gain to 15

c) Press "Capture" again on HSDC Pro

d) How much did the fundamental power change?

5.2 Spurious output

5.2.1 What is the spurious output at around 80 MHz?

5.2.2 "Move" the spurious frequency to 40 MHz.

5.3 Spread around the fundamental

5.3.1 What is the source of the noise hump around the fundamental?

5.3.2 Eliminate the noise around the fundamental

a) HSDC Pro>Test Options>Notch Frequency Bins

b) Change "Number of bins…" to: 2500

c) Press "OK"

d) How did the SNR change as a result?

e) Change notch bins back to: 100

5.4 Change the Power level

5.4.1 *DAC38RF8x* tab > *Digital(DACA)* tab > Mixer Gain = 0 dB

5.4.2 HSDC Pro > "Capture"

5.4.3 How much does the fundamental power change?

5.4.4 Change back;

a) *DAC38RF8x* tab > *Digital(DACA)* tab > Mixer Gain = 6 dB

b) HSDC Pro > "Capture"

***** Leave set-up as-is for use in the next session *****

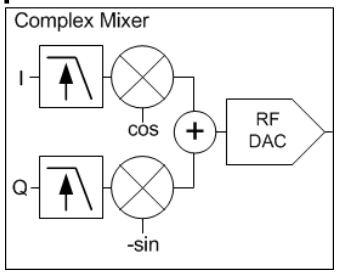
Texas Instruments

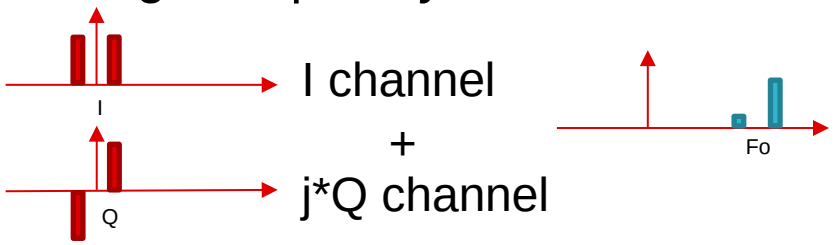
DAC38RF8x DUC Features

Lecture 4

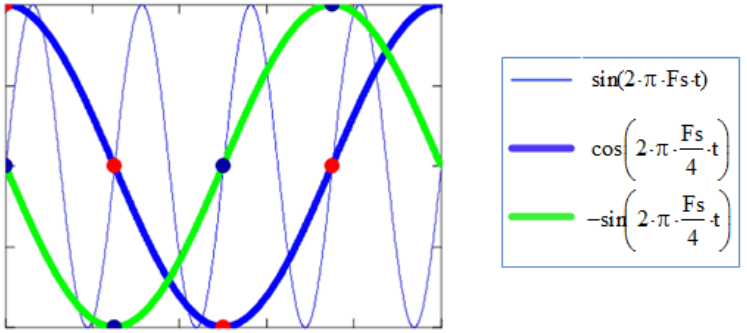
Digital Mixers: Coarse Mixers

- Complex mixers naturally suppress image frequency





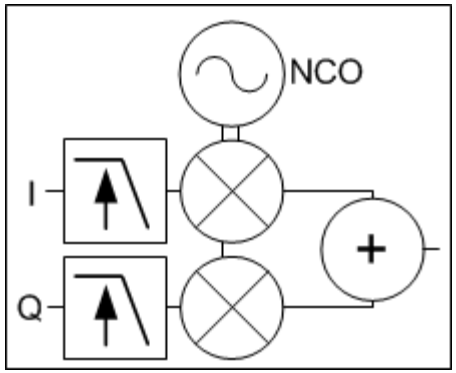
- Fixed oscillator frequency based on sampling rate: Fs/2, Fs/4, -Fs/4
  - sin & cos terms simplify to -1, 0, 1
  - e.g. Fs/4 case:

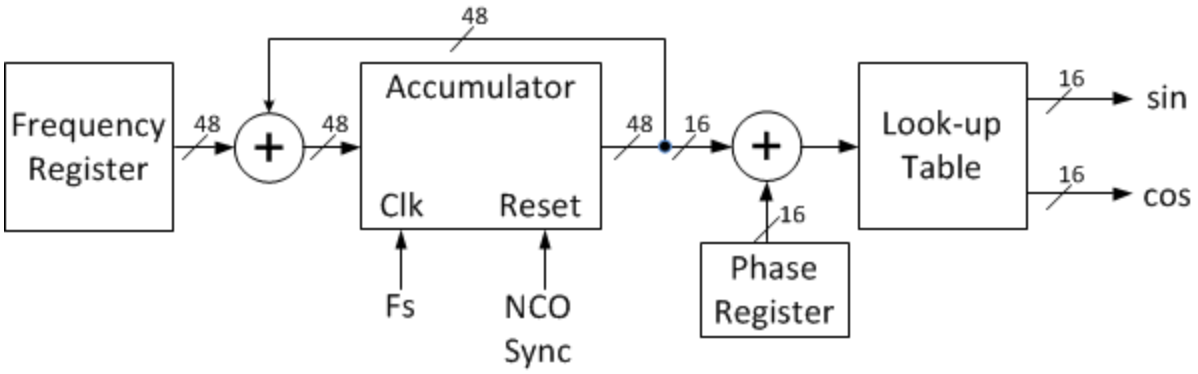


- Device supports: +/-Fs/4, Fs/2, Fs/8, 3Fs/8, 5Fs/8 and 7Fs/8
- The coarse mixers use less power than the NCO because the mixing sequences are simple combinations of +/- I and +/- Q

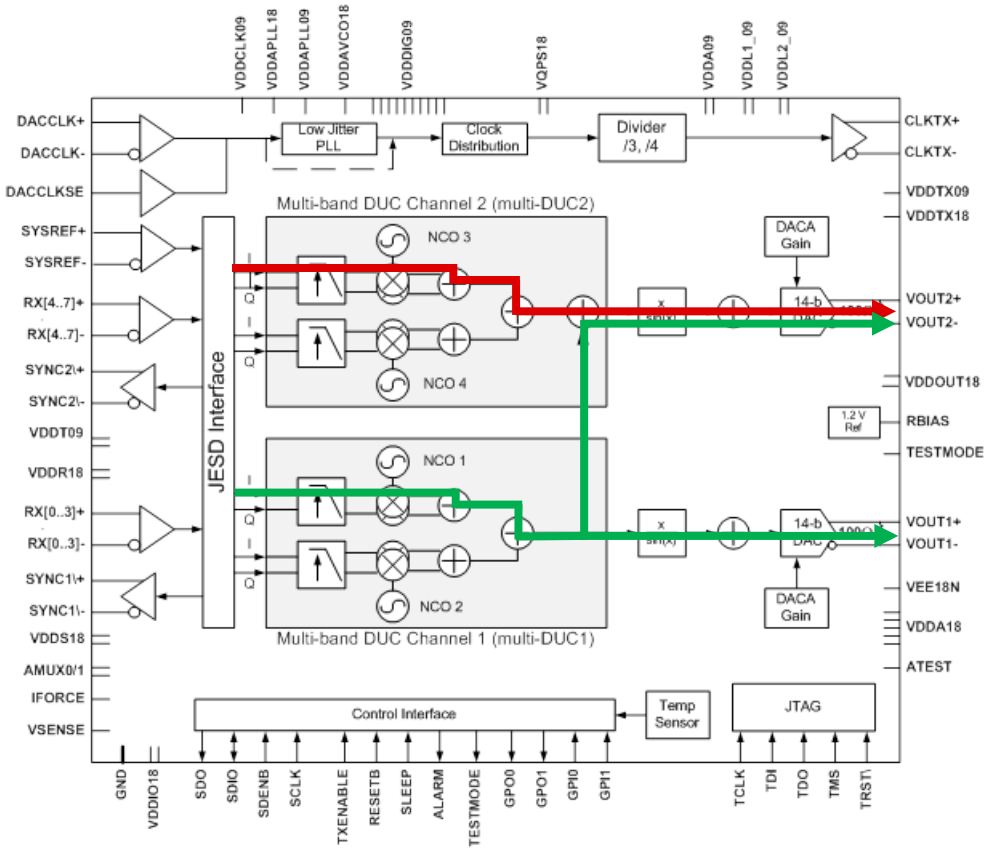
Full Complex Mixer (NCO)

- The full complex mixer uses a fine resolution numerically controlled oscillator to provide sub-hertz shifting of the digital signal
  - Shift signal to arbitrary frequency location within output sample clock Nyquist zone
  - Shift signal to proper RF frequency band / RF Channel
  - NCO takes the place of tunable frequency synthesizer in RF mixer to shift signal to desired IF band.
- A look-up table containing a digital sine wave is used for quick generation of the mixing frequency





Modes of Operation: Real Input



Single / Dual DAC

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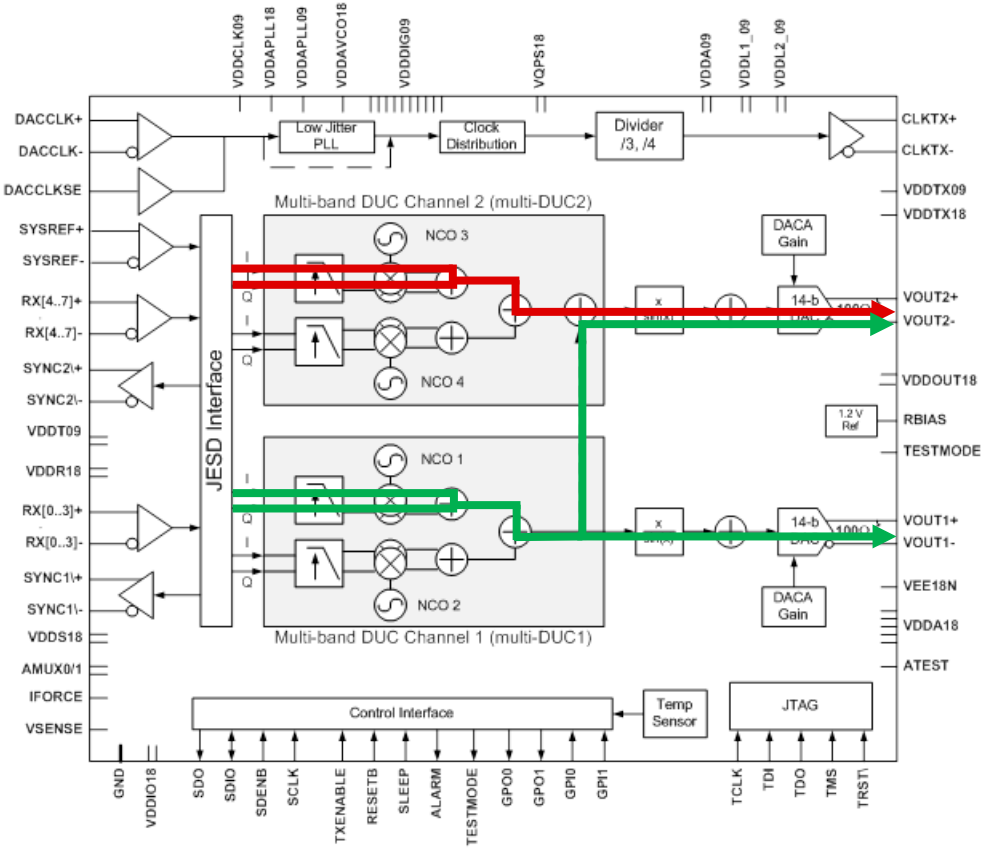
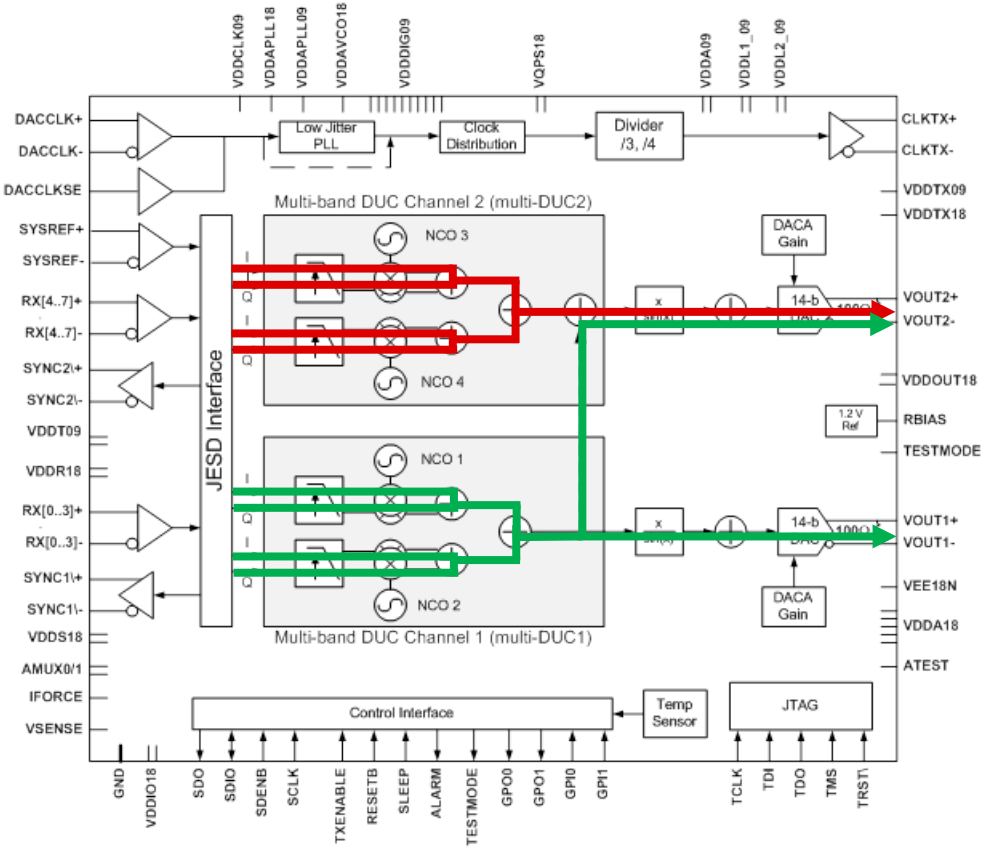
Modes of Operation: 1 IQ pair



Single / Dual DAC

Texas Instruments

Modes of Operation: 2 IQ pairs



Single / Dual DAC

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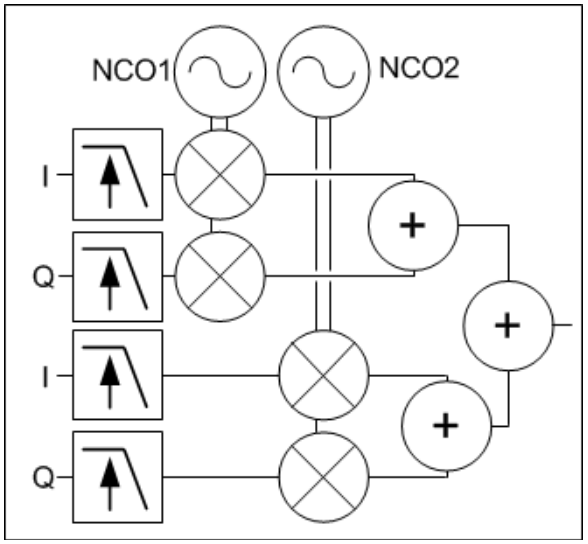
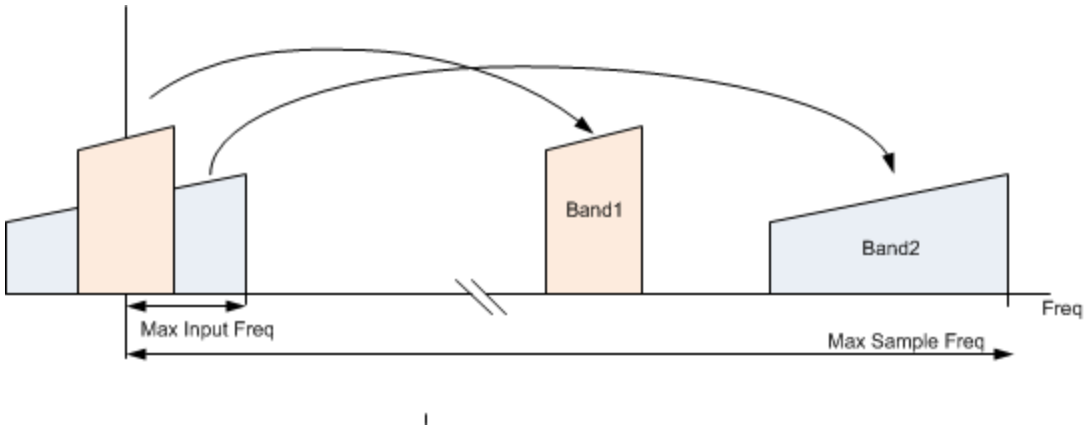
Multiple NCO – Multi-Band

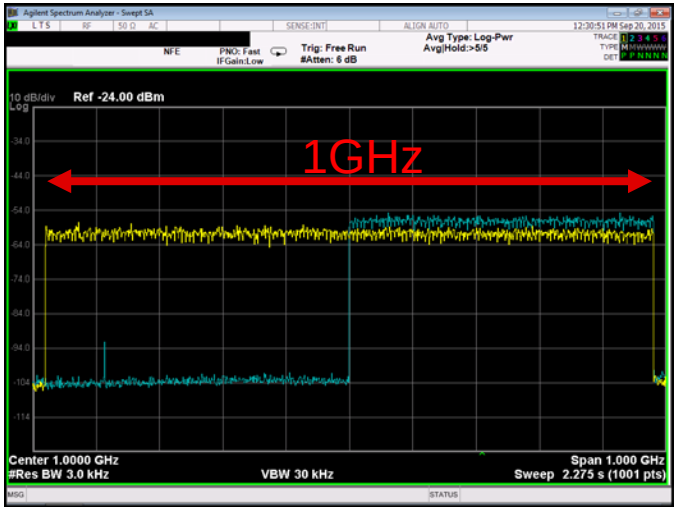
- Include multiple NCOs to tune separate channels to arbitrary RF frequency location
  - Supports non-contiguous multi-carrier operation
  - Supports multi-band or multi-mode operation
- Keeps input data rates low; sufficient to meet bandwidth requirements of each signal
- Supports very wide effective output bandwidth

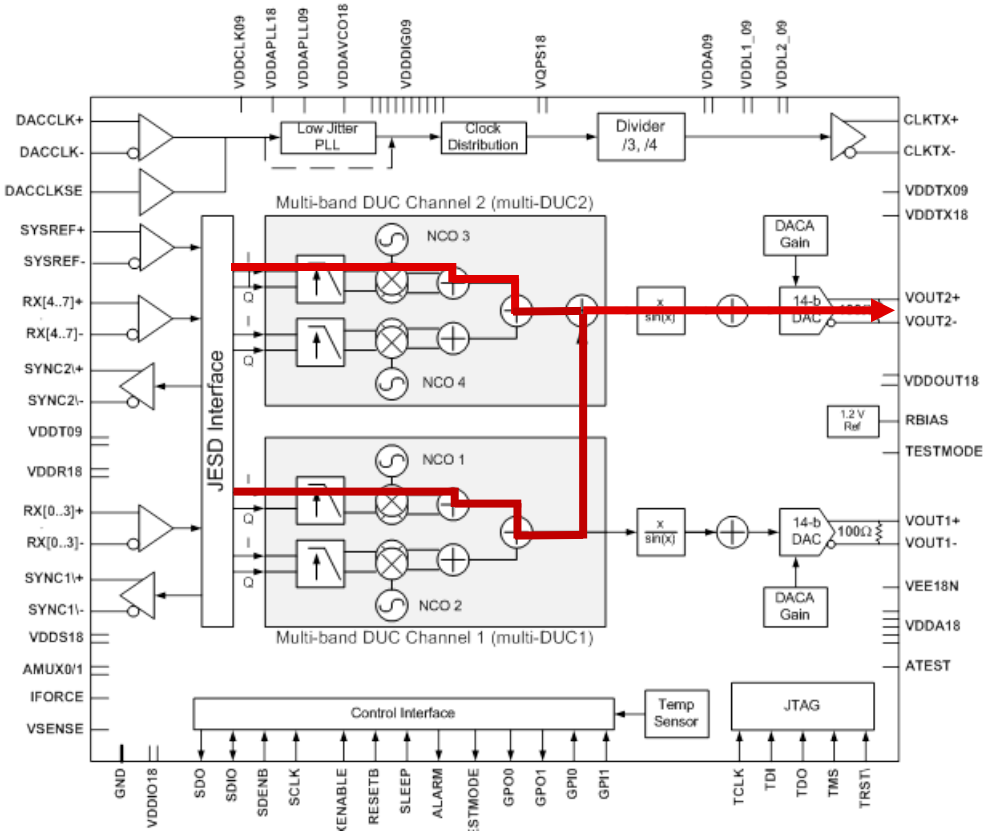




Wideband Mixing (DAC38RF82)

- Send separate I/Q data to each converter
  - I-data
    - slice0
    - NCO phase = 0^o
  - Q-data
    - slice1
    - NCO phase is set to 90^o
- Total BW = 1 GHz





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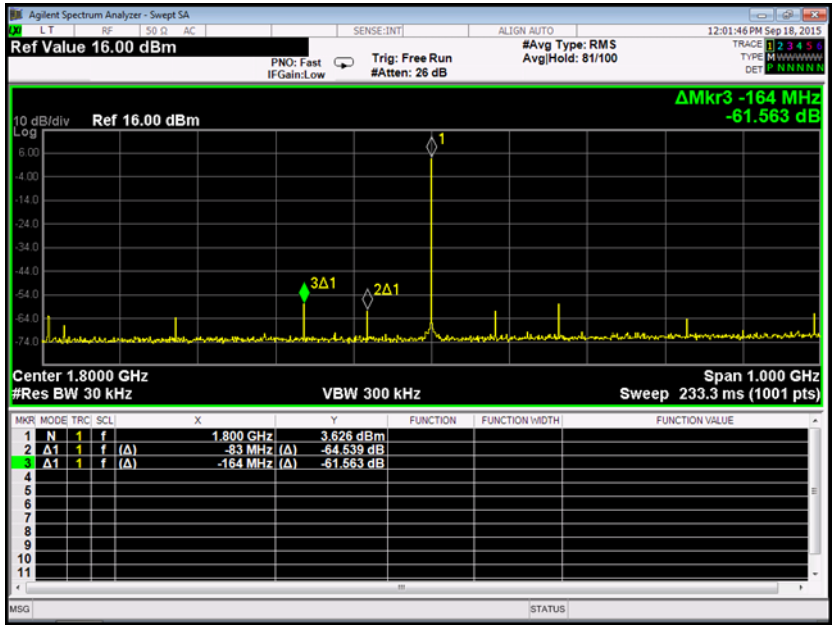
Interpolation and Clock Mixing Products

- Spurs located at $\frac{+/-Fclk}{n}$ offset the output signal frequency
- Isolation improvement achieved with modified substrate and with final silicon.
- Example: 24x interpolation
  - Anticipate CMP at Fs/192, Fs/96, Fs/48, Fs/24
  - Typically CMP > 70 dBc

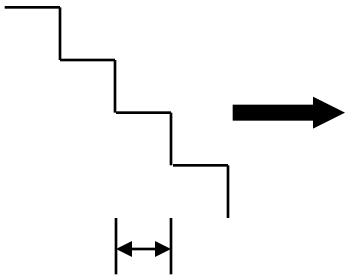
Interpolation	n			
6	48	24		
8	64	32	16	
10	80	20		
12	96	48	24	
16	128	64	32	16
18	144	72	24	36
20	160	80	20	
24	192	96	48	24



Inverse SINC filter

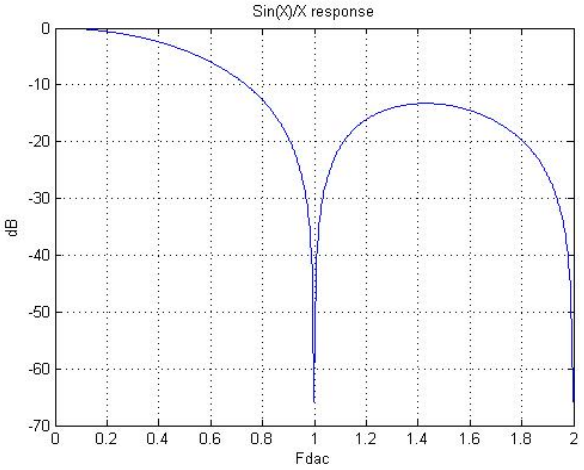
- Digital pre-emphasis filter corrects for the expected SINC response
- The Inverse SINC filter will create a flat spectrum out to 0.4 * F_S
- Corrects SINC response only in 1st Nyquist Zone
- May need to back-off input signal to avoid digital clipping

DAC S/H output time domain

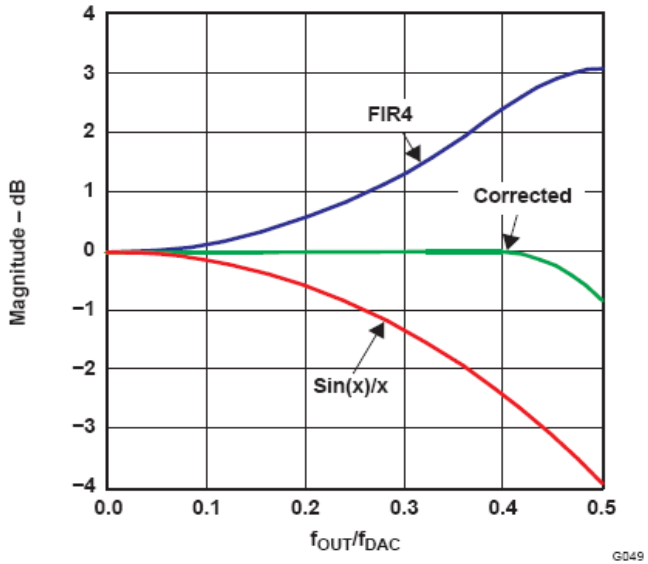


T=1/Fdac

S/H time domain results in SinX/X response Frequency domain

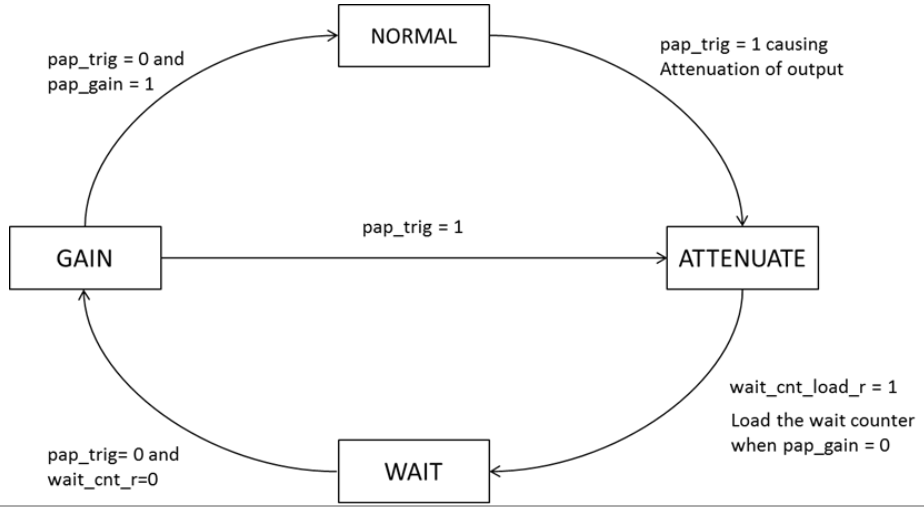


SinX/X correction Filter



Power Amplifier Protection (PAP)

- Normal state:
  - Monitors the average amplitude of input data and compares with threshold
  - The threshold value is set through SPI. When average amplitude exceeds threshold then trigger Attenuation state
- Attenuate state:
  - The PAP gain is ramped down to zero
- Wait state: Wait time between the Attenuate and Gain states
- Gain state: Ramps up the PAP gain to 1 to restore back to Normal



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End of Lecture 4

1.0 **Session #3** Objective: **Exercise the DAC38RF8x Digital Up-Converter (DUC) features**

2.0 Initial hardware set-up

- 2.1 TSW14J56 (#2): Keep same connections from Session #2
- 2.2 DAC38RF80 EVM: Keep same connections from Session #2

3.0 Software setup

- 3.1 ADC32RFxx: Keep same set-up as Session #2
- 3.2 HSDC Pro (RFDAC); modify the following from Lab Session #2
  - 3.2.1 Switch to HSDC Pro (RFDAC)
    - a) Instrument Options>Disconnect from Board
    - b) Instrument Options>Connect to Board
    - c) Select the serial number of the 'J56 connected to the RF DAC EVM; press "OK".
    - d) Select DAC tab
  - 3.2.2 Load "DAC38RF8x_LMF_882_RevD" Ini file
  - 3.2.3 Change Data Rate (SPS) field to: 368.64M (Fclk/Int)
  - 3.2.4 I/Q Multitone Generator> Press "Create Tones" button
  - 3.2.5 Press Send; hit "OK" on the pop-up window
- 3.3 DAC38RF80
  - 3.3.1 On *Quick Start* tab
    - a) # of IQ Pairs per DAC > 2 IQ Pairs
    - b) Desired Interpolation > 24
    - c) Press "Configure DAC"
    - d) Press "PLL Auto Tune"
    - e) Press "Reset DAC…Trigger"
  - 3.3.2 On *DAC38RF8x* tab> *Overview* tab: Set *Coarse DAC Gain* = 15
  - 3.3.3 On *DAC38RF8x* tab> *Digital(DAC A)* tab
    - a) Mixer: enable Path CD
    - b) Mixer: Change Path CD Mixer Gain to 6 dB
    - c) NCO: enable Path CD
    - d) NCO: change Path CD frequency to 1940
    - e) Press "Update NCO"
    - f) Output sum selector: toggle "Add Path CD sample"
- 3.4 HSDC Pro (RFADC)
  - 3.4.1 Switch back the HSDC Pro for RFADC
    - a) Instrument Options>Disconnect from Board
    - b) Instrument Options>Connect to Board
    - c) Select the serial number of the 'J56 connected to the RF ADC EVM; press "OK".
  - 3.4.2 Re-set-up ADC Configuration
    - a) Change to "Channel 5/8"

b) Toggle ADC Output Setup icon

i. Click “Enable?”

ii. Change ADC Sampling rate to: 2949.12M

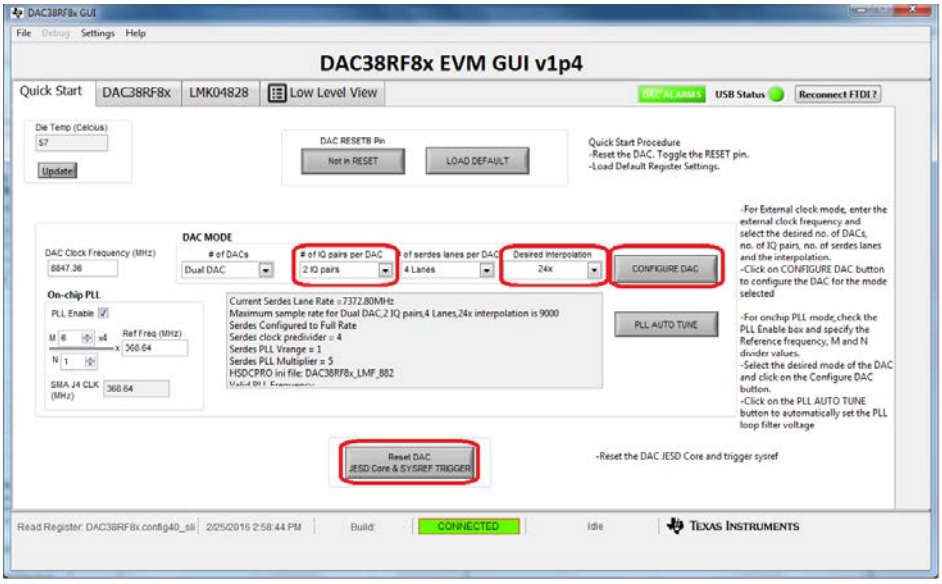
iii. Change ADC Input Frequency to: 1960M

iv. Change NCO to: -1859.985M

v. Change Decimation to: 8

vi. Press “OK”; press “OK” on the pop-up window

3.4.3 Press “Capture” button



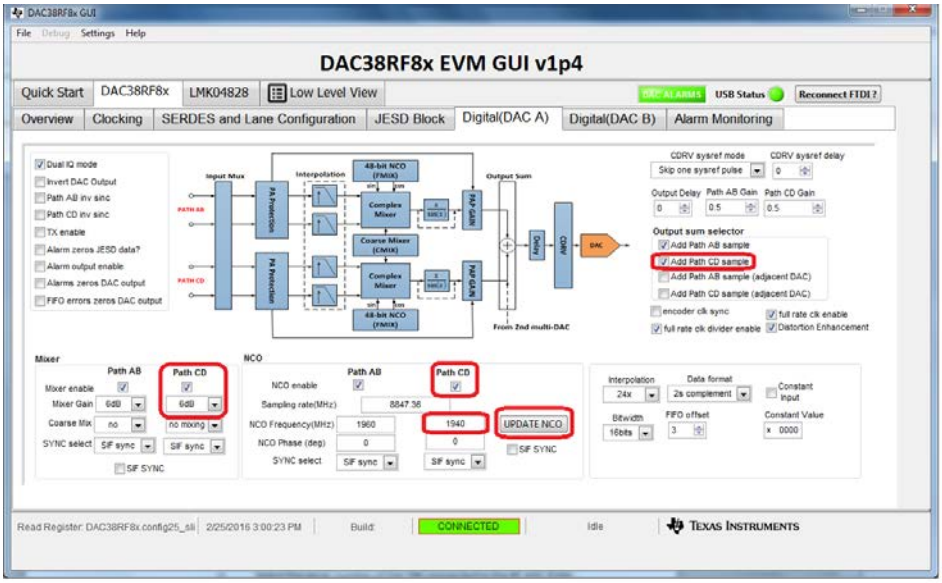


Figure 3.0: DAC38RFxx GUI Settings

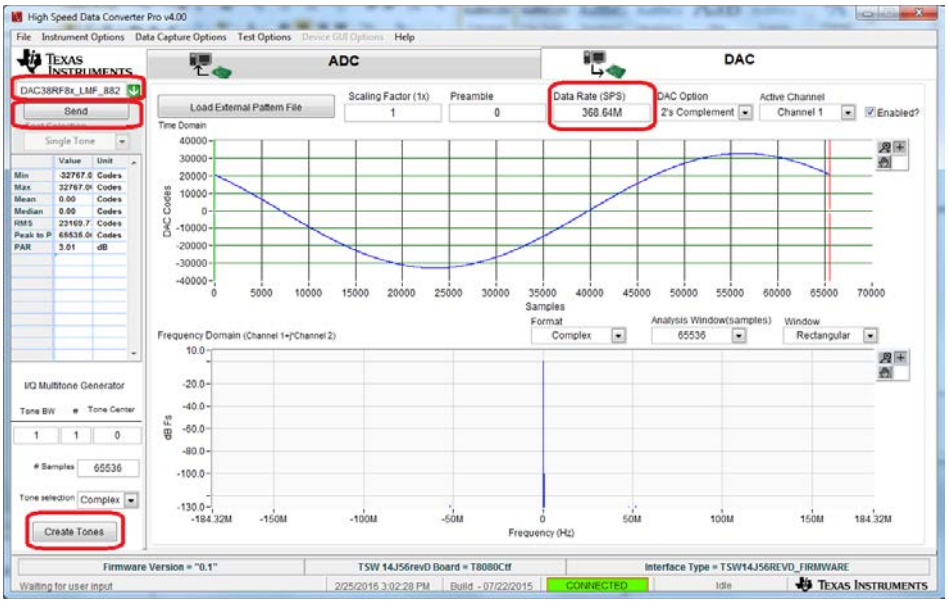


Figure 3.1: HSDC Pro (RF DAC) software set-up

4.0 Measurement results

4.1 Verify that you get a clean capture

4.2 Signal Observations

4.2.1 What is the “spur” that is designated in the spectrum?

4.2.2 Is that tone at the frequency expected?

4.2.3 What are the “spurs” that are 20 MHz above and below the tones?

4.3 Set-up for 2-tone observation

4.3.1 HSDC Pro (RFADC): Change Test Selections to: Two Tone

4.3.2 Change ADC Input Target Frequency to: 100M

4.3.3 Change ADC 2nd Input Frequency to: 80M

4.3.4 What is the power level of the fundamental tones?

5.0 Additional measurements

5.1 Move the frequency

5.1.1 DAC38RF8x GUI

a) Change *Digital(DAC A)>NCO>NCO Frequency (MHz)* [Path CD]: 1870

b) Press “Update NCO”

5.1.2 HSDC PRO (RFADC): Press Capture

a) Where did the tone show up? Is this expected?

b) Change “ADC 2nd Input Frequency” to: 10M

c) What are the levels of the tones?

d) Why is it F2 amplitude lower than F1? Is this expected?

e) How much bandwidth is represented by this configuration?

5.1.3 What is the IMD3 level in dBc?

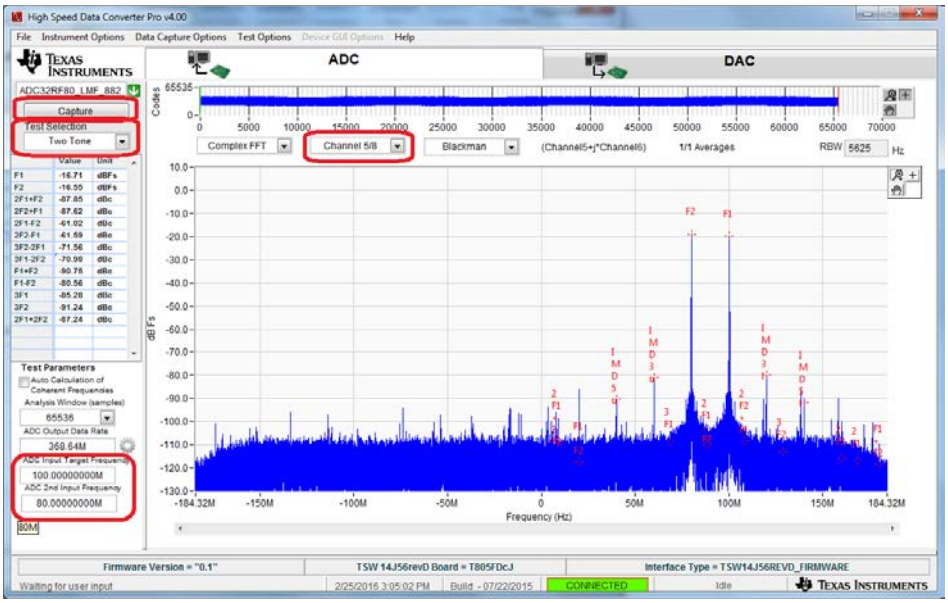


Figure 3.2: HSDC Pro (RF ADC) software set-up/results

5.2 Engage DACB side

5.2.1 DAC38RF8x GUI

a) *DAC38RF8x* tab>*Digital(DACB)* tab> Mixer

i. Toggle Path CD on

ii. Change *Mixer Gain* to: 6dB

b) *DAC38RF8x* tab>*Digital(DACB)* tab> NCO

i. Toggle Path CD on

ii. Change Path CD Frequency to: 1820

iii. Change Path AB Frequency to: 1900

iv. Press “Update NCO” button

c) *DAC38RF8x* tab>*Digital(DACA)* tab> Output Sum Selector:

i. Toggle “Add Path AB sample” to: Off

ii. Toggle “Add Path CD sample” to: Off

iii. Toggle “Add Path AB sample (adjacent DAC)” to: On

iv. Toggle “Add Path CD sample (adjacent DAC)” to: On

5.2.2 HSDC Pro (RFADC)> Press “Capture” button

a) Where are the tones located?

b) Modify the HSDC Pro ADC input target frequencies to determine the tone levels.

5.3 Combine Both Channels

5.3.1 DAC38RF8x GUI> *DAC38RF8x* tab>*Digital(DACA)* tab> *Output sum selector*

a) Toggle “Add Path AB sample” to: On

b) Toggle “Add Path CD sample” to: On

5.3.2 HSDC Pro (RFADC): Press “Capture” button

5.3.3 Verify that you can see all four tones in the spectrum

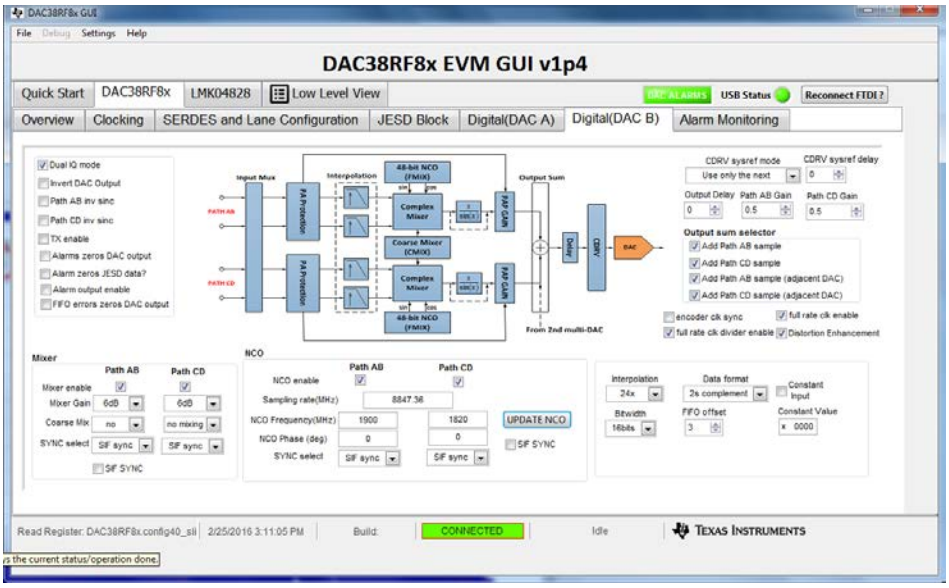


Figure 3.3: DAC38RFxx GUI adjusted set-up

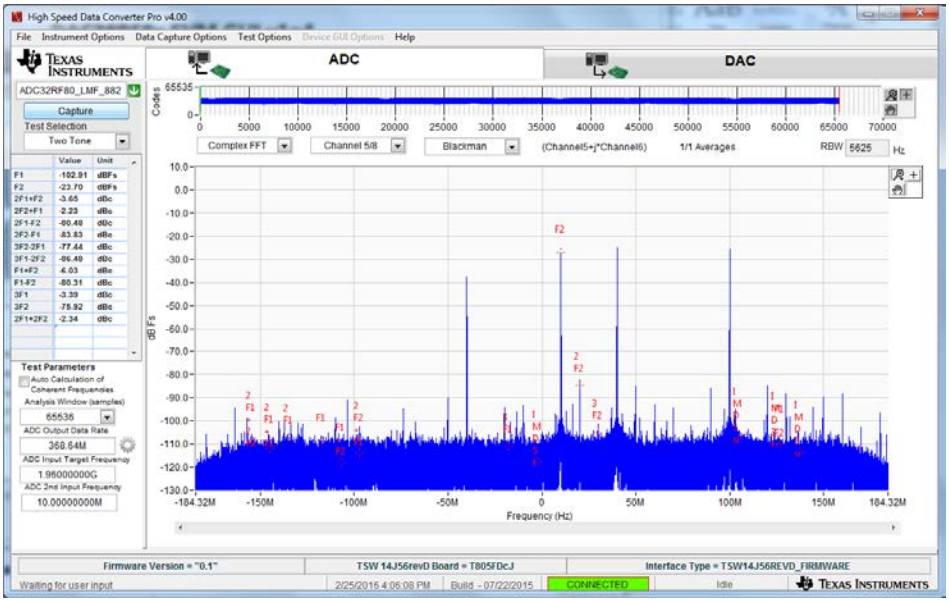


Figure 3.4: Measured results

***** Leave set-up as-is for use in the next session *****

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ADC32RFxx DDC Features

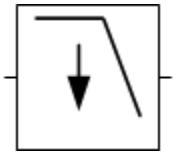
Lecture 5

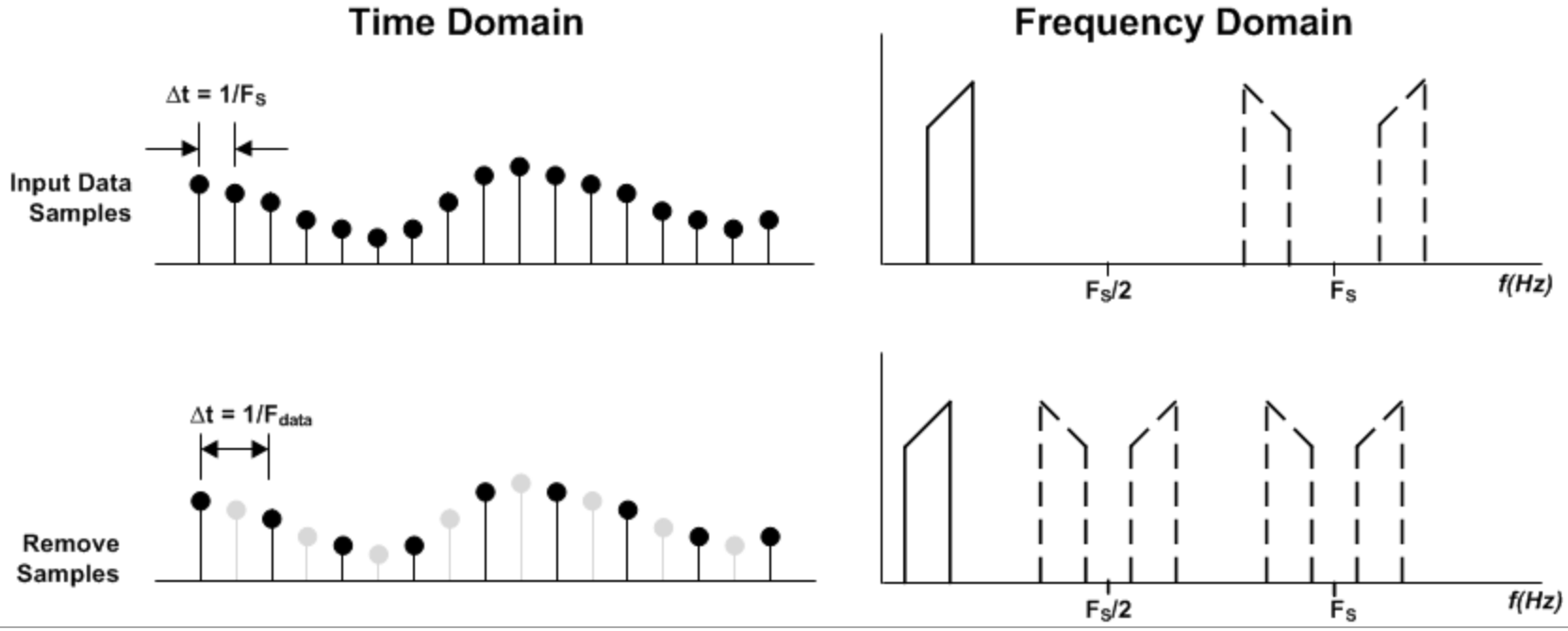
What is Decimation?

- Decimation decreases the sample rate of a signal by removing samples from the data stream
- Decimation includes digital low pass (anti-aliasing) filter followed by a decimator
  - The operation is equivalent to utilizing an analog anti-aliasing filter at fc = F_S /2M and sampling a converter at F_d = F_S /M, where M = decimation count (i.e. 2)
- Decimation is used to:
  1. Decrease the ADC data rate to reasonable levels for data capture
  2. Maintain high output sampling rate for more flexible frequency planning
  3. Take advantage of decimation filtering for improved spectral performance

Time/Freq Domain View of Decimation

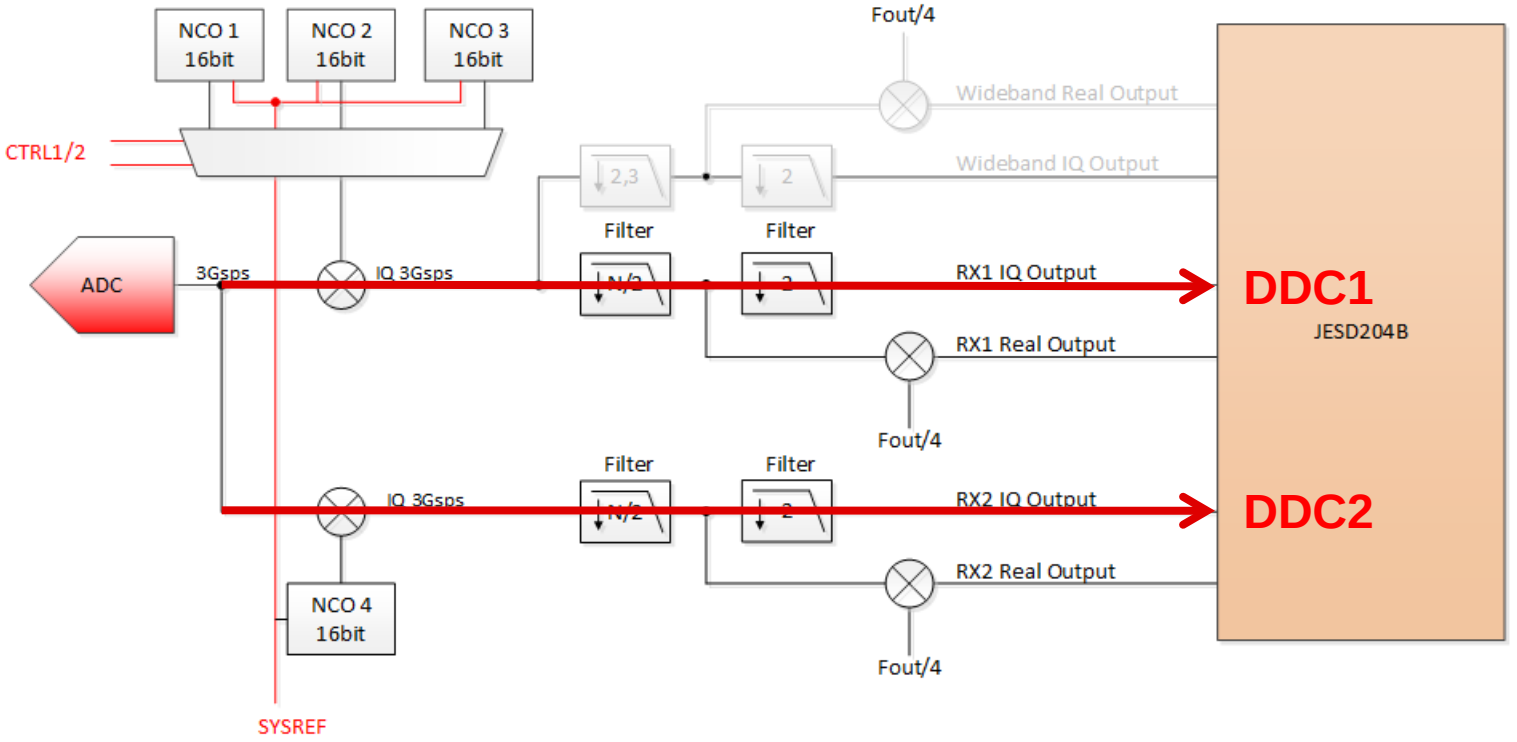
- Images created with each decimation
- Low Pass filter provides anti-aliasing protection
- Data rate reduced for easier processing





Digital Down Converter (DDC) - Receiver
Single/Dual Complex DDC

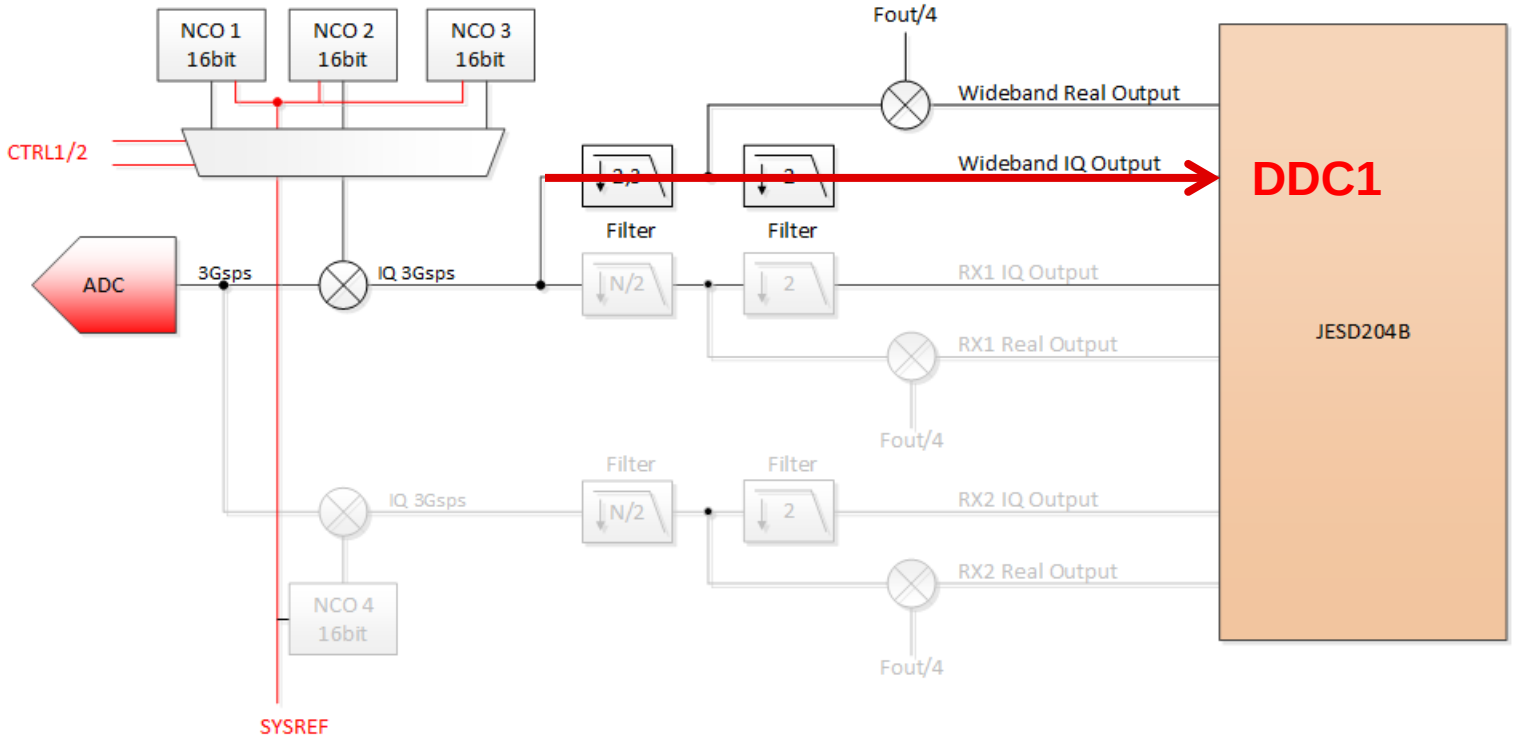
- Single or Dual complex Digital Down Converter
- Decimation modes: 8, 9, 10, 12, 16, 18, 20, 24, 36



DDC – Wideband Receiver

Single Complex DDC

- Decimation modes: 4, 6
- Signal bandwidth: 750 MHz, 500 MHz



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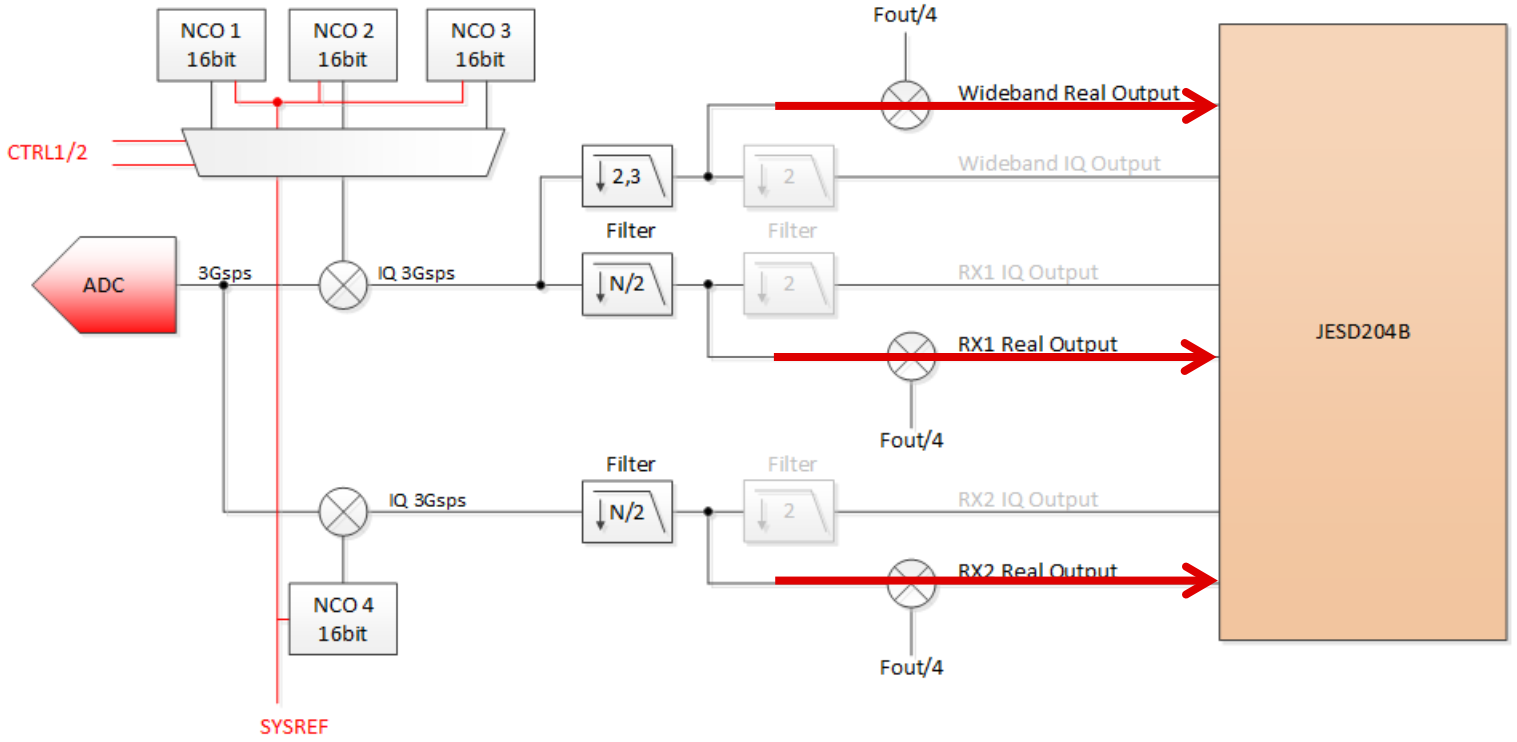
DDC – Real Mixer

- Real output: Fs/4 mixer
  - Dual DDC: Decimation options 8, 9, 10, 12, 16, 18, 20, 24, 36
  - Single Wideband DDC: Decimation 4, 6



Key Decimation Advantage

- Decimation provides SNR processing gain
- Frequency Domain View
  - Signal remains constant
  - Noise power is reduced by decimation filter
  - Improved SNR performance
- Time Domain View
  - Form over averaging samples to reduce overall noise
- Decimation “Penalty”
  - Increased digital power consumption
  - Reduced signal bandwidth capability

Decimation Setting	# of DDCs available per Channel
/ 4 complex	1
/ 6 complex	1
/ 8 complex	2
/ 9 complex	2
/ 10 complex	2
/ 12 complex	2
/ 16 complex	2
/ 18 complex	2
/ 20 complex	2
/ 24 complex	2
/ 32 complex	2

NCO (Numerically Controlled Oscillator)

- Total of 4 NCOs per channel
- NCO frequency is set as a fraction of sampling frequency (Fs)
- Each NCO has a 16-bit control value (Freq[n])

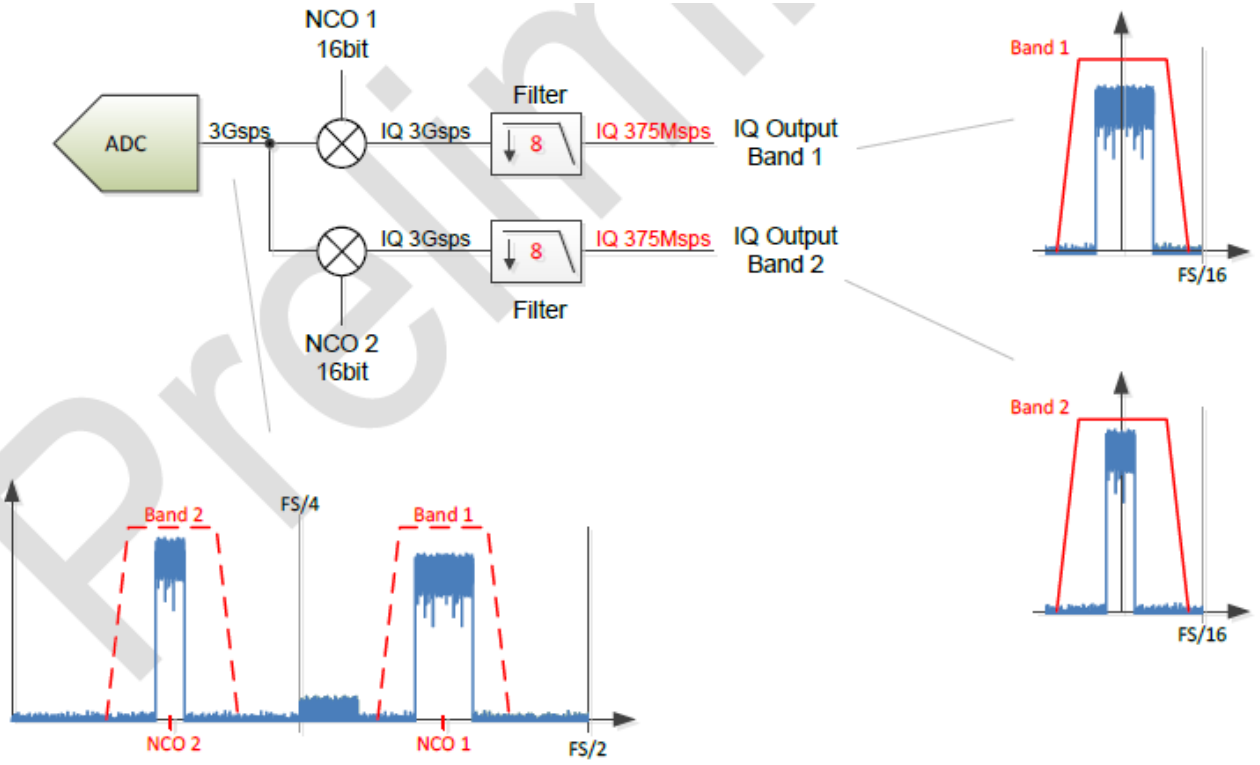
$$F_{NCO} = \frac{NCO\ Freq\ [n] * FS}{2^{16}}$$

- NCO frequency step size: Fs/65,535 = ~45.776 kHz at 3 GSPS

- DDC0 employs 3 switchable NCOs
  - Each NCO can be pre-set via (slow) SPI control
  - NCO switched by external GPIO quickly
  - Supports switching between multiple DPD feedback channels

Dual DDC Receiver Example

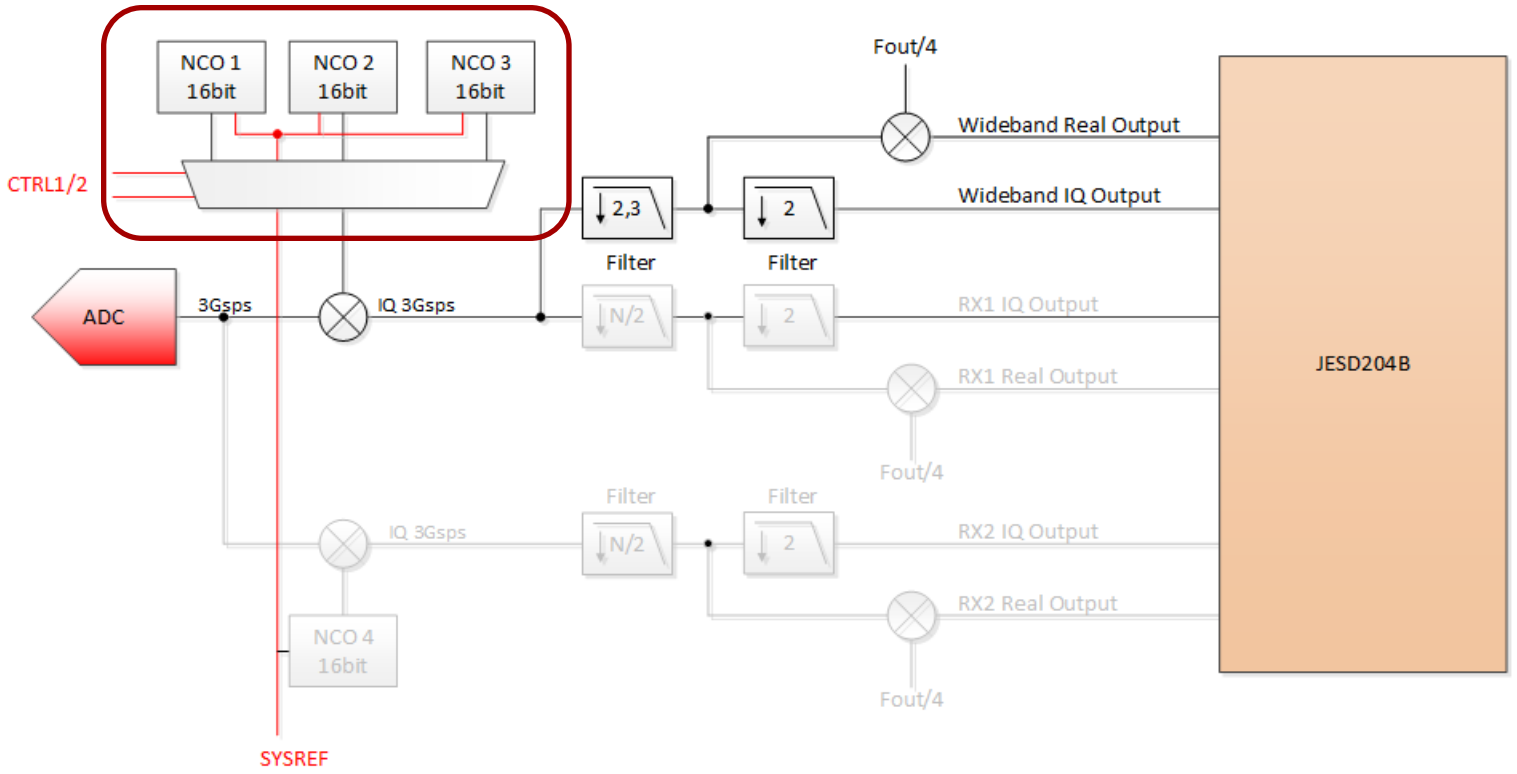
- Each NCO tuned to different RF band
- Signal decimated and mixed down to digital baseband
- Captures desired signals; “filters” unwanted spectrum



Preliminary

Wideband DPD Feedback Example

- Utilize NCO 1, 2, 3 to program to DPD feedback channels
- Employ wideband I/Q output to capture expansion bandwidth



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End of Lecture 5

1.0 **Session #4** Objective: **Exercise the ADC Digital Down-Converter (DDC) features**

2.0 Initial hardware set-up: Keep same connections as the end of Session #3

3.0 Software setup: Keep initial GUI settings the same as the end of Session #3

4.0 Measurement Experiments

4.1 Exercise the Multiple NCO capability

4.1.1 ADC32RFxx GUI > *ADC32RFxx* tab > *DDC Configuration* tab

a) Verify *DDC Channel B* > *ChB DDC0 NCO1* to: 41333 (~1860 MHz)

b) Set *DDC Channel B* > *ChB DDC0 NCO2 freq* to: 1935 MHz

c) Set *DDC Channel B* > *ChB DDC0 NCO3* to: 1785 MHz

d) Change *DDC Channel B* > *ChB NCO Select* to: "DDC0 NCO 2"

4.1.2 HSDC Pro (RFADC): Press "Capture"

4.1.3 Verify new location of the tones. $F_n = F_{in} - F_{NCO}$

4.1.4 Adjust the NCO selection

a) ADC32RFxx GUI > *ADC32RFxx* tab > *ChB NCO Select* to: "DDC0 NCO 3"

b) HSDC Pro (RFADC): Press "Capture"

4.1.5 Verify new location of the tones. $F_n = F_{in} - F_{NCO}$

4.1.6 Why is the highest frequency tone attenuated in this case?

4.1.7 Adjust the NCO frequency

a) ADC32RFxx GUI > *ADC32RFxx* tab > *ChB DDC0 NCO 3* to: 1695 MHz

b) HSDC Pro (RFADC): Press "Capture"

4.1.8 What happened to the two missing tones?

4.1.9 How can this feature be used in a practical design?

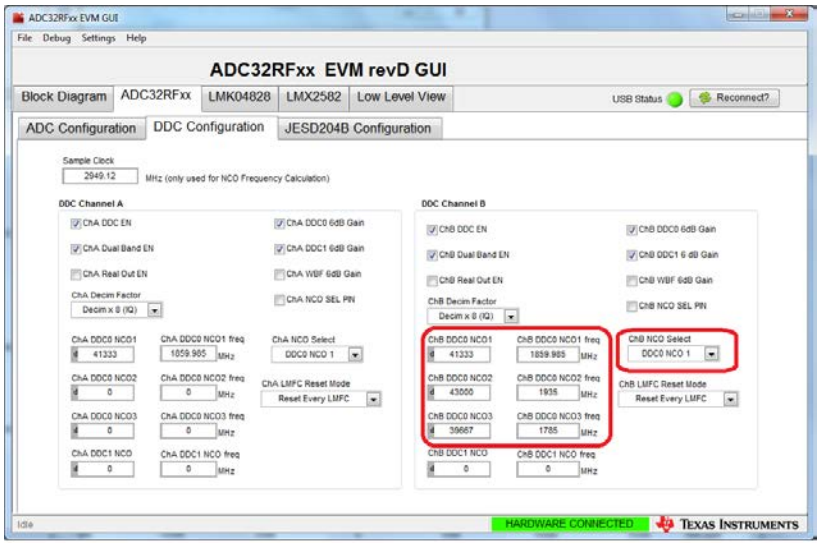

Figure 4.0: ADC32RFxx GUI set-up

4.2 Exercise the Real output with coarse mixer

- 4.2.1 ADC32RFxx GUI > *ADC32RFxx* tab: Toggle "CHB Real Out EN" to: On
- 4.2.2 HSDC Pro (RFADC)>
  - a) Change FFT to: Real FFT
  - b) Press "Capture"
  - c) Note: ini file kept same as change in decimation plus real mode "cancel" each other out.
- 4.2.3 What happened to the tone locations?
- 4.2.4 Calculate the frequency location of the tones.
  - a) Hint: Fs/Dec/4 – (Fin-NCO); note the change in decimation value
  - b) Change *ADC Input Target Frequency* values to confirm

4.3 Exercise the Multiple Output channels

- 4.3.1 ADC32RFxx GUI > *ADC32RFxx* tab:
  - a) Toggle "CHB Real Out EN" to: Off
  - b) Verify "CHB Dual Band EN" is: On
  - c) Change "ChB DDC1 NCO" to: 1850 MHz
- 4.3.2 HSDC Pro (RFADC)
  - a) Change FFT to: "Complex FFT"
  - b) Press "Capture"
  - c) Change Channel Selection to: "Channels 7/8"
- 4.3.3 What happens to the tones? Why?

4.4 Determine the impact of decimation on SNR performance

- 4.4.1 Disconnect the cable to the RF ADC input
- 4.4.2 HSDC Pro (RFADC)
  - a) Change *Test Selection* to: "Single Tone"
  - b) Change Channel Selection to: "Channels 5/8"
  - c) Press "Capture"
  - d) Record the SNR value in dBFS units.
- 4.4.3 ADC32RFxx GUI
  - a) In the *Low Level View* tab > Select "Open Configuration" folder icon
  - b) Select "ADC32RF80_DDC" folder
  - c) Load: "ADC32RF80_ 16xIQ_lmfs8821.cfg"
  - d) Select "Read All" icon
  - e) *ADC32RFxx* tab> *DDC Configuration* tab > Verify NCO values loaded
- 4.4.4 HSDC Pro (RFADC):
  - a) Press "Capture"
  - b) What is the SNR level? How much improvement from /8 case?

4.4.5 ADC32RFxx GUI

a) In the *Low Level View* tab > Select “Open Configuration” folder icon
b) Select “ADC32RF80_DDC” folder
c) Load: “ADC32RF80_ 4xIQ_lmfs8411.cfg”
d) Select “Read All” icon
e) Select *ADC32RFxx* tab> *DDC Configuration* tab
f) Change “ChB DDC0 NCO1 freq” to 1850; verify NCO value loaded

4.4.6 HSDC Pro (RFADC)

a) Change ini file to: “ADC32RF80_LMF_8411_isync0”
b) Change NCO setting to Decimation to 4
c) Press “Capture”

4.4.7 What is the SNR level? How much did it degrade from /8 case?

4.4.8 Are the above results expected?

4.4.9 Re-connect the RF cable to J3

***** Leave set-up as-is for use in the next session *****

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RF Sampling Clocking

Lecture 6

Clocking for RF Sampling

- RF sampling requires high frequency clock source
- Jitter or Phase Noise performance of the clock is critical to maintain best performance
- High Frequency Clock in RF Sampling vs. High Frequency Synthesizer in super-heterodyne architecture
  - RF Sampling only needs one frequency clock. No tuning is required.
    - Narrow band VCO or VCXO is sufficient
      - Easier to achieve very good phase noise performance
    - No channel tuning required
      - Channel allocation is accomplished digitally
  - Pure sinusoid not absolutely needed; only concerned with transitions

Clock Jitter Impact in Data Converters

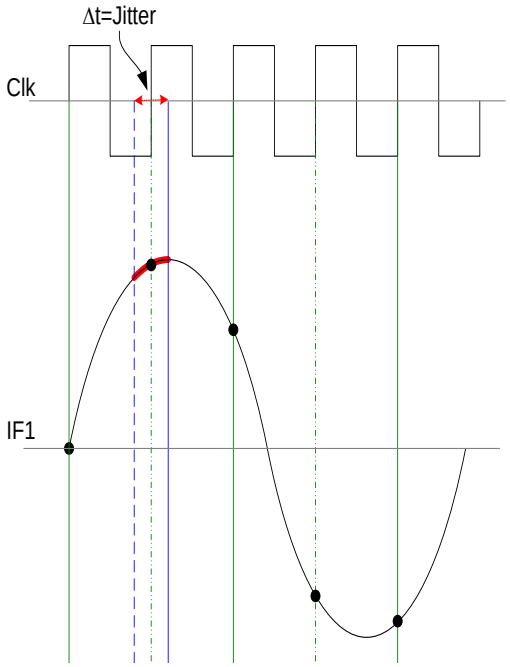
- Random variation of the clock position compared to its ideal position with respect to time
- As clock position varies, the position of the sampling point varies
- Sampling at imprecise locations yield SNR degradation
- Theoretical limit of SNR due to jitter:

$$SNR_j = -20 \cdot \log(2\pi f_{in} \cdot \tau_j)$$

where:

f_{in} = input frequency

τ_j = clock jitter

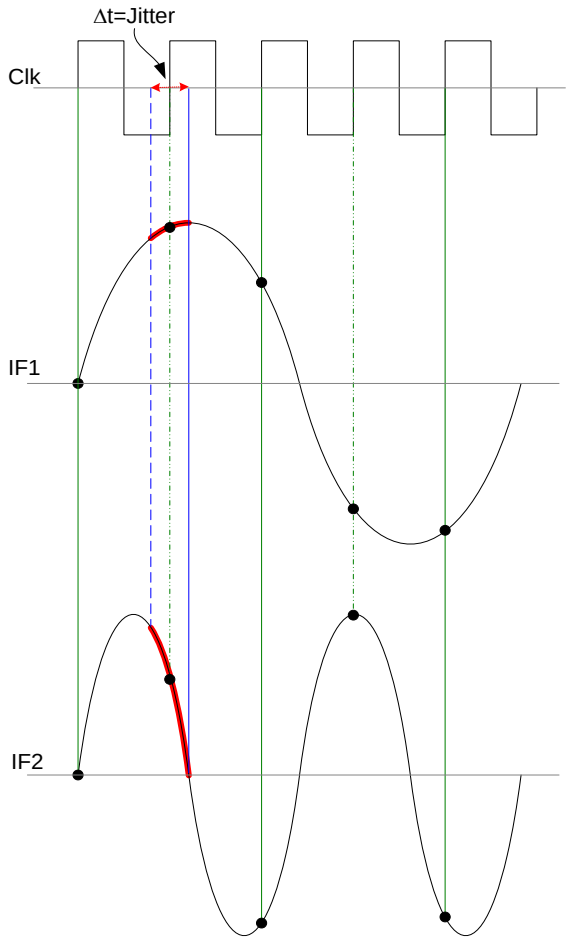


Jitter Impact with respect to Frequency

- SNR is independent of sampling rate
- SNR is dependent on input frequency
  - For a given amount of jitter, SNR degrades as input frequency increases

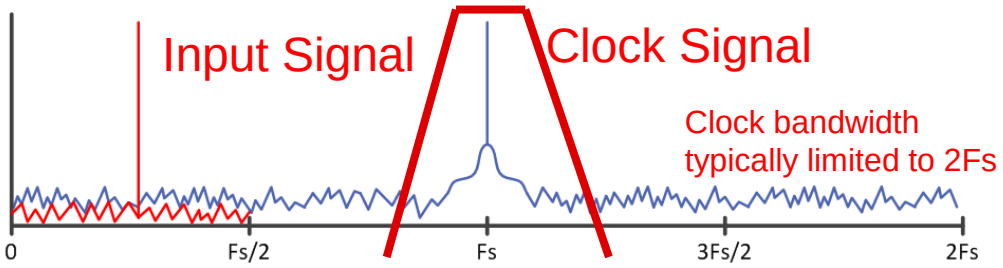
- Higher sampling rates indirectly lead to more stringent jitter requirements
  - High sampling rate device are not “more sensitive”; rather, high sampling rates allow higher input frequencies

$$SNR_j = -20 \cdot \log(2\pi f_{in} \cdot \tau_j)$$

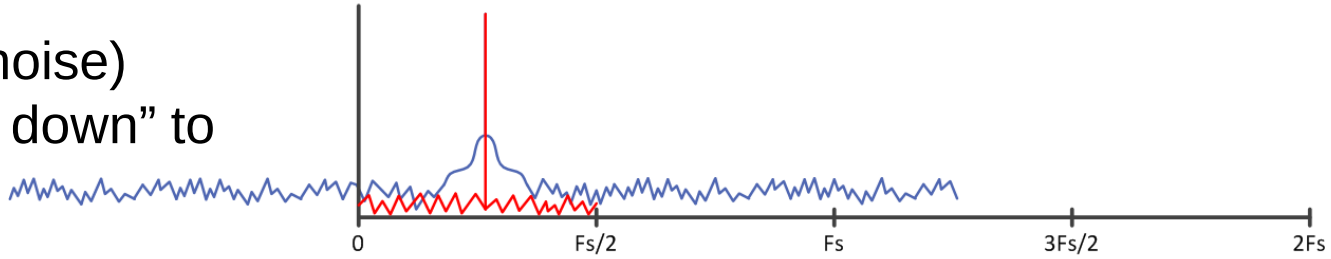


Impact of Wideband Clock Noise

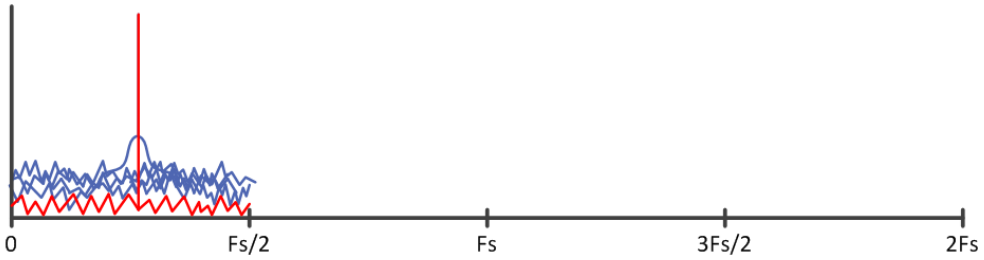
- Input signal and clock signal



- Clock (signal+noise) effectively “mix down” to input signal



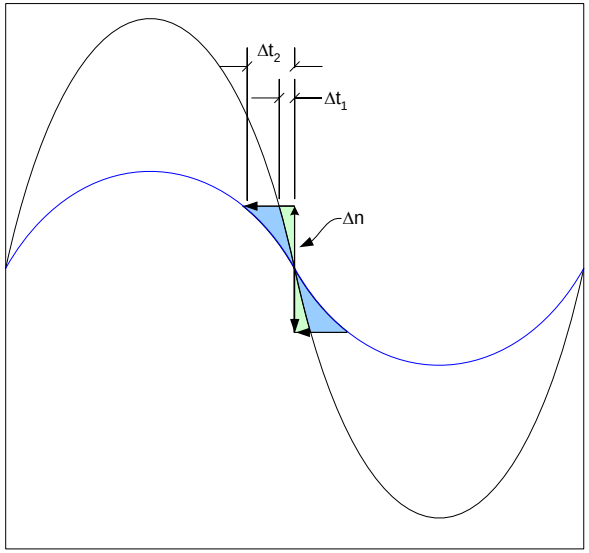
- All noise aliases down to 1st Nyquist zone

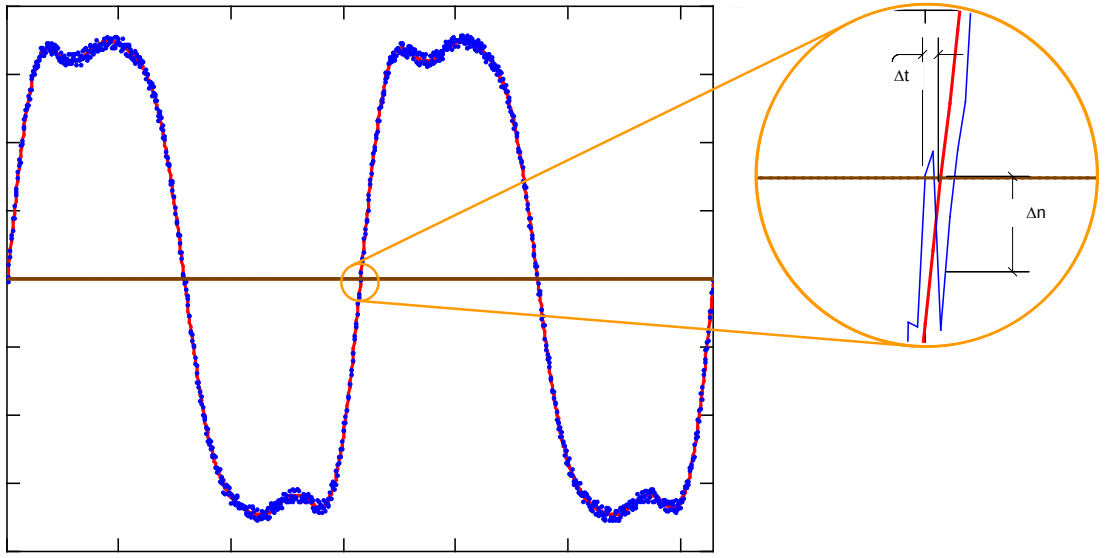


- Low clock noise floor or clock band-pass filter is critical

Slew Rate and Jitter Performance

- Slower slew rate is more susceptible to variations in the zero crossing point due to noise
- BPF filters broadband noise but also removes harmonics
  - Square-wave-like clocks become sinusoid clocks
  - Sinusoid signals have lower slew rate
- Increase signal to large amplitude to minimize slew rate impact



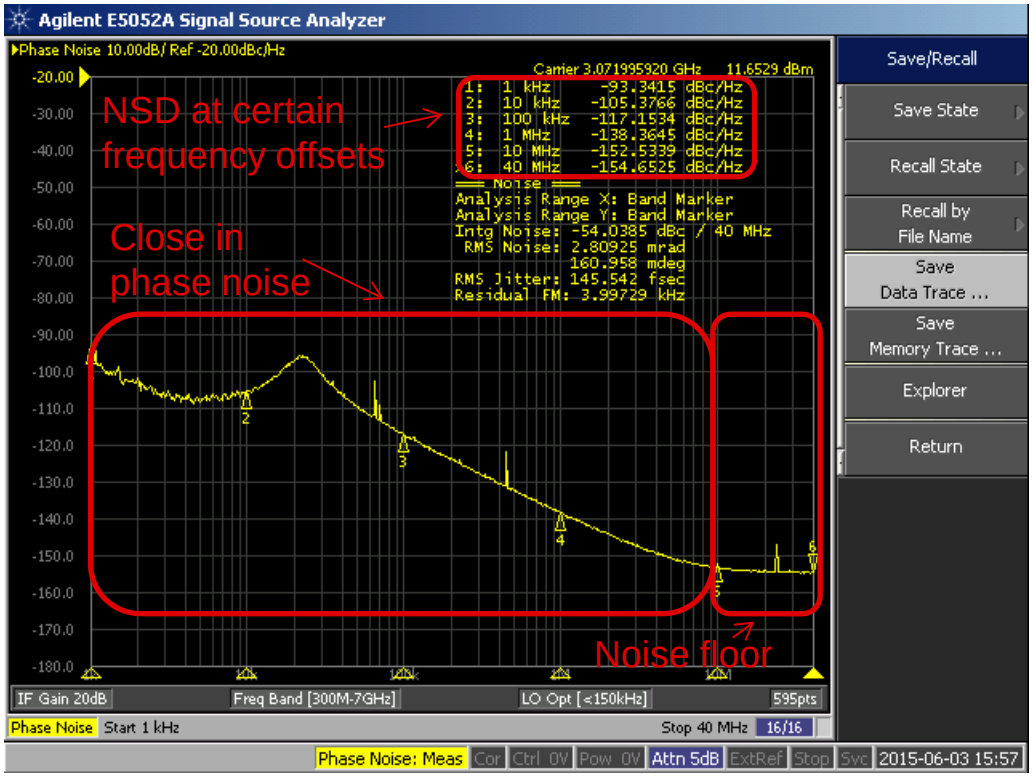


Total Clock Noise

- The total clock noise calculated by integrating the phase noise

$$N_{clk}[dBc] = 10log\left(\int_{f_1}^{f_2} 10^{\frac{\Phi(f)[dBc]}{10}} df\right)$$

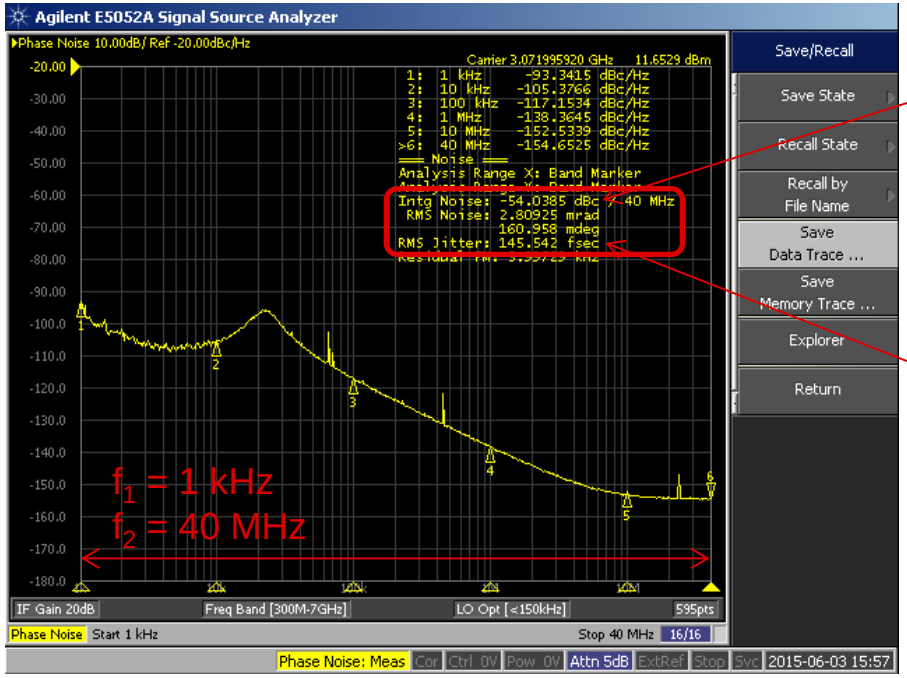
- How are f_1 and f_2 chosen?
  - Limited bandwidth
    - ACPR contribution
    - In-band (e.g. EVM/MER)
  - Data Converter SNR:
    - f_1 = ~0 Hz
    - f_2 = Converter's clock bandwidth (worst case)



Clock Noise to “Jitter”

- Jitter is a conversion of clock noise (power) to the rms movement of the clock sampling instant (time) measured in seconds:

$$\tau_j[s,rms] = \frac{\sqrt{10^{\frac{N_{CLK}[dBc]}{10}}}}{2\pi f_{clk}}$$



Total noise (SSB) = -54.0385 dBc

x2 for DSB

$$\tau_j[s,rms] = \frac{\sqrt{2*10^{\frac{-54.0385}{10}}}}{2\pi f_{clk}}$$

RMS Jitter = 145.542 fs

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ADC SNR Calculations

- Typically use “Jitter” to calculate ADC performance for a given clock:

$$SNR_{CLK}[dBc] = -20 \cdot \log(2\pi f_{in} \cdot \tau_{CLK})$$
$$f_{in} = input\ \ frequency$$
$$\tau_{CLK} = clock\ \ jitter$$

- This readily allows the addition of the ADC’s clock noise (aperture jitter) by:

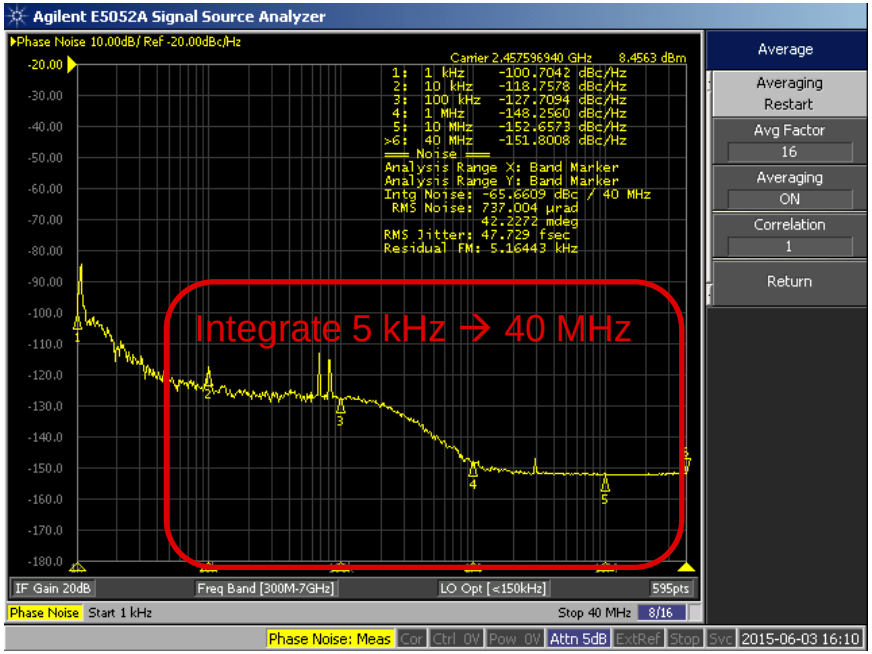
$$\tau_j = \sqrt{\tau_{CLK}^2 + \tau_{APERTURE}^2}$$

- To find SNR from jitter in dBFS (used for total noise calculation):

$$SNR_{CLK}[dBFS] = -20 \cdot \log(2\pi f_{in} \cdot \tau_j) - S_{FUND}$$
$$S_{FUND} = Input\ Signal\ Level\ in\ dBFS$$

Example ADC Calculation

- ADC32RF80 w/ 4x decimation
  - Fs = 2.4576 Gsps
  - Fin = 1.75 GHz, -3 dBFS
  - Aperture jitter = 70 fs
  - SNR_{THERM} = 65 dBFS
- Clock phase noise
  - Integration BW
    - f1 = ~ 5 kHz (from FFT bin size)
    - F2 = 40 MHz (instrument max)
  - $\Phi_{closein}$ = -70.59 dBc
- Calculate clock jitter



$$\tau_{Clk}[s,rms] = \frac{\sqrt{2 * 10^{\frac{-70.59}{10}}}}{2\pi f_{Clk}} = 27.06\, fs$$

Example ADC Calculation (Continued)

- ADC32RF80 w/ 4x decimation
  - Fs = 2.4576 Gsps
  - Fin = 1.75 GHz, -3 dBFS
  - Aperture jitter = 70 fs
  - Clock jitter = 27.06 fs (from previous calculations)
  - SNR_{THERM} = 65 dBFS
- Total jitter:

$$\tau_j = \sqrt{\tau_{Clk}^2 + \tau_{APERTURE}^2} = 75.05\,fs$$

- ADC SNR due to jitter:

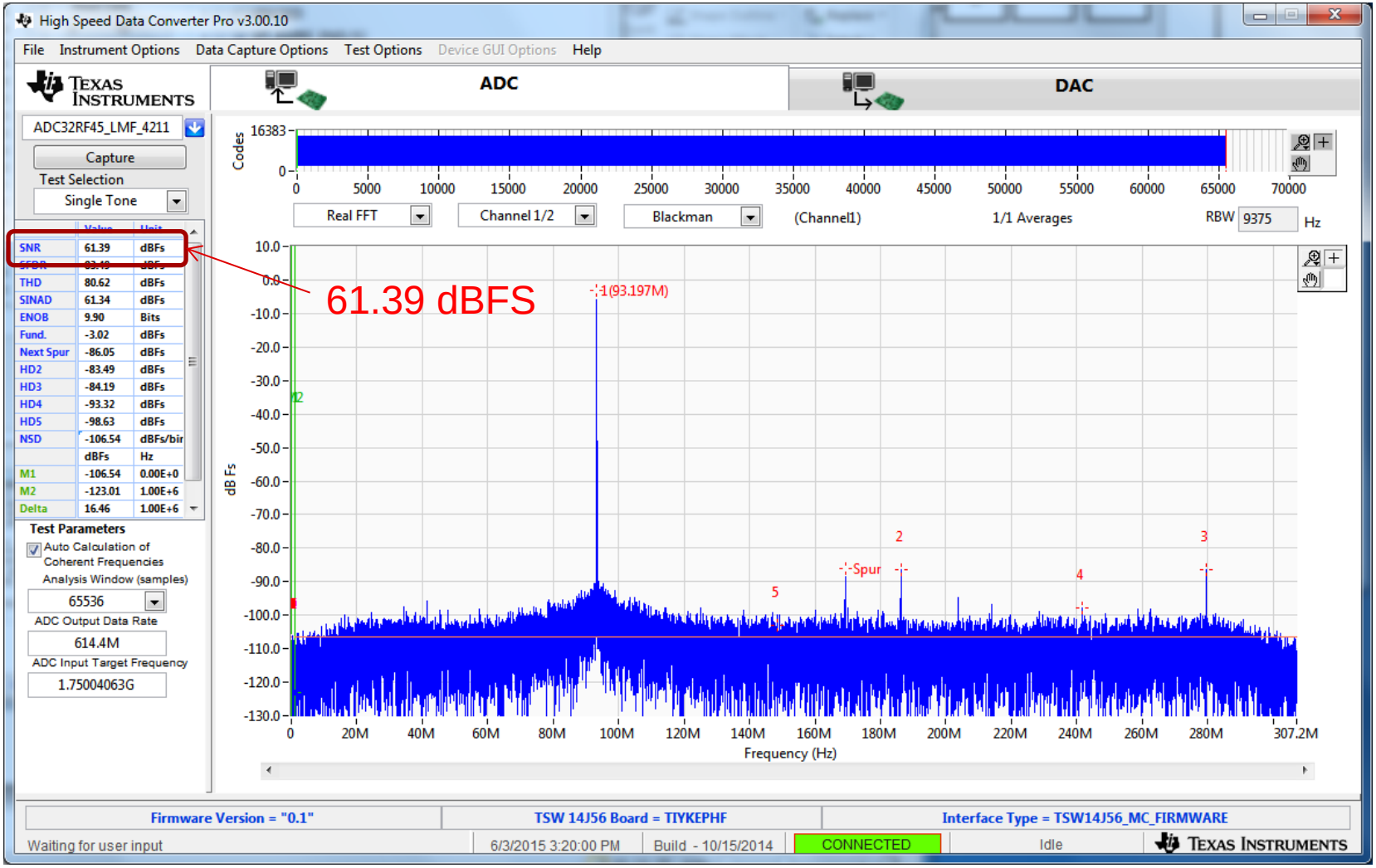
$$SNR_{CLK}[dBc] = -20 \cdot \log(2\pi f_{in} \cdot \tau_j) = 61.67\ \text{dBc} \Rightarrow 64.67\ \text{dBFS}$$

- Total ADC SNR:

$$SNR_{total} = -10\log\left(10^{-SNR_{JITTER}/10} + 10^{-SNR_{THERM}/10}\right)$$

$$SNR_{total} = -10\log\left(10^{-64.67/10} + 10^{-65/10}\right) = 61.82\,dBFS$$

Measured Result w/ 4x decimation



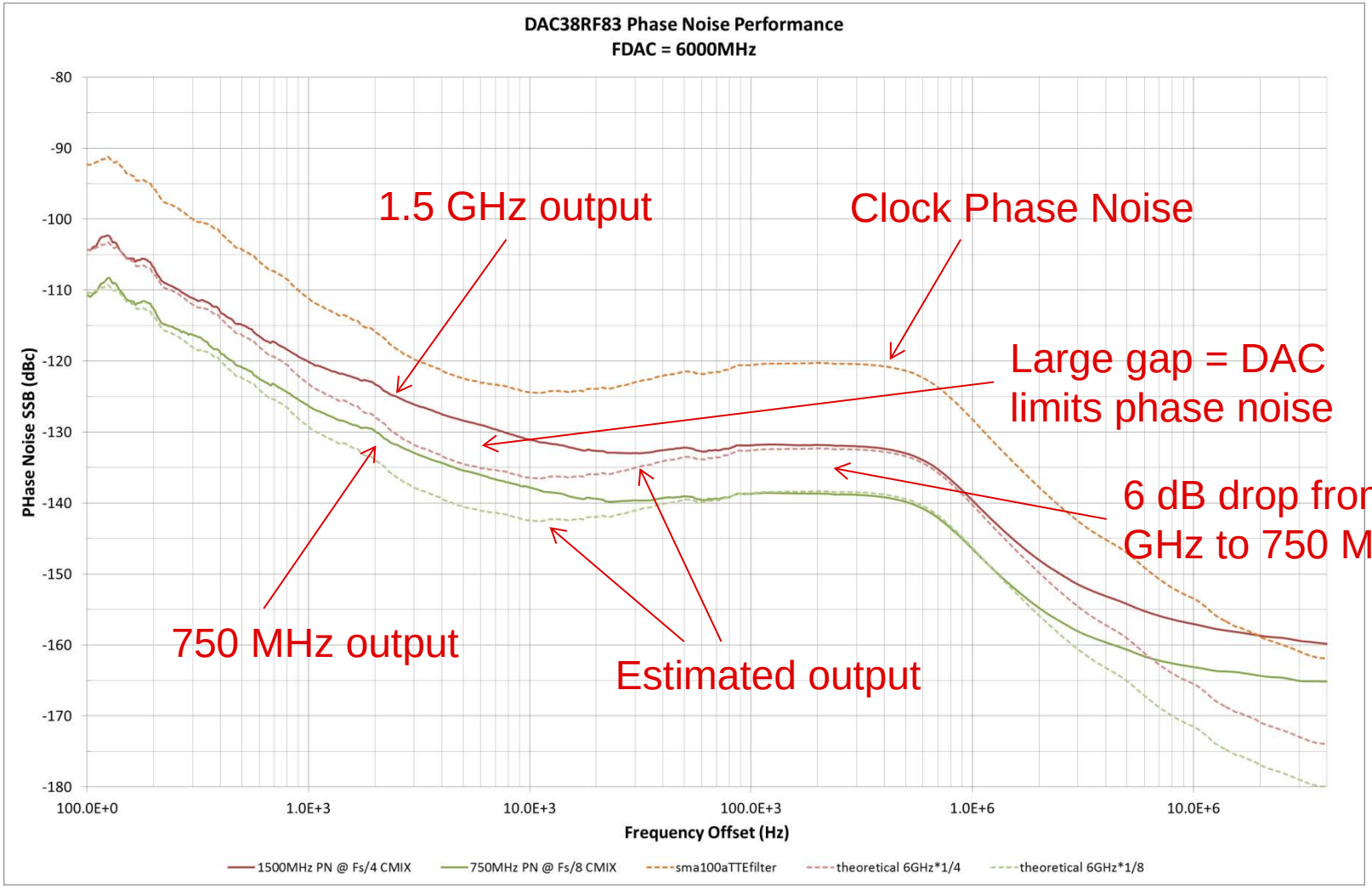
Observations

- Thermal noise is a dominant factor in SNR performance
  - Decimation eliminates noise that falls outside of the decimation filter

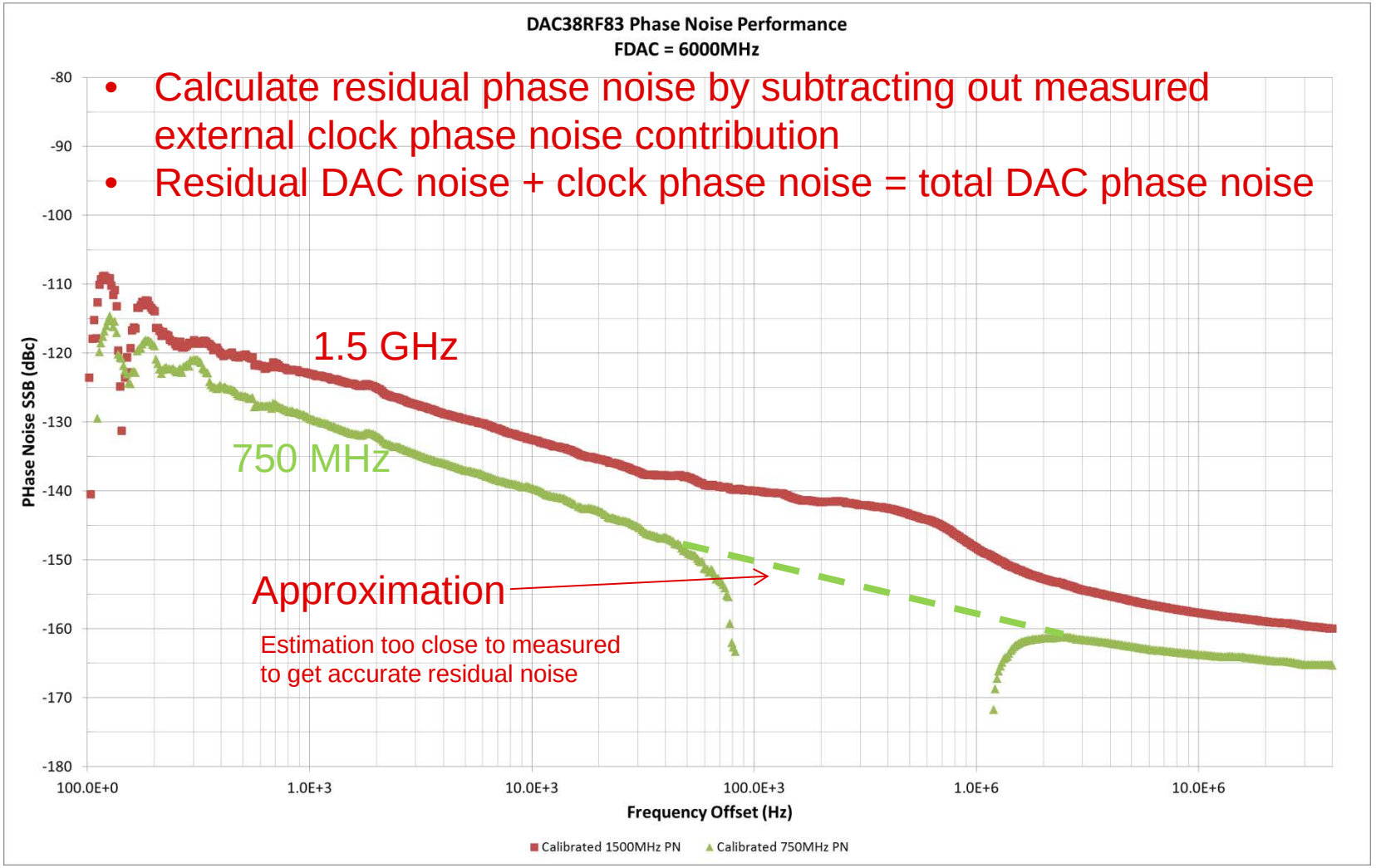
$$SNR_{Decimated} = SNR_{total} + 10\log(Decimation)$$

  - Decimate by 2 = 3 dB SNR improvement
- Reducing input power reduces impact of clock jitter to SNR
  - Backing off from full scale improves performance
- Clock filtering improves SNR performance
  - Changes limits of integration; reduces clock jitter
- Increasing clock amplitude improves performance
  - Higher clock amplitude increases slew rate which reduces thermal noise impact to clock jitter

Example Measurement – DAC38RF83



DAC Residual Phase Noise



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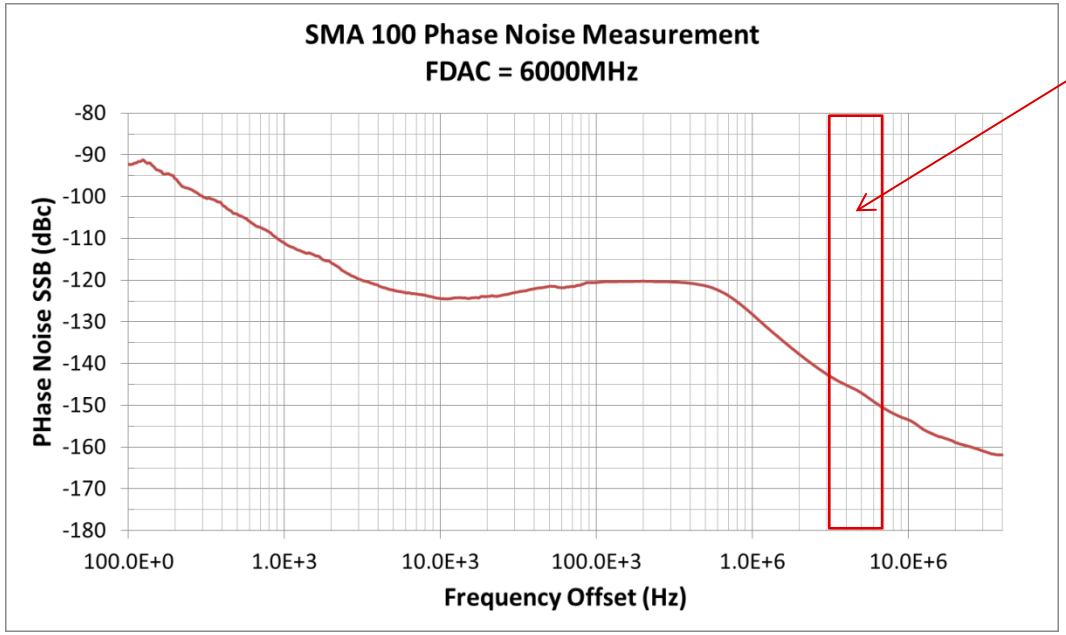
Example DAC Calculation – ACPR/ACLR

- Estimate clock's phase noise contribution to ACPR/ACLR
- Use previous phase noise measurement @ 1.5 GHz output
- For W-CDMA, BW = 3.84 MHz, channel spacing = 5 MHz
- Clock source = SMA 100 (excellent phase noise)



Integrate phase noise from 3.08 MHz to 6.92 MHz

N_{ACPR_CLK} = -80.97 dBc
N_{ACPR_DAC} = -80.97-20log(1.5G/6G)
N_{ACPR_DAC} = -93 dBc

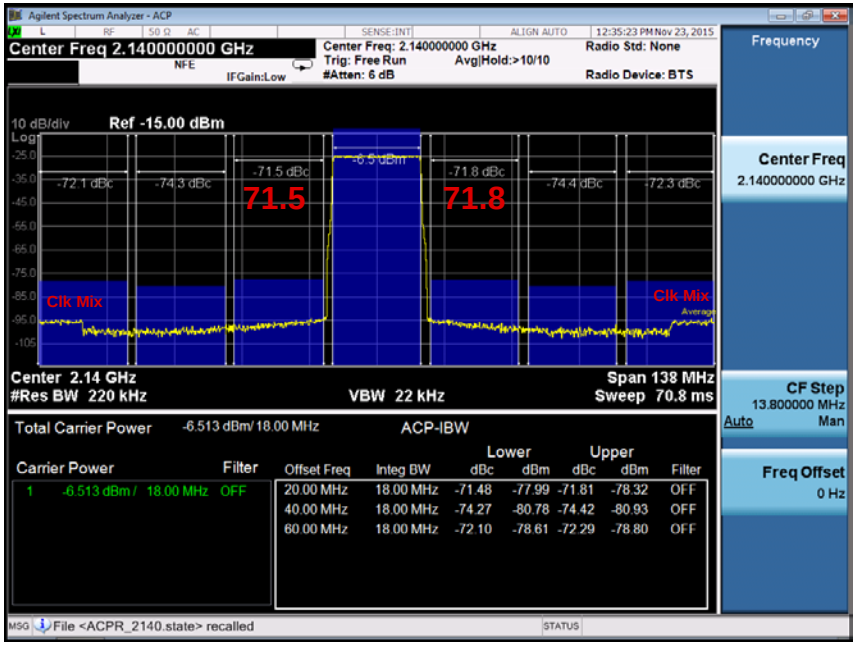
DAC ACPR is worse than -93 dB, so clock noise will not limit ACPR in this case

What about 3 GHz center frequency with same clock?

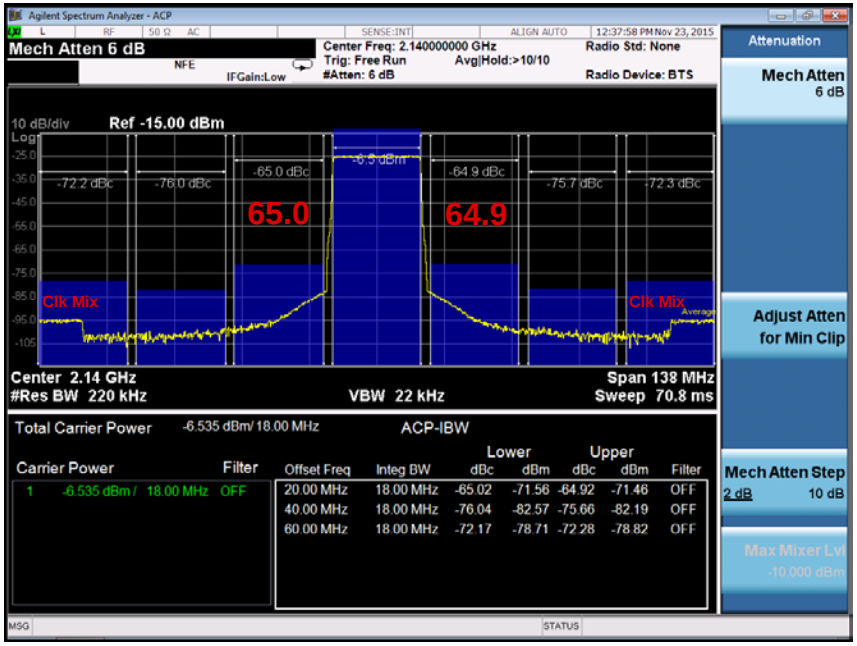
DAC ACPR Comparison

Ext Clk vs. On-chip PLL

Ext Clock: 8847.36 MHz



On-chip PLL: 8847.36 MHz



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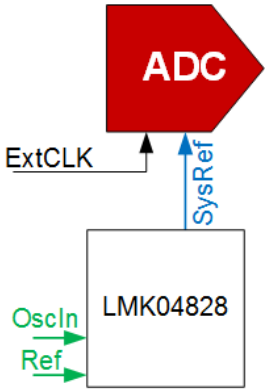
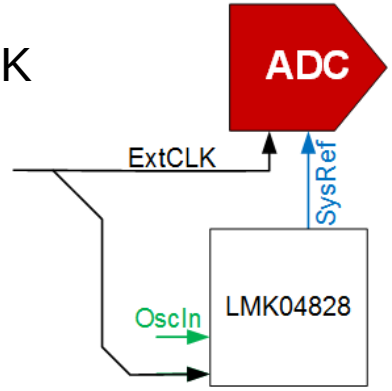
RF ADC EVM External Clocking Options

- External sig gen to the ADC (transformer coupled)
  - LMK04828 generates *same* rate so that SysRef to ADC and clk/sysref to FPGA is coherent
    - Requires 10M sync signal between sig gen and LMK
  - Convenient set up *if* LMK can generate the rate from the 122.88MHz reference oscillator. (such as 2.4576 GHz)



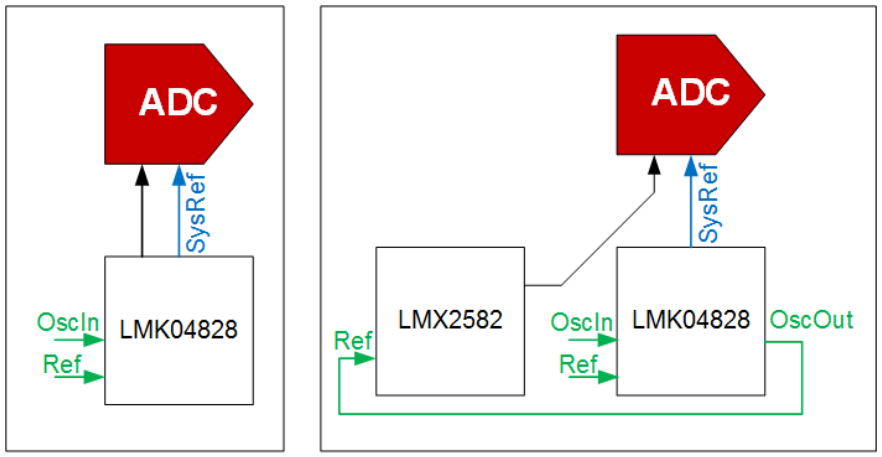
- External sig gen to the ADC and LMK
  - Copy of the *same* clock provided as reference to the LMK
    - Either a splitter on the clock or two sync'd sig gens
  - LMK uses this external clock as its 'VCO' in place of the internal VCO



- Most flexible/baseline ADC performance

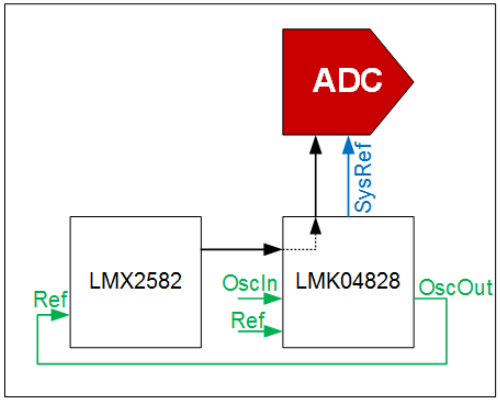
On-board Clocking Options

- Option 1: LMK04828 to ADC (solder mod needed on EVM)
  - Limited to ~2.5GHz or ~3.0GHz due to LMK VCO frequencies
  - ~3 to 4 dB SNR loss due to VCO phase noise
  - Sample Clock and SysRef are well synchronized
- Option 2: LMX2582 to ADC (standard EVM set-up)
  - Limited to LMK internal VCO frequencies which derive SysRef
  - Equivalent SNR performance with baseline S/G clock source
  - Sample Clock and SysRef not definitively phase aligned

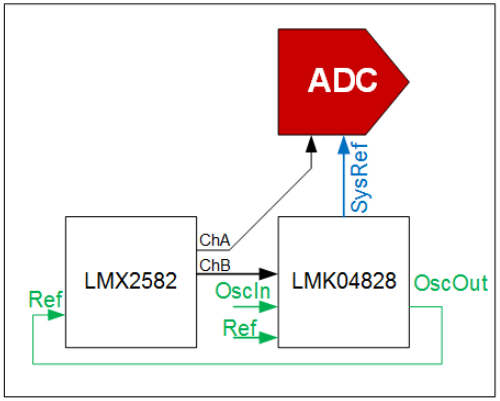


On-board Clocking Options (cont)

- Option 3: LMX2582 to LMK04828 to ADC (solder mod needed on EVM)
  - LMK operated in clock distribution mode
  - Any frequency generated by LMX is allowable
  - Sample Clock and SysRef are well synchronized
  - SNR degradation due to LMK buffer roll-off at high frequencies
- Option 4: LMX2582 ChA/B to ADC/LMK (no option on EVM)
  - Any frequency generated by LMX is allowable
  - Sample Clock and SysRef are well synchronized
  - Equivalent SNR performance with baseline S/G clock source



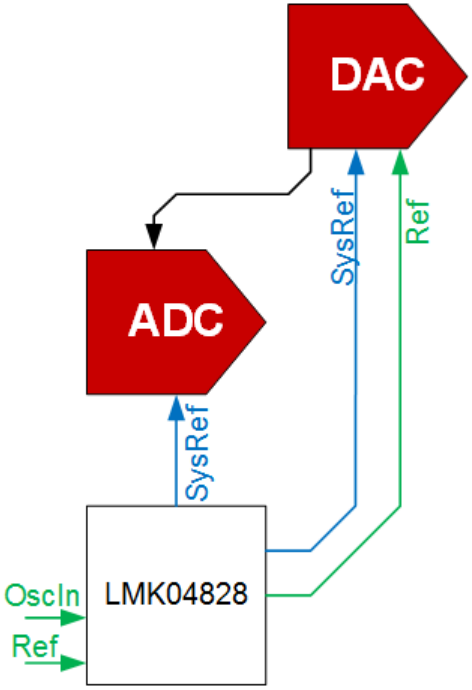
Option 3



Option 4

System Clocking Option

- LMK provides:
  - SysRef to DAC and ADC
  - Limited to internal VCO frequencies which derive SysRef
  - Supplies low frequency reference to DAC PLL
- RF DAC PLL
  - Provides DAC sample clock
  - Integrated divider: /2, /3/, /4
  - Provides ADC sample clock
- DAC/TX and ADC/RX share correlated clock source
  - Allows noise cancellation in DPD feedback applications



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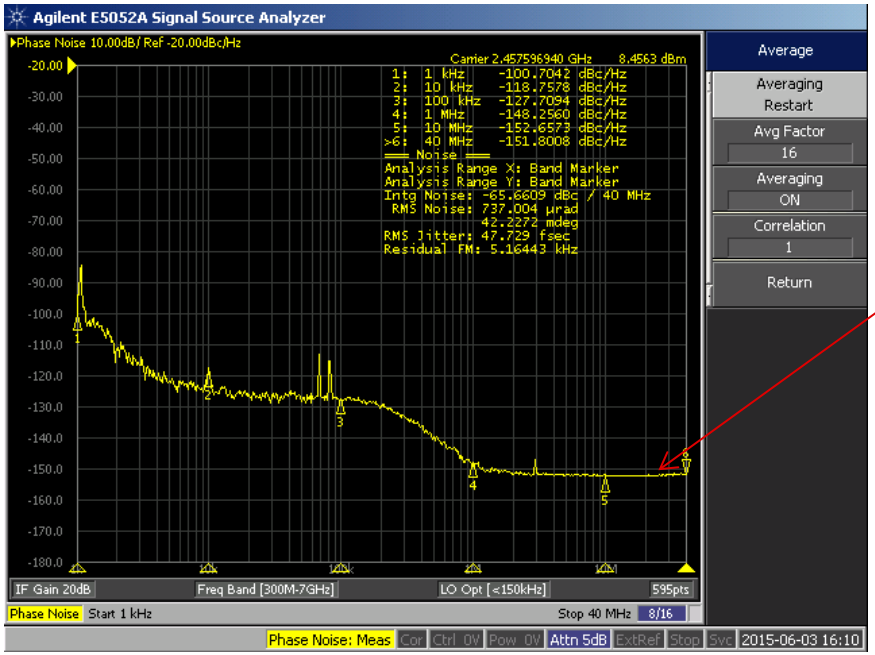
End of Lecture 6

Additional Material

Clock Calculations for DDC Bypass

- ADC32RF45 w/ DDC bypass
  - Fs = 2.4576 Gsps
  - Fin = 1.75 GHz, -3 dBFS
  - Aperture jitter = 70 fs
  - SNR_{THERM} = 61.5 dBFS
- Clock source phase noise:



Remove Close in BW (may be negligible)

Roughly 2*Fs_{MAX}

$$\Phi_{farout} = \mathrm{NSD}_{floor} + 10\log(BW_{CLKIN} - 2 * f_2)$$

$$\Phi_{farout} = -152 + 10\log(6GHz) = -54.3\ dBc$$

$$\tau_j[s, rms] = \frac{\sqrt{2 * 10^{\frac{-70.59}{10}} + 10^{\frac{-54.3}{10}}}}{2\pi f_{clk}}$$

$$\tau_j[s, rms] = 127.7\ fs$$

Example ADC Calculation Continued

- ADC32RF45 w/ DDC bypass
  - Fs = 2.4576 Gsps
  - Fin = 1.75 GHz, -3 dBFS
  - Aperture jitter = 70 fs
  - SNR_{THERM} = 61.5 dBFS
- Total jitter:

From previous slide:

$$\tau_j[s,rms] = 127.7\ fs$$

$$\tau_{TOTAL} = \sqrt{\tau_{EXTERNAL}^2 + \tau_{APERTURE}^2}$$

$$\tau_{TOTAL} = 145.63\ fs$$

What happens if Fin = -10 dBFS?

- ADC SNR due to jitter:

$$SNR_{CLK}[dBc] = -20 \cdot \log(2\pi f_{in} \cdot \tau_j) = 55.91\,\text{dBc} => 58.91\,\text{dBFS}$$

- Total ADC SNR:

$$SNR_{total} = -10\log\left(10^{-SNR_{JITTER}/10} + 10^{-SNR_{THERM}/10}\right)$$

$$SNR_{total} = -10\log\left(10^{-58.91/10} + 10^{-61.5/10}\right) = 57.00\,dBFS$$

1.0 **Session #5** Objective: **Examine a 600 MHz wide band signal**

2.0 Initial hardware set-up: Keep same connections as the end of Lesson #4

3.0 Software setup:

- 3.1 HSDC Pro (RF DAC)
  - 3.1.1 Switch to HSDC Pro (RFDAC)
    - a) Instrument Options>Disconnect from Board
    - b) Instrument Options>Connect to Board
    - c) Select the serial number of the 'J56 connected to the RF DAC EVM; press "OK".
    - d) Select DAC tab
  - 3.1.2 I/Q Multitone BW> Tone BW = 150M
  - 3.1.3 I/Q Multitone BW> # = 25
  - 3.1.4 Press "Create Tones"
  - 3.1.5 Press "Send"; press "OK" in the pop-up window
- 3.2 HSDC Pro (RFADC)
  - 3.2.1 Switch to HSDC Pro (RFADC)
    - a) Instrument Options>Disconnect from Board
    - b) Instrument Options>Connect to Board
    - c) Select the serial number of the 'J56 connected to the RF ADC EVM; press "OK".
  - 3.2.2 Toggle ADC Output Setup icon
    - a) Click "Enable?"
    - b) Change ADC Sampling rate to: 2949.12M
    - c) Change ADC Input Frequency to: 1960M
    - d) Change NCO to: -1859.985M
    - e) Change Decimation to: 4
    - f) Press "OK"; press "OK" on the pop-up window
- 3.3 DAC38RF8x GUI
  - 3.3.1 *DAC38RF8x* tab>*Digital(DAC B)* tab>
    - a) NCO Frequency Path AB = 2085
    - b) NCO Frequency Path CD = 1635
    - c) Press "Update NCO"
  - 3.3.2 *DAC38RF8x* tab>*Digital(DAC A) tab*>
    - a) NCO Frequency Path AB = 1935
    - b) NCO Frequency Path CD = 1785
    - c) Press "Update NCO"
    - d) Verify all paths in *Output sum selector* are toggled to On
- 3.4 HSDC Pro (RF ADC): Press "Capture"

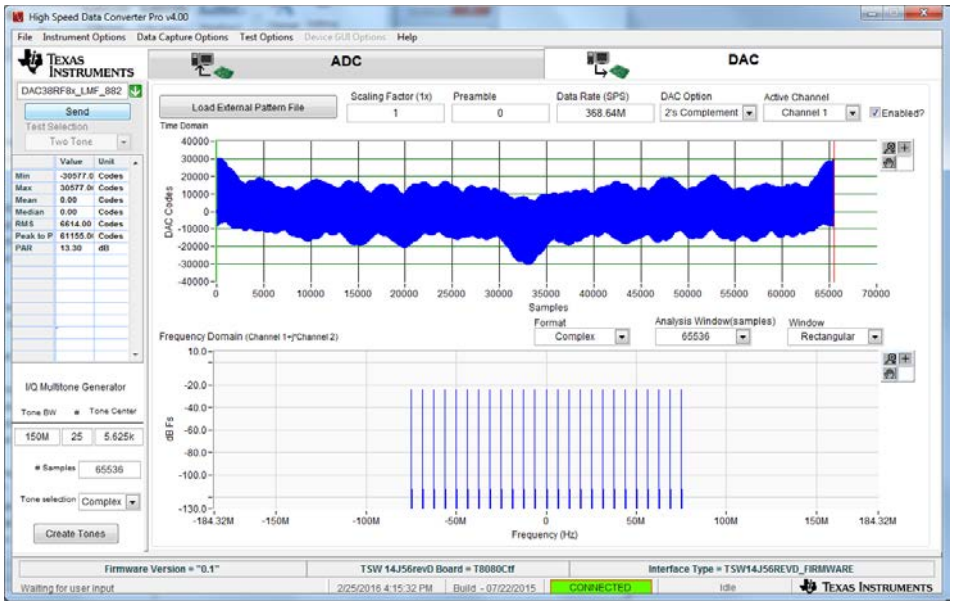


Figure 5.0: HSDC Pro (RF DAC) software set-up

4.0 Measurement Experiments

- 4.1 How much signal bandwidth is represented in the capture?
- 4.2 Why are the tones at different amplitudes?
- 4.3 Remove BPF and re-capture
- 4.4 How much signal bandwidth is represented in the capture?

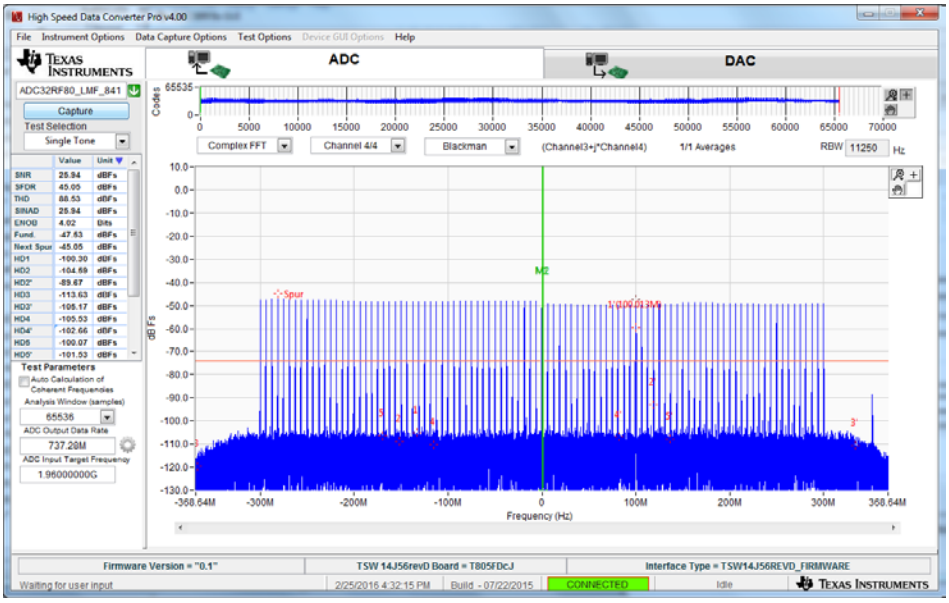


Figure 5.1: Capture results

5.0 Additional Experiments

5.1 Analog Gain

5.1.1 Modify *DAC38RF8x* tab>*Overview* tab>*DAC Configuration*>DAC Coarse gain: 15

5.1.2 Press HSDC Pro (RF ADC) "Capture" after the change

5.1.3 Observe level of the tones

5.2 Digital Gain

5.2.1 Modify *DAC38RF8x* tab>*Digital(DAC A)* tab>Path AB Gain to: 1

5.2.2 Press "Capture"

5.2.3 What do you observe?

5.2.4 Use digital gain adjustment to flatten out the response over frequency.

5.2.5 Note: digital gain should hover around 0.5 to ensure device is not overdriven

5.3 Examine Inverse Sinc

5.3.1 Toggle *DAC38RF8x* tab>*Digital(DAC B)* tab> Path AB inv sinc to: On

5.3.2 Press "Capture"

5.3.3 Toggle *DAC38RF8x* tab>*Digital(DAC B)* tab> Path AB inv sinc to: Off

5.3.4 Press "Capture"

5.3.5 What do you observe?

5.4 Examine output sum selector

5.4.1 Toggle various combinations of *output sum selector*

5.4.2 Press "Capture"

5.4.3 What do you observe?

5.4.4 How does the amplitude of the tones change?

5.5 Investigate NCO Phase

5.5.1 *DAC38RF8x* tab>*Digital(DAC A)* tab>

a) NCO Frequency Path CD = 1935

b) Press "Update NCO"

5.5.2 HSDC Pro (RFADC): Press "Capture"

5.5.3 What do you observe? Is it expected?

5.5.4 *DAC38RF8x* tab>*Digital(DAC A)* tab>

a) NCO Phase (deg) Path CD = 180

b) Press "Update NCO"

5.5.5 HSDC Pro (RFADC): Press "Capture"

5.5.6 What do you observe? Is it expected?