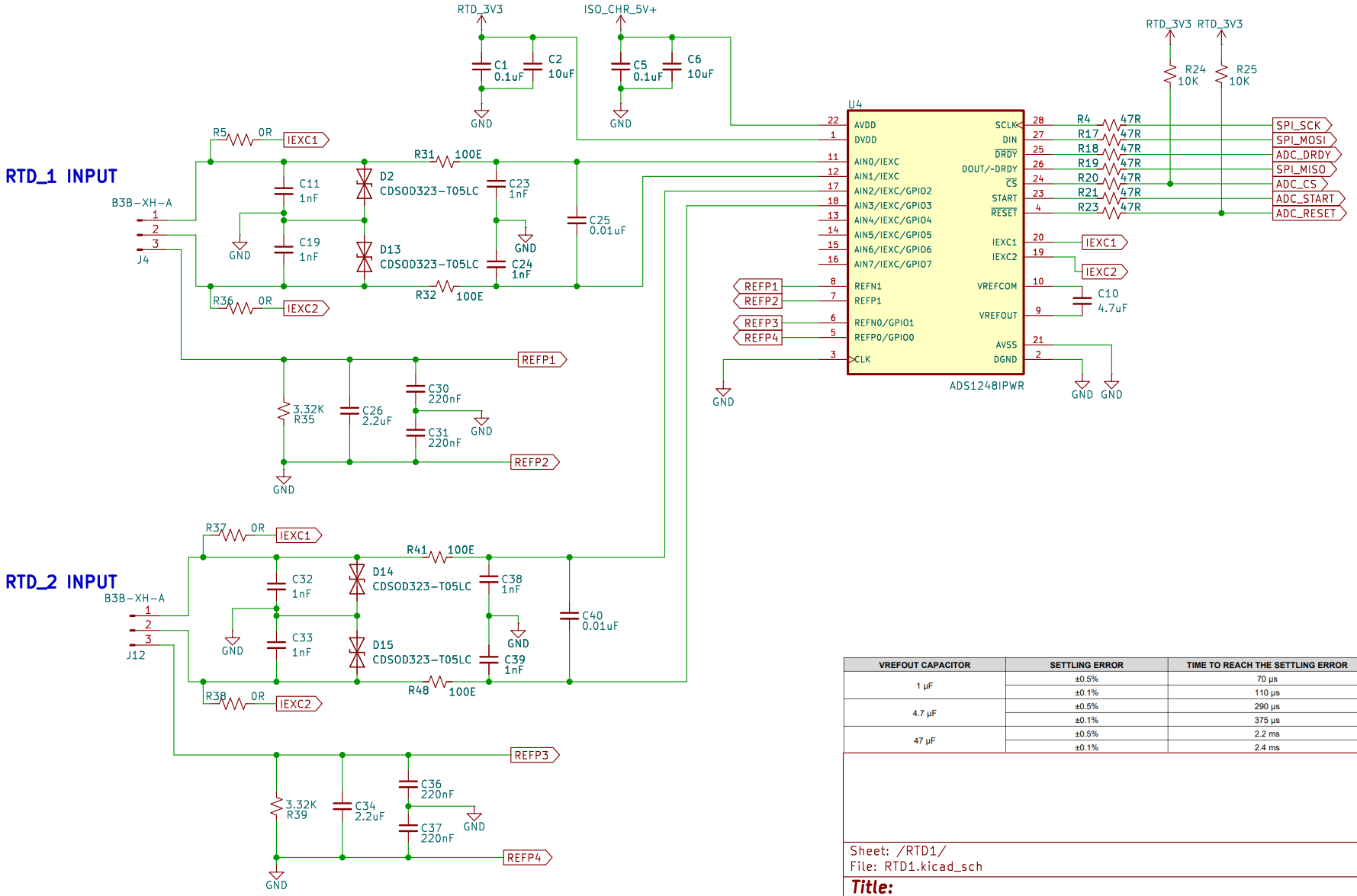

VREFOUT CAPACITOR	SETTLING ERROR	TIME TO REACH THE SETTLING ERROR
1 µF	±0.5%	70 µs
	±0.1%	110 µs
4.7 µF	±0.5%	290 µs
	±0.1%	375 µs
47 µF	±0.5%	2.2 ms
	±0.1%	2.4 ms

Sheet: /RTD1/
File: RTD1.kicad_sch

Title:

Size: A4	Date: 29-01-2026	**Rev: V1**
KiCad E.D.A. 9.0.7		Id: 11/11