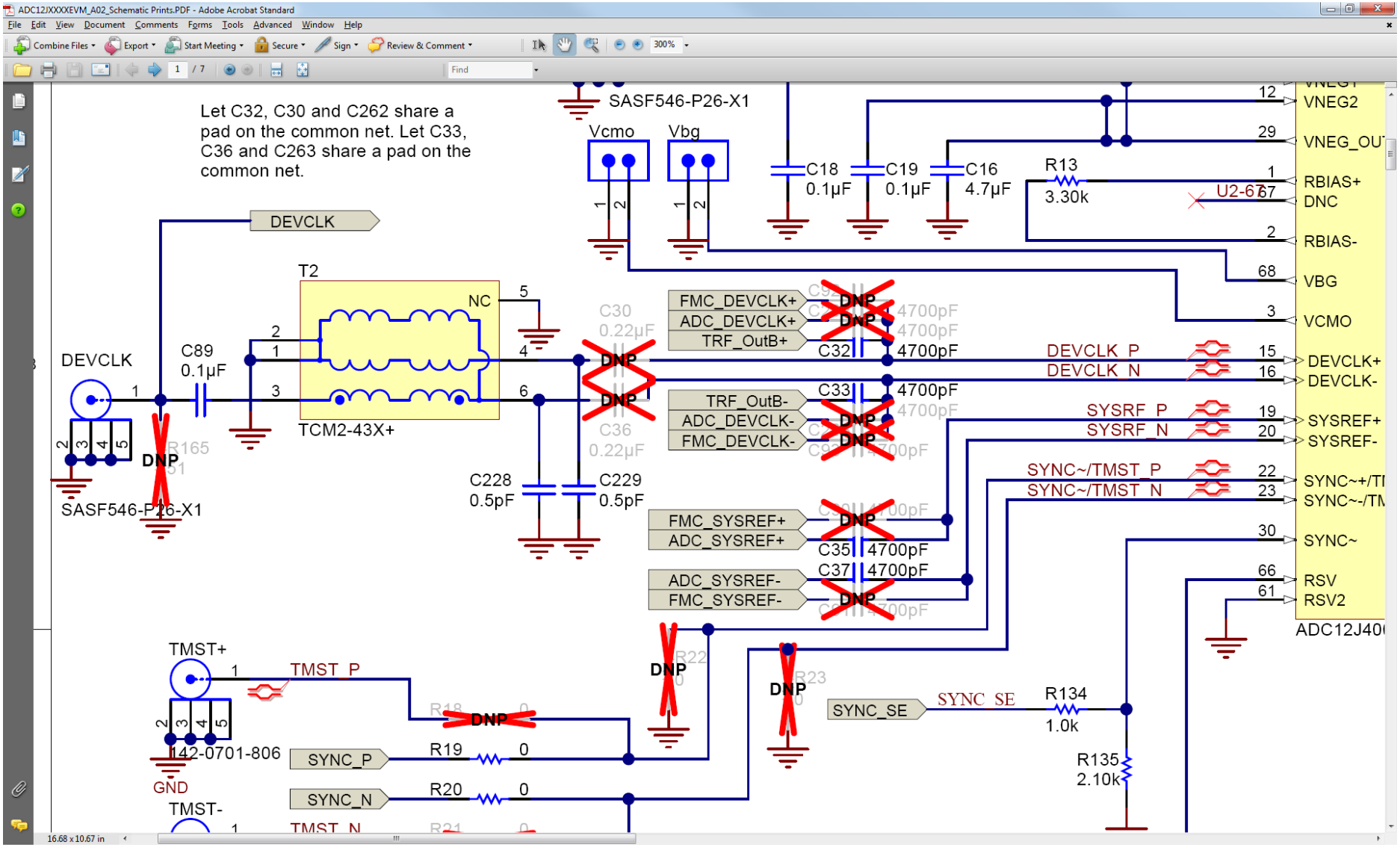
## External Clocking of ADC12DJxx00EVM and LM15851EVM Rev A0

Using external clock generators is possible. Two separate generators will be needed for clocking, one at the ADC sample rate applied to the DEVCLK input connector, and one at exactly ½ the ADC sample rate applied to the LMKCLK connector. The clock source generators must be frequency locked using the 10 MHz reference input/output connectors. If coherent sampling is desired the input signal source should be synchronized to the clock generators.

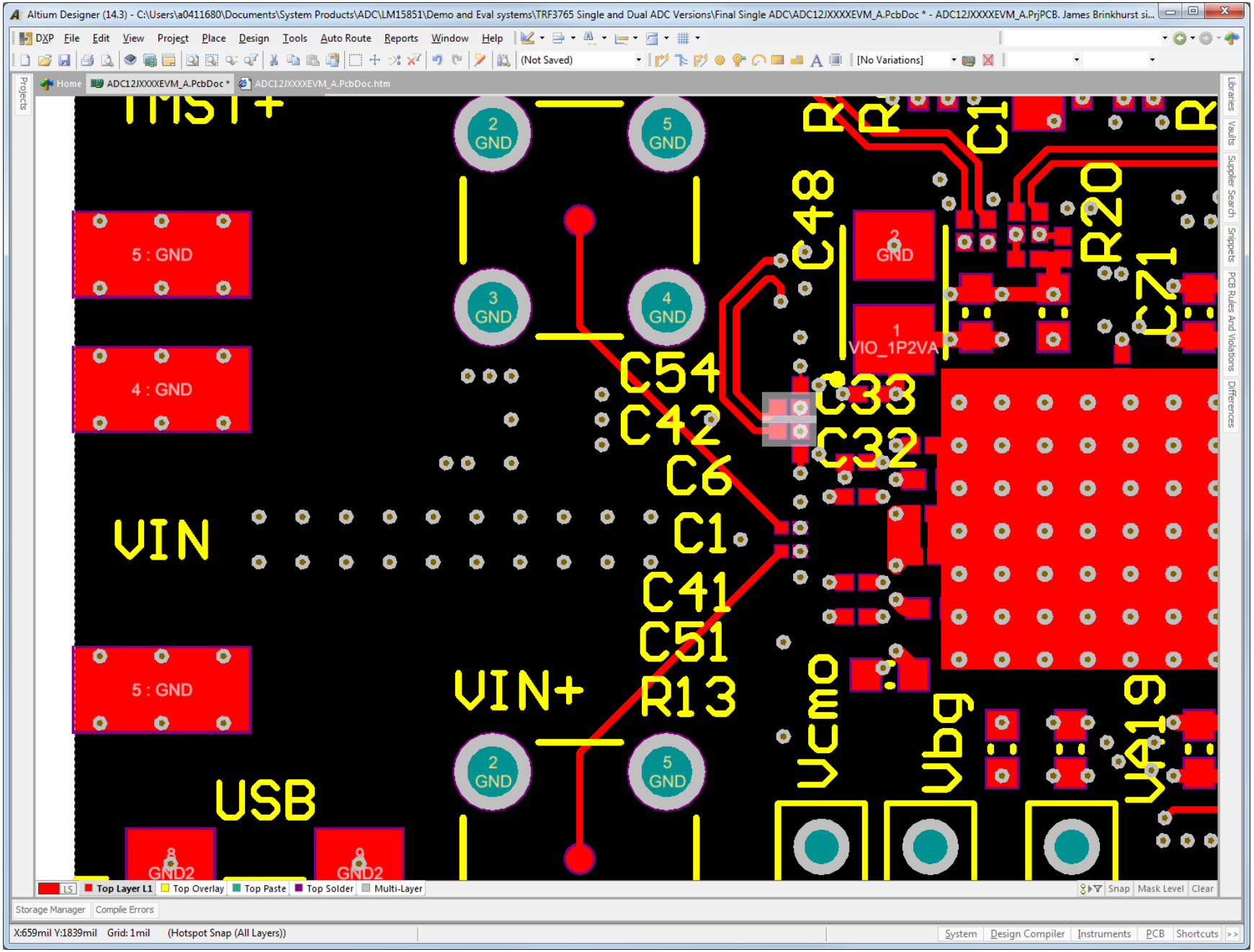
The required board modifications are shown on the following pages.

**External Clocking – Single Ended DEVCLK and LMKCLK inputs**

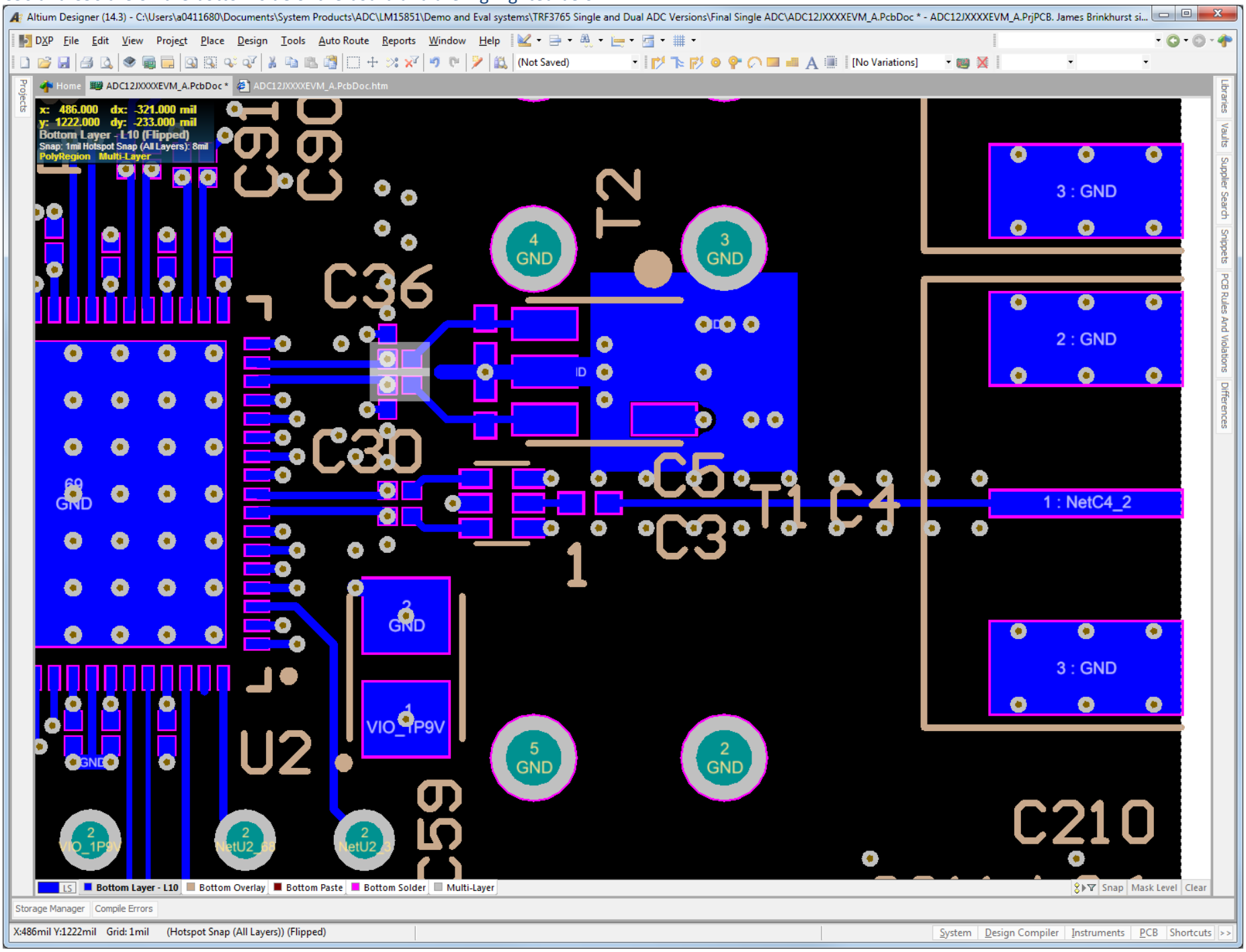
**DEVCLK - Remove capacitors C32 and C33 (top side of board near VIN- SMA connector) and move them to locations for C30 and C36 (opposite side of board in same area)**



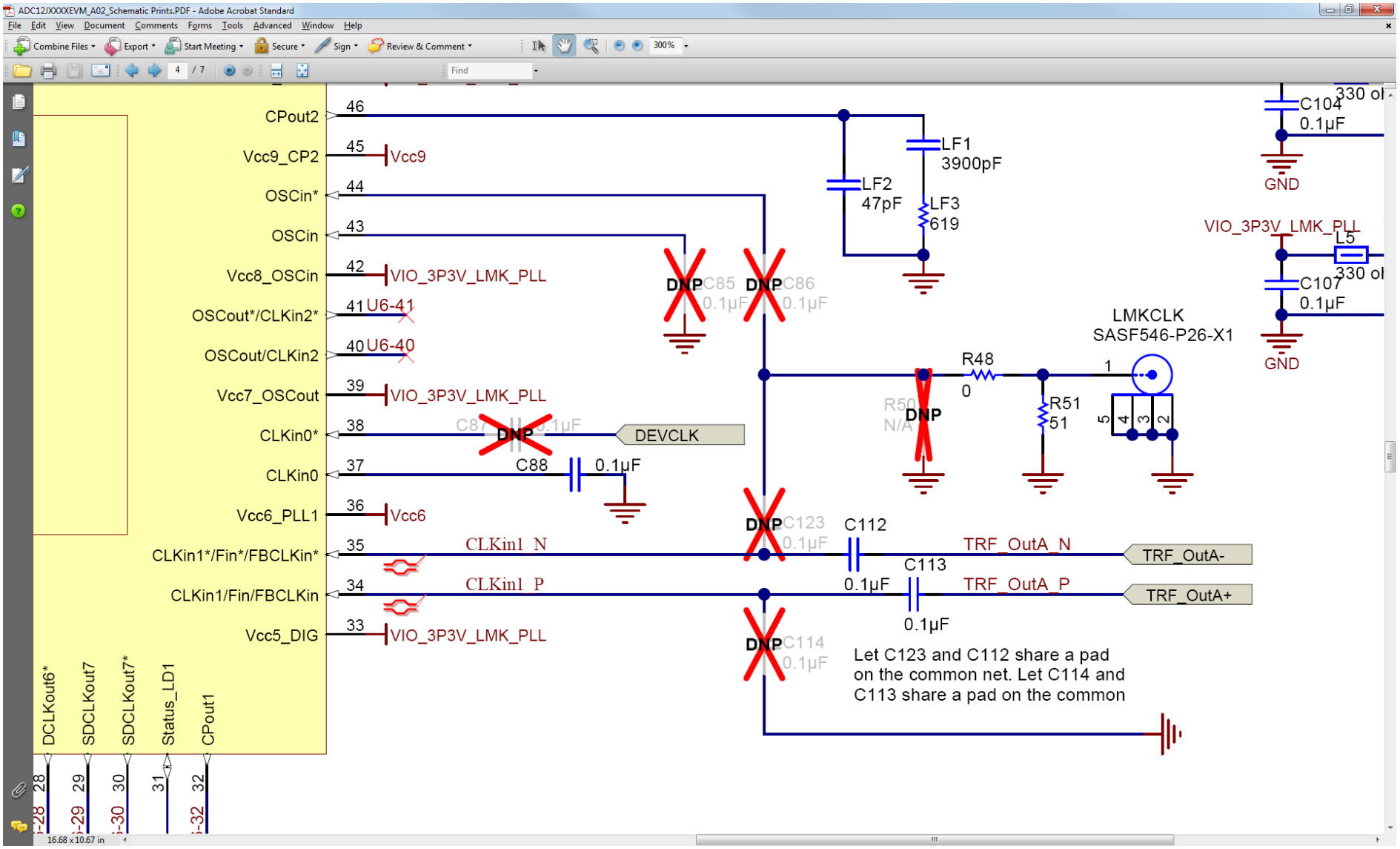
C32 and C33 are on the top side of the board as shown. Silkscreen designators for highlighted capacitors C33 and C32 have been added to this image for clarity but are not printed on the board:



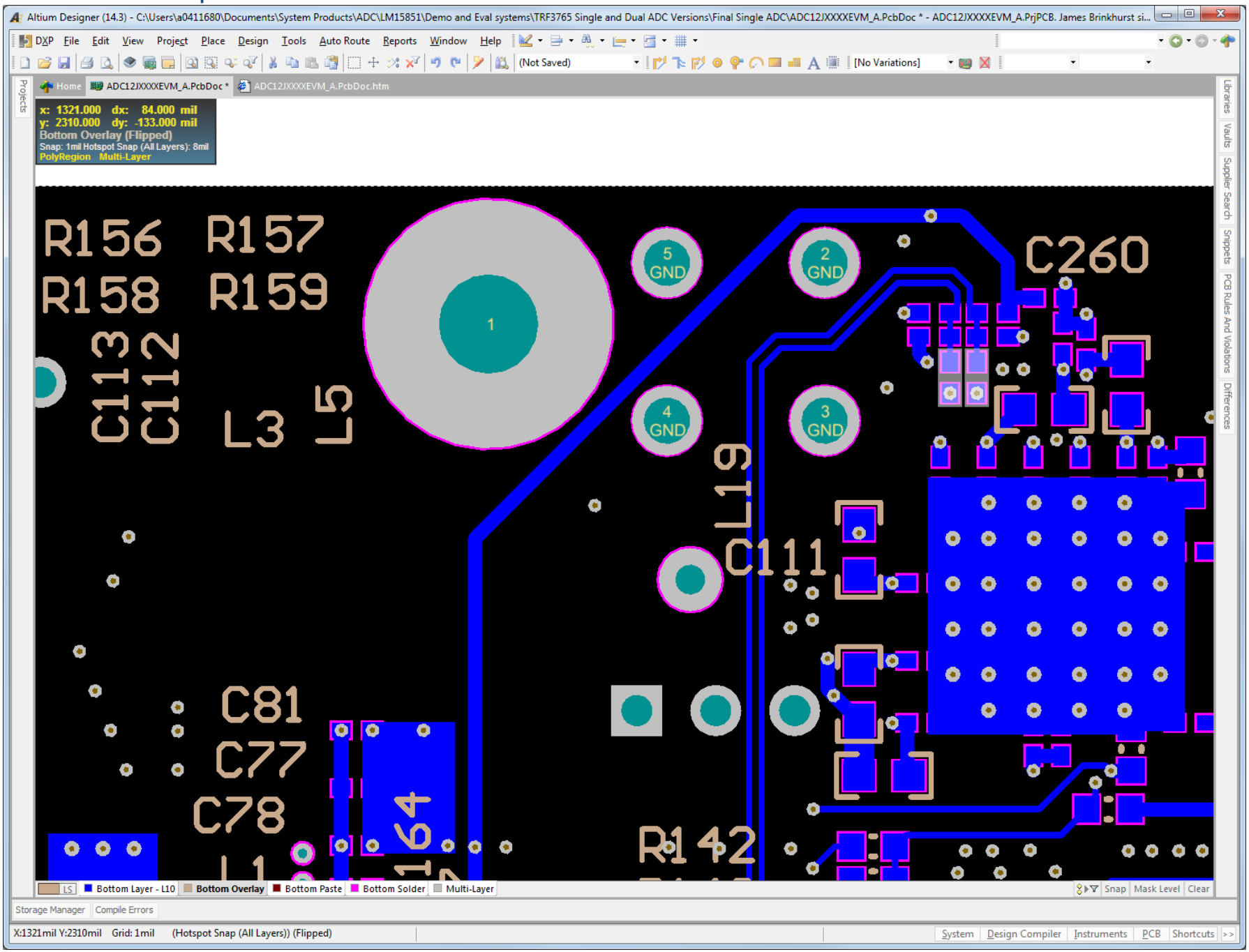
C30 and C36 are on the bottom side of the board and are highlighted below:



**LMKCLK – (Move capacitors from sites for C112 and C113 (bottom of board near LMKCLK SMA) to sites for C123 and C114, (top side of board near LMKCLK SMA connector).**



**C112 and C114 are on the bottom side of the board as shown below. The designators for this block of components are offset to the left where there is room to show the relationships:**



**C114 and C123 are on the top side of the board near the LMKCLK connector:**