ADS7042EVM-PDK

This user's guide describes the characteristics, operation and use of the ADS7042-EVM performance demonstration kit (PDK). This kit is an evaluation platform for the ADS7042 low power, 12-bit, successive approximation register (SAR) analog-to-digital converters (ADCs) that supports single-ended analog inputs.

This EVM eases the evaluation of the ADS7042 device with hardware and software for computer connectivity through universal serial bus (USB). This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials.

The following related documents are available through the Texas Instruments web site at http://www.ti.com.

Table 1. Related Documentation

Device	Literature Number
OPA835	SLOS713
TPS79101	SLVS325
REG71055	SBAS221
TPS62080	SLVSAE8
TPS3836K33	SGLS322

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1 Overview

The ADS7042EVM-PDK is a platform for evaluation of the ADS7042 ADC. The evaluation kit combines the ADS7042EVM board with a Simple Capture Card controller board. This controller card consists of a TI Sitara embedded microcontroller (AM3352) and a field-programmable gate array (FPGA). It provides an interface from the EVM to the computer through a universal serial bus (USB) port. The included software communicates with the Simple Capture Card, and the controller card provides the power and digital signals used to communicate with the ADS7042EVM board. These demonstration kits include the ADS7042EVM board, the Simple Capture Card, a microSD memory card, and an A-to-micro-B USB cable.

1.1 ADS7042 EVM Features

- Contains support circuitry as a design example to match ADC performance
- 3.3-V slave serial peripheral interface (SPI)
- Onboard 5-V analog supply
- Onboard OPA835 (56-MHz bandwidth, Rail-to-Rail Out) ADC input drivers

1.2 ADS7042EVM-PDK Features

- USB port for computer interface
- Easy-to-use evaluation software for Microsoft® Windows® XP, Windows 7, and Windows 8 operating systems
- Built-in analysis tools including scope, FFT, and histogram displays
- Data collection to text files supported

2 EVM Analog Interface

The ADS7042 is an extremely low-power, extremely small size ADC that supports single-channel ended analog inputs. The ADS7042EVM uses an OPA835 amplifier to drive the inputs of the ADC. The ADS7042EVM is designed for easy interfacing to multiple analog sources. SMA connector J3 (please refer to the schematics in Section 7.3) allows the EVM to have input signals connected through a coaxial cable. In addition, header connector P2 provides a convenient way to connect input signals. All analog inputs are buffered by the OPA835 amplifier in order to properly drive the ADS7042 ADC inputs.

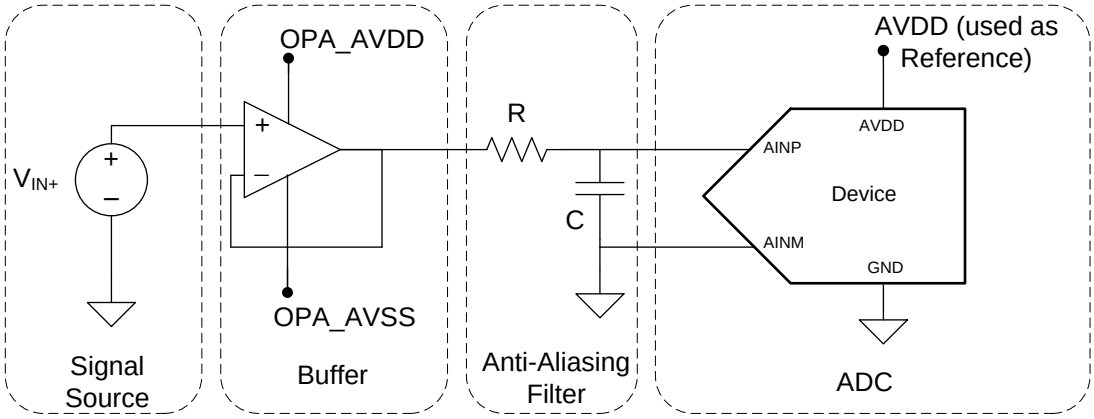

Figure 1. ADS7042EVM Analog Input Connections

Table 2 lists the analog interface connectors available. Since the AVDD supply functions as the reference for the ADC, the voltage provided on the J3 or P2 connector can vary from 0 V to AVDD. Connecting an input signal greater than AVDD would cause the ADC output codes to saturate.

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Table 2. Analog Input Connections

Reference Designator	Signal	Description
J3	INP	Positive single-ended input provided at the SMA
P2	INP	Alternate location to provide the positive single-ended input. Normally not populated on the board.

3 Power Supplies

The ADS7042 supports a wide range of operation on its analog supplies. The AVDD can operate from 1.8V to 3.6V. The DVDD operates from 1.65 V to 3.6 V, independent of the AVDD supply.

The analog portion of the ADS7042EVM-PDK operates from a 5-V supply. The ADS7042EVM-PDK is configured to use the onboard regulated analog 5-V supply that in turn generates an AVDD analog supply using the low-noise TPS79101 LDO. This supply is nominally set to 3.3 V at the factory, but this voltage maybe changed to any value within the valid range, by modifying the value of R46 as per Table 3. In case any intermediate value needs to be set, the detailed formula to arrive at these values are available in the TPS79101 (SGLS160) datasheet.

Table 3. AVDD Voltage Settings

AVDD Voltage	R46	R45	C34
1.8 V	14.2 kΩ	30.1 kΩ	33 pF
2.0 V	19.1 kΩ	30.1 kΩ	27 pF
2.5 V	31.6 kΩ	30.1 kΩ	22 pF
3.0 V	43.7 kΩ	30.1 kΩ	15 pF
3.3 V (default)	51.1 kΩ	30.1 kΩ	15 pF
3.6 V	59.0 kΩ	30.1 kΩ	15 pF

Alternatively, AVDD may be set by connecting an external power source through P3. Table 4 describes the modifications required for on-board or external AVDD supply.

Table 4. AVDD Voltage Settings

AVDD Source	Position	Setting
Onboard regulated AVDD (set to 3.3 V)	P3	Closed
External AVDD	P3	Open
	R47	Disassembled

CAUTION

The external AVDD supply applied to external connector P3 must not exceed 3.6 V as this may damage the device. The external AVDD supply must be in the range of 1.8 V to 3.6 V for proper operation of the ADS7042EVM.

The digital portion of the ADS7042 ADC operates from a 3.3-V supply from the Simple Capture Card. The buffer U12 is included to ensure that the SDO can be driven to the controller with minimal distortion.

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4 Digital Interface

The ADS7042 digital output is available in SPI-compatible format, which makes interfacing with microprocessors, digital signal processors (DSPs) and FPGAs easy. The ADS7042EVM offers 50-Ω resistors between the SPI signals and edge connector J1 to aid with signal integrity. Typically, in high-speed SPI communication, fast signal edges can cause overshoot; these resistors slow down the signal edges in order to minimize signal overshoot.

The ADS7042EVM has clearly marked test points for all the SPI signals to allow observation of the interface signals using an oscilloscope.

5 ADS7042EVM-PDK Initial Setup

This section presents the steps required to set up the ADS7042EVM-PDK kit before operation.

5.1 Default Jumper Settings

A silkscreen plot detailing the default jumper settings is shown in Figure 2.

Table 5 explains the configuration for these jumpers.

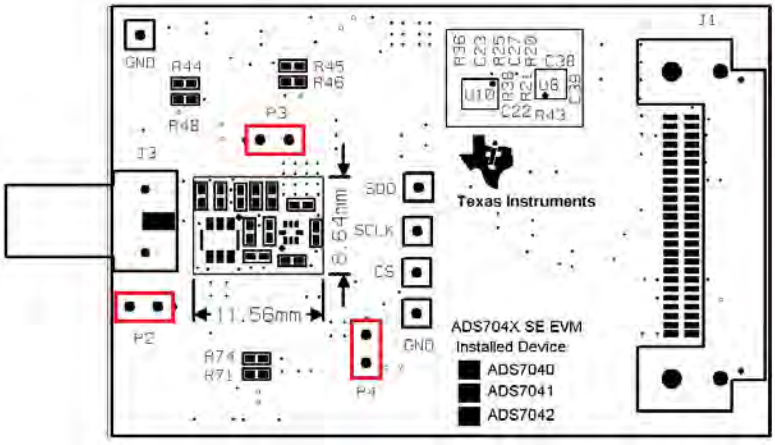

Figure 2. ADS7042EVM Default Jumper Settings

Table 5. Default Jumper Configurations

Reference Designator	Default Position	Description
P2	Open	Alternate location for the analog input to the ADS7042EVM (unassembled by default)
P3	Closed	Closed to connect on-board 3.3-V supply directly to AVDD of the ADS7042
P4	Open	Unassembled, by default

5.2 Software Installation

This section presents the steps required to the install the software. Section 6 explains how to operate the software to acquire data.

NOTE: Ensure the microSD memory card included in the kit is installed in the microSD socket (P6) on the back of the Simple Capture Card as well as the microSD socket (J2) before connecting the EVM to the PC. Also ensure that the cards are not swapped or overwritten. If the contents of these cards are not available during boot up, Windows will not recognize the ADS7042EVM-PDK as a connected device.

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Complete the following steps to install the software:

Step 1. Ensure that the microSD memory cards on both the Simple Capture Card and ADS7042 are installed.

Step 2. Verify jumpers are in the factory-default positions and connect the hardware.

Step 3. Locate, copy and install the ADS7042EVM software to the PC.

Step 4. Complete the device driver installation.

Each of these steps is described in the following subsections.

5.2.1 Install the microSD Memory Cards on the Simple Capture Card Controller Board

As mentioned in the previous section, the ADS7042EVM-PDK includes two microSD memory cards. One is installed on the microSD socket (P6) at the back of the Simple Capture Card as shown in Figure 3. The second microSD memory card is installed on the mircoSD socket (J2) at the back of the ADS7042EVM as shown in Figure 4.

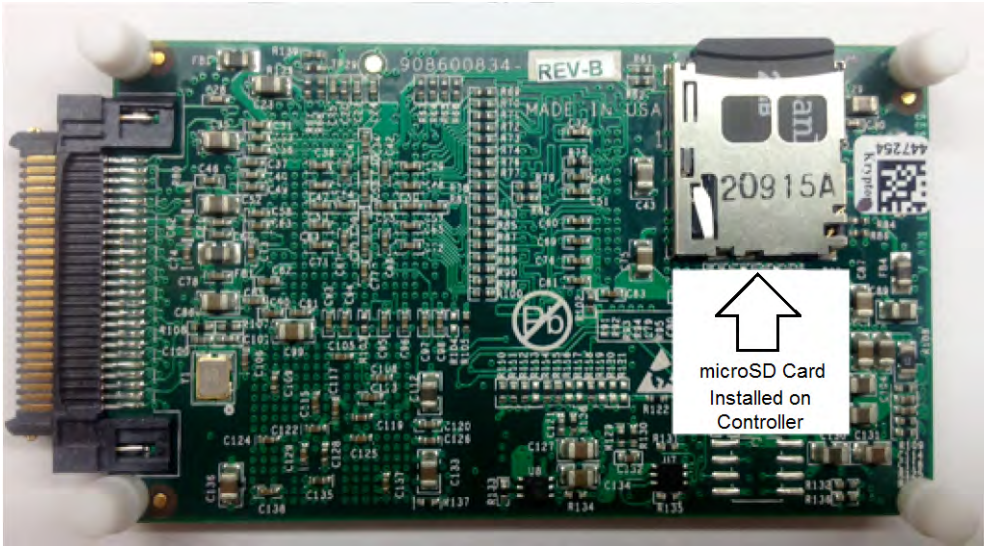

Figure 3. Bottom View of Simple Capture Card with microSD Memory Card Installed

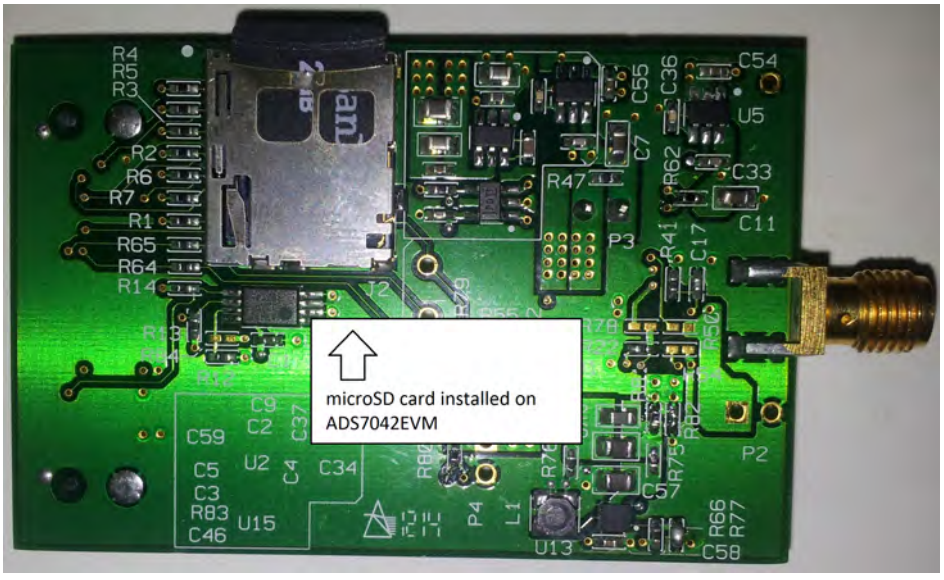

Figure 4. Bottom View of ADS7042EVM Board with microSD Memory Card Installed

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The microSD memory card is formatted at the factory with the necessary firmware files for the Simple Capture Card to boot properly. In addition to this the microSD card on the EVM contain Simple Capture Card firmware files (app and MLO files) and the ADS7042EVM-PDK software installation files inside the ADS7042 EVM V#.#.# folder. <V#.#.#> refers to the installation software version number, and increments with software installer releases.

5.2.2 Verify Jumpers are in the Factory-Default Position and Connect the Hardware

The ADS7042EVM-PDK includes both the ADS7042EVM and the Simple Capture Card; however, the boards are shipped unconnected.

Follow these steps to verify that ADS7042EVM-PDK kit is configured and connected properly:

Step 1. Verify the ADS7042EVM jumpers are configured as shown in Figure 2.

Step 2. Verify the microSD card is installed on the back of the Simple Capture Card, as shown in Figure 3.

Step 3. Verify the microSD card is installed on the back of the EVM board, as shown in Figure 4.

Step 4. Connect the ADS7042EVM board to the Simple Capture Card as Figure 5 illustrates.

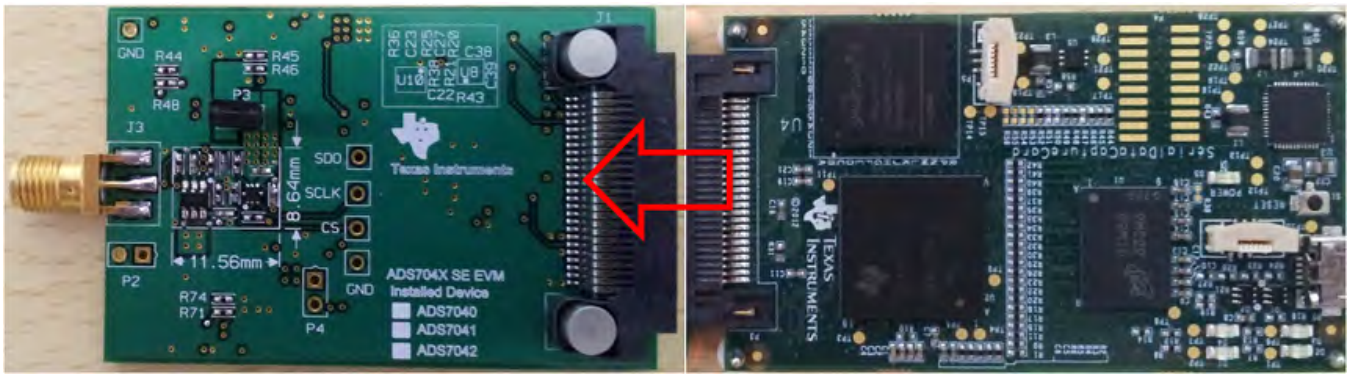

Figure 5. Connecting ADS7042EVM Board to Simple Capture Card

Step 5. Connect the Simple Capture Card to the PC through the micro USB cable.

Step 6. Verify that the LED D5 Power Good indicator is illuminated. Wait approximately ten seconds and verify that diode D2 blinks, indicating that USB communication with the host PC is functioning properly. Figure 6 shows the location of the LED indicators in the Simple Capture Card.

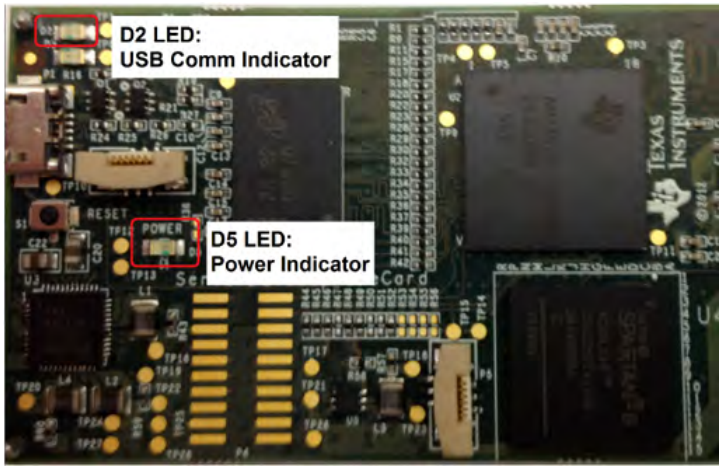

Figure 6. LED Indicators on the Simple Capture Card

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5.2.3 Install the ADS7042EVM-PDK Software

The ADS7042 EVM V#.#.# software must be installed on the PC. This software supports the ADS7042-PDK. Administrator privileges are required to install the EVM software. The following steps list the directions to install the software:

Step 1. Open Windows Explorer and find the microSD memory card in the browser as a storage device.

Step 2. Navigate to the ...*ADS7042 EVM Vx.x.x**Volume*\ folder.

Step 3. Run the installer by double-clicking the file *setup.exe*. This action installs the EVM GUI software and the required and device driver components.

Step 4. After the installer begins, a welcome screen displays. Click *Next* to continue.

Step 5. A prompt appears with the destination directory; select the default directory under: ...*Program Files(x86)**Texas Instruments**ADS7042evm*\.

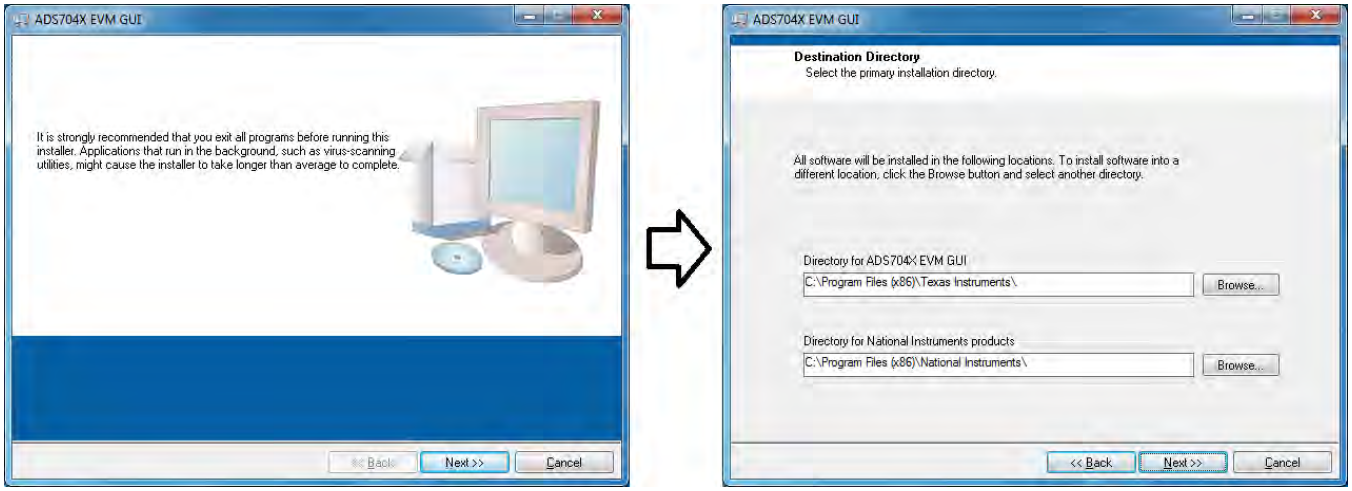

Figure 7. Welcome Screen and Destination Directory Screens

Step 6. One or more software license agreements appear. Select *I Accept the License Agreement* and click *Next*.

Step 7. The *Start Installation* screen appears. Click *Next*.

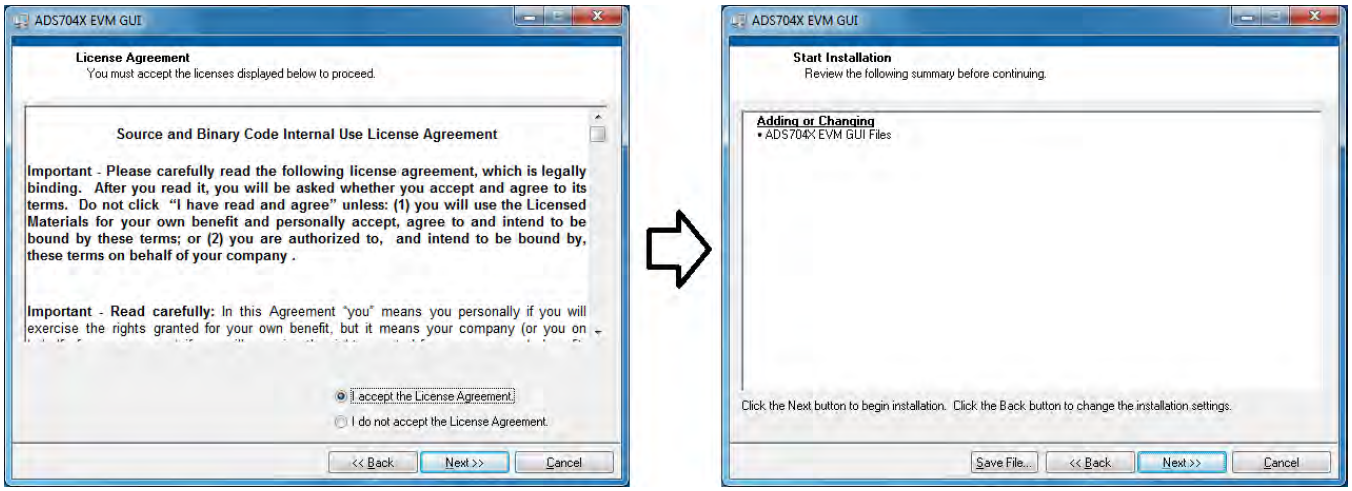

Figure 8. License Agreement and Start Installation Screens

Step 8. A progress bar appears; this step takes a few minutes.

Step 9. The progress bar is followed by an *Installation Complete* notice.

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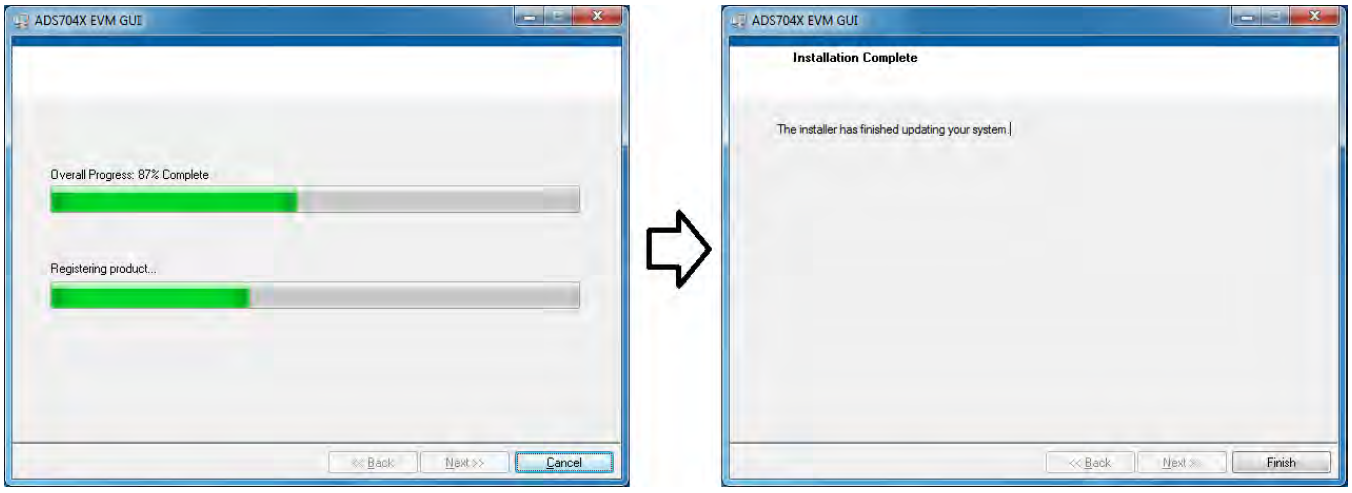

Figure 9. Progress Bar and Installation Complete Screens

5.2.4 Complete the Simple Capture Card Driver Installation

During installation of the Simple Capture Card driver, a prompt may appear with the Windows security message shown in Figure 10. Select *Install this driver software anyway* to install the driver required for proper operation of the software. The drivers contained within the installers are safe for installation to your system.

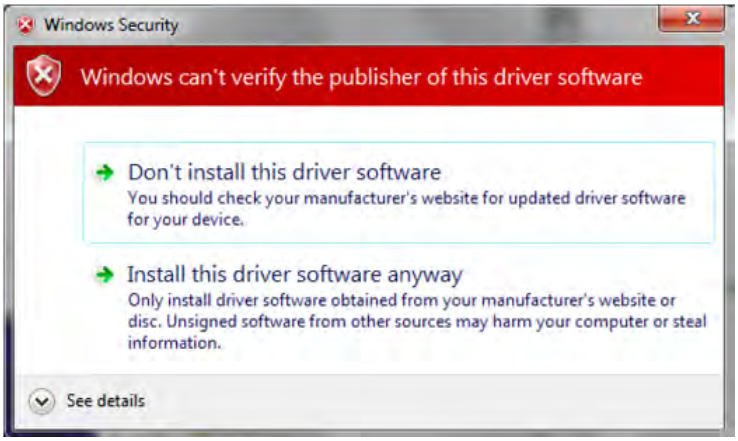

Figure 10. Windows 7 Driver Installation Warning

NOTE: Driver installation prompts do not appear if the Simple Capture Card driver has been installed on your system previously.

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The following steps describe how to install the Simple Capture Card driver:

Step 1. Immediately after the ADS7042 EVM software installation is complete, prompts appear to install the Simple Capture Card driver, as shown in Figure 11 and Figure 12.

Step 2. A computer restart may be required to finish the software installation. If prompted, restart the PC to complete the installation.

Figure 11. Simple Capture Card Driver Installation

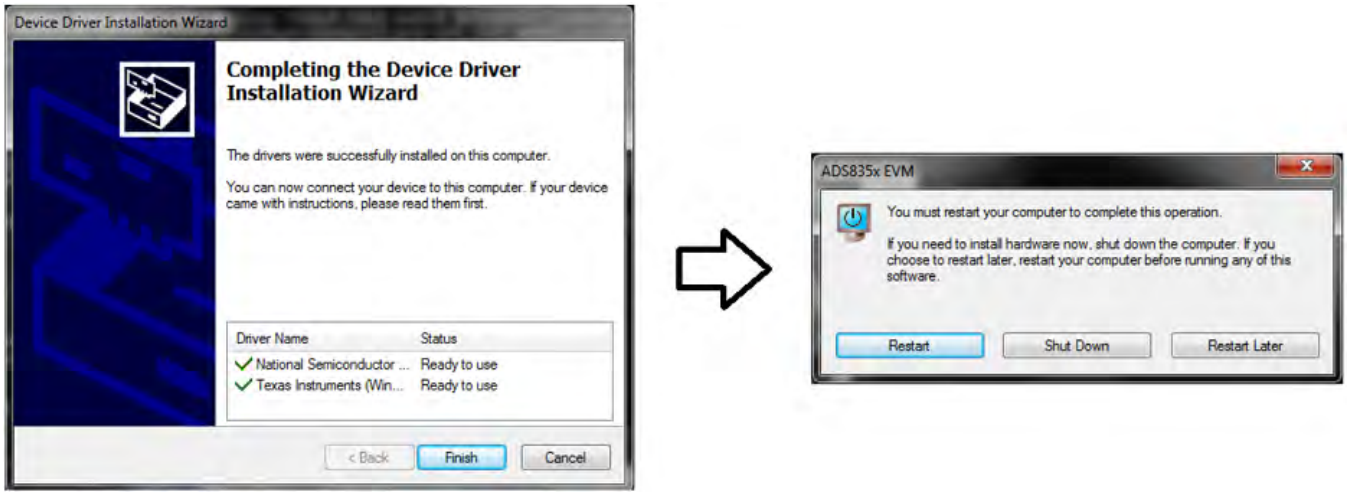

Figure 12. Simple Capture Card Driver Completion

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6 ADS7042EVM-PDK Kit Operation

This section describes how to use ADS7042EVM-PDK and the ADS7042EVM software to configure the EVM and acquire data.

6.1 About the SCC Controller Board

The SCC controller board provides the USB interface between the PC and the ADS7042. The controller board is designed around the AM335x processor, a USB 2.0 high-speed capability, 32-bit ARM core. The SCC controller board incorporates an onboard FPGA subsystem and 256MB of onboard DDR SRAM memory. The SCC controller board is not sold as a development board, and it is not available separately. TI cannot offer support for the SCC controller` board except as part of this EVM kit.

6.2 Loading the ADS7042EVM Software

The ADS7042 EVM software provides the ability to capture and analyze data from the ADS7042.

To load the ADS7042 EVM software, follow these steps:

Step 1. Make sure the EVM kit is configured and powered up as explained in Section 5.

Step 2. Start the ADS7042 EVM software. Go to Start → All Programs →Texas Instruments → ADS7042 EVM and click ADS7042 EVM to run the software.

Step 3. Verify that the software detects the ADS7042. The GUI identifies the EVM hardware that is connected to the controller board and displays the *ADS7042EVM Front Page*. After the settings are loaded, *ADS7042EVM GUI* is displayed at the top of the GUI screen, which the device identified indicated at the right hand top corner as shown in Figure 13.

Figure 13. GUI Display Prompt

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6.3 Capturing Data with the ADS7042-PDK

Access the *Data Capture* page in the GUI to monitor data acquired by the ADS7042. This GUI page displays the acquired data versus time. To access the *Data Capture* page, hover the cursor over the blue arrow at the left center side of the GUI screen; a menu with different GUI pages appears. Click on the *Data Capture* option in the menu as shown in Figure 14.

Figure 14. Open the Data Capture Page on the GUI

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Figure 15 shows the *Data Capture* page of the EVM GUI. The device SCLK frequency and capture settings can be configured at the top right hand corner of the *Data Capture* page. Changes made to the configuration settings are executed on pressing the *Capture* button. The following list describes the different options available on the *Data Monitor* page.

- **SCLK:** This control sets the clock frequency used by the SPI interface to capture data. By configuring the SCLK frequency, the sampling rate of the ADS7042 is set. The ADS7042EVM-PDK software supports SCLK frequencies of 3.2 MHz to 16 MHz. In case the input in this field is beyond the capability of the device, it will be adjusted to the nearest value that can be supported.
- **Sampling Rate:** The upper limit of the sampling rate (displayed in ksps) is set based on the SCLK frequency selected. However, sampling rates lower than this displayed value may be set. The GUI supports these lower rates by increasing the CS high time between frames. Details of the interface protocol can be studied in the serial interface timing diagrams in the ADS7042 datasheet (SBAS608). In case the input to this field is beyond the capability calculated based on SCLK, it will be constrained to the maximum sampling rate possible at that SCLK frequency.
- **Sample Count:** This option is used to select the number of contiguous samples captured in a block. The drop-down menu can be used to select a data block in the range of 1024 samples to 1,048,576 samples per channel. The interface provides a drop-down list for values restricted to 2n, where n is an integer.

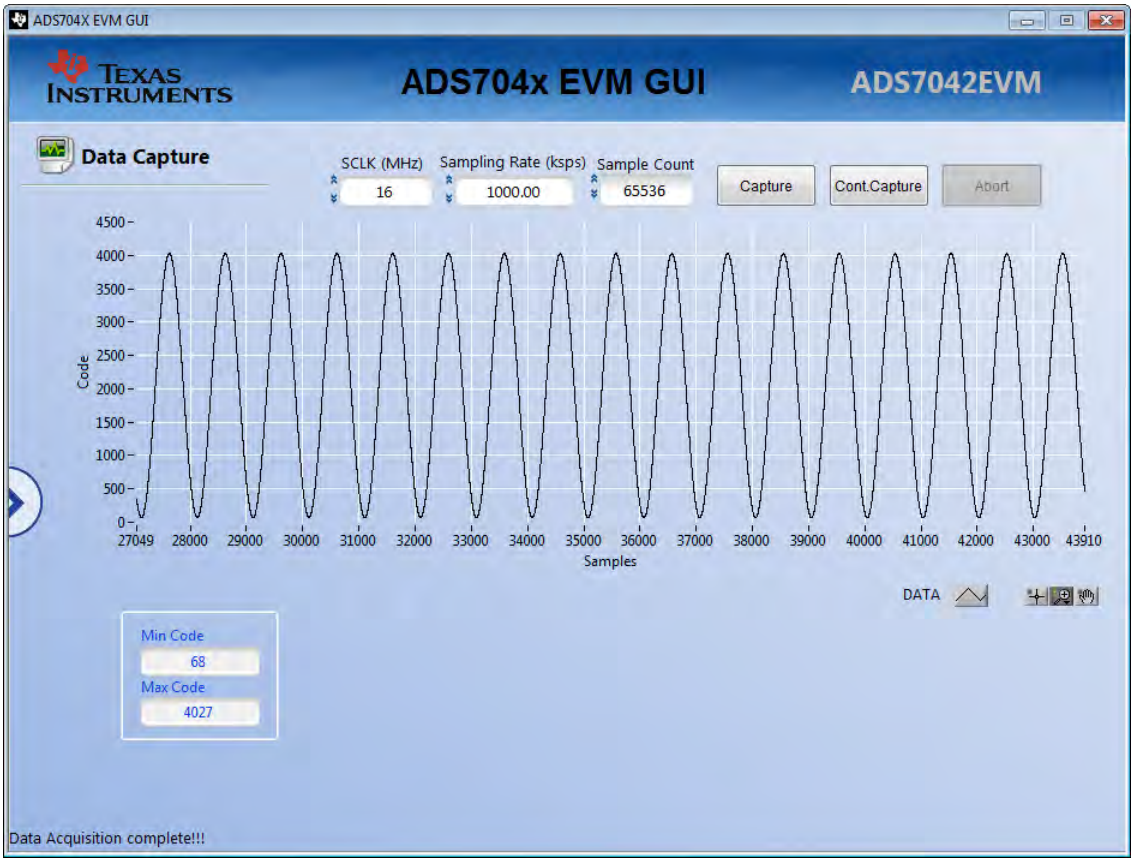

Figure 15. Data Capture Page

Once the ADC data is captured by the GUI using either of the *Capture* buttons, it is displayed on the graph area on this tab as shown in Figure 15. Once plotted, the graph can be zoomed into, panned, or resized by using the controls at the bottom of the graph area. The data captured may also be transferred to a file for further analysis by right clicking on the body of the graph and using the various options listed under *Export*.

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6.4 FFT Analysis

The *Performance Analysis* page in the GUI performs the fast Fourier transform (FFT) of the captured data and displays the resulting frequency domain plot. This page also calculates key ADC dynamic performance parameters, such as signal-to-noise ratio (SNR), total harmonic distortion (THD), signal-to-noise and distortion ratio (SINAD), and spurious-free dynamic range (SFDR). Figure 16 shows the FFT performance analysis display. The FFT calculated parameters are shown on the bottom right side of the display.

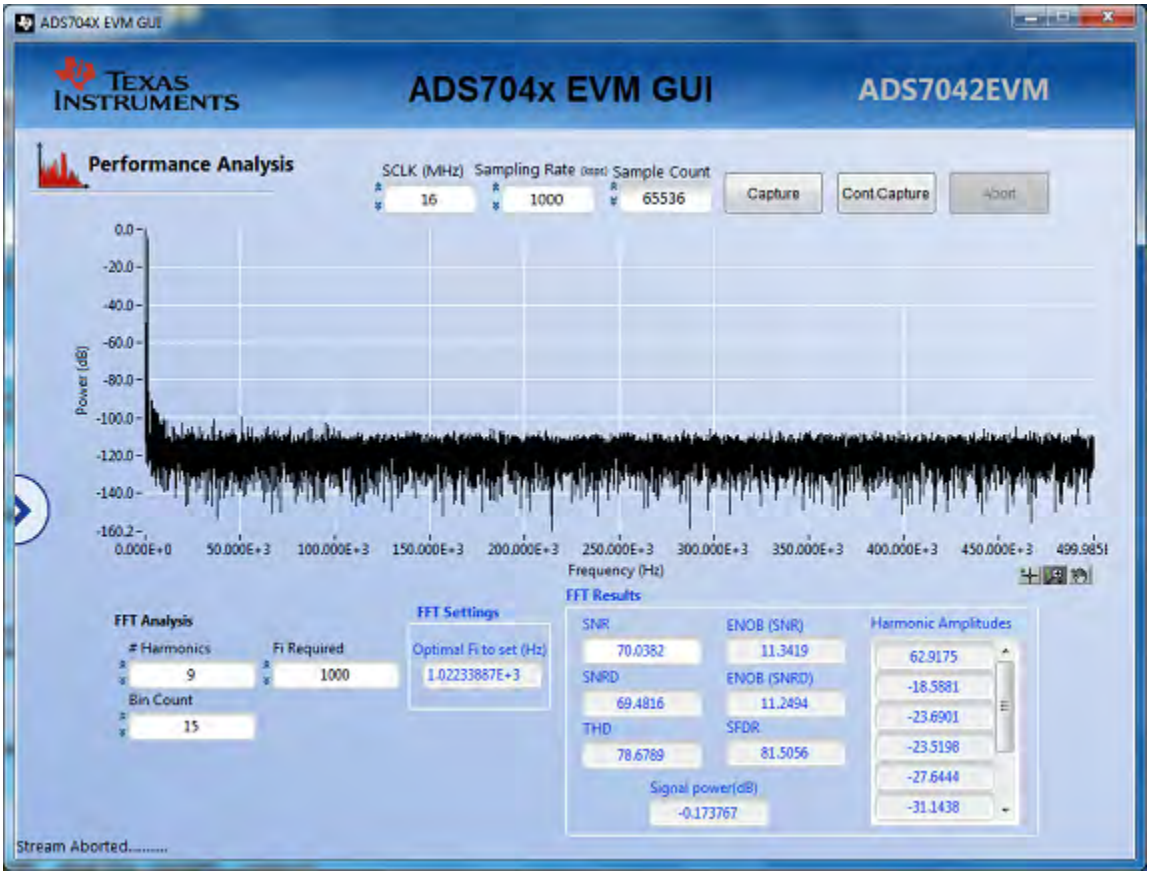

Figure 16. FFT Performance Analysis Page

6.4.1 FFT Analysis Settings and Controls

The SCLK, Sampling Rate and Sample Count fields are the same as described in Section 6.3.

Fi Required: Enter the frequency of the largest amplitude analog input signal here.

Optimal Fi to set: Adjust your input frequency from the signal source to this value computed by the GUI based on the *Fi Required* value entered. A minor difference from *Fi Required* will be seen here to enable a system to be coherent in nature.

Window: The window function is a mathematical function that reduces the signal to zero at the end points of the data block. In applications where coherent sampling cannot be achieved, a window-weighting function can be applied to the data to minimize spectral leakage. The following options are available:

- No windowing (no window weighting function applied; use for coherent data)
- Windowing. In this case the 7-Term Blackman-Harris window is applied by default. For a more thorough discussion of windowing, refer to IEEE1241-2000.
- # Harmonics: This field sets the number of harmonics to be included in the calculations of the harmonic distortion. Any harmonic signal greater than this number is treated as noise in the performance calculations. The typical value used in this analysis is 9 as per the ADS7042 datasheet (SBAS608).

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6.5 Histogram Analysis

Histogram testing is commonly used when characterizing ADCs. A histogram is merely a count of the number of times a code has occurred in a particular data set. The *Histogram Analysis* page of the GUI creates a histogram of the data of the acquired data set and displays it. Figure 17 shows the *Histogram Analysis* page of the GUI.

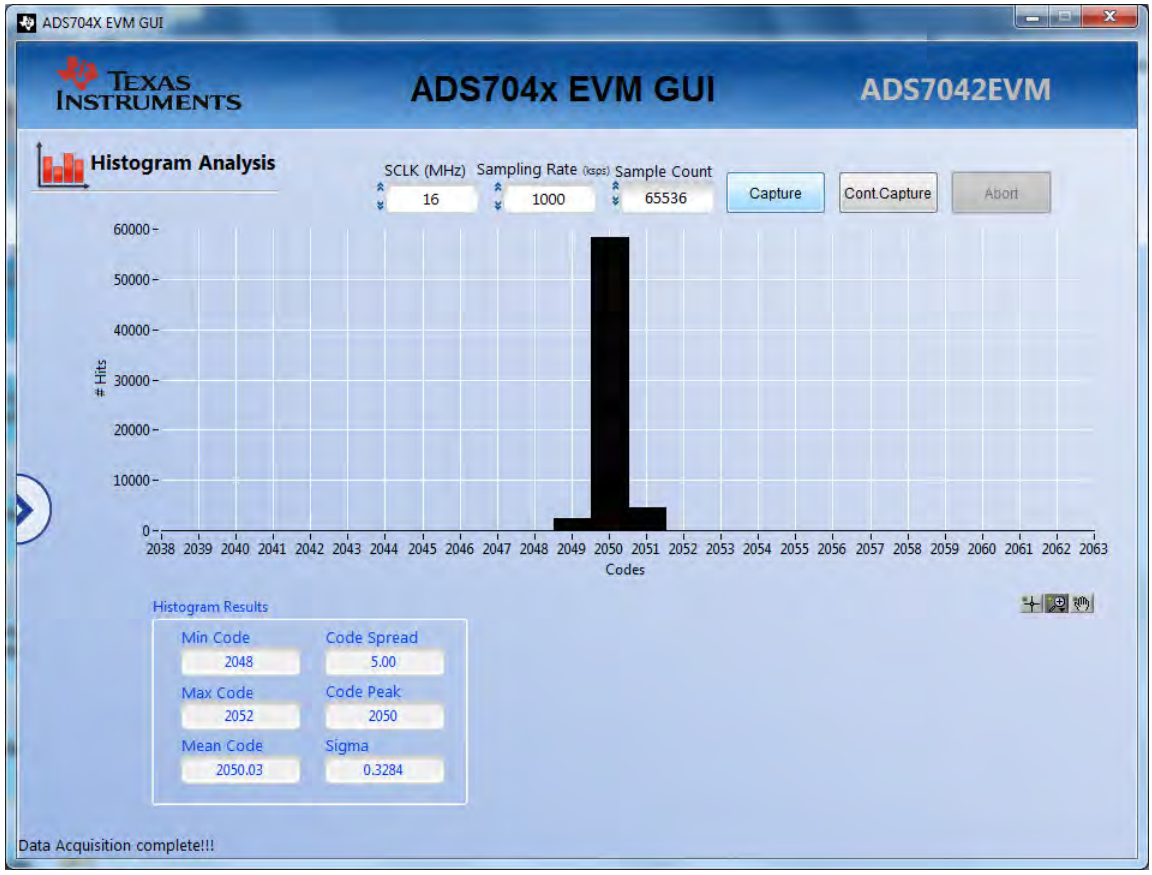

Figure 17. Histogram Analysis Page

The Histogram *Analysis* table shown in Figure 17 displays several parameters of the captured data set as described in the following list. Please note, all results displayed in this page are in LSBs.

- The *Min Code*, *Max Code*, and *Mean Code* indicators display the minimum, maximum and average value of the captured data set.
- The *Code Spread* column shows the peak-to-peak spread of the codes in the data set.
- The *Sigma* indicator displays standard deviation of the data set. This value is equivalent to the RMS noise of the signal when analyzing a dc data set.

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6.6 Offset Calibration

The ADS7042 device has the ability to calibrate its internal offset. The offset calibration can be initiated by the user either on power-up or during normal operation. During offset calibration, the analog input pins (AINP and AINM) are disconnected from the sampling stage and connected to an internal reference. The result of the offset calibration in stored in an internal register. For subsequent conversions, the device adjusts the conversion results provided on the SDO output with the value stored in this internal register.

The ADS7042 GUI implements offset calibration as described in the *Offset Calibration During Normal Operation* section of ADS7042 datasheet (SBAS608). Figure 18 depicts the *Offset Calibration* page of the GUI.

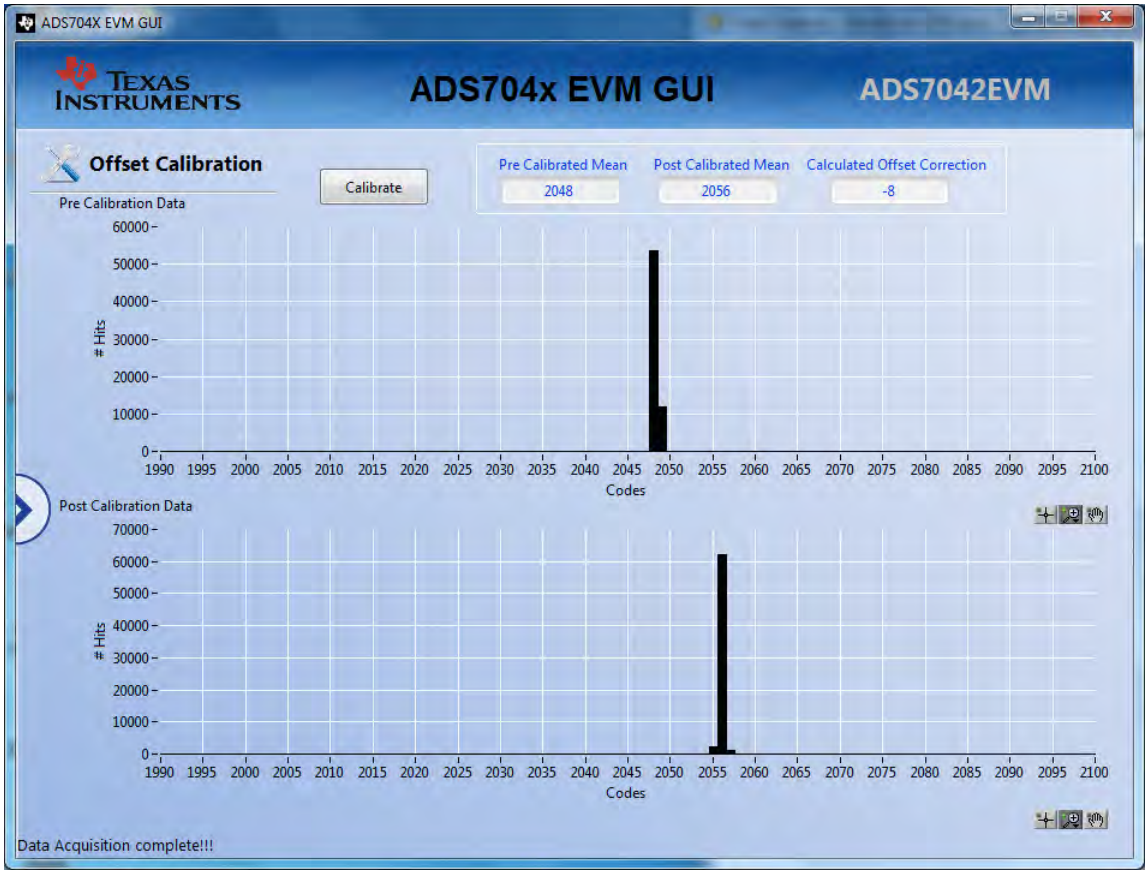

Figure 18. Offset Calibration Page

The Offset Calibration test is best conducted with a DC input at the Analog Input Terminal of the ADS7042EVM. Simply click the *Calibrate* button. The GUI first performs a histogram test for the device described in Section 6.5 and populates the first of the two graphs. The pre-calibrated Mean code is inserted in the indicator. Next, the calibration frame is sent to the ADS7042 device that enables the internal offset calibration logic. The GUI performs the histogram test for a second time and the second graph is populated and Post Calibrated Mean value computed. Finally, the difference between the first and second computed mean is populated in the Calculated Offset Correction indicator.

The computed offset for all subsequent attempts to calibrate the device will always yield a result of within the limits specified in the datasheet. This indicates that after the calibration is performed for the first time, the offset is actually being applied on all subsequent conversions. This computed offset will remain fixed, unless the device is reset or there is a significant change in operating temperature or analog supply voltage.

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6.7 Estimated Current Consumption

The last tab in the GUI tabs menu opens up an *Estimated Current Consumption* tab as shown in Figure 19. This tab highlights the extremely low current and power consumption of the ADS7042 device and its scaling with sampling rate and AVDD voltage. This is computed based on characterization data collected across multiple devices at room temperature and it not based on data from the actual board connected to the GUI.

Set the desired Sampling rate and AVDD using the two dial in the right hand side of the page and observe the estimated current and power on the graph and the indicators on this page.

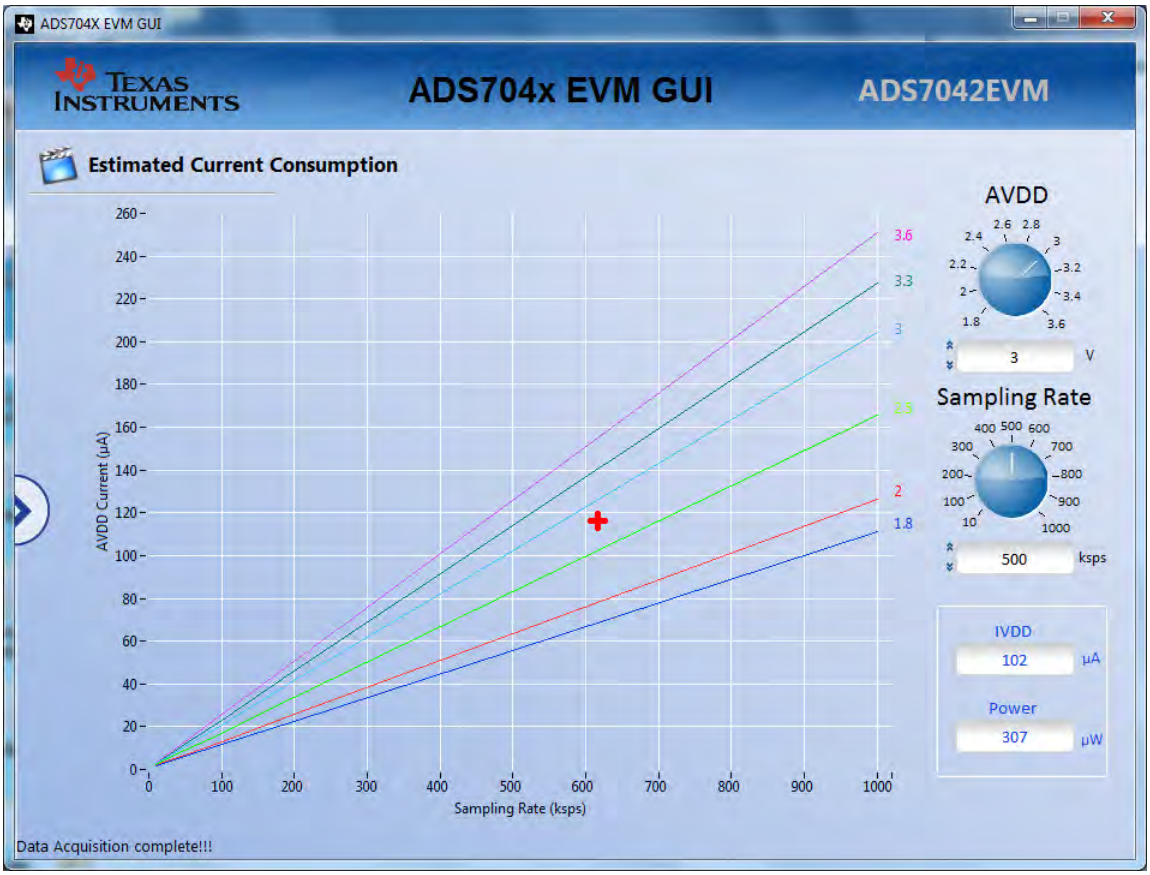

Figure 19. Estimated Current Consumption Page

6.8 Troubleshooting

Although the ADS7042EVM GUI rarely stops responding while the ADS7042EVM-PDK is connected, in case this does happen, unplug the USB cable from the EVM, unload the ADS7042EVM-PDK software, reconnect the ADS7042EVM-PDK to the PC and reload the ADS7042EVM software.

When initially setting up the EVM, the software detects the EVM hardware, and loads the appropriate hardware settings. If the EVM hardware is not detected, the GUI defaults to the *Capture Mode: Simulation* mode of operation using a preloaded captured data file for demonstration purposes.

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7 Bill of Materials, PCB Layout, and Schematics

This section lists the bill of materials of the ADS7042EVM, shows the printed circuit board (PCB) layout for the ADS7042EVM. The schematics for the ADS7042EVM are appended to the end of this user's guide.

7.1 Bill of Materials

NOTE: All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant.

Table 6. ADS7042EVM Bill of Materials

Qty	Reference Designators	Description	Vendor	Part Number
6	C1 ,C22, C23, C40, C41, C46	Capacitor, 0402, Ceramic, 0.1µF, 10V, 10%, X5R	Murata	GRM155R61A104KA01
1	C2	Capacitor, 0402, Ceramic, 2.2µF, 4V, 20%, X5R	Murata	GRM155R60G225ME15D
6	C3, C38, C39, C54, C55, C58	Capacitor, 0402, Ceramic, 1µF,10V,10%,X7S	TDK	C1005X7S1A105K050BC
1	C4	Capacitor, 0402, Ceramic, 0.22µF,16V,10%	Murata	GRM155R71C224KA12
5	C5, C7, C9, C11, C52	Capacitor, 0603, Ceramic, 10µF,6.3V,20%,X5R	Murata	GRM188R60J106ME47D
2	C17, C27	Capacitor, 0402, Ceramic, 1500pF,50V,5%,C0G/NP0	Kemet	C0402C152J5GACTU
2	C33, C34	Capacitor, 0402, Ceramic, 15pF,50V,1%,C0G/NP0	Murata	GRM1555C1H150FZ01D
2	C36, C37	Capacitor, 0402, Ceramic, 10000pF,50V,10%,X7R	Murata	GRM155R71H103KA88D
3	C56, C57, C59	Capacitor, 0805, Ceramic, 47µF,6.3V,20%,X5R	Murata	GRM21BR60J476ME15L
1	J1	Connector, Female, 50P, .8mmLS	SAMTEC	ERF8-025-01-L-D-RA-L-TR
1	J2	Connector, Micro SD Card,SMD,8P	TYCO Electronic	5025700893
1	J3	SMA Jack, Edge Mount, Gold, Straight, 50Ω	SAMTEC	SMA-J-P-X-ST-EM1
1	L1	Inductor, 2P, Power Choke 1uH, 30%	Wurth	744029001
2	P2, P4	Uninstalled	Uninstalled	Header,MalE,2Pin,0.100CC
1	P3	Header W/Shunt,2P,100LS TL=.125	TYCO Electronics	103321-2
9	R1, R2, R3, R4, R5, R6,R7, R83, R85	Resistor, 0402,10.0K,1%,1/16W	Panasonic	ERJ-2RKF1002X
6	R12, R22, R62, R79, R80, R81	Resistor, 0402,0Ω,1/16W, Zero Jumper	Venkel	CR0402-16W-000T
2	R13, R14	Resistor, 0402, Thick Film,5%,1/16W,1.5K	Panasonic	ERJ-2GEJ152
3	R20, R21, R25	Resistor, 0402,25.5Ω,1%,1/16W	Panasonic	ERJ-2RKF25R5X
5	R36, R38, R43, R64, R65	Resistor, 0402,49.9Ω,1/16W, 1%, 100ppm	VISHAY	CRCW040249R9F100
1	R41	Resistor, 0402, Thick Film,5%,1/16W,1.0M	Panasonic	ERJ-2GEJ105
3	R44, R45, R71	Resistor, 0402, Thick Film,30.1KΩ,1%,1/10W	Panasonic	ERJ-2RKF3012X
1	R46	Resistor, 0402,51.1K,1%,1/16W	Panasonic	ERJ-2RKF5112X
3	R47, R75, R76	Resistor, 0402,10Ω,1/16W,1%,100ppm	VISHAY	CRCW040210R0F100
1	R48	Resistor, 0402, 88.7KΩ, 1/16W, 1%	VISHAY	CRCW040288K7FKED
5	R50, R54, R55, R78, R82	Uninstalled	Uninstalled	CRCW04020000Z0ED
1	R66	Resistor, 0402, Thick Film,5%,1/16W,5.6K	Panasonic	ERJ-2GEJ562
1	R74	Resistor, 0402,16.2KΩ,1/16W,1%	VISHAY	CRCW040216K2FKED
1	R77	Resistor, 0402,3.3K,1/16W,1%,100ppm	VISHAY	CRCW04023301F100
1	R84	Uninstalled	Uninstalled	CRCW04021002F100
5	TP1, TP2, TP3, TP4, TP5	Testpoint, Thru-hole, Miniature, 0.1LS,120TL, Black	Keystone Electronics	5001
1	U1	IC, I2C Compatible, Serial EEPROM, TSSOP-8	ATMEL	AT24C02C-XHM
1	U2	IC,60mA, 5.0V, Buck/Boost Charge Pump, TSOT23-6	Texas Instruments	REG71055DDC
2	U4, U5	1.2~5.5V,Ultralow Noise High PSRR Fast RF 100mA LDO Linear Regulator	Texas Instruments	TPS79101DBVREP
1	U8	IC, Low-power SAR ADC, RUG-8, 1.5x1.5x0.4mm	Texas Instruments	ADS7042IRUG

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Table 6. ADS7042EVM Bill of Materials (continued)

Qty	Reference Designators	Description	Vendor	Part Number
1	U10	Ultralow Power Regulator	Texas Instruments	OPA835IDBV
1	U12	Single-Bit Dual-supply Bus Transceiver	Texas Instruments	SN74AVCH1T45DBVR
1	U13	IC, 1.2A, High Efficient Step Down Converter with Snooze Mode, SON-8	Texas Instruments	TPS62080DSG
1	U15	IC, Nanopower Supervisory Circuits, SOT23-5	Texas Instruments	TPS3836K33DBVR
1	for J2	SanDisk microSDHC™ Card - 4GB	SANDISK	SDSDQ-004G-A11M

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7.2 PCB Layout

Figure 20 through Figure 23 show the PCB layouts for the ADS7042EVM.

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing ADS7042EVM PCBs.

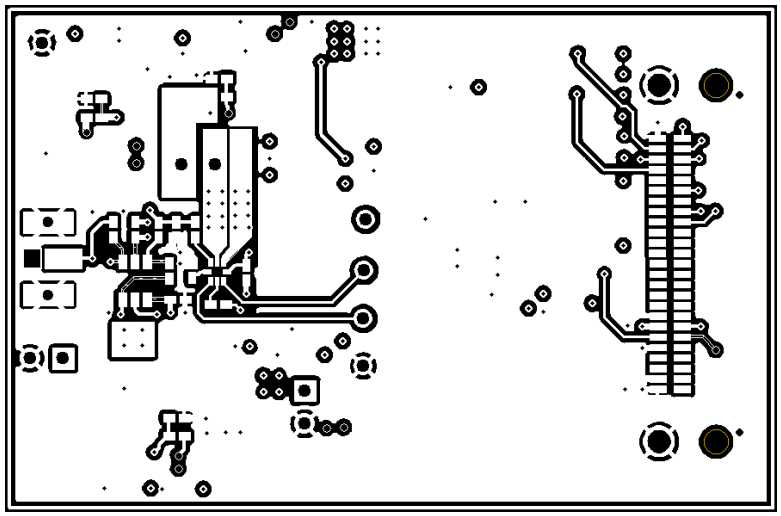

Figure 20. ADS7042EVM PCB: Top Layer (L1)

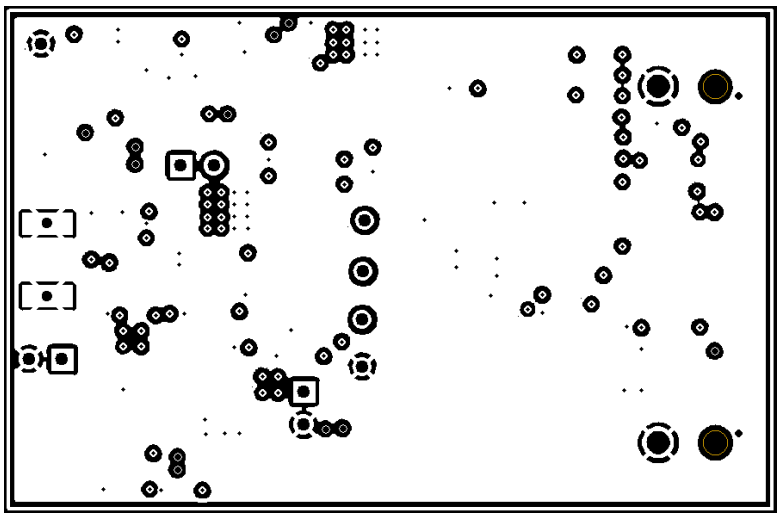

Figure 21. ADS7042EVM PCB: GND Layer (L2)

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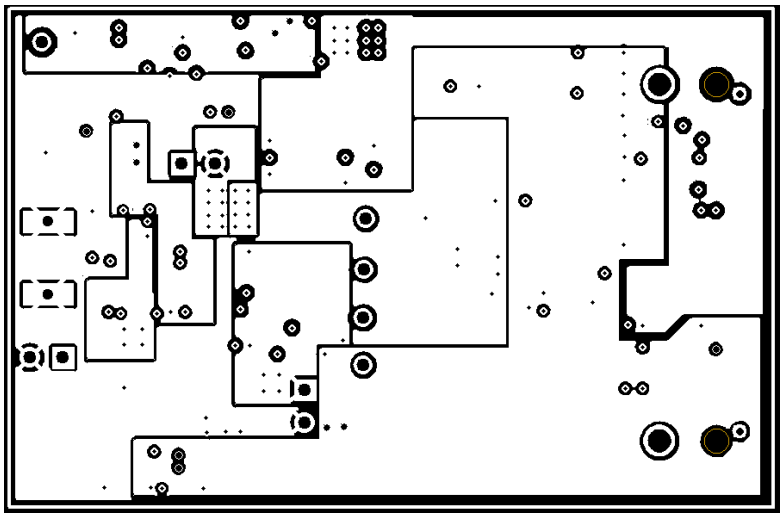

Figure 22. ADS7042EVM PCB: Power Layer (L3)

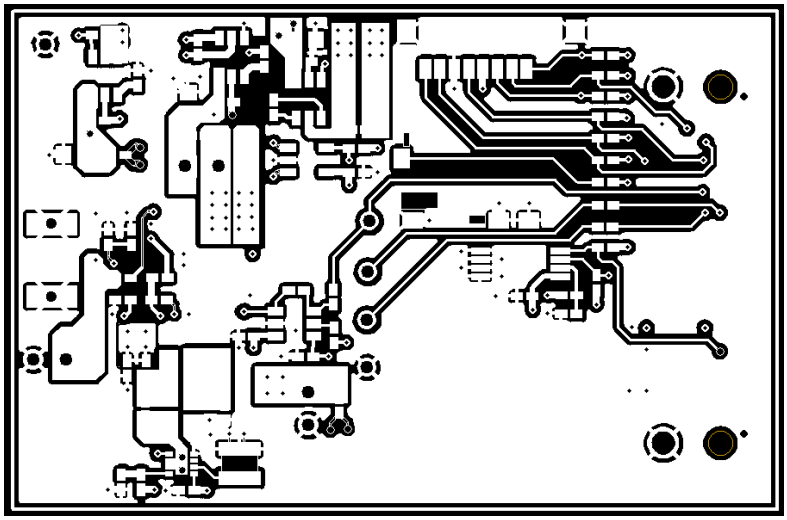

Figure 23. ADS7042EVM PCB: Bottom Layer (L4)

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7.3 Schematics

The schematics for the ADS7042EVM are appended to the end of this user's guide.

Revision History

Changes from Original (June 2014) to A Revision	Page
• Changed serial data capture card to simple capture card globally, beginning in the *Overview*.	3
• Changed wording in first paragraph after *ADS7042 EVM Analog Input Connections* image.	3

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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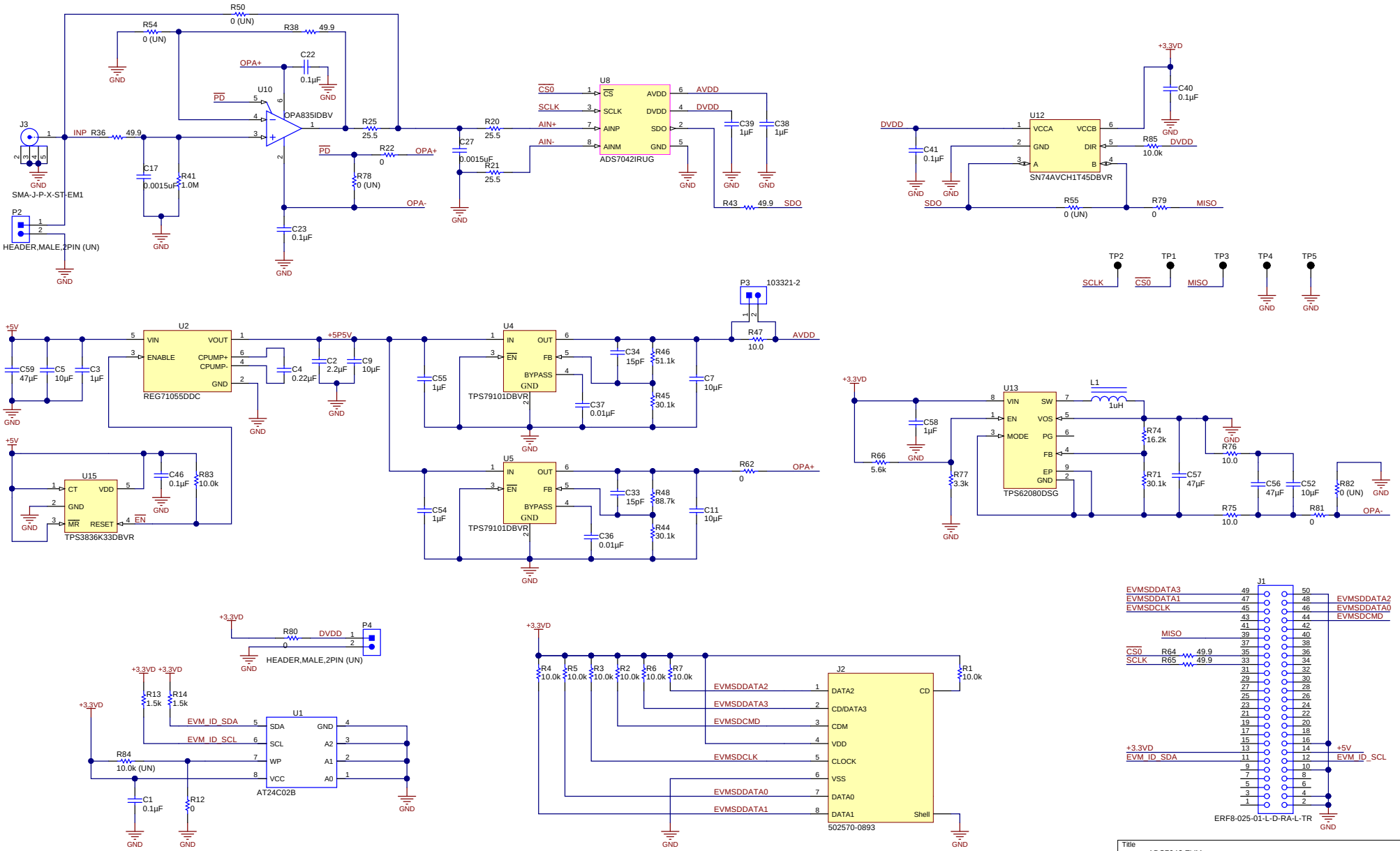
R50 0 (UN)
R54 0 (UN)
R38 49.9
OPA+
C22 0.1µF
U10
OPA835IDBV
PD
J3
SMA-J-P-X-ST-EM1
INP
R36 49.9
C17 0.0015µF
R41 1.0M
P2
HEADER,MALE,2PIN (UN)
R25 25.5
R22 0
R78 0 (UN)
OPA-
C23 0.1µF
R20 25.5
R21 25.5
C27 0.0015µF
U8
ADS7042IRUG
CS0
SCLK
AIN+
AIN-
AVDD
DVDD
SDO
GND
C39 1µF
C38 1µF
R43 49.9 SDO
+3.3VD
C40 0.1µF
U12
SN74AVCH1T45DBVR
DVDD
C41 0.1µF
R85 10.0k
R55 0 (UN)
R79 0
MISO
TP2
TP1
TP3
TP4
TP5
SCLK
CS0
MISO
P3 103321-2
R47 10.0
AVDD
+5V
U2
REG71055DDC
VIN
VOUT
ENABLE
CPUMP+
CPUMP-
C59 47µF
C5 10µF
C3 1µF
C4 0.22µF
C2 2.2µF
C9 10µF
+5P5V
U4
TPS79101DBVR
IN
OUT
EN
FB
BYPASS
C55 1µF
C34 15pF
R46 51.1k
R45 30.1k
C37 0.01µF
C7 10µF
U5
TPS79101DBVR
C54 1µF
C33 15pF
R48 88.7k
R44 30.1k
C36 0.01µF
C11 10µF
R62 0
OPA+
U15
TPS3836K33DBVR
CT
VDD
MR
RESET
C46 0.1µF
R83 10.0k
EN
+3.3VD
U13
TPS62080DSG
VIN
SW
EN
VOS
MODE
PG
FB
EP
L1 1uH
C58 1µF
R66 5.6k
R77 3.3k
R74 16.2k
R71 30.1k
C57 47µF
R76 10.0
R75 10.0
C56 47µF
C52 10µF
R82 0 (UN)
R81 0
OPA-
J1
ERF8-025-01-L-D-RA-L-TR
EVMSDDATA3
EVMSDDATA1
EVMSDCLK
MISO
CS0
SCLK
R64 49.9
R65 49.9
EVMSDDATA2
EVMSDDATA0
EVMSDCMD
+3.3VD
EVM_ID_SDA
+5V
EVM_ID_SCL
P4
HEADER,MALE,2PIN (UN)
R80 0
DVDD
U1
AT24C02B
SDA
SCL
WP
VCC
GND
A2
A1
A0
EVM_ID_SDA
EVM_ID_SCL
R84 10.0k (UN)
R13 1.5k
R14 1.5k
C1 0.1µF
R12 0
J2
502570-0893
DATA2
CD/DATA3
CDM
VDD
CLOCK
VSS
DATA0
DATA1
CD
Shell
R4 10.0k
R5 10.0k
R3 10.0k
R2 10.0k
R6 10.0k
R7 10.0k
R1 10.0k
Title
ADS7042 EVM
Size
B
Number
Revision
A
Date: 13-11-2014
Sheet 1 of 1
File: D:\ADS704x EVM\..\ADS704x_SE_EVM.SchDoc
Drawn By:

STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.

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   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.

   2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan are NOT certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】

本開発キットは技術基準適合証明を受けておりません。

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2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

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西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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