DAC38RF8x EVM

File Debug Settings Help

DAC38RFxx EVM GUI v3p1

Quick Start | DAC38RF8x | LMK04828 | Low Level V

Reconnect?

Overview | Clocking | SERDES and Lane Configuration | JESD Block | Digital(DAC A) | Digital(DAC B) | PAP | Alarm Monitoring

SERDES Configuration

☑ Enable Offset Compensation

Equalizer Mode
Fully Adaptive

Gain Boost | Hold EQ
6 dB | Off

CDR Algorithm | LOS
0 | Disabled

Align
Comma Alignment

Rate | RX Sleep
Half Rate | ☐

Termination | Buswidth
AC Coupled | 20-bit

SERDES Lane Testing

SERDES Test Pattern
Test mode disabled

DTEST
Test Disabled

DTEST Lane Select
0

3: SYNC SOURCE (PIN)

None | GPO0
None | GPO1
SLICE0 | SYNC0B
None | SYNC1B

SYNCB Vcm
1.2 V

SYNCB Sleep
☐

	SLICE0 Lane Configuration			SLICE1 Lane Configuration		
	SERDES Lanes	JESD Lanes		SERDES Lanes	JESD Lanes	
Invert?	EN	Lane ID	Which RX?	EN	Lane ID	Which RX?
RX0 ☐	☑	0	3	☐	0	5
RX1 ☐	☑	1	2	☐	1	7
RX2 ☐	☑	2	1	☐	2	6
RX3 ☐	☑	3	0	☐	3	4
RX4 ☐	☐	4	5	☑	4	3
RX5 ☐	☐	5	7	☑	5	2
RX6 ☐	☐	6	6	☑	6	1
RX7 ☐	☐	7	4	☑	7	0

SLICE 1 JESD BLOCK

Equalizer, Sampler, Deserializer, Muxing and FIFOs

SLICE 0 JESD BLOCK

Idle

HARDWARE CONNECTED

TEXAS INSTRUMENTS

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