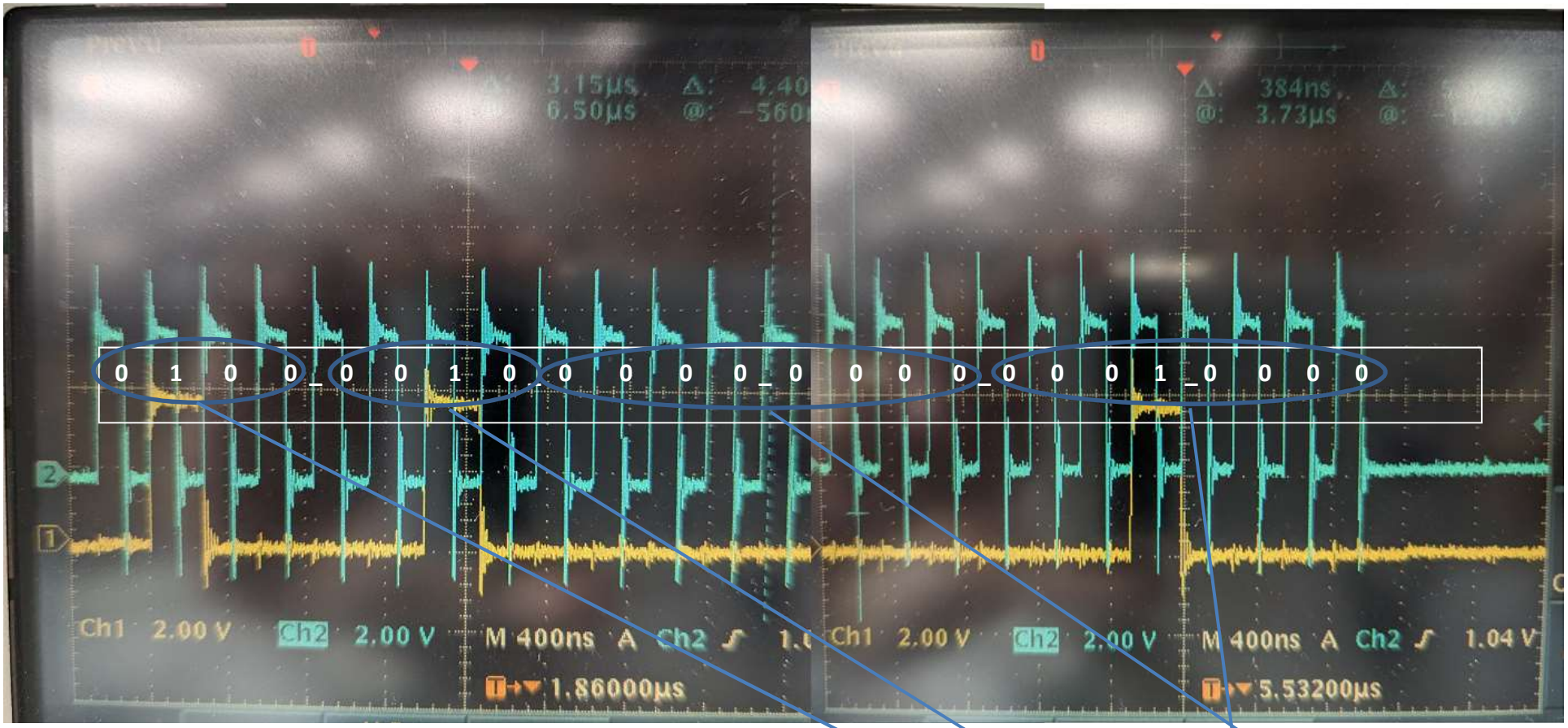
**SPI Communication –**

**Write Register WREG for Internal Test Signal**

**Ch2 is SCLK; Ch1 is DIN**




| REGISTER READ COMMANDS | | | |
|---|---|---|---|
| RREG | Read *n nnnn* registers starting at address *r rrrr* | 001*r rrrr* (2xh)(2) | 000*n nnnn* (2) |
| WREG | Write *n nnnn* registers starting at address *r rrrr* | 010*r rrrr* (4xh)(2) | 000*n nnnn* (2) |

(1) When in RDATAC mode, the RREG command is ignored.
(2) *n nnnn* = number of registers to be read/written – 1. For example, to read/write three registers, set *n nnnn* = 0 (0010). *r rrrr* = starting register address for read/write opcodes.

### 9.6.1.3 CONFIG2: Configuration Register 2 (address = 02h) (reset = 40h)

Configuration register 2 configures the test signal generation. See the *Input Multiplexer* section for more details.

**Figure 76. CONFIG2: Configuration Register 2**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | WCT_CHOP | INT_TEST | 0 | TEST_AMP | TEST_FREQ[1:0] | |
| R/W-1h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 19. Configuration Register 2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:6 | RESERVED | R/W | 1h | **Reserved**<br>Always write 0h |
| 5 | WCT_CHOP | R/W | 0h | **WCT chopping scheme**<br>This bit determines whether the chopping frequency of WCT amplifiers is variable or fixed.<br>0 = Chopping frequency varies, see Table 7<br>1 = Chopping frequency constant at $f_{MOD}$ / 16 |
| 4 | INT_TEST | R/W | 0h | **TEST source**<br>This bit determines the source for the test signal.<br>0 = Test signals are driven externally<br>1 = Test signals are generated internally |
| 3 | RESERVED | R/W | 0h | **Reserved**<br>Always write 0h |
| 2 | TEST_AMP | R/W | 0h | **Test signal amplitude**<br>These bits determine the calibration signal amplitude.<br>0 = 1 × –(VREFP – VREFN) / 2400 V<br>1 = 2 × –(VREFP – VREFN) / 2400 V |
| 1:0 | TEST_FREQ[1:0] | R/W | 0h | **Test signal frequency**<br>These bits determine the calibration signal frequency.<br>00 = Pulsed at $f_{CLK}$ / $2^{21}$<br>01 = Pulsed at $f_{CLK}$ / $2^{20}$<br>10 = Not used<br>11 = At dc |

Device Registers

| Register | Address | Value | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| ID | 0x00 | 0xD2 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| CONFIG1 | 0x01 | 0x86 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| CONFIG2 | 0x02 | 0x10 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

**START Command OpCode**

**Ch2 is SCLK; Ch1 is DIN**

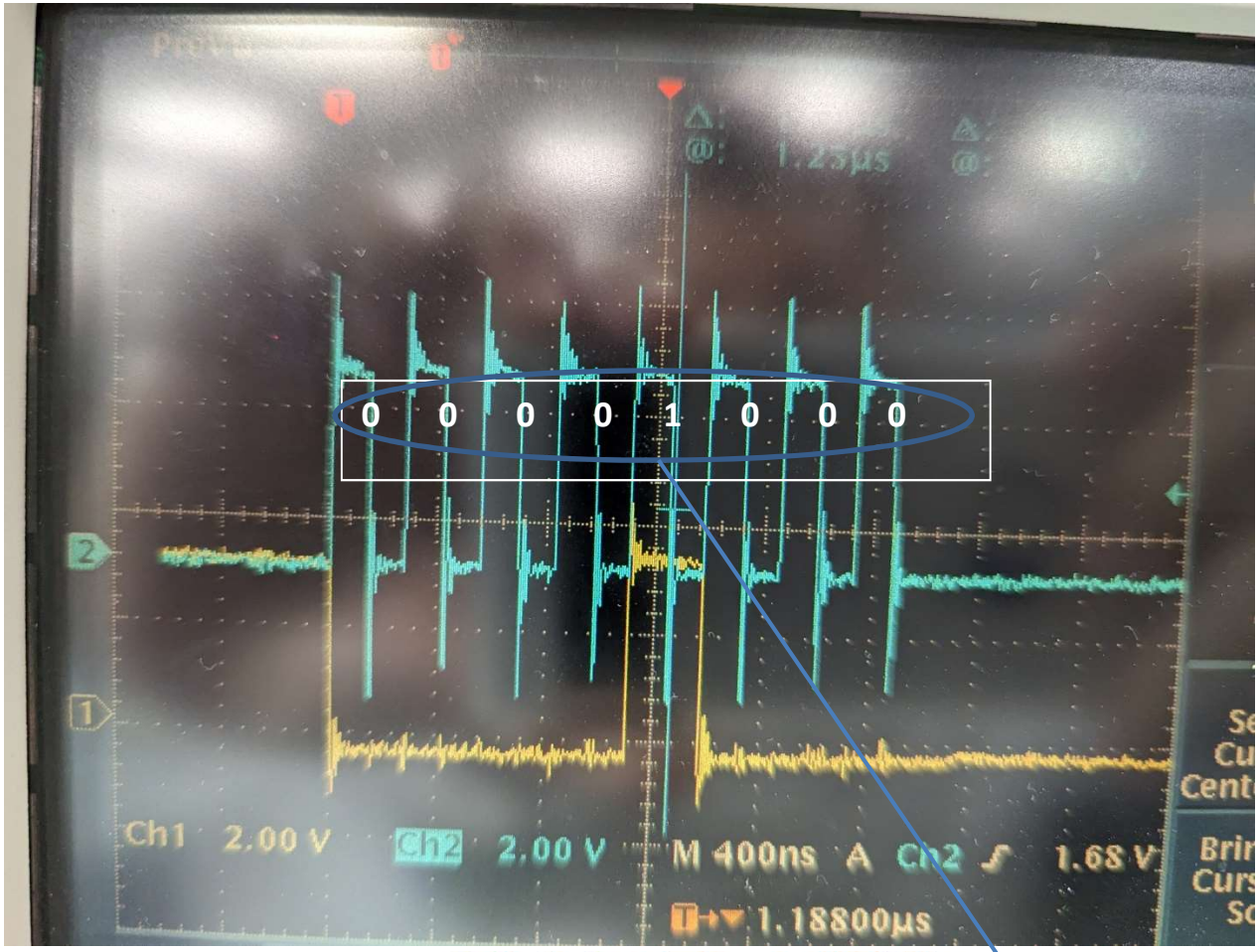



**Table 15. Opcode Command Definitions**

| COMMAND | DESCRIPTION | FIRST BYTE | SECOND BYTE |
|---|---|---|---|
| **SYSTEM COMMANDS** | | | |
| WAKEUP | Wakeup from standby mode | 0000 0010 (02h) | — |
| STANDBY | Enter standby mode | 0000 0100 (04h) | — |
| RESET | Reset the device | 0000 0110 (06h) | — |
| START | Start/restart (synchronize) conversions | 0000 1000 (08h) | — |

**Read Continuous(RDATAC) OpCode**

**Ch2 is SCLK; Ch1 is DIN**

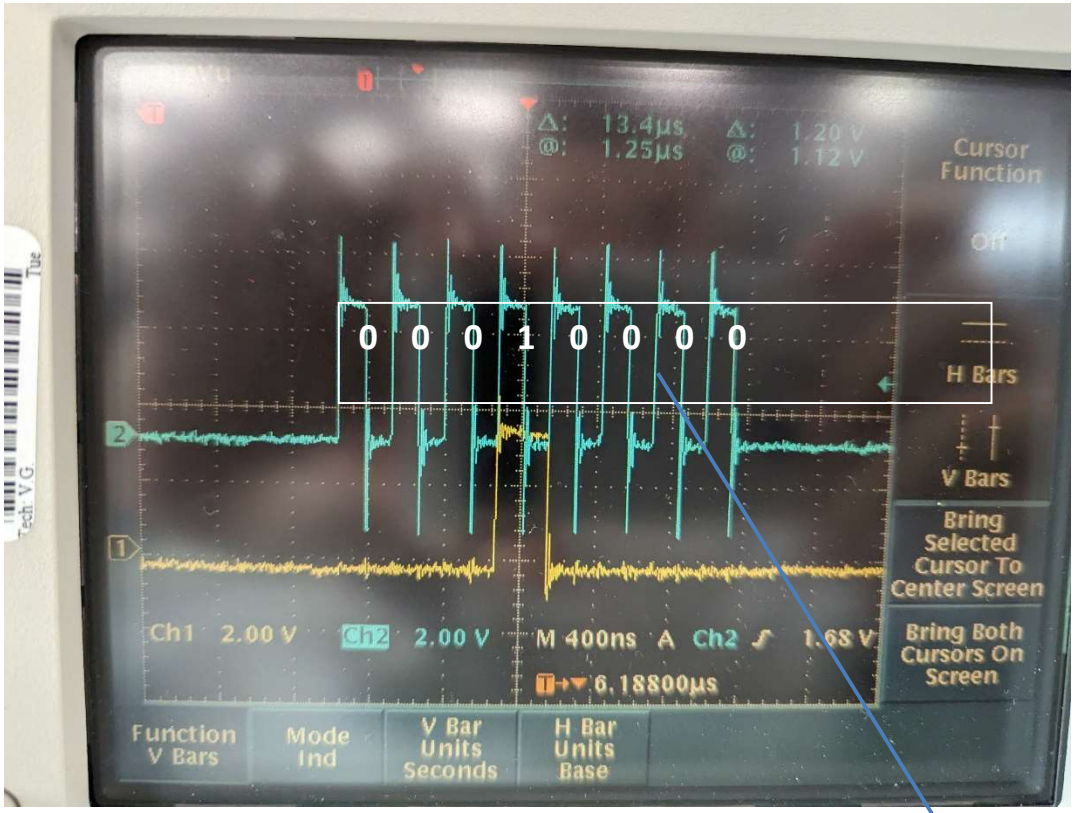



**Table 15. Opcode Command Definitions**

| COMMAND | DESCRIPTION | FIRST BYTE | SECOND BYTE |
|---|---|---|---|
| **SYSTEM COMMANDS** | | | |
| WAKEUP | Wakeup from standby mode | 0000 0010 (02h) | — |
| STANDBY | Enter standby mode | 0000 0100 (04h) | — |
| RESET | Reset the device | 0000 0110 (06h) | — |
| START | Start/restart (synchronize) conversions | 0000 1000 (08h) | — |
| STOP | Stop conversion | 0000 1010 (0Ah) | — |
| **DATA READ COMMANDS** | | | |
| RDATAC | Enable Read Data Continuous mode.<br>This mode is the default mode at power up.(1) | 0001 0000 (10h) | — |
| SDATAC | Stop Read Data Continuously mode | 0001 0001 (11h) | — |