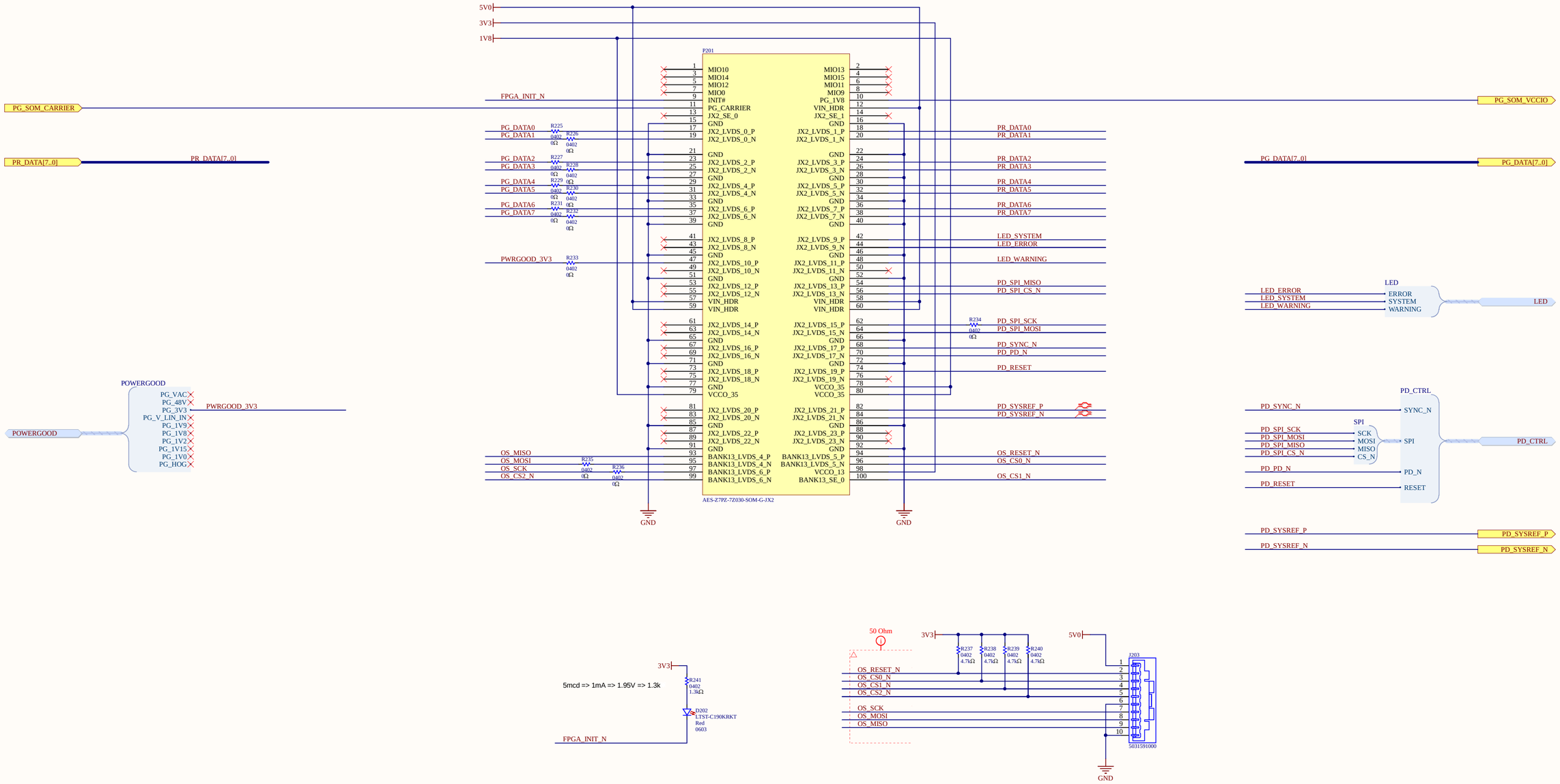
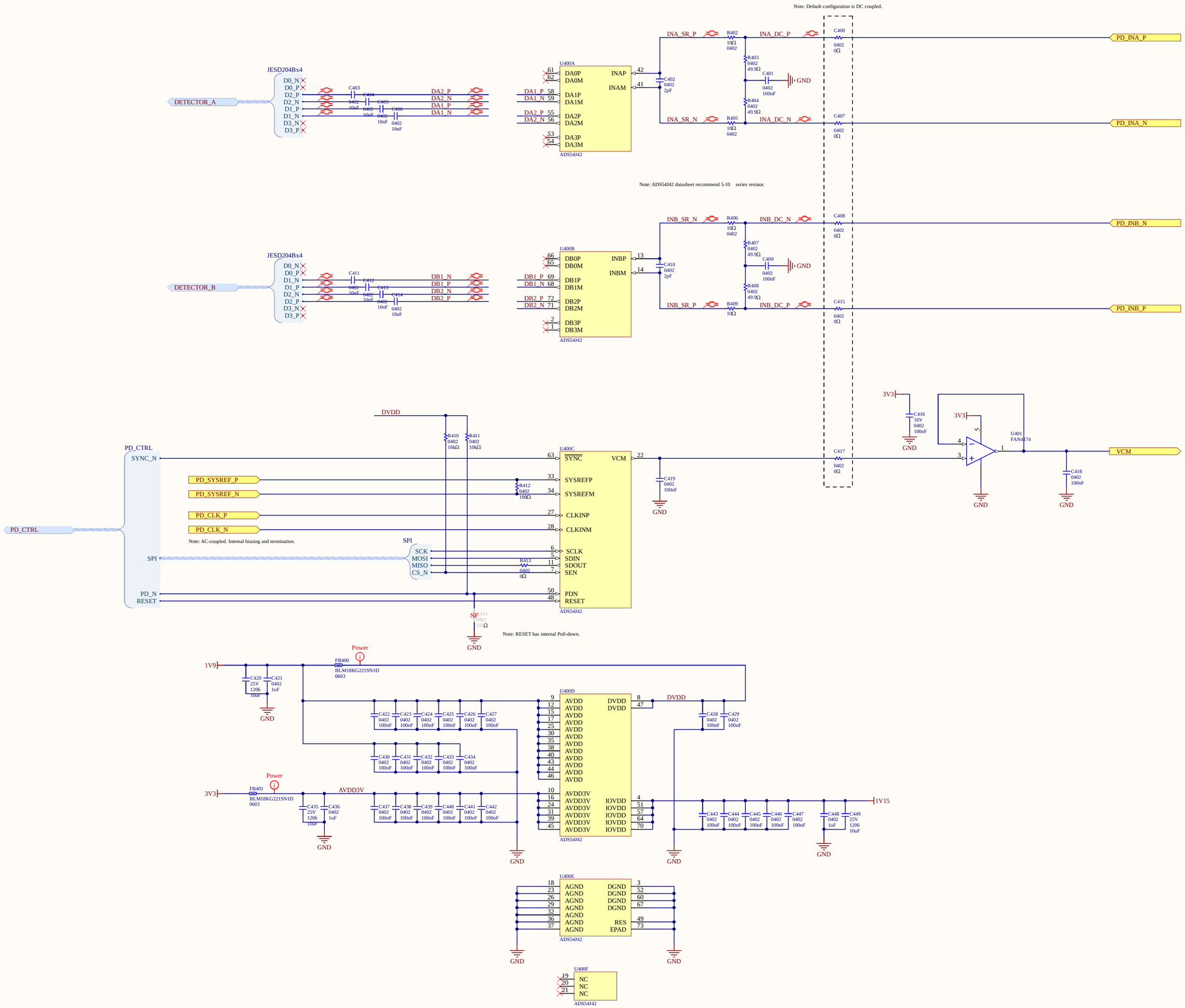
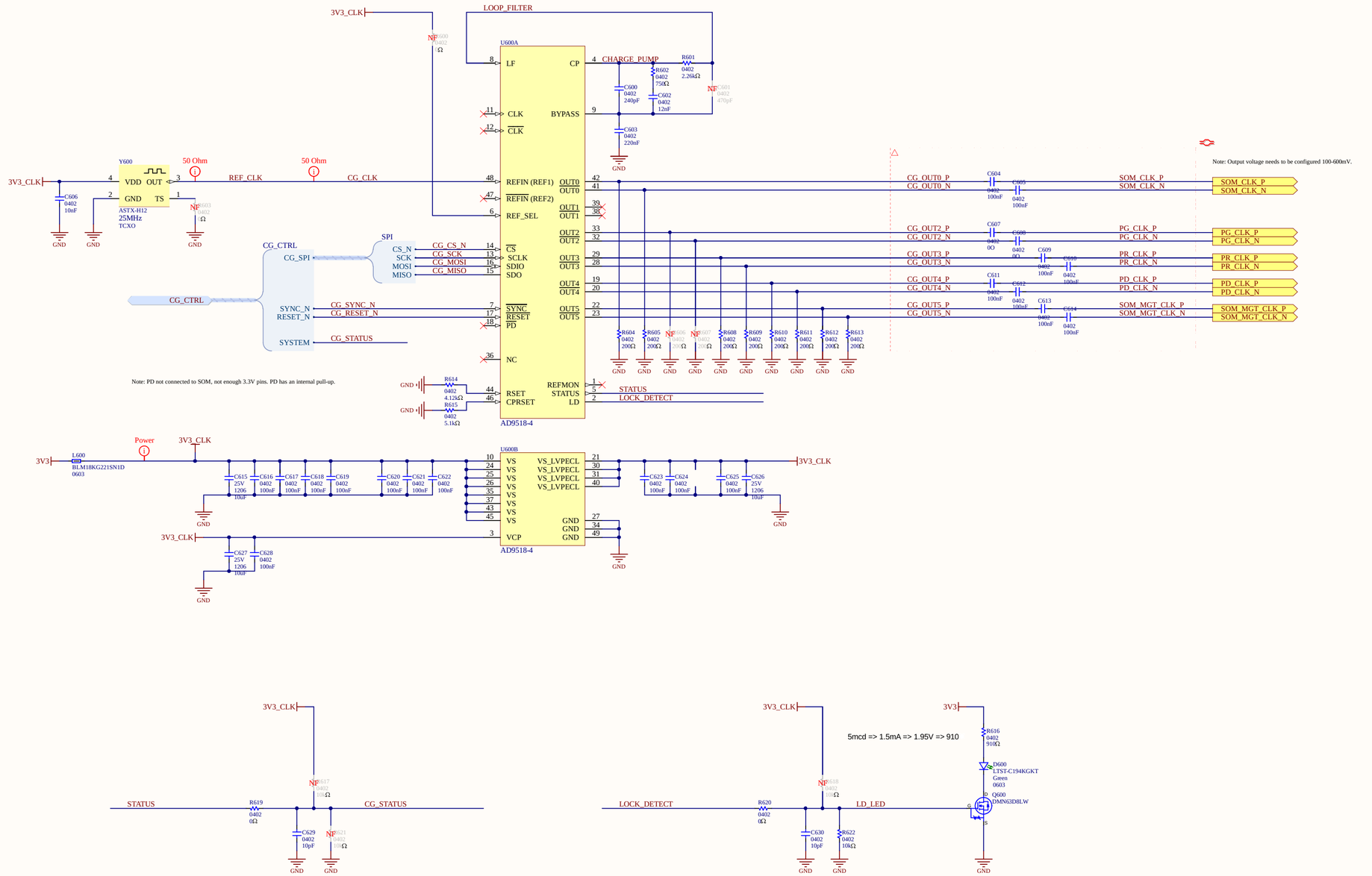

5V0
3V3
1V8
P201
AES-Z7PZ-7Z030-SOM-G-JX2
MIO10
MIO14
MIO12
MIO0
INIT#
PG_CARRIER
JX2_SE_0
GND
JX2_LVDS_0_P
JX2_LVDS_0_N
JX2_LVDS_2_P
JX2_LVDS_2_N
JX2_LVDS_4_P
JX2_LVDS_4_N
JX2_LVDS_6_P
JX2_LVDS_6_N
JX2_LVDS_8_P
JX2_LVDS_8_N
JX2_LVDS_10_P
JX2_LVDS_10_N
JX2_LVDS_12_P
JX2_LVDS_12_N
VIN_HDR
JX2_LVDS_14_P
JX2_LVDS_14_N
JX2_LVDS_16_P
JX2_LVDS_16_N
JX2_LVDS_18_P
JX2_LVDS_18_N
VCCO_35
JX2_LVDS_20_P
JX2_LVDS_20_N
JX2_LVDS_22_P
JX2_LVDS_22_N
BANK13_LVDS_4_P
BANK13_LVDS_4_N
BANK13_LVDS_6_P
BANK13_LVDS_6_N
MIO13
MIO15
MIO11
MIO9
PG_1V8
VIN_HDR
JX2_SE_1
JX2_LVDS_1_P
JX2_LVDS_1_N
JX2_LVDS_3_P
JX2_LVDS_3_N
JX2_LVDS_5_P
JX2_LVDS_5_N
JX2_LVDS_7_P
JX2_LVDS_7_N
JX2_LVDS_9_P
JX2_LVDS_9_N
JX2_LVDS_11_P
JX2_LVDS_11_N
JX2_LVDS_13_P
JX2_LVDS_13_N
JX2_LVDS_15_P
JX2_LVDS_15_N
JX2_LVDS_17_P
JX2_LVDS_17_N
JX2_LVDS_19_P
JX2_LVDS_19_N
VCCO_35
JX2_LVDS_21_P
JX2_LVDS_21_N
JX2_LVDS_23_P
JX2_LVDS_23_N
BANK13_LVDS_5_P
BANK13_LVDS_5_N
VCCO_13
BANK13_SE_0
PG_SOM_CARRIER
FPGA_INIT_N
PG_SOM_VCCIO
PR_DATA[7..0]
PG_DATA[7..0]
PG_DATA0
PG_DATA1
PG_DATA2
PG_DATA3
PG_DATA4
PG_DATA5
PG_DATA6
PG_DATA7
R225 0402 0Ω
R226 0402 0Ω
R227 0402 0Ω
R228 0402 0Ω
R229 0402 0Ω
R230 0402 0Ω
R231 0402 0Ω
R232 0402 0Ω
PWRGOOD_3V3
R233 0402 0Ω
R234 0402 0Ω
OS_MISO
OS_MOSI
OS_SCK
OS_CS2_N
R235 0402 0Ω
R236 0402 0Ω
PR_DATA0
PR_DATA1
PR_DATA2
PR_DATA3
PR_DATA4
PR_DATA5
PR_DATA6
PR_DATA7
LED_SYSTEM
LED_ERROR
LED_WARNING
PD_SPI_MISO
PD_SPI_CS_N
PD_SPI_SCK
PD_SPI_MOSI
PD_SYNC_N
PD_PD_N
PD_RESET
PD_SYSREF_P
PD_SYSREF_N
OS_RESET_N
OS_CS0_N
OS_CS1_N
GND
LED
ERROR
SYSTEM
WARNING
POWERGOOD
PG_VAC
PG_48V
PG_3V3
PG_V_LIN_IN
PG_1V9
PG_1V8
PG_1V2
PG_1V15
PG_1V0
PG_HOG
PD_CTRL
SYNC_N
SPI
SCK
MOSI
MISO
CS_N
PD_N
RESET

50 Ohm
3V3
5V0
R237 0402 4.7kΩ
R238 0402 4.7kΩ
R239 0402 4.7kΩ
R240 0402 4.7kΩ
OS_RESET_N
OS_CS0_N
OS_CS1_N
OS_CS2_N
OS_SCK
OS_MOSI
OS_MISO
J203
5031591000
GND

3V3
5mcd => 1mA => 1.95V => 1.3k
R241 0402 1.3kΩ
D202
LTST-C190KRKT
Red
0603
FPGA_INIT_N


Note: Default configuration is DC coupled.
Note: ADS54J42 datasheet recommend 5-10 series resistor.
Note: AC-coupled. Internal biasing and termination.
Note: RESET has internal Pull-down.
JESD204Bx4
DETECTOR_A
DETECTOR_B
U400A
U400B
U400C
U400D
U400E
U400F
ADS54J42
INA_SR_P
INA_SR_N
INA_DC_P
INA_DC_N
INB_SR_N
INB_SR_P
INB_DC_N
INB_DC_P
PD_INA_P
PD_INA_N
PD_INB_N
PD_INB_P
DVDD
PD_CTRL
SYNC_N
PD_SYSREF_P
PD_SYSREF_N
PD_CLK_P
PD_CLK_N
SPI
SCK
MOSI
MISO
CS_N
PD_N
RESET
VCM
U401
FAN4174
3V3
1V9
1V15
AVDD3V
Power
GND
NP


3V3_CLK
LOOP_FILTER
U600A
LF
CP
CHARGE_PUMP
R601 0402 2.26kΩ
R602 0402 750Ω
C600 0402 240pF
C602 0402 12nF
C601 0402 470pF
CLK
BYPASS
C603 0402 220nF
GND
Y600
VDD OUT
GND TS
ASTX-H12 25MHz TCXO
50 Ohm
REF_CLK
CG_CLK
C606 0402 10nF
REFIN (REF1)
REFIN (REF2)
REF_SEL
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
CG_OUT0_P
CG_OUT0_N
C604 0402 100nF
C605 0402 100nF
SOM_CLK_P
SOM_CLK_N
Note: Output voltage needs to be configured 100-600mV.
CG_OUT2_P
CG_OUT2_N
C607 0402 0Ω
C608 0402 0Ω
PG_CLK_P
PG_CLK_N
CG_OUT3_P
CG_OUT3_N
C609 0402 100nF
C610 0402 100nF
PR_CLK_P
PR_CLK_N
CG_OUT4_P
CG_OUT4_N
C611 0402 100nF
C612 0402 100nF
PD_CLK_P
PD_CLK_N
CG_OUT5_P
CG_OUT5_N
C613 0402 100nF
C614 0402 100nF
SOM_MGT_CLK_P
SOM_MGT_CLK_N
CG_CTRL
CG_SPI
SPI
CS_N
SCK
MOSI
MISO
CG_CS_N
CG_SCK
CG_MOSI
CG_MISO
CS
SCLK
SDIO
SDO
SYNC_N
RESET_N
CG_SYNC_N
CG_RESET_N
SYNC
RESET
PD
SYSTEM
CG_STATUS
NC
Note: PD not connected to SOM, not enough 3.3V pins. PD has an internal pull-up.
R614 0402 4.12kΩ
R615 0402 5.1kΩ
RSET
CPRSET
REFMON
STATUS
LD
LOCK_DETECT
R604 0402 200Ω
R605 0402 200Ω
R608 0402 200Ω
R609 0402 200Ω
R610 0402 200Ω
R611 0402 200Ω
R612 0402 200Ω
R613 0402 200Ω
AD9518-4
3V3
L600 BLM18KG221SN1D 0603
Power
C615 25V 1206 10uF
C616 0402 100nF
C617 0402 100nF
C618 0402 100nF
C619 0402 100nF
C620 0402 100nF
C621 0402 100nF
C622 0402 100nF
U600B
VS
VS_LVPECL
VCP
GND
C623 0402 100nF
C624 0402 100nF
C625 0402 100nF
C626 25V 1206 10uF
C627 25V 1206 10uF
C628 0402 100nF
STATUS
R619 0402 0Ω
C629 0402 10pF
CG_STATUS
5mcd => 1.5mA => 1.95V => 910
R616 0402 910Ω
D600 LTST-C194KGKT Green 0603
Q600 DMN63D8LW
LOCK_DETECT
R620 0402 0Ω
C630 0402 10pF
R622 0402 10kΩ
LD_LED