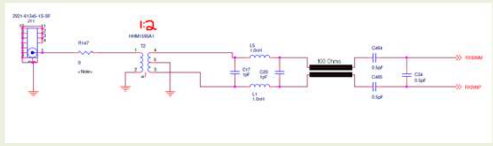
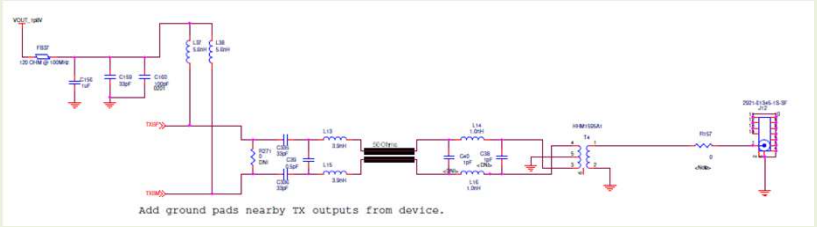
Check list

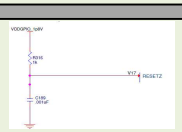
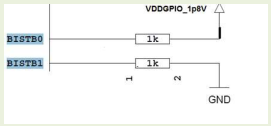
Items on the page are related to the following Device and Configuration Mode

Device-Family	AFE
Device	AFE79xx
Package	FCBGA
Max lane rate	24.33gbps
FDD or TDD	TDD
Configuration	4T4R-1F
Frequency Band (Mhz)	3.5Ghz

RF INPUTS/OUTPUTS

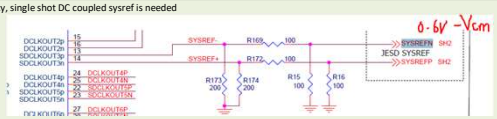
Item	TI Recommendation	Actual Implementation	Status	Comments	Additional Information
Rx/FB INPUT	Rx/FB input differential impedance is 100 ohm 1. Rx/FB Input path needs a 1:2 Transformer 2. Each single ended trace after transformer to be 50ohm and effective differential impedance of 100 ohms		Not Checked	Refer to Marketing EVM schematic	
Rx/FB INPUT	1. Rx/FB input needs differenital π-based LC matching circuit 2. Rx/FB Inputs needs to be AC coupled		Not Checked	Refer to Marketing EVM schematic	
TX OUTPUT	Tx supports both 50ohm output differential impedance. 50 ohm is chosen for wide bandwidth matching. 100 ohm option is available to provide higher output power, but the IMD3 degrades by 3db for 100 ohm option. 1. For 50 ohm differential impedance, 1:1 balun is needed 2. Each single ended trace after transformer to be 25ohm and effective differential impedance of 50 ohms		Not Checked	Refer to Marketing EVM schematic	
TX OUTPUT	1. TX output needs differenital π-based LC matching circuit 2. Tx outputs need DC bias Feed from VOUT_1p8V		Not Checked	Refer to Marketing EVM schematic	

GPIOS

Item	TI Recommendation	Actual Implementation	Status	Comments	Additional Information
RESETZ	RESETZ is active low signal. Add a pull-up resistance of 10k to VDD1P8VGPIO		Not Checked		
SEN	SEN is active low signal. Add a pull-up resistance of 10k to VDD1P8VGPIO 1. Do this for SPIASEN 2. For SPIB1SEN and SPIB2SEN, if used		Not Checked		
BIST-B0 and BIST-B1	Bist-B0-> needs logic high, pull-up to 1.8V Bist-B1-> Needs logic low, pull down to ground		Not Checked		
SYNCIN LVDS	If LVDS is used, device has 100 ohm differential termination across sync-in pins, so no external termination used. Programming the pins for LVDS mode available by SPI		Not Checked		

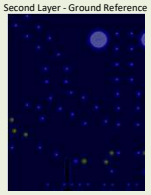
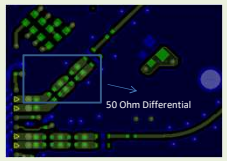
SYNCOUT LVDS	For syncout, lvds 100 ohm differential termination at ASIC/FPGA is needed		Not Checked		

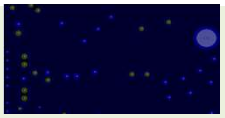
CLOCK,SYSREF,SERDES

Item	TI Recommendation	Actual Implementation	Status	Comments	Additional Information
Serdes Inputs/outputs	All serdes inputs and outputs needs to be AC coupled. Serdes Routing is 100 ohm differential		Not Checked	Refer to Marketing EVM schematic	1. Typical serdes common mode is 450mV 2. Device offers programmability to invert the serdes lanes for ease of routing on board 3. If the number of lanes required is <=6, DO NOT USE STX1 and STX8, this is to avoid noise coupling from these lanes to RF INPUTS 2RXIN+/- and 3RXIN+/-
REFCLK	REFclock needs to AC coupled REFclock has inbuilt 100 ohm differential termination and does not require external termination		Not Checked		Refclock has internal common mode set to 0.6V
SYSREF	Sysref common mode needs to be set externally to 0.6V. Sysref has internal termination of 100 ohms Typical differential swing needed is 750mVpp		Not Checked		1. For deterministic latency, single shot DC coupled sysref is needed 
PLL_LDOOUT	In testchip & Pg1.0, Add 100nF to the PLL_LDOOUT pin The component needs to be placed close to the device		Not Checked		

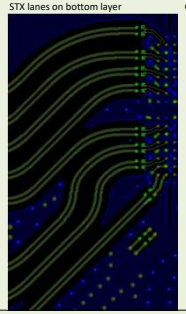
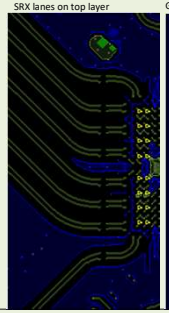
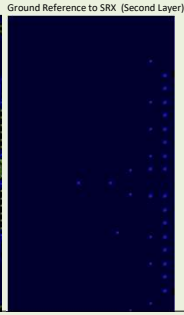
LAYOUT CONSIDERATIONS

RF INPUTS/OUTPUTS

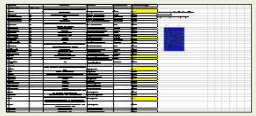
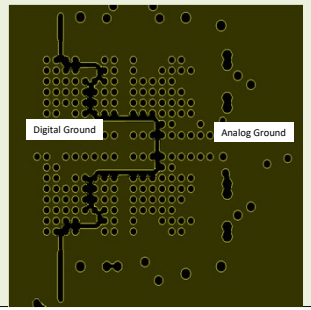
Item	TI Recommendation	Actual Implementation	Status	Comments	Additional Information
RX/FB INPUT LAYOUT	1. Each single ended trace after transformer to be routed 50ohm and differential trace before transformer to be routed with a differential impedance of 100 ohms. 2. Avoid sharp bends in the RF path to minimize impedance discontinuities. 3. Pour the adjacent layer with ground plane to provide a good reference to RF path. 4. For better isolation between the transformers adjacent channels can be placed on opposite layers.		Not Checked	Refer to Marketing EVM layout	Top Layer - RF input path  Second Layer - Ground Reference 
TX OUTPUT LAYOUT	Based on the choice made during schematic phase follow the appropraiate recommendations. **Case 1 : TX - Differential 50 ohm** Differential trace before transformer needs to be routed with differential 50 ohm impedance. (See additional information - traces are wider compared to 100 ohm differential routing in case of RX/FB) After the 1:1 transformer, routing needs to be 50 ohm single ended. **Case 2 : TX - Differential 100 ohm** Differential trace before transformer needs to be routed with differential 100 ohm impedance. After the 1:2 transformer, routing needs to be 50 ohm single ended.		Not Checked	Refer to Marketing EVM layout	Top Layer - RF output path  Second Layer - Ground Reference  Bottom Layer - DC Biasing 

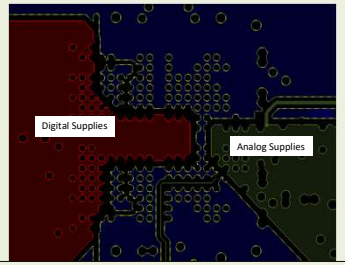
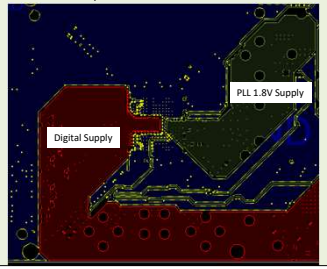
TX OUTPUT LAYOUT	1. The DC bias circuitry can be placed on the opposite layer to RF output path. 2. Avoid sharp bends in the RF path to minimize impedance discontinuities. 3. Pour the adjacent layer with ground plane to provide a good reference to RF path. 4. Similar to concern of isolation between transformers in RX/FB, adjacent TX output channels can be placed on opposite layers.		Not Checked	Refer to Marketing EVM layout	

CLOCK, SERDES

Item	TI Recommendation	Actual Implementation	Status	Comments	Additional Information
SERDES INPUT/OUTPUT LAYOUT	1. Serdes lanes to be routed with 100 ohm differential impedance. 2. Pour the adjacent layer with ground plane to provide a good reference to RF path. 3. Stubs to be avoided to minimize the routing loss. This can be done by the following. The serdes lanes can be routed only on either top or bottom layers. (or) In case lanes need to routed in one of the middle layers, blind vias or back drilling can be implemented. Maximum loss tolerated on each lanes is 15dB across temperature.		Not Checked		STX lanes on bottom layer  Ground Reference to STX (Last but one Layer)  SRX lanes on top layer  Ground Reference to SRX (Second Layer) 
REFCLK LAYOUT	1. Ref Clock needs to be routed as a 100 ohm differential trace. 2. It is to be ensured that all along the routing, care must be taken to avoid any potential coupling such as - switching supplies, RF paths. Clock path needs to be properly shielded by ground planes on the routing layer as well as adjacent layers.		Not Checked		

Supply and Ground

Item	TI Recommendation	Actual Implementation	Status	Comments	Additional Information
SUPPLY/ GROUND PAIRS	Each supply needs to be paired with its corresponding ground. Use the excel to identify the supply and ground pairs		Not Checked		Refer to Marketing EVM schematic and ppt below for groups (double click on the document)
DECOUPLING CAPACITORS	One decap of 0.1uF for every two DVDD balls recommended		Not Checked		 
GROUNDS LAYOUT	It is highly recommended to implement ground slotting (shown on the right) to minimize coupling of digital onto RF path. **Note:** 1. The ground slotting has to be implemented on all ground layers. 2. The ground slotting is local to each AFE. In case where multiple AFEs are used, the ground separation is to be done individually for each AFE. The grounds can be shorted just outside the device boundary as shown.		Not Checked		

SUPPLIES LAYOUT	The supplies also should follow the same slotting procedure as grounds. The planes of digital supplies need to be exactly above the digital ground. Similarly analog supplies should follow. Avoid overlap of analog supply or grounds with the digital supply and grounds on adjacent layer Illustration of the above in marketing EVM is shown on the right. Notice that the slot shape is identical in both ground and supplies.		Not Checked		
PLL VCO SUPPLY LAYOUT	Routing of PLL 1.8V supply must be done very carefully to avoid coupling. Any coupling to the supply would translate to multiplicative spurs on sampling clock. For example, switching supplies like digital must be well shielded to PLL 1.8V supply by having ground planes between the digital supply routing and PLL 1.8V routing. As shown on the right, adjacent layers to PLL 1.8V are ground planes. Also,Digital and PLL supply routing are well separated and hround is poured between the two supplies.		Not Checked		PLL 1.8V on 10th Layer  Ground planes on 9th and 11th Layer