**Procedure to edit TX/RX .MIF file**

Note: Please note the server location hsp\_dt002 is moved to \\Xle3090dm44\HSC\_DC\

*Note*: .MIF files contains all values which are to be updated to respective registers in the JESD PHY registers of J57revE (Arria10) Firmware.

Example considered below is for TX but it applies for RX as well

1. Please find the .MIF files present in the HSDC Installed location:

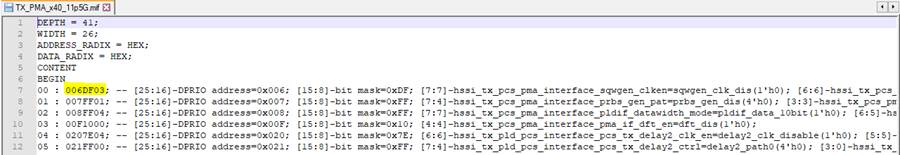
C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J57revE Details\MIF Files\

There will be 4 folders within MIF files: x5, x10, x20 and x40. These indicate reference clock ratios, it can be lanerate/5 (x5), lanerate/10 (x10), lanerate/20 (x20) or lanerate/40 (x40). Depending on the clock frequency sent from device EVM to FPGA, the MIF files of corresponding folder needs to be used

1. Select the .MIF file which is **close or equal** **to** your targeted lane rate.

*For Example:* If you targeted lane rate is 11.7 G ( for which .MIF file is not present) then you can select the nearest 11.5G MIF file (named as, **TX\_PMA\_x40\_11p5G.mif**).

1. The .MIF file will appear as below,



Open .MIF file and Edit it for required voltage swing value you require.

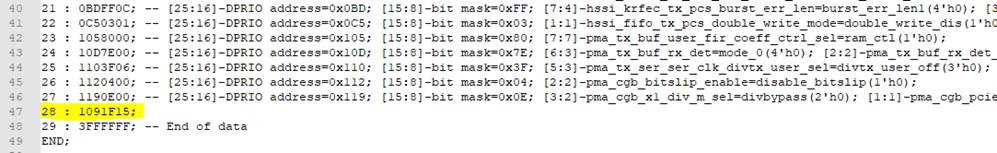
1. *For example*, to set a TX output voltage swing register value as **21**, we need to write the equivalent HEX value **0x15** to register **0x109[4:0]** bits.

For this to take effect, In the MIF file we need to add an entry ‘**1091F15**’ at the end of file (edited snapshot shown below).

**1091F15**                -     109 indicates the **register address.**

* 1F indicates the **bit mask value** since we need to write to the **lower 5 bits** ---- [4:0] bits in 0x109.
* 15 is the **value** (in HEX) that we need to write to the register.

In a similar way, form the Address+ Bit Mask + Value string for voltage swing register as required and add it to the .MIF file.



1. Once done, save the .MIF file and proceed with testing for the respective lane rate.

Kindly refer the Intel’s “**Arria10 JESD PHY IP Register Map**” placed parallel to this document to understand the register address, bit mask and values required for changing any other JESD PHY parameters like transceiver AC or DC gains and for other adaptive Equalization settings