Synchronizing Multiple GSPS ADCs in a System

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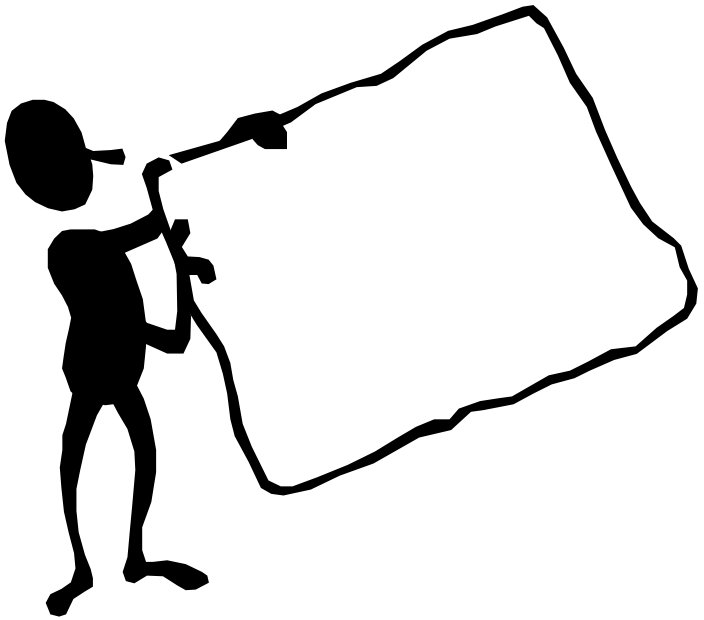
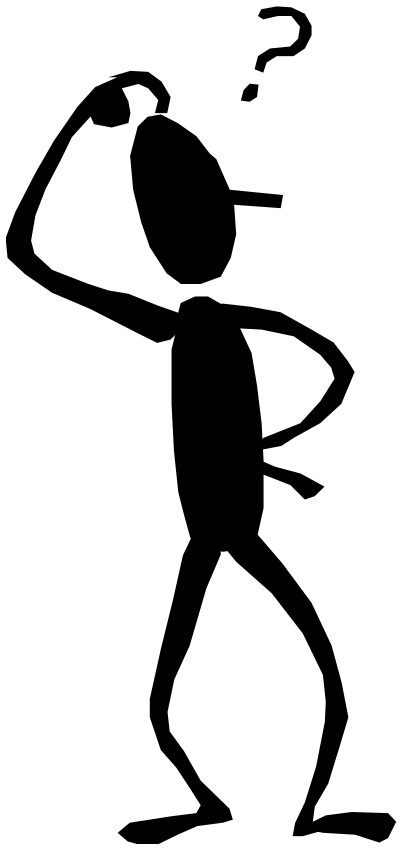
Outline



- Overview of the issue
- Synchronizing data outputs
- Synchronizing analog sample instant
- Summary and recommendations

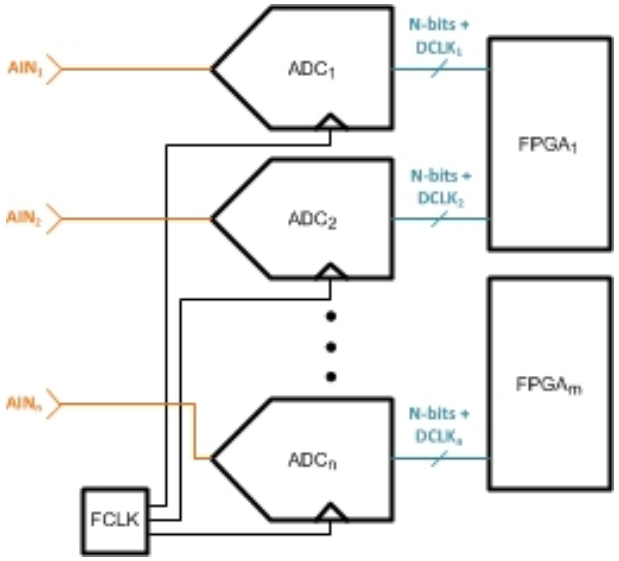
AN OVERVIEW OF THE ISSUE

Problem statement



How can multiple GSPS ADCs in one system be synchronized?

What exactly are we synchronizing?



What?	Why?	How?
Data Clocks and Data	Ease of data capture at FPGA	AutoSync feature
Analog sample instant	If application requires < 1 sample instant difference between ADCs	TimeStamp feature*

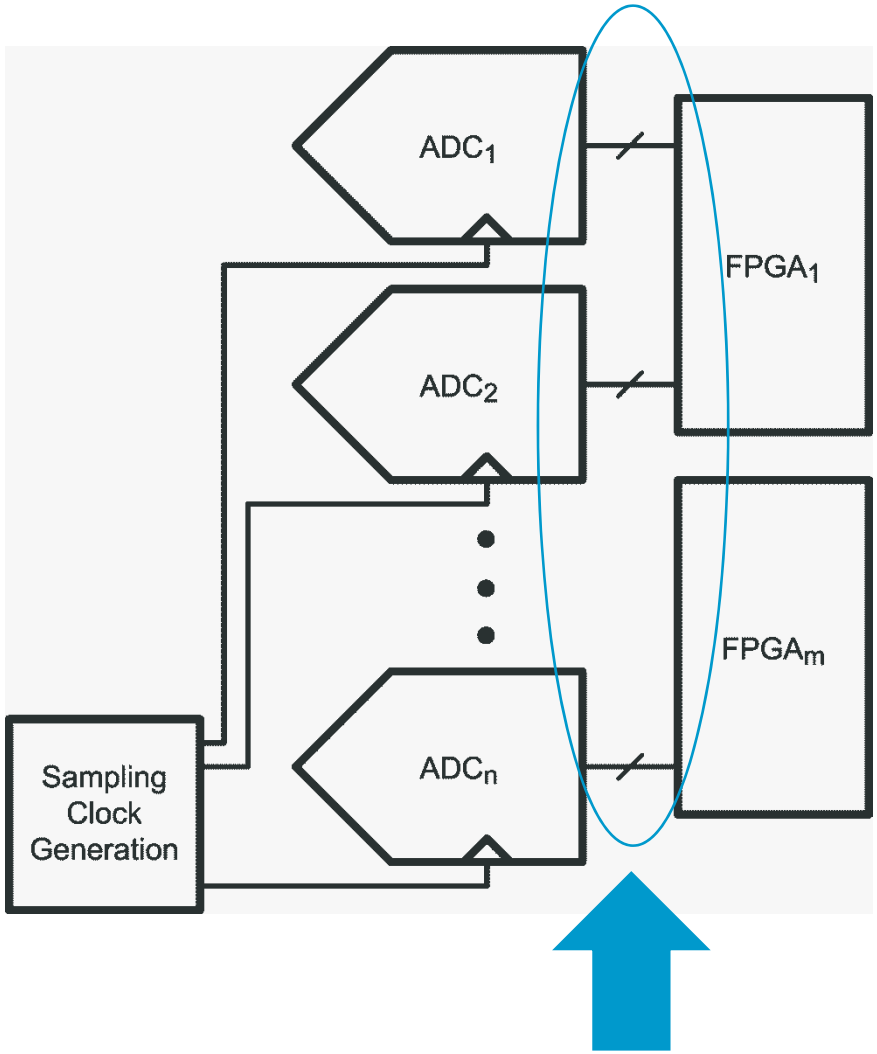
*TimeStamp alone is not sufficient to characterize all applications

Products covered

- Which products does the presentation pertain to?
  - ADC12D1800/1600/1000/800/500RF
  - ADC12D1800/1600/1000
  - ADC10D1500/1000 (no TimeStamp)

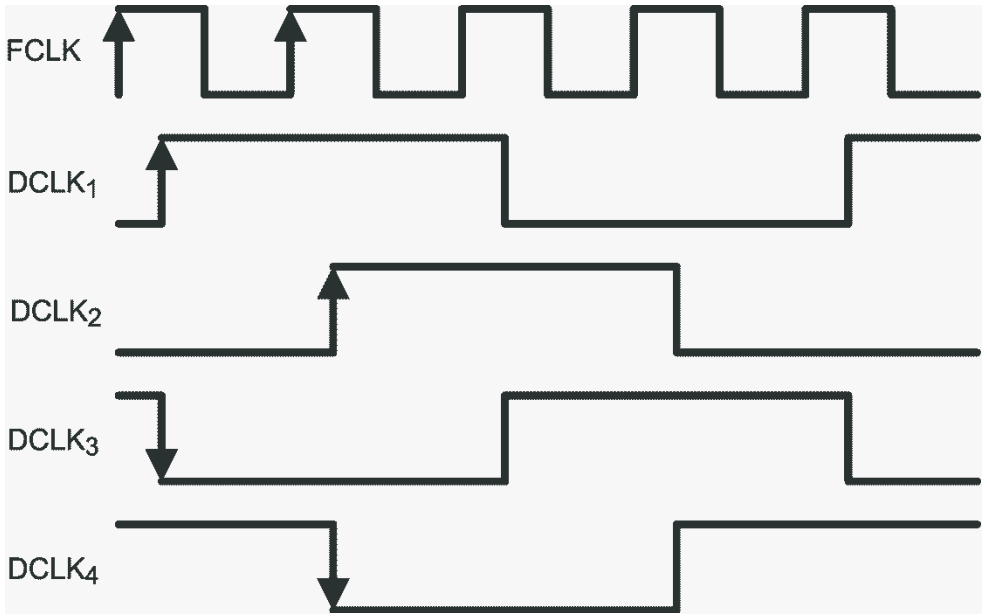
SYNCHRONIZING DATA OUTPUTS

The Goal: Synchronizing Multiple ADCs



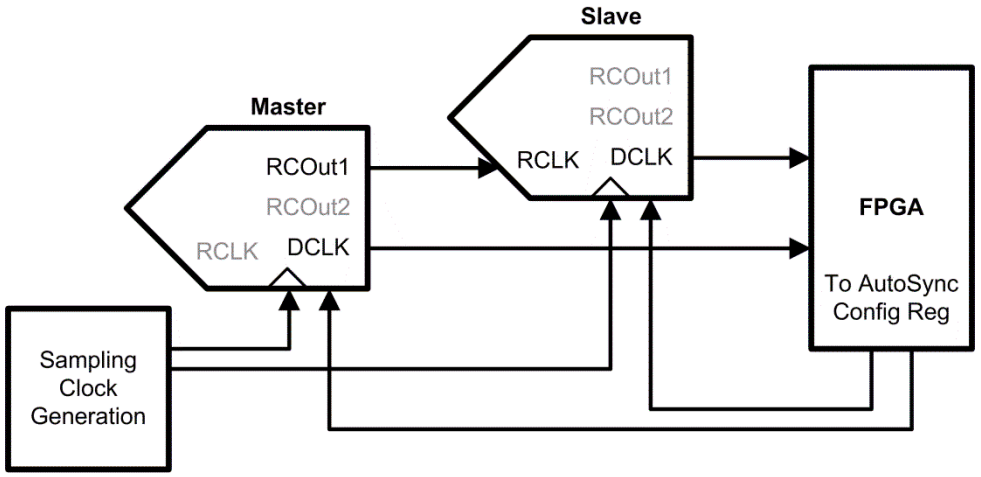
- Data Clocks (DCLK) and Data from multiple ADCs should be synchronized to simplify data capture at one FPGA.

The Problem: Unsynchronized DCLKs



- DCLK can be ÷2 or ÷4 sub-harmonic of FCLK
- ÷4 sub-harmonic possibilities for Demux Mode are shown
- Actual DCLK sub-harmonic can change from power-on to power-on

The Solution: the AutoSync feature



- One ADC provides the Master DCLK phase
- Reference Clock controls the Slave DCLK phase
- DCLK phases are compared at the FPGA
- Control signals complete the loop

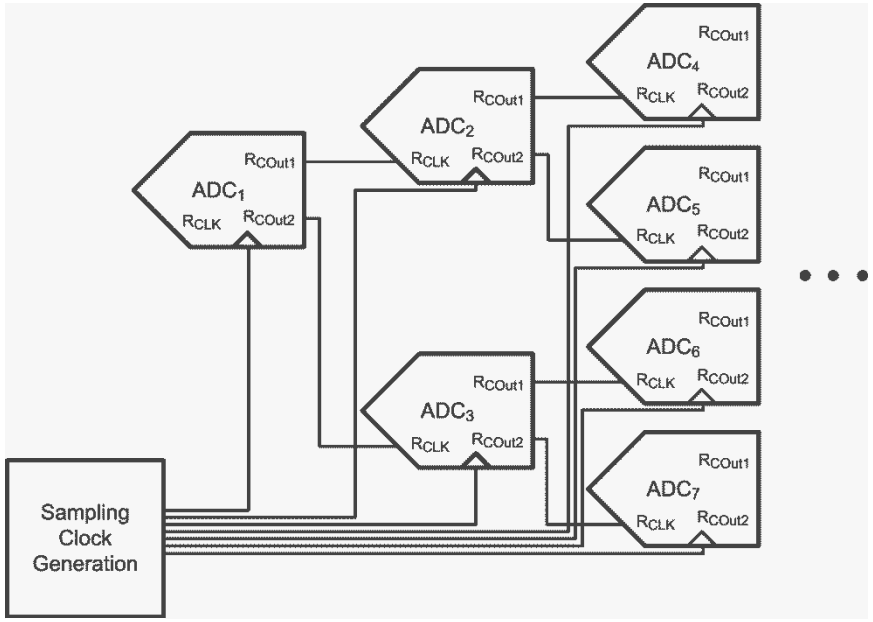
Advantages of AutoSync

- System can automatically recover from a spontaneous loss of synchronization because it is continuously active
- No precise setup / hold times required for RCLK
- System configuration is flexible, i.e. binary tree, daisy chain, independently sourced
- Once configured, control registers are valid for all production units

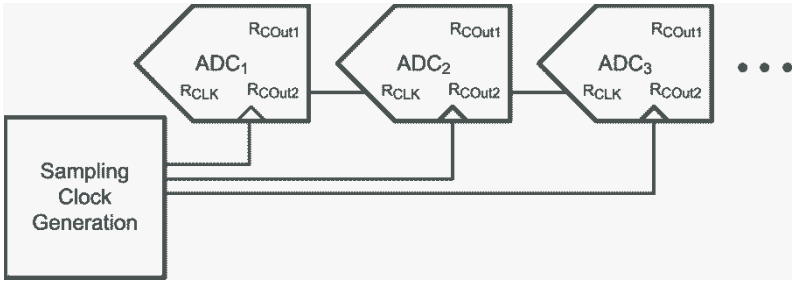
Limitations of AutoSync

- Cannot guarantee analog input synchronization
- PVT variation limits feature to use for FCLK < 1.8GHz, recommendation to independently source RCLK for FCLK > 1GHz
- Cannot account for phase error in sampling clocks arriving at multiple ADCs
- In case multiple ADCs are located on different boards, feature may be difficult to verify

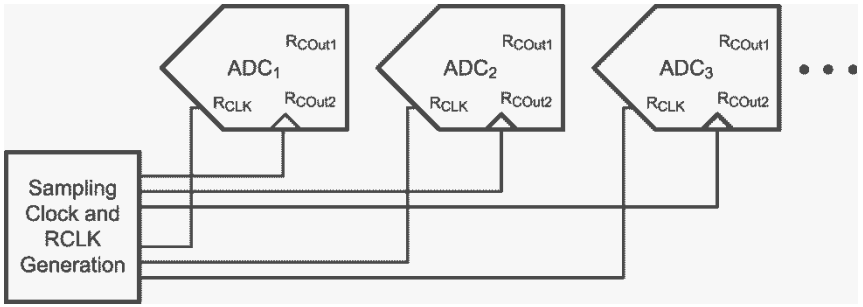
Possible System Configurations



Binary Tree



Daisy Chain

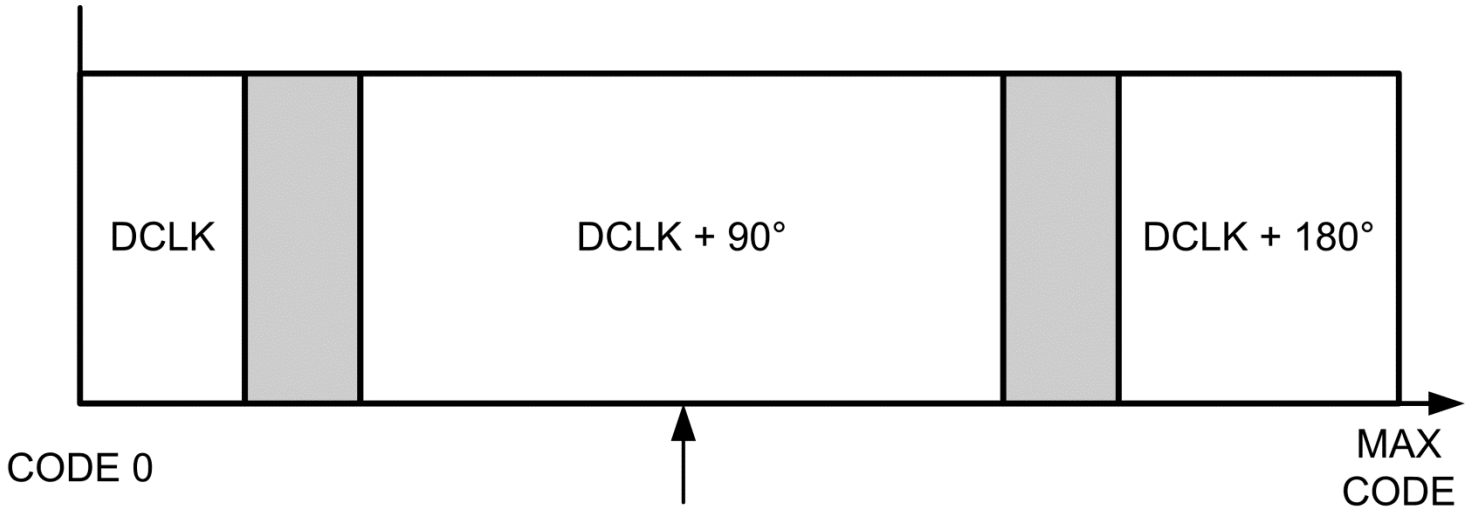


Driving RCLK Externally

Texas Instruments

Configuring AutoSync (1 of 2)

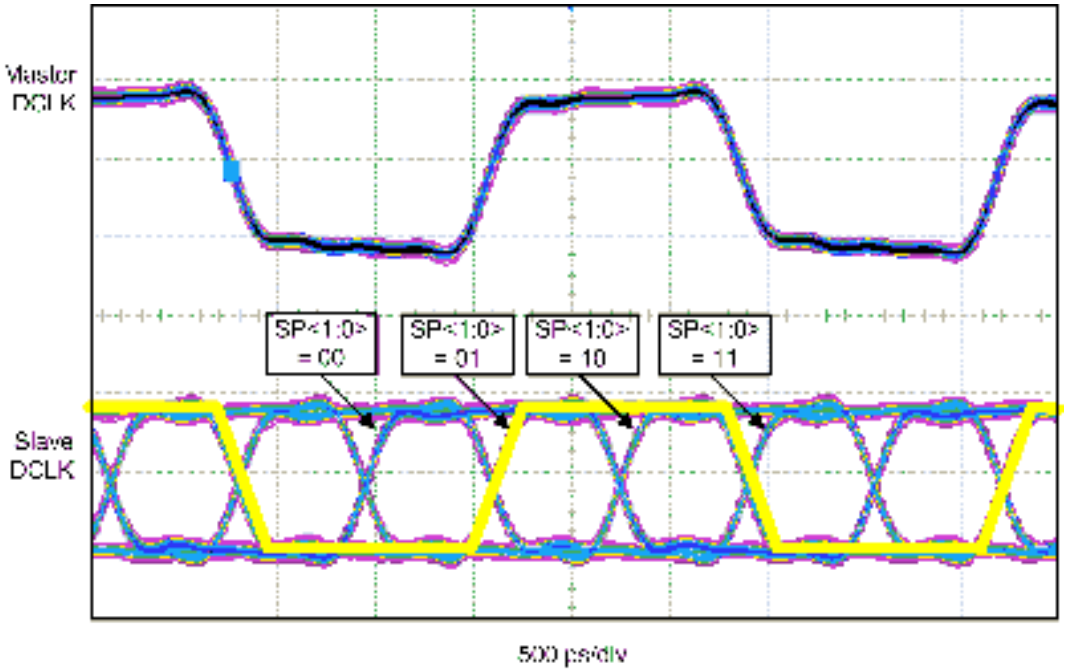
1. Select Master / Slave Mode
2. Enable the Reference Clocks, as necessary
3. Adjust Slave ADC RCLK for clean capture



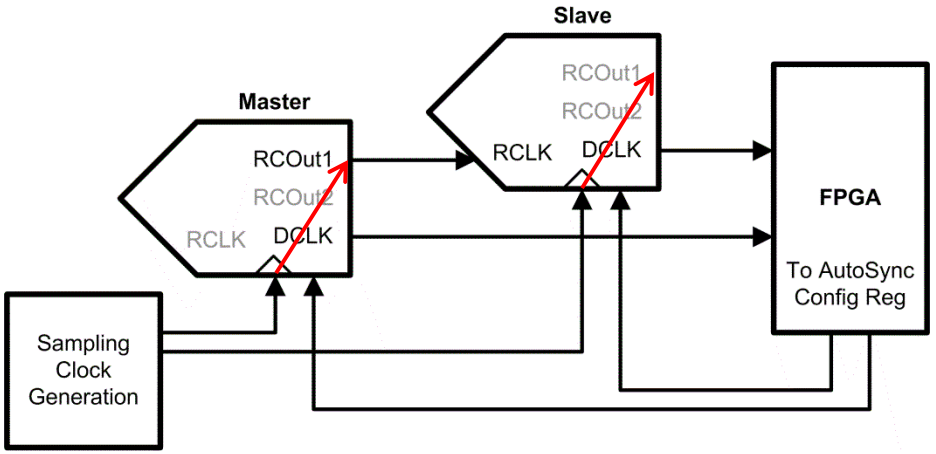
DRC Code vs. DCLK Behavior

Configuring AutoSync (2 of 2)

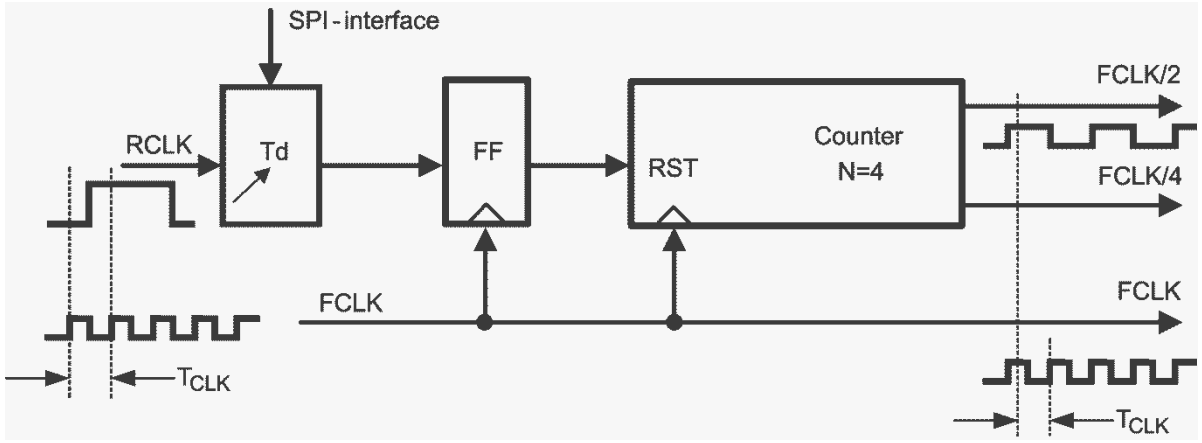
4. Select correct DCLK phase for each Slave ADC



PVT System Variation



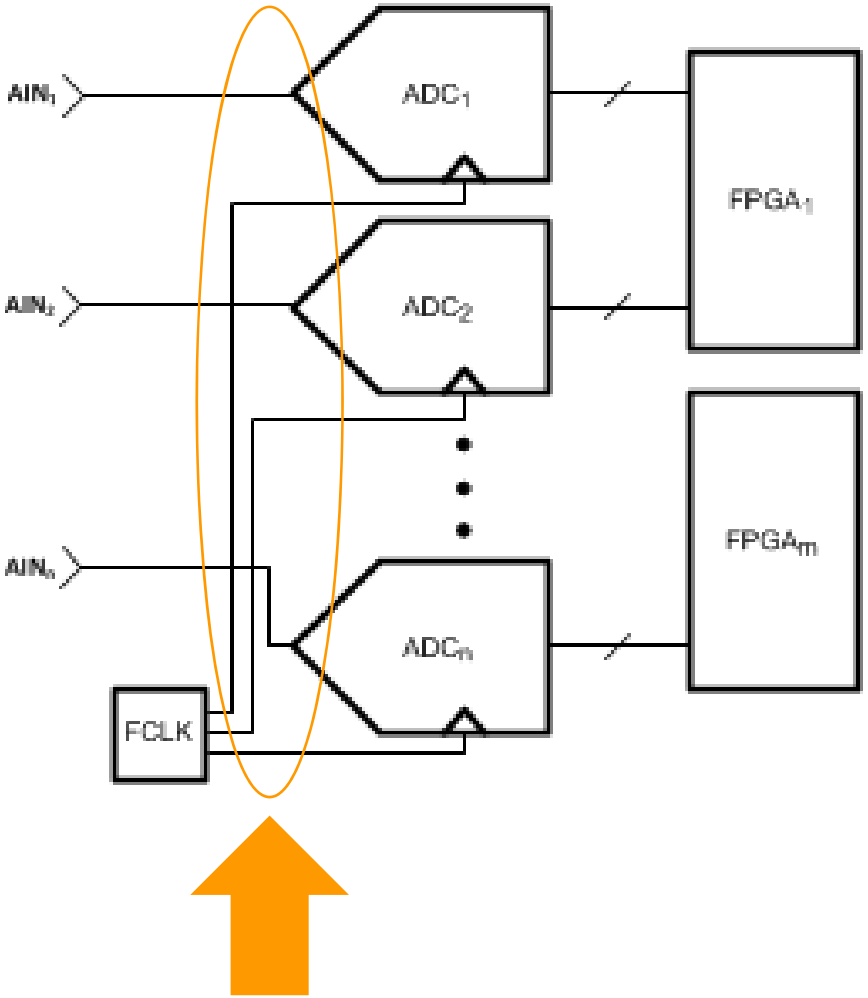
- $dt(PVT)_{MASTER}$ = ±170ps
- $dt(PVT)_{SLAVE}$ = ±100ps
- Maximum PVT for any system = ±270ps



Clock generation in Slave ADC

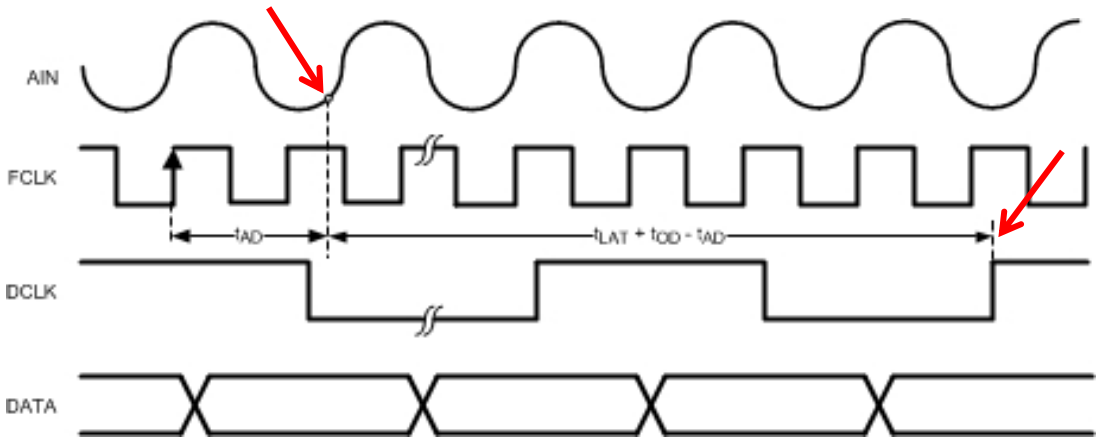
SYNCHRONIZING ANALOG SAMPLE INSTANT

The Goal: Synchronizing Multiple ADCs



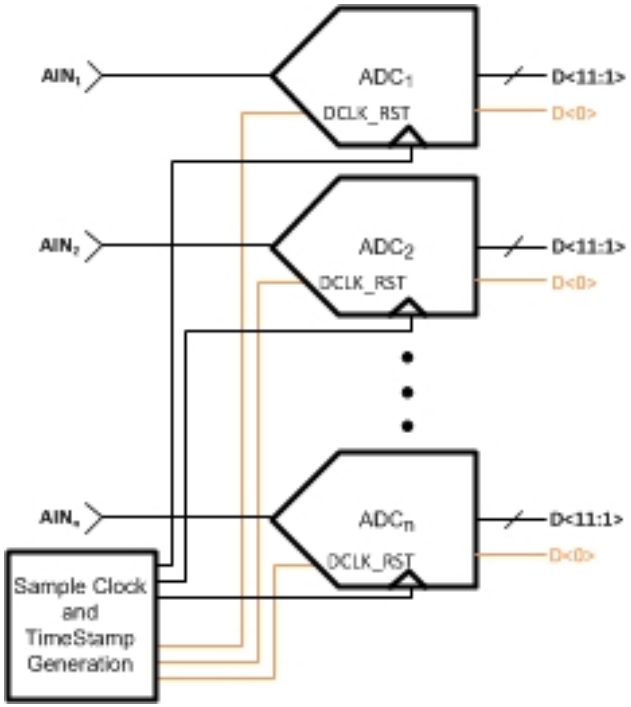
- Digital output samples from multiple ADCs should be from the same sample instant (if the application requires)

The Problem: Variation in Latency



- Total ADC latency is $t_{LAT} + t_{OD} - t_{AD}$
- t_{AD} and t_{OD} are a function of process, voltage, and temperature (PVT)
- Δt_{LAT_ADC} can be greater than one sample period

A Solution: the TimeStamp feature



- The LSB of each 12-bit ADC is used for the TimeStamp signal
- Latency of the analog input and TimeStamp is identical
- When applied synchronously to the sample clock, a pulse with a fast edge reveals the Δt_{LAT_ADC}
- Any necessary adjustments can be made in the FPGA

Advantages of TimeStamp

- Allows for empirical calculation of total ADC latency to within one sample instant
- Once characterized in a system, the Δt_{LAT_ADC} will not vary, unless $\Delta T_1 \neq \Delta T_2$
- TimeStamp signals can conveniently be generated from the same clocking IC which generates sample clocks

Limitations of TimeStamp

- Only available on 12-bit GSPS ADCs, not the 10-bit family
- Must be calculated for each system
- Cannot account for phase error in sampling clocks arriving at multiple ADCs
- Cannot account for Δ latency in signal path before ADC
- In case multiple ADCs are located on different boards, feature may be challenging to implement

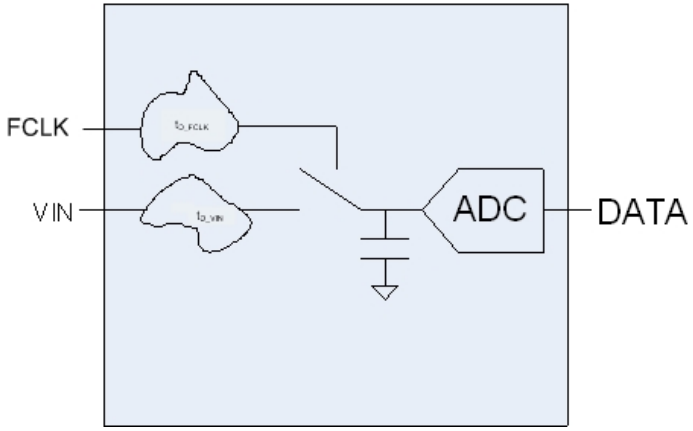
t_{LAT}: Conversion Latency

- Same ADC and same sampling clock frequency implies identical conversion latency between ADCs
- Hence, t_{LAT} does not contribute to Δt_{LAT_ADC}

ADC12D1800RF

t_{LAT}	Latency in 1:2 Demux Non-DES Mode (*Note 9*)	DI, DQ Outputs		34	Sampling Clock Cycles
		DId, DQd Outputs		35	
	Latency in 1:4 Demux DES Mode (*Note 9*)	DI Outputs		34	
		DQ Outputs		34.5	
		DId Outputs		35	
		DQd Outputs		35.5	
	Latency in Non-Demux Non-DES Mode (*Note 9*)	DI Outputs		34	
		DQ Outputs		34	
	Latency in Non-Demux DES Mode (*Note 9*)	DI Outputs		34	
		DQ Outputs		34.5	

t_{OD} & t_{AD}: Sample Clock-to-Data Output Delay and Aperture Delay



Aperture Delay Concept

- t_{OD} is due to trace delays and parasitics, in addition to t_{LAT}
- t_{AD} is difference between arrival of analog input and sample clock at track-and-hold circuit

ADC12D1800RF

t_{AD}	Aperture Delay (*Note 10*)	Sampling CLK+ Rise to Acquisition of Data	1.29		ns
t_{OD}	Sampling Clock-to Data Output Delay (in addition to Latency)	50% of Sampling Clock transition to 50% of Data transition (*Note 10*)	3.2		ns

Maximum Δt_{LAT_ADC}

- Total ADC latency is $t_{LAT} + t_{OD} - t_{AD}$
- t_{LAT} is the same for all ADCs, when run at the same Sampling Clock rate
- Maximum Δt_{LAT_ADC}

$$= (t_{LAT} + t_{OD} - t_{AD})_{MAX} - (t_{LAT} + t_{OD} - t_{AD})_{MIN}$$
$$= (t_{OD} - t_{AD})_{MAX} - (t_{OD} - t_{AD})_{MIN}$$

Parameter	Maximum Variation
Temperature	±8.3%
Supply	±3.6%
Process	±19.2%
Composite PVT	±29.7%

Measuring Δt_{LAT_ADC} is not always required

	Δ < 1	Δ < 2	Δ < 3
ADC10D1x00	{150, 1295} MHz	{1295, 1500} MHz	N/A
ADC12D1x00	{150, 821} MHz	{821, 1642} MHz	{1642, 1800} MHz
ADC12Dx00RF	{150, 800} MHz	N/A	N/A
ADC12D1x00RF	{150, 881} MHz	{881, 1762} MHz	{1762, 1800} MHz

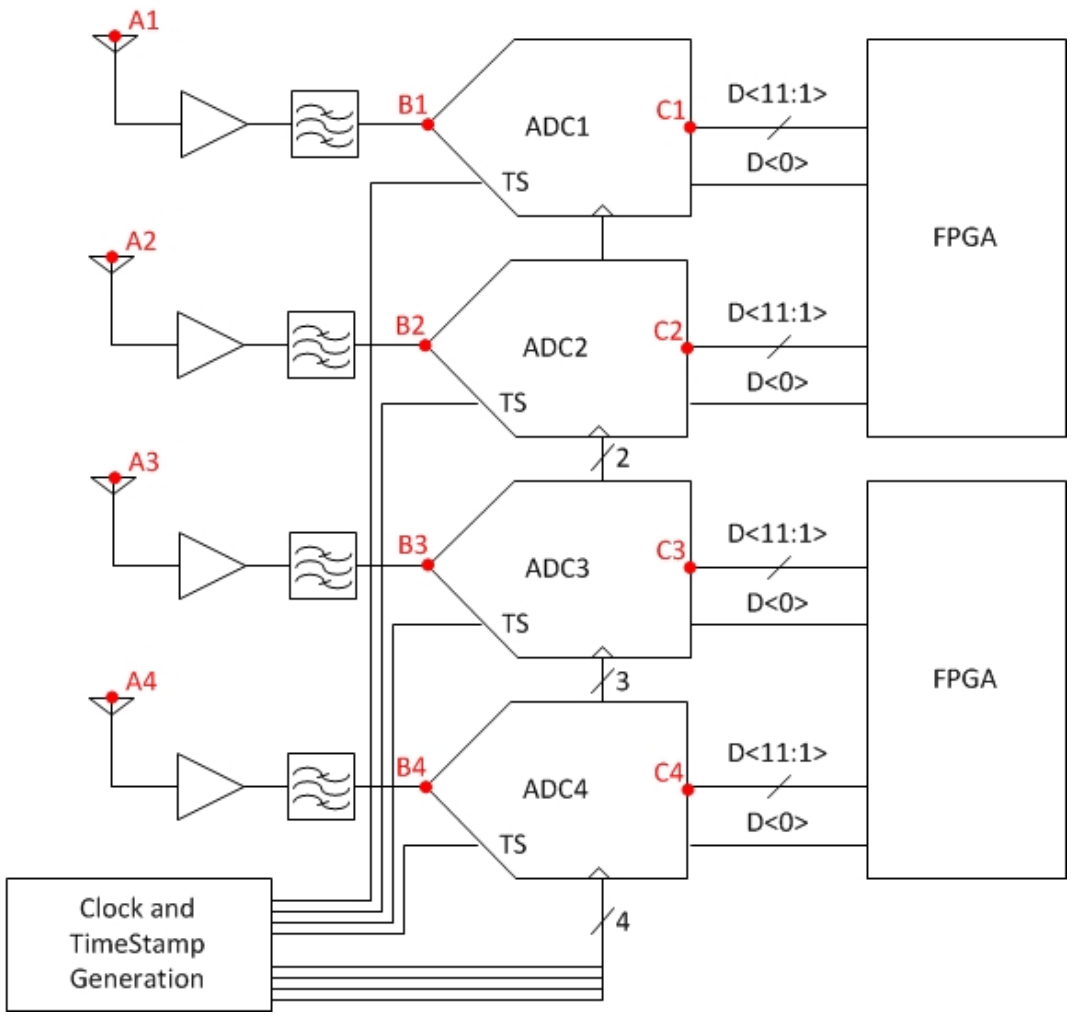
- Δt_{LAT_ADC} < 1 may or may not be required by application
- These numbers represent what may be guaranteed
- If the sampling rate is slow enough, then for some cases Δ < 1

Resolution of TimeStamp

	TS Asynchronous	TS Synchronous to FCLK
Non-DES Mode	1/FCLK	< 1/FCLK
DES Mode	1/(2*FCLK)	< 1/(2*FCLK)

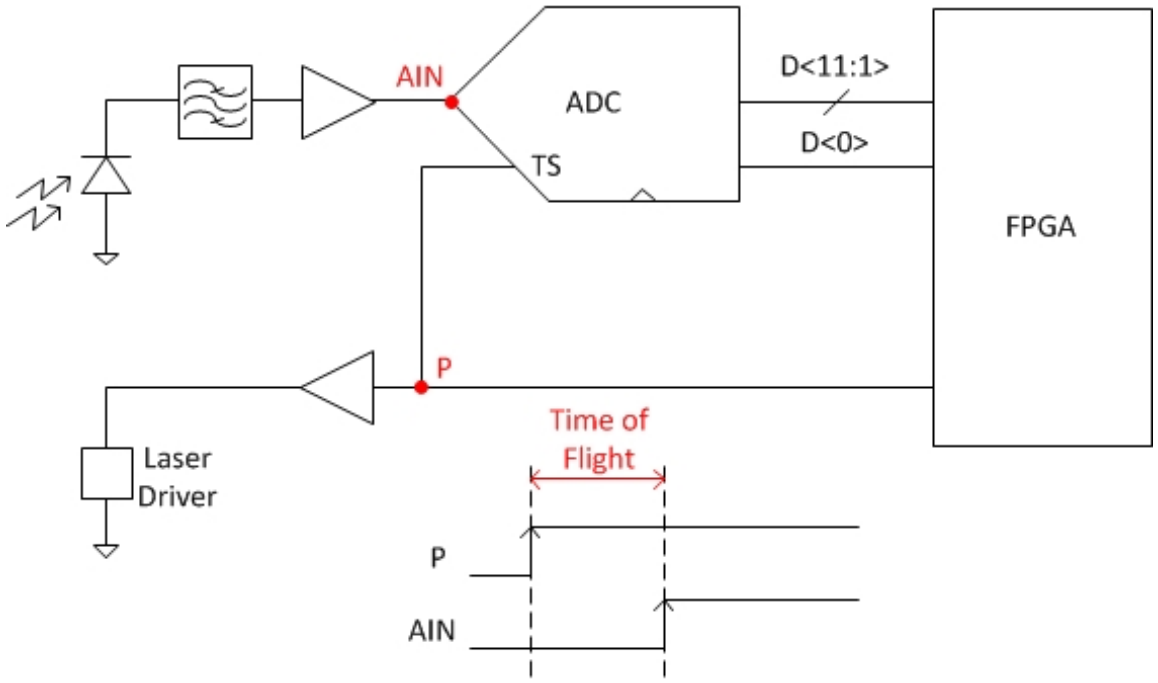
- TimeStamp may be applied synchronously or asynchronously to the FCLK
- To achieve a resolution of less than one sampling period, it must be synchronous to the FCLK
- Convenient way to implement synchronous TimeStamp is to use the LMK048xx, which has multiple, divided outputs

Application Example: Phased Array Radar



- TimeStamp cannot solve all system synchronization issues
- Need to characterize relative latency from A to C
- TimeStamp can only characterize latency from B to C
- Need to use external synchronization signal

Application Example: LIDAR



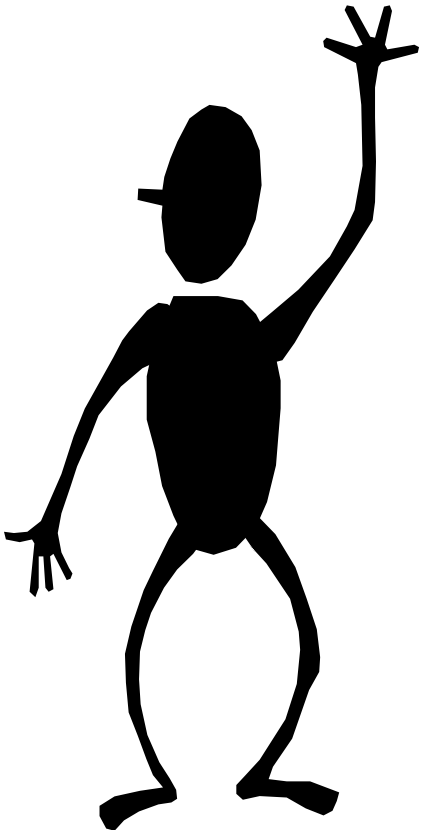
- TimeStamp can be used to precisely measure a trigger signal relative to the analog input
- Because the TS and AIN latency are constant, this allows for accurate characterization of time of flight

SUMMARY AND RECOMMENDATIONS

Summary and Recommendations

- AutoSync feature may be used to synchronize data outputs in multi-GSPS ADC applications
- AutoSync cannot guarantee synchronization of analog sample instant
- To guarantee analog sample instant synchronization, use combination of TimeStamp and system synchronization techniques
- TimeStamp feature can be used to time stamp trigger signal relative to analog input
- For further reading, see Apps Notes:
  - AN2132: *Synchronizing Multiple GSPS ADCs in a System: The AutoSync Feature*
    http://www.ti.com/lit/an/snaa073d/snaa073d.pdf
  - SNAA198: *From Sample Instant to Data Output: Understanding Latency in the GSPS ADC*
    http://www.ti.com/general/docs/lit/getliterature.tsp?literatureNumber=snaa198&fileType=pdf

Questions?



- Thank you for attending!
- Any questions?