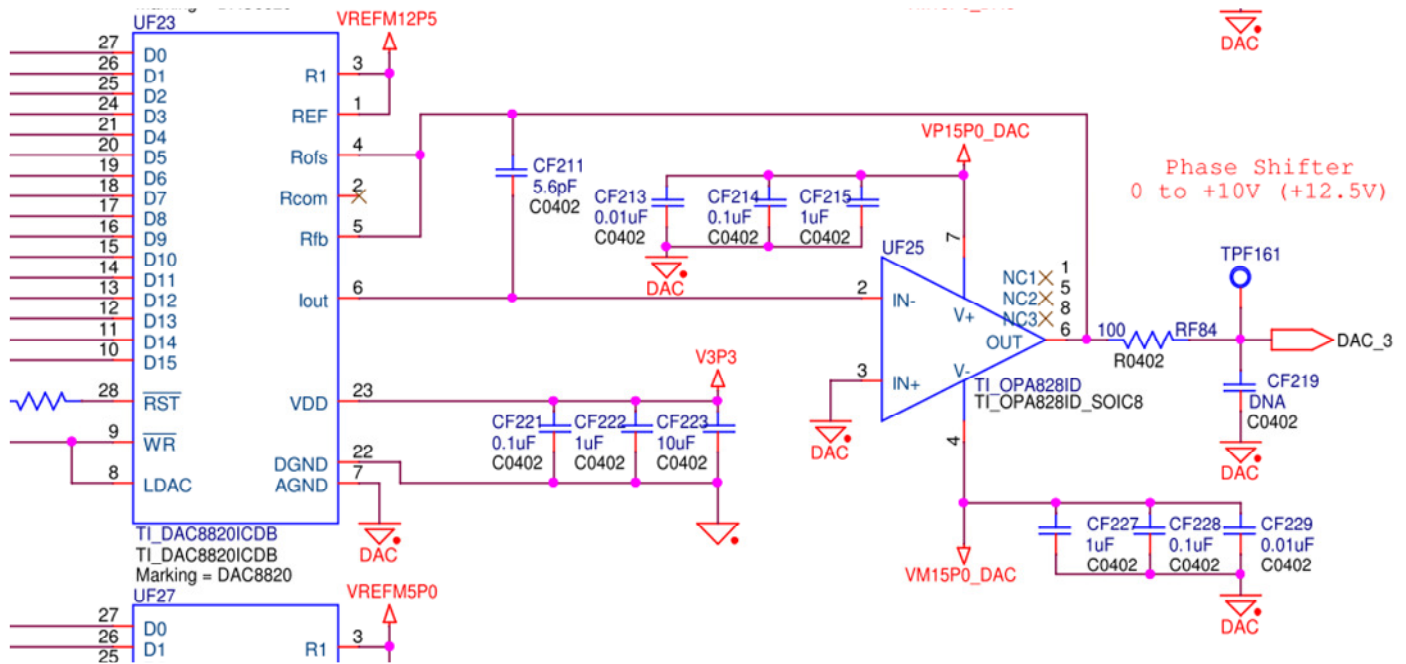# "Long Term" vs. "Short term" settling time or drift based on size of digital code jump – DAC8820 + OPA828

Schematic Basic Information
- Multi-layered PCB w/ground planes, etc.

- VREFM12P5 = -12.50v
  Generated by a string of REF5025 voltage reference ICs followed by a OPA828 inverting op-amp

- VP15P0_DAC = +15.0v, VM15P0_DAC= -15.0v (each generated by a linear regulator)

- For this test circuit, there is no load on the output DAC_3

- There are 8 identical DAC circuits on this PCB (all exhibit exactly the same behavior described below)

- The scope images shown below appear "noisy", this is due to the common 16-bit digital bus which is active
  even when no new data is latched into each of the 8 DACs. That is not the subject of the settling time issue.

- During all the images shown below, all VREF and power supply voltages are perfectly stable
  and do not show any "bumps"

What appears to be the problem
IMAGE #1: When the digital value input to the DAC represents a "large" jump (Decimal 65,536 to 20,000 for the DAC falling edge scenario), the DAC output takes a very long time to settle to its final value (≈2msec or more).

IMAGE #2: When we change the step to a small range (Decimal 30,00 to 20,000), this phenomenon does not exist.

IMAGES #3 & 4: Timescale is changed to 200nsec/div to show the "short term" settling time of the op-amp output to be within the 0.5µsec data sheet spec.

Discussion
- The downwards slope in IMAGE #1 gets less steep with smaller DAC steps, and bigger with bigger steps
  (bigger steps take longer to reach the correct final output voltage value).
- In all cases the correct final voltage value is reached if we wait long enough
- The same behavior occurs on the DAC output rising edge (e.g., a smaller DAC value going to a larger DAC value)
  but the effect is not as strong as for falling edges.
- In our application, we intend to change the DAC output every 2µsec, and need to generate a voltage range
  from 0 to +12V.
- We did not use the recommended OPA277 due to its low Gain-BW. Is it possible that the OPA828 is the culprit?

Image #1

Op-amp voltage output falling edge →

Digital code 65,536 → 20,000
200mV/div
500usec/div
Long settling time to reach 3.80v

Image #2

Digital code 30,000 → 20,000
200mV/div
500usec/div
Short settling time to reach 3.80v

Image #3

Digital code 65,536 → 20,000
200mV/div
200nsec/div
"Short term" settling time <0.5μsec per data sheet
But with a large undershoot

Image #4

Digital code 30,000 → 20,000
200mV/div
200nsec/div
"Short term" settling time faster
with a smaller undershoot