User's Guide

SLAU580B – June 2014 – Revised August 2016

TSW14J10 FMC-USB Interposer Card

This user's guide describes the functionality, hardware, operation, and software instructions for the TSW14J10 FMC-USB interposer card. Throughout this document, the abbreviations TSW14J10EVM, EVM, and the term *evaluation module* are synonymous with the TSW14J10 Evaluation Module, unless otherwise noted.

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1 Introduction

The Texas Instruments TSW14J10 Evaluation Module (EVM) allows users to operate the High Speed Data Converter Pro Graphic User Interface (HSDC Pro GUI) Software on certain Xilinx® and Altera® development kits that incorporate the FMC connector. This FMC-FMC adapter has a four bus FTDI USB-to-GPIO device, that when connected to a PC, provides an interface to the FPGA on the development platform allowing the HSDC Pro GUI to operate as if it were connected to a TI development board. The TSW14J10 is compatible with all TI ADC and DAC JESD204B-based EVMs. Contact FPGA vendors for other available firmware not provided by HSDC Pro Software to test ADC and DAC EVMs with their development platform.

2 Functionality

The TSW14J10 uses two industry standard FMC connectors that provide an interface between an FMC-based development board and all TI JESD204B ADC and DAC EVMs. To acquire data, receive data, and do register read and writes using a host PC, the FPGA transmits and receives data across three Serial Peripheral Interface (SPI) busses using dedicated pins on the FMC that connect to the FTDI on the TSW14J10. The fourth bus connects to a JTAG connector. When connecting the provided cable between this connector and a JTAG connecter on a FPGA development platform, the HSDC Pro GUI can be used to configure the FPGA. This interface is also routed to the FMC connector when setting jumpers to the appropriate configuration (see Table 1).

The TSW14J10 routes the SPI busses through level translators that allow the signals going to the FPGA development board and the ADC/DAC EVM to be either 3.3-V or 1.8-V levels. All devices on the TSW14J10 are powered from the USB connection.

Figure 1 shows an ADS42JB69EVM connected to a Xilinx Kintex® KC705 development board using a TSW14J10EVM.

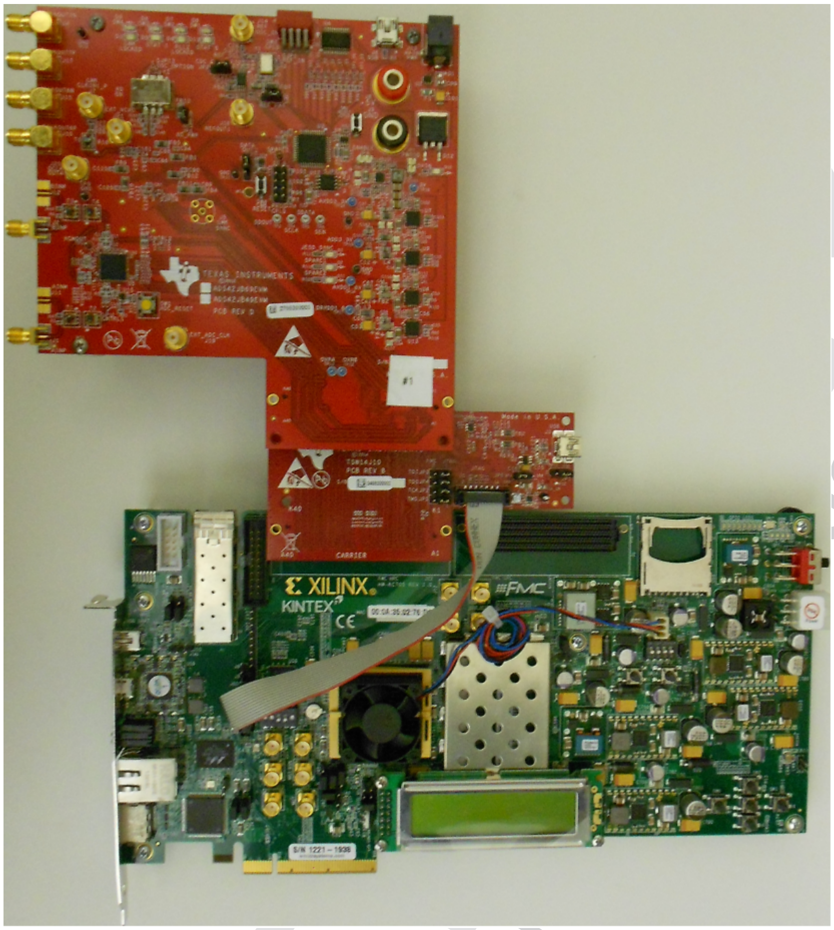


Figure 1. TSW14J10EVM, ADS42JB69EVM, and Kintex KC705 Development Card

The major features of the TSW14J10 are:

- 10 transceiver lanes with speeds up to 12.5Gbps
- Industry-standard JTAG connector
- Supports 1.8-V, 3.3-V CMOS IO interface
- Onboard FT4232HL USB device for JTAG, SPI interface
- Supported by TI HSDC PRO software
- 2 Samtec high-speed, high-density FMC connectors

Figure 2 shows a block diagram of the TSW14J10 EVM.

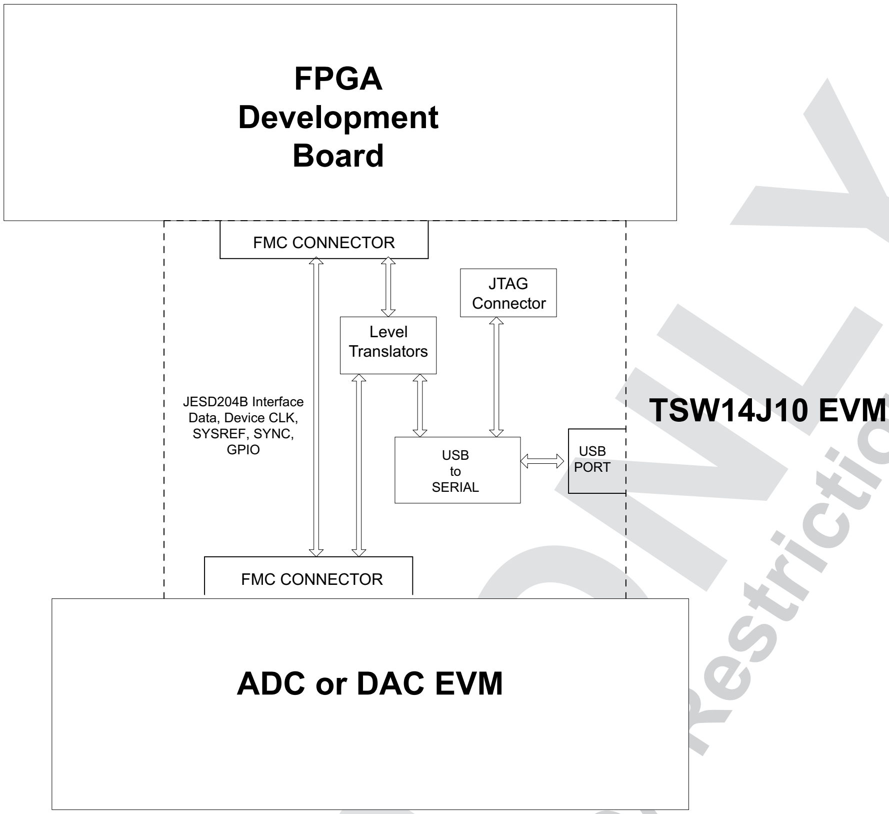


Figure 2. TSW14J10 EVM Block Diagram

3 Hardware Configuration

In this section, the various portions of the TSW14J10EVM hardware are described. The TSW14J10EVM comes with a 10 pin ribbon cable that is used as a programming option for the FPGA on the FPGA Development Board, plastic screws and nuts to secure the three boards together, and stand-off extenders to be used on the ADC/DAC EVM due to the new height of the interface FMC connector.

3.1 Power Connections

The TSW14J10EVM hardware is designed to operate from a single-supply voltage of +5 VDC. By default, this power input is provided by the USB connection. A second option is to provide external +5 V to test point TP12 and shunt pins 1-2 on JP1. This will remove the USB power from the +5-V power traces and connect it to TP12. The external source should be able to provided 0.5 A.

3.2 Jumpers

The TSW14J10 contains several jumpers (JP) and solder jumpers (SJP) that enable certain functions on the board. The description of the jumpers are found in Table 1. In addition to the jumpers, there are several 0 Ohm resistors that are used as jumpers. If using the TSW14J10EVM with the Xilinx ZC706 and a TI DAC EVM, the following resistors need to be removed or installed to route the SYNC signals from the DAC EVM to the correct pins on the ZC706 board:

Install R142, R144, R146 and R148

Remove R143 and R145

Table 1. TSW14J10 Jumper Descriptions

Component	Description	Default
JP1	USB power select. Default is power from the USB interface.	2-3
JP2-JP5	FTDI connected to JTAG connector or FMC. Default is JTAG connector.	1-2
JP6	Translator voltage level select (1.8 V or 3.3 V). Default is 3.3 V.	2-3
SJP1	Direction control for buffer U9. Default is A to B.	1-2
SJP2	Direction control for buffer U10. Default is B to A.	2-3
SJP3	Direction control for buffer U11. Default is B to A.	2-3

3.3 Connectors

3.3.1 FPGA Development Platform FMC Connector

The TSW14J10 EVM has one FPGA Mezzanine Card Connector (FMC) to allow for direct plug in of a TI JESD204B serial interface ADC or DAC EVM and another to plug into an FPGA development board. The specifications for this connector were mostly derived from the ANSI/VITA 57.1 FPGA Mezzanine Card Standard. This standard describes the compliance requirements for a low overhead protocol bridge between a carrier card's IO and an FPGA processing device on a carrier card. This specification is being used by FPGA vendors on their development platforms.

FMC connector J5 provides the interface between the TSW14J10EVM and a FPGA development platform. This 400-pin Samtec high-speed, high- density connector, part number SEAF-40-05.0-S-10-2-A-K, is suitable for high-speed differential pairs up to 21Gbps. In addition to the JESD204B standard signals, 13 CMOS single-ended signals are sourced from the USB interface to the FMC connector. These signals are used by the HSDC Pro GUI to program internal registers and read and write data to the FPGA. The connector pinout description is shown in Table 2.

Table 2. FPGA FMC Connector (J5) Description of the TSW14J10

FMC Signal Name	FMC Pin	Standard JESD204 Application Mapping	Description
DP0_M2C_P/N	C6/C7	Lane 0+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP1_M2C_P/N	A2/A3	Lane 1+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP2_M2C_P/N	A6/A7	Lane 2+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP3_M2C_P/N	A10/A11	Lane 3+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP4_M2C_P/N	A14/A15	Lane 4+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP5_M2C_P/N	A18/A19	Lane 5+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP6_M2C_P/N	B16/B17	Lane 6+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP7_M2C_P/N	B12/B13	Lane 7+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP8_M2C_P/N	B8/B9	Lane 8+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP9_M2C_P/N	B4/B5	Lane 9+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP0_C2M_P/N	C2/C3	Lane 0+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP1_C2M_P/N	A22/A23	Lane 1+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP2_C2M_P/N	A26/A27	Lane 2+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP3_C2M_P/N	A30/A31	Lane 3+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP4_C2M_P/N	A34/A35	Lane 4+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP5_C2M_P/N	A38/A39	Lane 5+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP6_C2M_P/N	B36/B37	Lane 6+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP7_C2M_P/N	B32/B33	Lane 7+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP8_C2M_P/N	B28/B29	Lane 8+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP9_C2M_P/N	B24/B25	Lane 9+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
GTX_CLKP/M	D4/D5	DEVCLKA+/- (M->C)	Primary carrier-bound reference clock required for FPGA gigabit transceivers. Equivalent to device clock.
Device Clock, SYSREF, and SYNC			
FMC Signal Name	**FMC Pin**	**Standard JESD204 Application Mapping**	**Description**

Table 2. FPGA FMC Connector (J5) Description of the TSW14J10 (continued)

CLK_LA0_P/N	G6/G7	DEVCLKB+/- (M->C)	Secondary carrier-bound device clock. Used for special FPGA functions such as sampling SYSREF.
D8/D9	D8/D9	DEVCLK+/- (C->M)	Mezzanine-bound device Clock. Used for low noise conversion clock.
CAR_SYSREFP/M	G9/G10	SYSREF+/- (M->C)	Carrier-bound SYSREF signal
D11/D12	D11/D12	SYSREF+/- (C->M)	Mezzanine-bound SYSREF signal
SYNCP/M	G12/G13	SYNC+/- (C>M)	ADC Mezzanine-bound SYNC signal for use in class 0/1/2 JESD204 systems
DAC_SYNC_P/M	F10/F11	DAC SYNC+/- (M>C)	Carrier-bound SYNC signal for use in class 0/1/2 JESD204 systems.
ALT_DAC_SYNC_PM	F19/F20	Alt. DAC SYNC+/- (M>C)	Alternate Carrier-bound SYNC signal for use in class 0/1/2 JESD204B systems.
ALT_SYNCP/M	H31/H32	Alt. SYNC+/- (C>M)	Alternate ADC Mezzanine-bound SYNC signal. For use when SYNC (C->M) is not available.
SYNC	K22	DAC SYNC (M>C)	Alternate Carrier-bound CMOS level SYNC signal for use in class 0/1/2 JESD204 systems.
Special Purpose I/O			
FMC Signal Name	**FMC Pin**	**Direction**	**Description**
F1	F1		Power good from mezzanine to carrier
D1	D1		Power good from carrier to mezzanine
PRESENT	H2	ADC/DAC-to-FPGA	EVM Present indicator
ADBUS0_T	C14	USB-to-FPGA	USB SPI Interface signal
ADBUS1_T	C15	USB-to-FPGA	USB SPI Interface signal
ADBUS2_T	H8	FPGA-to-USB	USB SPI Interface signal
ADBUS3_T	D14	USB-to-FPGA	USB SPI Interface signal
ADBUS4_T	C10	USB-to-FPGA	USB SPI Interface signal
BDBUS0_T	D15	USB-to-FPGA	USB SPI Interface signal
BDBUS1_T	G15	USB-to-FPGA	USB SPI Interface signal
BDBUS2_T	H10	FPGA-to-USB	USB SPI Interface signal
BDBUS3_T	G16	USB-to-FPGA	USB SPI Interface signal
CDBUS0_T	H16	USB-to-FPGA	USB SPI Interface signal
CDBUS1_T	H17	USB-to-FPGA	USB SPI Interface signal
CDBUS2_T	H11	FPGA-to-USB	USB SPI Interface signal
CDBUS3_T	H7	USB-to-FPGA	USB SPI Interface signal
TCK	D29	USB-to-JTAG	JTAG connector clock
TDI	D30	USB-to-JTAG	JTAG connector TDI
TDO	D31	JTAG-to-USB	JTAG connector TDO
TMS	D33	USB-to-JTAG	JTAG connector TMS
OVRA	K19	ADC-to-FPGA	ADC over range indicator
OVRB	E18	ADC-to-FPGA	ADC over range indicator
OVRC	J22	ADC-to-FPGA	ADC over range indicator
OVRD	J21	ADC-to-FPGA	ADC over range indicator
DAC-SYNC+/-	E2/E3	DAC-to-FPGA	Spare sync
FPGA_CLK2P/N	J2/J3	FPGA-to-DAC	Spare clock
FPGA_CLK1P/N	K4/K5	FPGA-to-DAC	Spare clock
LED_SYNC1	C18	FPGA-to-ADC	SYNC LED indicator
SPLED0	D17	FPGA-to-ADC	Spare LED
SPLED1	D18	FPGA-to-ADC	Spare LED
C19	C19		Spare connection
C26	C26		Spare connection
C27	C27		Spare connection
D26	D26		Spare connection
E19	E19		Spare connection
G27	G27		Spare connection

Table 2. FPGA FMC Connector (J5) Description of the TSW14J10 (continued)

G36	G36		Spare connection
G37	G37		Spare connection
H37	H37		Spare connection
H38	H38		Spare connection

3.3.2 ADC/DAC FMC Connector

FMC connector J4 provides the interface between the TSW14J10EVM and an ADC or DAC EVM. In addition to the JESD204B standard signals, 8 CMOS single-ended signals are sourced from the USB interface to the FMC connector. These signals are used to allow the HSDC Pro GUI to control the SPI serial programming of an ADC or DAC EVM that supports this feature. Several other spare signals are available that connect between this connector and the FPGA FMC connector. The connector pinout description is shown in Table 3.

Table 3. ADC/DAC EVM FMC Connector (J4) Description of the TSW14J10

FMC Signal Name	FMC Pin	Standard JESD204 Application Mapping	Description
DP0_M2C_P/N	C6/C7	Lane 0+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP1_M2C_P/N	A2/A3	Lane 1+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP2_M2C_P/N	A6/A7	Lane 2+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP3_M2C_P/N	A10/A11	Lane 3+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP4_M2C_P/N	A14/A15	Lane 4+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP5_M2C_P/N	A18/A19	Lane 5+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP6_M2C_P/N	B16/B17	Lane 6+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP7_M2C_P/N	B12/B13	Lane 7+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP8_M2C_P/N	B8/B9	Lane 8+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP9_M2C_P/N	B4/B5	Lane 9+/- (M->C)	JESD Serial data transmitted from Mezzanine and received by Carrier
DP0_C2M_P/N	C2/C3	Lane 0+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP1_C2M_P/N	A22/A23	Lane 1+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP2_C2M_P/N	A26/A27	Lane 2+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP3_C2M_P/N	A30/A31	Lane 3+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP4_C2M_P/N	A34/A35	Lane 4+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP5_C2M_P/N	A38/A39	Lane 5+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP6_C2M_P/N	B36/B37	Lane 6+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP7_C2M_P/N	B32/B33	Lane 7+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP8_C2M_P/N	B28/B29	Lane 8+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
DP9_C2M_P/N	B24/B25	Lane 9+/- (C->M)	JESD Serial data transmitted from Carrier and received by Mezzanine
GTX_CLKP/M	D4/D5	DEVCLKA+/- (M->C)	Primary carrier-bound reference clock required for FPGA gigabit transceivers. Equivalent to device clock.
Device Clock, SYSREF, and SYNC			
FMC Signal Name	**FMC Pin**	**Standard JESD204 Application Mapping**	**Description**
CLK_LA0_P/N	G6/G7	DEVCLKB+/- (M->C)	Secondary carrier-bound device clock. Used for special FPGA functions such as sampling SYSREF.
D8/D9	D8/D9	DEVCLK+/- (C->M)	Mezzanine-bound device clock. Used for low noise conversion clock.
CAR_SYSREFP/M	G9/G10	SYSREF+/- (M->C)	Carrier-bound SYSREF signal
D11/D12	D11/D12	SYSREF+/- (C->M)	Mezzanine-bound SYSREF signal
SYNCP/M	G12/G13	SYNC+/- (C>M)	ADC Mezzanine-bound SYNC signal for use in class 0/1/2 JESD204 systems
DAC_SYNC_P/M	F10/F11	DAC SYNC+/- (M>C)	Carrier-bound SYNC signal for use in class 0/1/2 JESD204 systems
ALT_DAC_SYNC_PM	F19/F20	Alt. DAC SYNC+/- (M>C)	Alternate Carrier-bound SYNC signal for use in class 0/1/2 JESD204B systems
ALT_SYNCP/M	H31/H32	Alt. SYNC+/- (C>M)	Alternate ADC Mezzanine-bound SYNC signal. For use when SYNC (C->M) is not available.
Special Purpose I/O			

Table 3. ADC/DAC EVM FMC Connector (J4) Description of the TSW14J10 (continued)

FMC Signal Name	FMC Pin	Direction	Description
F1	F1	ADC/DAC-to-FPGA	Power good from mezzanine to carrier
D1	D1	FPGA-to-ADC/DAC	Power good from carrier to mezzanine
PRESENT	H2	ADC/DAC-to-FPGA	EVM Present indicator
ADBUS5_T	C15	USB-to-ADC/DAC	USB SPI Interface signal
ADBUS6_T	D14	USB-to-ADC/DAC	USB SPI Interface signal
ADBUS7_T	D15	USB-to-ADC/DAC	USB SPI Interface signal
BDBUS4_T	G15	USB-to-ADC/DAC	USB SPI Interface signal
BDBUS5_T	G16	USB-to-ADC/DAC	USB SPI Interface signal
BDBUS6_T	H16	USB-to-ADC/DAC	USB SPI Interface signal
BDBUS7_T	H17	USB-to-ADC/DAC	USB SPI Interface signal
CDBUS4_T	C14	USB-to-ADC/DAC	USB SPI Interface signal
OVRA	K19	ADC-to-FPGA	ADC over range indicator
OVRB	E18	ADC-to-FPGA	ADC over range indicator
OVRC	J22	ADC-to-FPGA	ADC over range indicator
OVRD	J21	ADC-to-FPGA	ADC over range indicator
FPGA_CLK2P/N	J2/J3	FPGA-to-DAC	Spare clock
FPGA_CLK1P/N	K4/K5	FPGA-to-DAC	Spare clock
LED_SYNC1	C18	FPGA-to-ADC	SYNC LED indicator
SPLED0	D17	FPGA-to-ADC	Spare LED
SPLED1	D18	FPGA-to-ADC	Spare LED
C19	C19		Spare connection
C26	C26		Spare connection
C27	C27		Spare connection
D26	D26		Spare connection
E19	E19		Spare connection
G27	G27		Spare connection
G36	G36		Spare connection
G37	G37		Spare connection
H37	H37		Spare connection
H38	H38		Spare connection
K20	K20		Spare connection
K23	K23		Spare connection

3.3.3 JTAG Connector

The TSW14J10EVM includes an industry-standard JTAG connector that is connected to the DDBUS of the USB interface device. This interface allows the HSDC Pro GUI the capability to configure an FPGA on a development platform if it has a corresponding JTAG connector that is routed directly to the FPGA JTAG pins. Connect the provide JTAG cable between the TSW14J10 JTAG connector and the FPGA development board JTAG connector.

NOTE: FPGA development boards may require jumpers and or switches be placed in a certain configuration to connect the JTAG connector to the FPGA JTAG pins.

If the FPGA development platform has the JTAG signals routed on the FMC connector, jumpers JP2-5 can be set (shunt pins 2-3) to route these signals to the FMC connector instead of the JTAG connector.

3.3.4 USB I/O Connection

HSDC Pro GUI control is accomplished through USB connector J3. This will provide the interface between HSDC Pro GUI running on a PC Windows operating system and a FPGA development platform. For the computer, the drivers needed to access the USB port are included in the HSDC Pro GUI installation software. The drivers are automatically installed during the installation process. On the TSW14J10EVM, the USB port is used to identify the type and serial number of the EVM under test, load the desired FPGA configuration file, capture ADC EVM data from the FPGA, and send test pattern data to the FPGA for DAC EVM testing.

4 Software Start Up

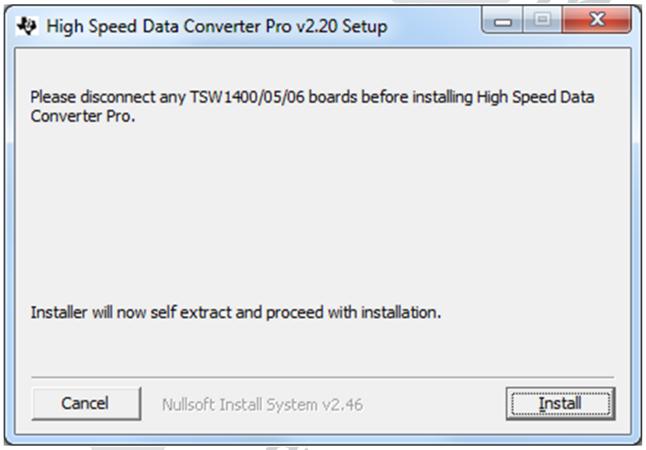
4.1 *Installation Instructions*

Download the latest version of the HSDC Pro GUI (slwc107x.zip) to a local directory on a host PC. This can be found on the TI website by entering “HIGH SPEED DATA CONVERTER PRO GUI INSTALLER” or “TSW14J10EVM” in the search parameter window at www.ti.com.

Unzipping the software package generates a folder called *High Speed Data Converter Pro - Installer vx.xx.exe*, where x.xx is the version number. Run this program to start the installation

Follow the on-screen instructions during installation.

NOTE: If an older version of the GUI has already been installed, make sure to uninstall it before loading a newer version.



High Speed Data Converter Pro v2.20 Setup

Please disconnect any TSW1400/05/06 boards before installing High Speed Data Converter Pro.

Installer will now self extract and proceed with installation.

Nullsoft Install System v2.46

Figure 3. GUI Installation

Make sure to disconnect all USB cables from any TSW14xxx boards before installing the software.

Click on the **Install** button. A new window opens. Click the **Next** button.

Accept the License Agreement. Click on **Next** to start the installation. After the installer has finished, click on **Next** one last time.

The installation is now complete. The GUI executable and associated files will reside in the following directory.

"C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro"

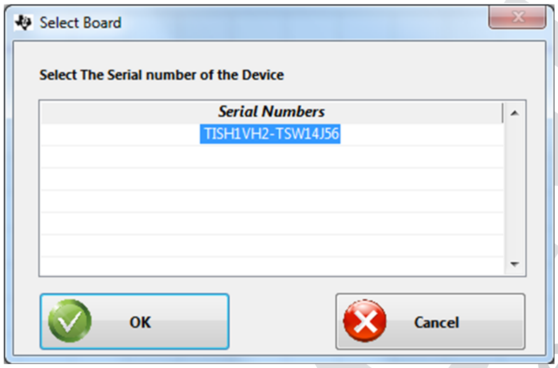
When new TI High Speed Data Converter EVM's or JESD204B interface modes become available that are not currently supported by the latest release of HSDC Pro GUI, the HSDCProv_xpxx_Patch_setup executable, available on the TI website under the High Speed Data Converer Pro Software product folder (http://www.ti.com/tool/dataconverterpro-sw), will allow the user to add these to the GUI device list. After the patch has been downloaded, follow the on screen instructions to run the patch. The software will display the files that will be added. After running the patch, go ahead and open HSDC Pro and the new parts and modes will appear in the ADC and DAC device drop down selection box. The patch is always specific to a core GUI version and will not work for a GUI version that the patch was not explicitly created for.

4.2 USB Interface and Drivers

Connect a USB cable between J3 of the TSW14J10EVM and a host PC.

Click on the High Speed Data Converter Pro icon that was created on the desktop panel or go to "C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro" and double click on the executable called *High Speed Data Converter Pro.exe* to start the GUI.

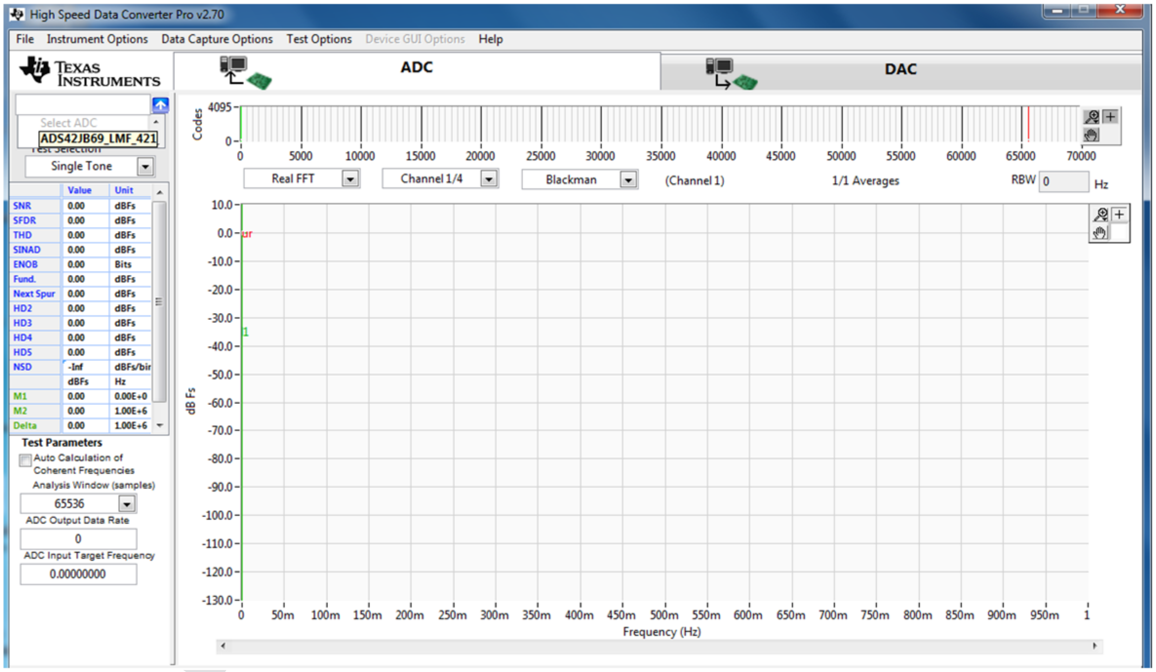
The GUI first attempts to connect to the EVM USB interface. If the GUI identifies a valid board serial number, a pop-up opens displaying this value, as shown in Figure 4. It is possible to connect several TSW14J10 EVMs to one host PC but the GUI can only connect to one at a time. In the case where multiple boards are connected to the PC, the pop-up will display all of the serial numbers found. The user then selects which board the GUI will be associated with.



TISH1VH2-TSW14J56

Figure 4. TSW14J10EVM Serial Number

Click on the **OK** button to connect the GUI to the board. The top-level GUI opens and appears as shown in Figure 5.



ADS42JB69_LMF_421

Single Tone

Real FFT | Channel 1/4 | Blackman | (Channel 1) | 1/1 Averages | RBW 0 Hz

	Value	Unit
SNR	0.00	dBFs
SFDR	0.00	dBFs
THD	0.00	dBFs
SINAD	0.00	dBFs
ENOB	0.00	Bits
Fund.	0.00	dBFs
Next Spur	0.00	dBFs
HD2	0.00	dBFs
HD3	0.00	dBFs
HD4	0.00	dBFs
HD5	0.00	dBFs
NSD	-Inf	dBFs/bin
	dBFs	Hz
M1	0.00	0.00E+0
M2	0.00	1.00E+6
Delta	0.00	1.00E+6

Test Parameters

☐ Auto Calculation of Coherent Frequencies

Analysis Window (samples): 65536

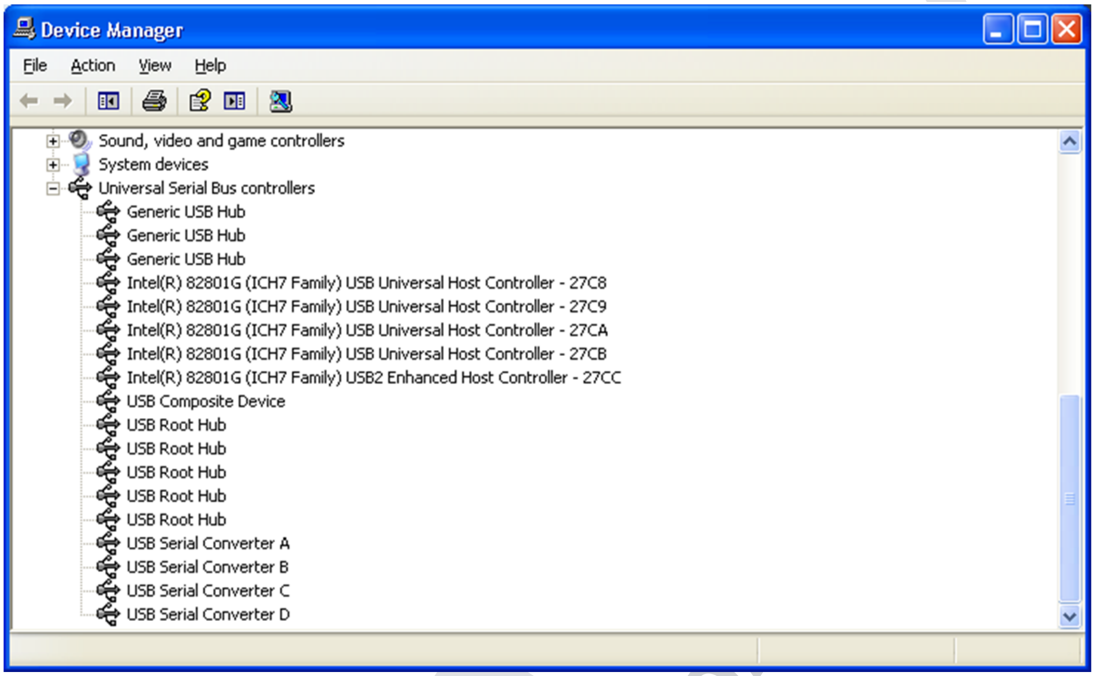
ADC Output Data Rate: 0

ADC Input Target Frequency: 0.00000000

Figure 5. High Speed Data Converter Pro GUI Top Level

If the message *No Board Connected* opens, double check the USB cable connection. If the cable connection appears fine, try establishing a connection by clicking on the *Instrument Option* tab at the top left of the GUI and select *Connect to the Board*. If this still does not correct this issue, check the status of the host USB port.

When the software is installed and the USB cable has been connected to the TSW14J10EVM and the PC, the TSW14J10 USB serial converter should be located in the Hardware Device Manager under the Universal Serial Bus controllers as shown in Figure 6. This is a quad device which is why there is an A, B, C, and D USB serial converter shown. When the USB cable is removed, these four will no longer be visible in the Device Manager. If the drivers are present in the Device Manager window and the software still does not connect, cycle power to the board and repeat the previous steps.



- Sound, video and game controllers
- System devices
- Universal Serial Bus controllers
  - Generic USB Hub
  - Generic USB Hub
  - Generic USB Hub
  - Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27C8
  - Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27C9
  - Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27CA
  - Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27CB
  - Intel(R) 82801G (ICH7 Family) USB2 Enhanced Host Controller - 27CC
  - USB Composite Device
  - USB Root Hub
  - USB Root Hub
  - USB Root Hub
  - USB Root Hub
  - USB Root Hub
  - USB Serial Converter A
  - USB Serial Converter B
  - USB Serial Converter C
  - USB Serial Converter D

Figure 6. Hardware Device Manager

5 Downloading Firmware Example

If the FPGA development platform is to be programmed using the TSW14J10EVM, either connect the provided ribbon cable between the TSW14J10 JTAG connector and the FPGA development platform JTAG connector or move the shunts on JP2-JP5 to pins 2-3 if the JTAG signals are routed to the FMC connector.

The HSDC Pro GUI software provides support for certain FPGAs and modes of operation. The firmware files needed are special .svf formatted files for Xilinx devices and .rbf formatted files for Altera devices. The files used by the GUI currently reside in the directory called "C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J10KC705 Details\ Firmware" for the Xilinx Kintex KC705 board, "C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J10VC707 Details\ Firmware" for the Xilinx Virtex VC707 board, and "C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J10ZC706 Details\ Firmware" for the Xilinx Zync ZC706 board.

To load a Xilinx KC705 development platform firmware after the GUI has established connection, click on the Select ADC window in the top left of the GUI and select ADS42JB69_LMF_421, as shown in Figure 5.

The GUI asks if you want to update the Firmware for the ADC. Click on Yes. The GUI starts loading the firmware from the PC to the Xilinx Kintex 7 FPGA. While the firmware is loading, the GPIO LED's on the FPGA platform will all be on. This process takes about 2 minutes. Once completed, the INIT LED (DS21) and DONE LED (DS20) will illuminate on the KC705. After the ADS42JBx9EVM is programmed, the KC705 GPIO LED status will be as follows:

0 – On (DAC SYNC indicator)

1 – On (ADC SYNC indicator)

2 – Off (JESD reset)

3 – On (ADC JESD mode enabled)

4 – Off (DAC JESD mode enabled)

5 – Blinking (System clock divided down)

6 – Blinking (JESD Core clock divided down)

7 – Blinking (Reference clock divided down)

These same status LED's apply to the Xilinx VC707 development platform. For the Xilinx Zync ZC706 platform, only three status LED's are used. After this board is programmed and running with an ADC or DAC, the status of the GPIO LED's will be as follows:

L - Blinking (Reference clock divided down)

C - Blinking (JESD Core clock divided down)

R - Blinking (System clock divided down)

If the ADS42Jx9EVM is not programmed, the GPIO LED status is as follows:

0 – On (DAC SYNC indicator)

1 – Off (ADC SYNC indicator)

2 – On (JESD reset)

3 – Off (ADC JESD mode enabled)

4 – Off (DAC JESD mode enabled)

5 – Blinking (System clock divided down)

6 – N/A (JESD Core clock divided down)

7 – N/A (Reference clock divided down)

If the two boards are not synchronized after both have been configured, this is indicated by GPIO LED 2 being *Off* on the KC705 board and D3 being *On* on the ADS42JB69EVM. Pressing the CPU reset (SW7) on the KC705 board resets the JESD204B link and should synchronize the two boards. After synchronization has been established, enter a valid sampling rate in the HSDC Pro GUI and click on *Capture* to display valid data from the ADC EVM.

For information regarding the use of the TSW14J10EVM with a TI ADC or DAC JESD204B serial interface EVM, consult the High Speed Data Converter Pro GUI User's Guide (SLWU087) along with the individual EVM User's Guide.

6 DAC and ADC GUI Configuration File Changes When Using a Xilinx Development Platform

The configuration files that come with the TI ADC and DAC EVM GUIs are setup to operate with the Altera-based TI TSW14J56EVM. These files will work with the TSW14J10EVM when using a Xilinx platform but need a couple of changes to the settings of the LMK04828 registers. The firmware for the Xilinx Development Platforms use a separate clock input for REFCLK and Core clock to give maximum flexibility and support all line rates and subclasses with a single programmable design. The Xilinx IP used in the firmware can be driven by a single clock in many circumstances (see the clocking section of the Xilinx IP product guide for more details).

The REFCLK and Core clock are determined by the following lane rate conditions:

REFCLK = Lane rate / 10, and Core clock = Lane rate / 10 when lane rate is between 1G and 3.2G

REFCLK = Lane rate / 20 and Core clock = Lane rate / 40 when lane rate is between 3.2G and 10.3125G*

Note: The GTEX2 transceivers with speed grade -2 devcies used on the Xilinx development platforms have a maximum rate of 10.3125Gbps. In addition, the KC705 transceivers have a frequency band gap from 8Gbps to 9.8Gbps.

The ADC and DAC GUIs do not always use the same LMK04828 outputs for these two clocks. The output from the LMK04828 connected to FMC connector pins D4 and D5 will be the REFCLK. The output from the LMK04828 connected to FMC connector pins G6 and G7 will be the Core clock. Consult the EVM schematic to verify the outputs.

On the KC705 platform, only 4 TX and 4 RX JESD204B lanes were routed to the HPC FMC connector. On the VC707 and ZC706, there are at least 8 RX and TX lanes routed. The Xilinx firmware designed to be used with the TSW14J10EVM running HSDC Pro GUI uses internal FPGA memory only. Due to both of these constraints, the user must be careful when selecting the number of samples and number of lanes to be used in both ADC and DAC testing. The total memory and JESD204B lanes that are available are as follows:

KC705 4 lanes RX and TX 128K total samples

VC707 8 lanes RX and TX 256K total samples

ZC706 8 lanes RX and TX 128K total samples

For example when using the KC705, if the user is capturing data from a dual ADC, the most lanes that can be used is 4 and the highest value that can be entered for number of samples in HSDC Pro GUI will be 64K.

6.1 DAC38J84EVM GUI Setup Example

This section provides an example of the TSW14J10EVM being used to test the DAC38J84EVM with a Xilinx VC707 development platform as shown in Figure 7. This example shows what must be modified in the DAC3XJ8X GUI for a setup using 4 lanes (LMFS = 4421), 1x interpolation, and a DAC sample rate of 368.64M. Setup the hardware as follows:

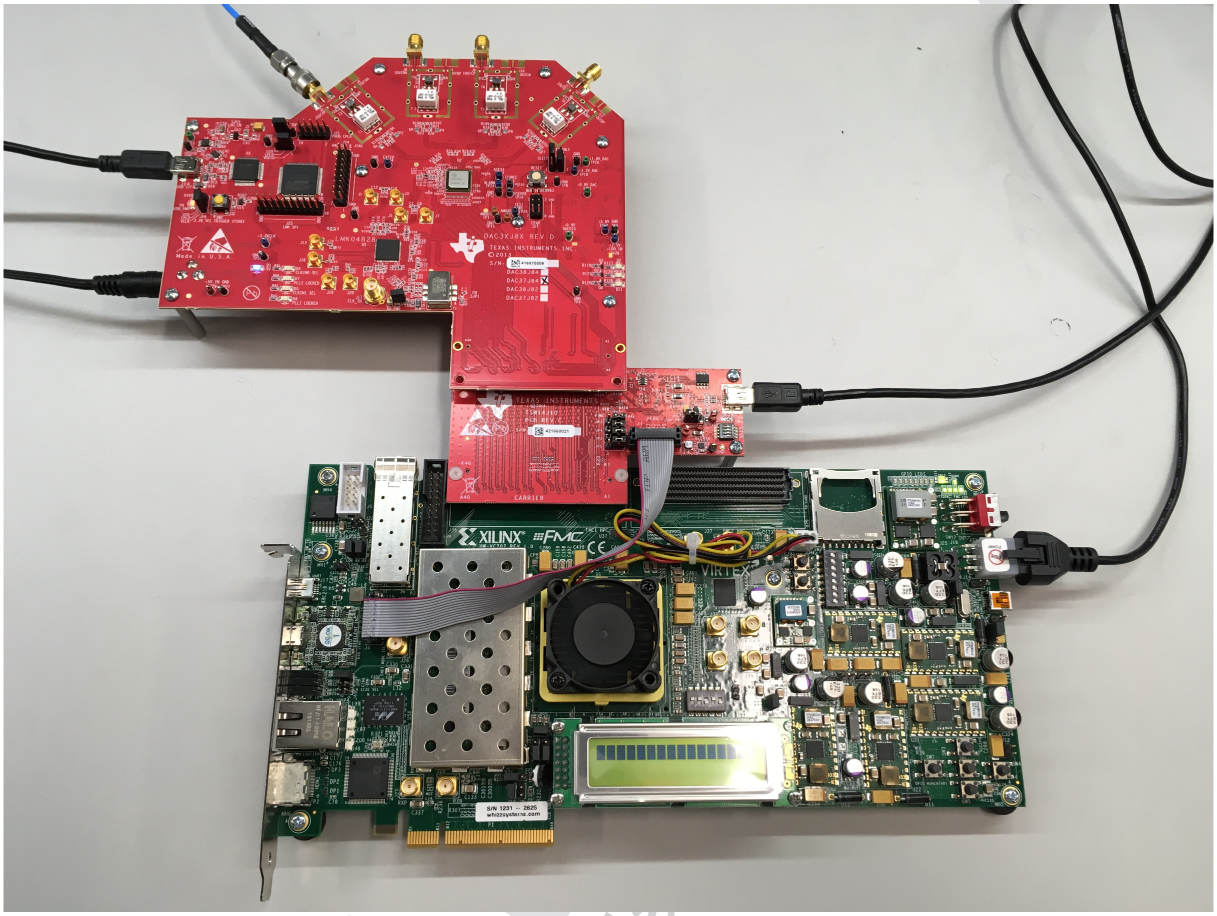
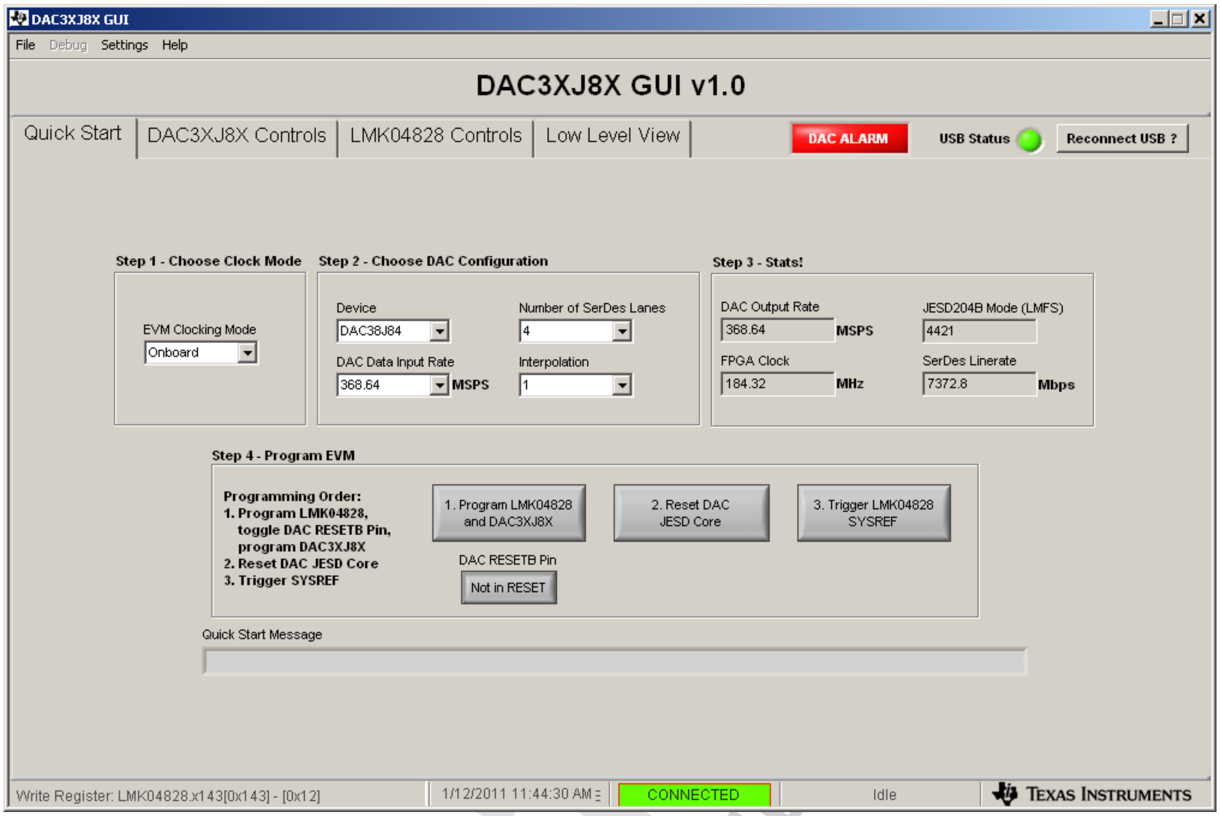


Figure 7. DAC38J84EVM GUI Setup Example

1. Connect J5 of the TSW14J10 to FMC HPC connector J35 on the VC707.
2. Connect the DAC to the other end of the TSW14J10.
3. Connect the power cables to the VC707 and DAC38J84.
4. Connect a USB cable between the TSW14J10 and a host computer with the HSDC Pro GUI loaded.
5. Connect a USB cable between the DAC38J84 and a host computer with the DAC3XJ8X GUI loaded.

Power up the DAC38J84 and VC707. Program the DAC38J84 as follows:

After opening the DAC GUI, enter the parameters as shown in Figure 8.



EVM Clocking Mode: Onboard

Device: DAC38J84

Number of SerDes Lanes: 4

DAC Data Input Rate: 368.64 MSPS

Interpolation: 1

DAC Output Rate: 368.64 MSPS

JESD204B Mode (LMFS): 4421

FPGA Clock: 184.32 MHz

SerDes Linerate: 7372.8 Mbps

Programming Order:
1. Program LMK04828, toggle DAC RESETB Pin, program DAC3XJ8X
2. Reset DAC JESD Core
3. Trigger SYSREF

DAC RESETB Pin: Not in RESET

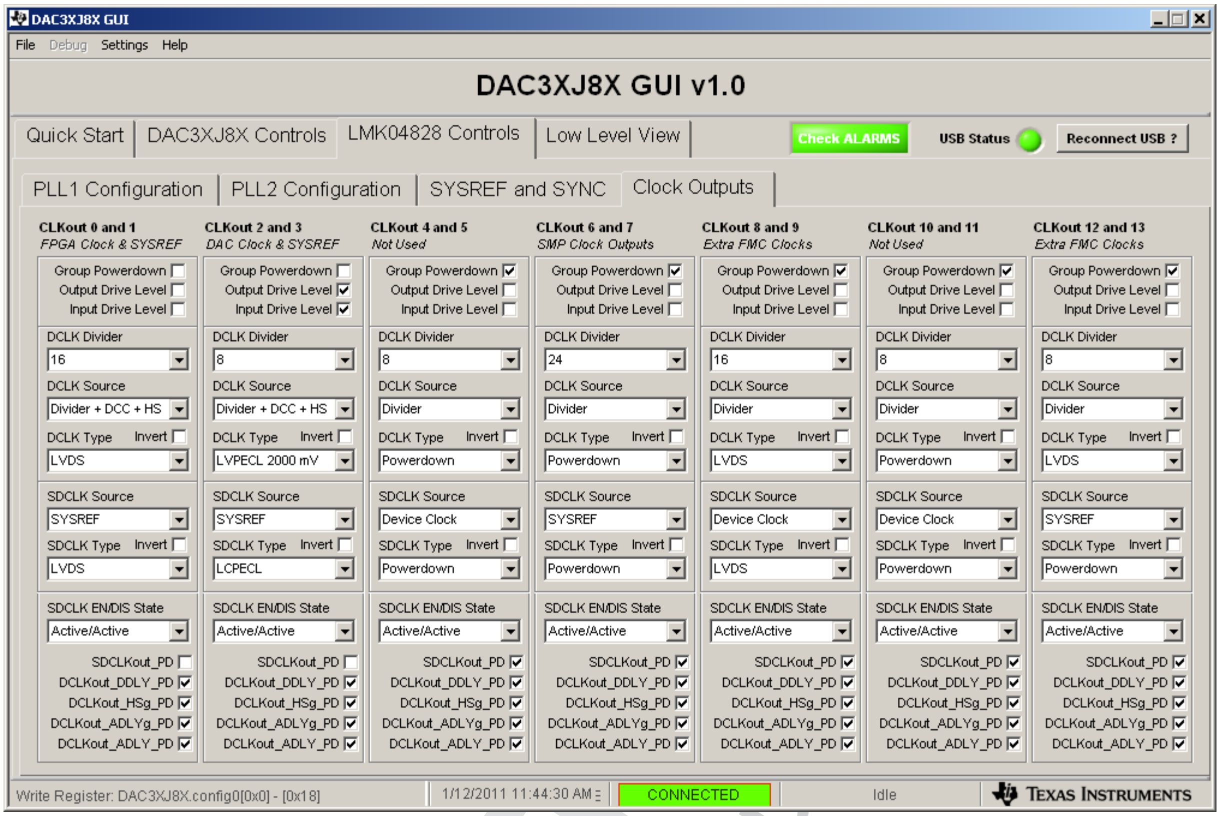
Write Register: LMK04828.x143[0x143] - [0x12] | 1/12/2011 11:44:30 AM | CONNECTED | Idle

Figure 8. Quick Start Menu

The GUI calculates the lane rate and displays it in the box called *SerDes Linerate*. For this example, the lane rate is 7372.8Mbps. Using the lane rate conditions in Section 6, REFCLK = 368.64 MHz and Core clock = 184.32 MHz.

Click on the *Program LMK04828 and DAC3XJ8X* button. After the programming has completed, click on the *LMK04828 Controls* tab. Next, click on the *Clock Outputs* tab.

For the DAC3XJ8X GUI, the REFCLK is provided by *CLKout 0* and the Core clock is provided by *CLKout 12*. Notice that the default setting for *CLKout 12* is *Group Powerdown*, as shown in Figure 9.



	CLKout 0 and 1 *FPGA Clock & SYSREF*	**CLKout 2 and 3** *DAC Clock & SYSREF*	**CLKout 4 and 5** *Not Used*	**CLKout 6 and 7** *SMP Clock Outputs*	**CLKout 8 and 9** *Extra FMC Clocks*	**CLKout 10 and 11** *Not Used*	**CLKout 12 and 13** *Extra FMC Clocks*
Group Powerdown	☐	☐	☑	☑	☑	☑	☑
Output Drive Level	☐	☑	☐	☐	☐	☐	☐
Input Drive Level	☐	☑	☐	☐	☐	☐	☐
DCLK Divider	16	8	8	24	16	8	8
DCLK Source	Divider + DCC + HS	Divider + DCC + HS	Divider	Divider	Divider	Divider	Divider
DCLK Type	LVDS	LVPECL 2000 mV	Powerdown	Powerdown	LVDS	Powerdown	LVDS
Invert	☐	☐	☐	☐	☐	☐	☐
SDCLK Source	SYSREF	SYSREF	Device Clock	SYSREF	Device Clock	Device Clock	SYSREF
SDCLK Type	LVDS	LCPECL	Powerdown	Powerdown	LVDS	Powerdown	Powerdown
Invert	☐	☐	☐	☐	☐	☐	☐
SDCLK EN/DIS State	Active/Active	Active/Active	Active/Active	Active/Active	Active/Active	Active/Active	Active/Active
SDCLKout_PD	☐	☐	☑	☑	☑	☑	☑
DCLKout_DDLY_PD	☑	☑	☑	☑	☑	☑	☑
DCLKout_HSg_PD	☑	☑	☑	☑	☑	☑	☑
DCLKout_ADLYg_PD	☑	☑	☑	☑	☑	☑	☑
DCLKout_ADLY_PD	☑	☑	☑	☑	☑	☑	☑

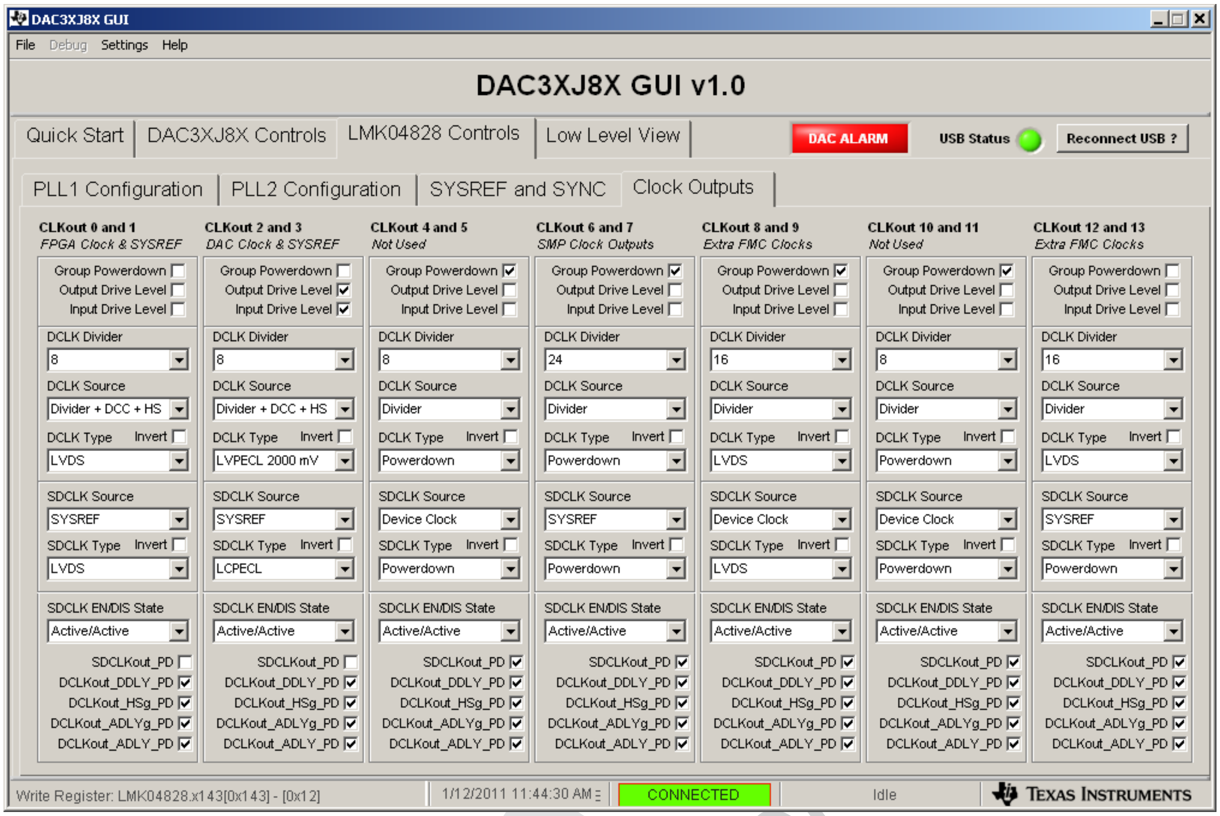
Write Register: DAC3XJ8X.config0[0x0] - [0x18]
1/12/2011 11:44:30 AM
CONNECTED
Idle

Figure 9. LMK04828 Clock Outputs Menu

Since the DAC Clock is 368.64 MHz, to provide a REFCLK of 368.64 MHz, change the *DCLK Divider* for *CLKout 0* to “8”.

To generate a Core clock of 184.32 MHz, set the *DCLK Divider* for *CLKout 12* to “16”. Also, remove the checkmark from the *Group Powerdown* box to enable this output.

The *Clock Outputs* menu is now as shown in Figure 10.



	CLKout 0 and 1 *FPGA Clock & SYSREF*	**CLKout 2 and 3** *DAC Clock & SYSREF*	**CLKout 4 and 5** *Not Used*	**CLKout 6 and 7** *SMP Clock Outputs*	**CLKout 8 and 9** *Extra FMC Clocks*	**CLKout 10 and 11** *Not Used*	**CLKout 12 and 13** *Extra FMC Clocks*
Group Powerdown	☐	☐	☑	☑	☑	☑	☐
Output Drive Level	☐	☑	☐	☐	☐	☐	☐
Input Drive Level	☐	☑	☐	☐	☐	☐	☐
DCLK Divider	8	8	8	24	16	8	16
DCLK Source	Divider + DCC + HS	Divider + DCC + HS	Divider	Divider	Divider	Divider	Divider
DCLK Type	LVDS	LVPECL 2000 mV	Powerdown	Powerdown	LVDS	Powerdown	LVDS
DCLK Invert	☐	☐	☐	☐	☐	☐	☐
SDCLK Source	SYSREF	SYSREF	Device Clock	SYSREF	Device Clock	Device Clock	SYSREF
SDCLK Type	LVDS	LCPECL	Powerdown	Powerdown	LVDS	Powerdown	Powerdown
SDCLK Invert	☐	☐	☐	☐	☐	☐	☐
SDCLK EN/DIS State	Active/Active	Active/Active	Active/Active	Active/Active	Active/Active	Active/Active	Active/Active
SDCLKout_PD	☐	☐	☑	☑	☑	☑	☑
DCLKout_DDLY_PD	☑	☑	☑	☑	☑	☑	☑
DCLKout_HSg_PD	☑	☑	☑	☑	☑	☑	☑
DCLKout_ADLYg_PD	☑	☑	☑	☑	☑	☑	☑
DCLKout_ADLY_PD	☑	☑	☑	☑	☑	☑	☑

Write Register: LMK04828.x143[0x143] - [0x12]

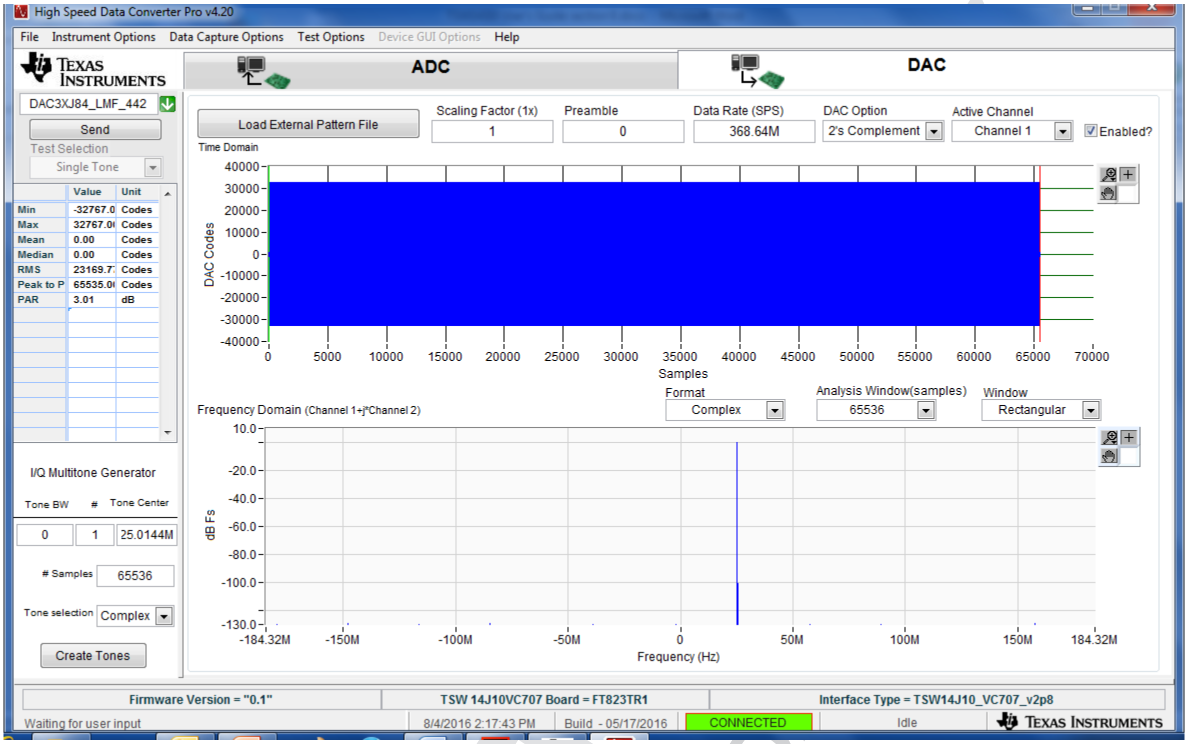
1/12/2011 11:44:30 AM

CONNECTED

Idle

Figure 10. LMK04828 Clock Outputs Menu

Open HSDC Pro GUI, select the *DAC* tab, then select *DAC3XJ84_LMF_442* in the device button. After the firmware is loaded, enter 368.64M in the *Data Rate (SPS)* window, select 2's Complement in the *DAC Option* window and generate a 10-MHz test tone using the *IQ Multitone Generator* located in the lower left of the GUI. Click on the *Create Tones* button. The display looks as shown in Figure 11.



High Speed Data Converter Pro v4.20

DAC3XJ84_LMF_442

Test Selection: Single Tone

	Value	Unit
Min	-32767.0	Codes
Max	32767.0	Codes
Mean	0.00	Codes
Median	0.00	Codes
RMS	23169.7	Codes
Peak to P	65535.0	Codes
PAR	3.01	dB

Scaling Factor (1x): 1

Preamble: 0

Data Rate (SPS): 368.64M

DAC Option: 2's Complement

Active Channel: Channel 1

☑ Enabled?

I/Q Multitone Generator

Tone BW: 0

#: 1

Tone Center: 25.0144M

Samples: 65536

Tone selection: Complex

Format: Complex

Analysis Window(samples): 65536

Window: Rectangular

Firmware Version = "0.1"

TSW 14J10VC707 Board = FT823TR1

Interface Type = TSW14J10_VC707_v2p8

Waiting for user input

8/4/2016 2:17:43 PM

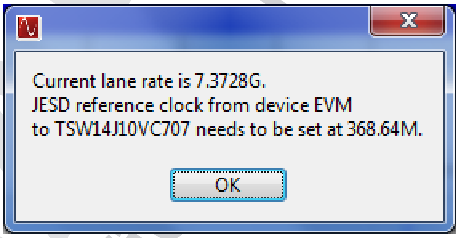
Build - 05/17/2016

CONNECTED

Idle

Figure 11. HSDC Pro GUI

Click the *Send* button. A new window opens showing the lane rate of the interface and the required frequency of REFCLK, as shown in Figure 12.



Current lane rate is 7.3728G.
JESD reference clock from device EVM
to TSW14J10VC707 needs to be set at 368.64M.

Figure 12. HSDC Pro GUI: Lane Rate and REFCLK Settings

Go back to the DAC GUI *Quick Start* tab and click the *Reset DAC JESD Core* button. Click on *Trigger LMK04828 SYSREF*.

There should now be a 10-MHz tone present at all four DAC EVM outputs.

Revision History

Changes from A Revision (October 2014) to B Revision	Page
• Updated *DAC38J84EVM GUI Setup Example* section.	16

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Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265