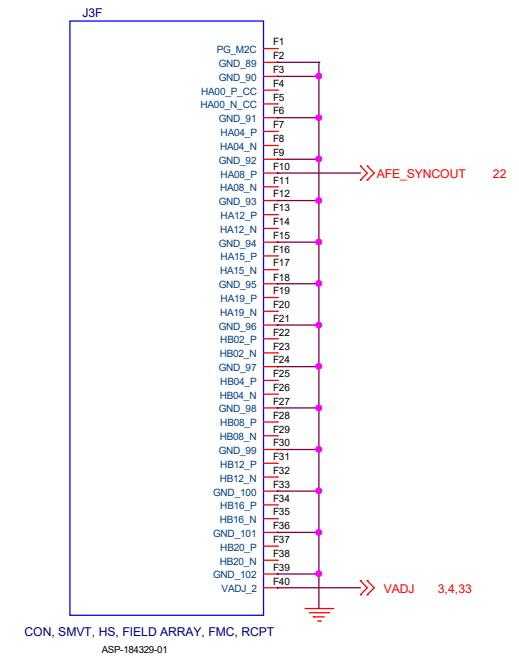
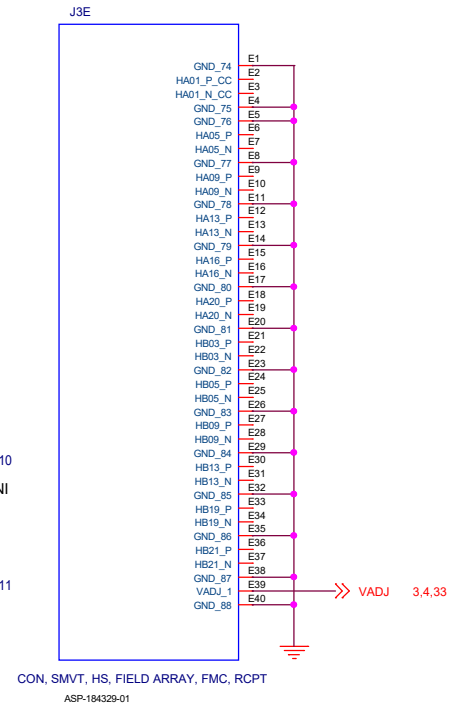
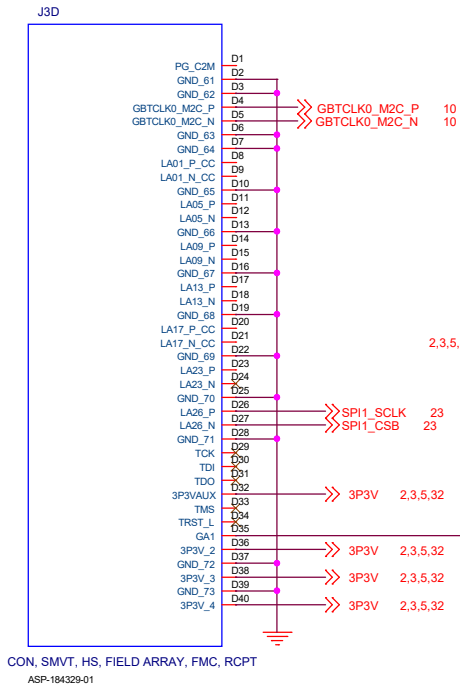


FMC CONNECTOR

TEXAS INSTRUMENTS

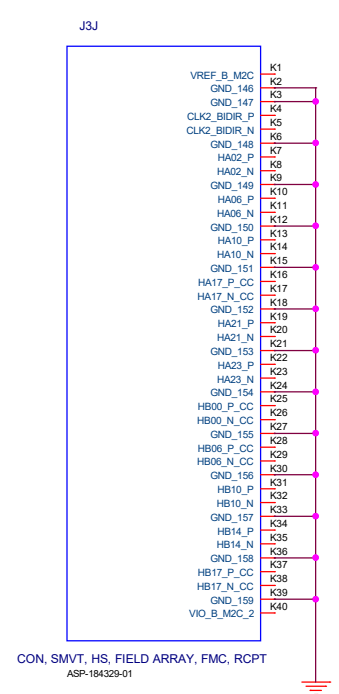
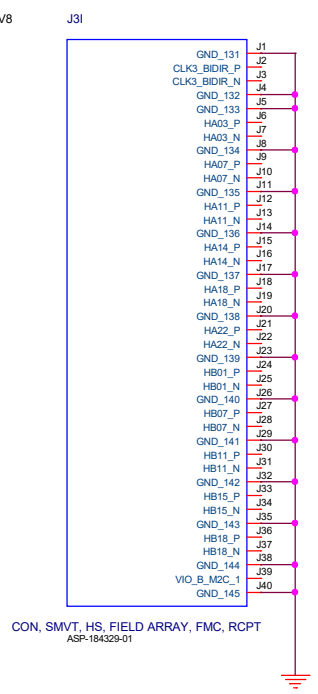
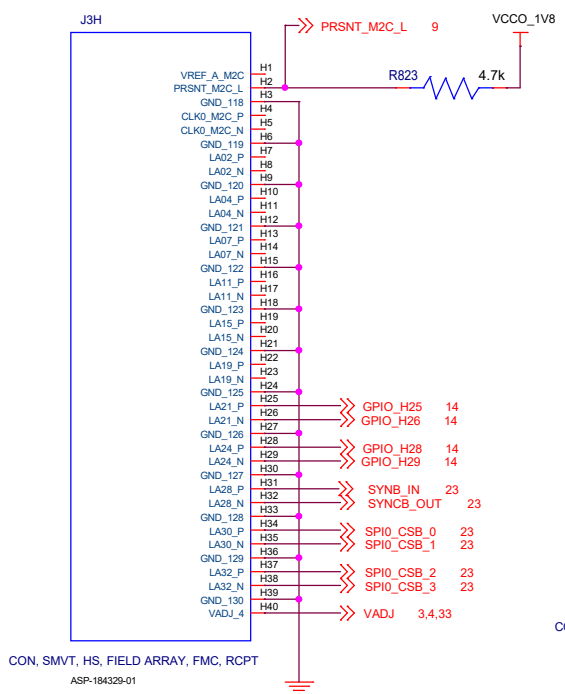
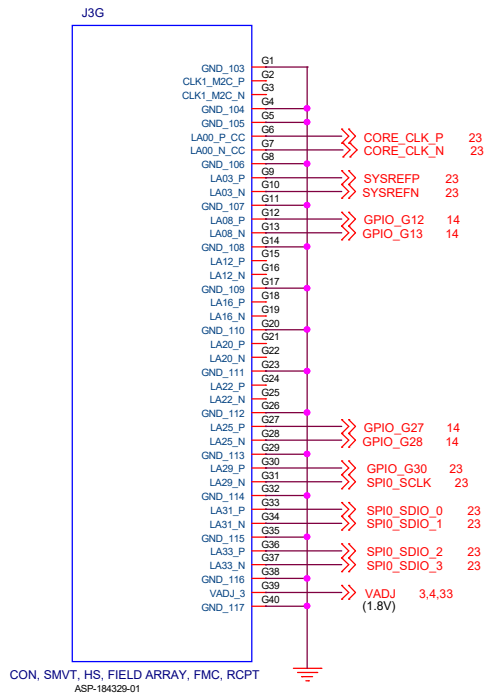
Title		
Size	Document Number	Rev
B	TSW14J58EVM	B
Date:	Friday, August 21, 2020	Sheet 2 of 36



FMC CONNECTOR

TEXAS INSTRUMENTS

Title		
Size	Document Number	Rev
	TSW14J58EVM	B
Date:	Friday, August 21, 2020	Sheet 3 of 38



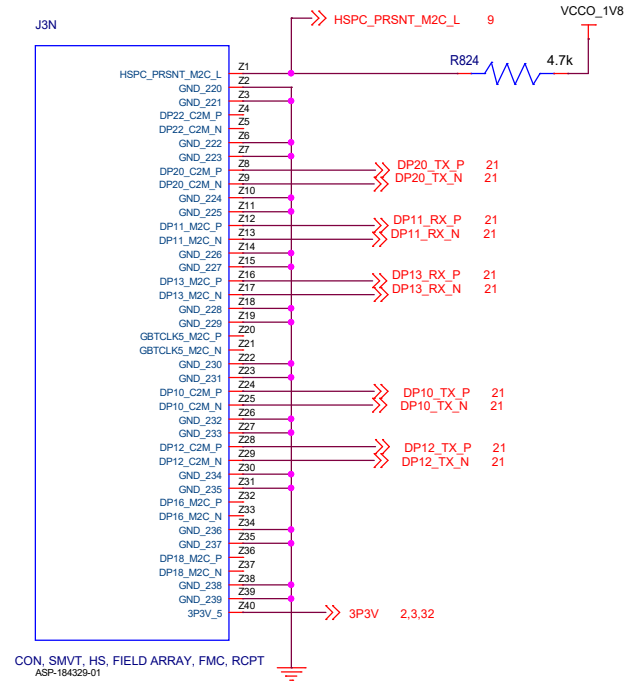
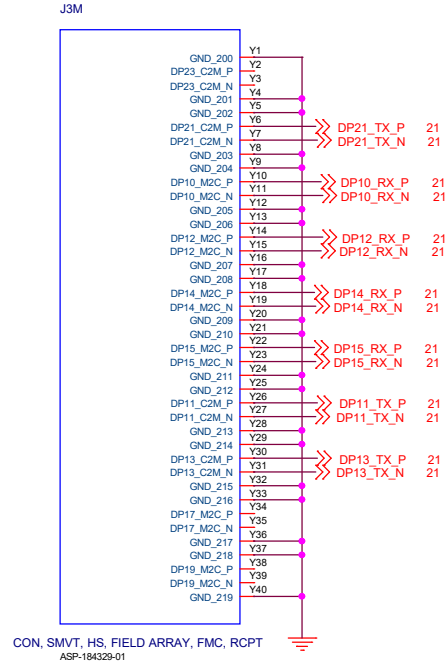
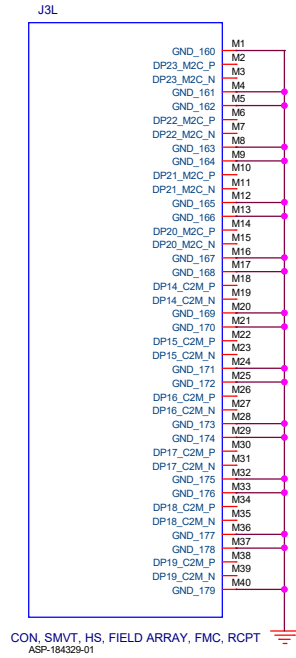
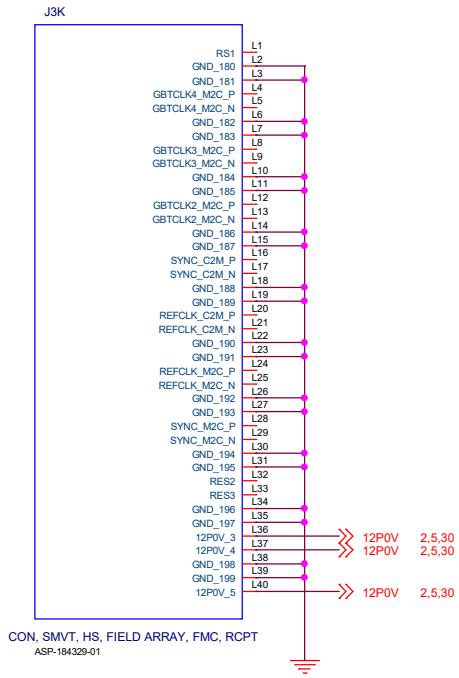
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Size B	Document Number TSW14J58EVM	Rev B
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Date: Friday, August 21, 2020 Sheet 4 of 36

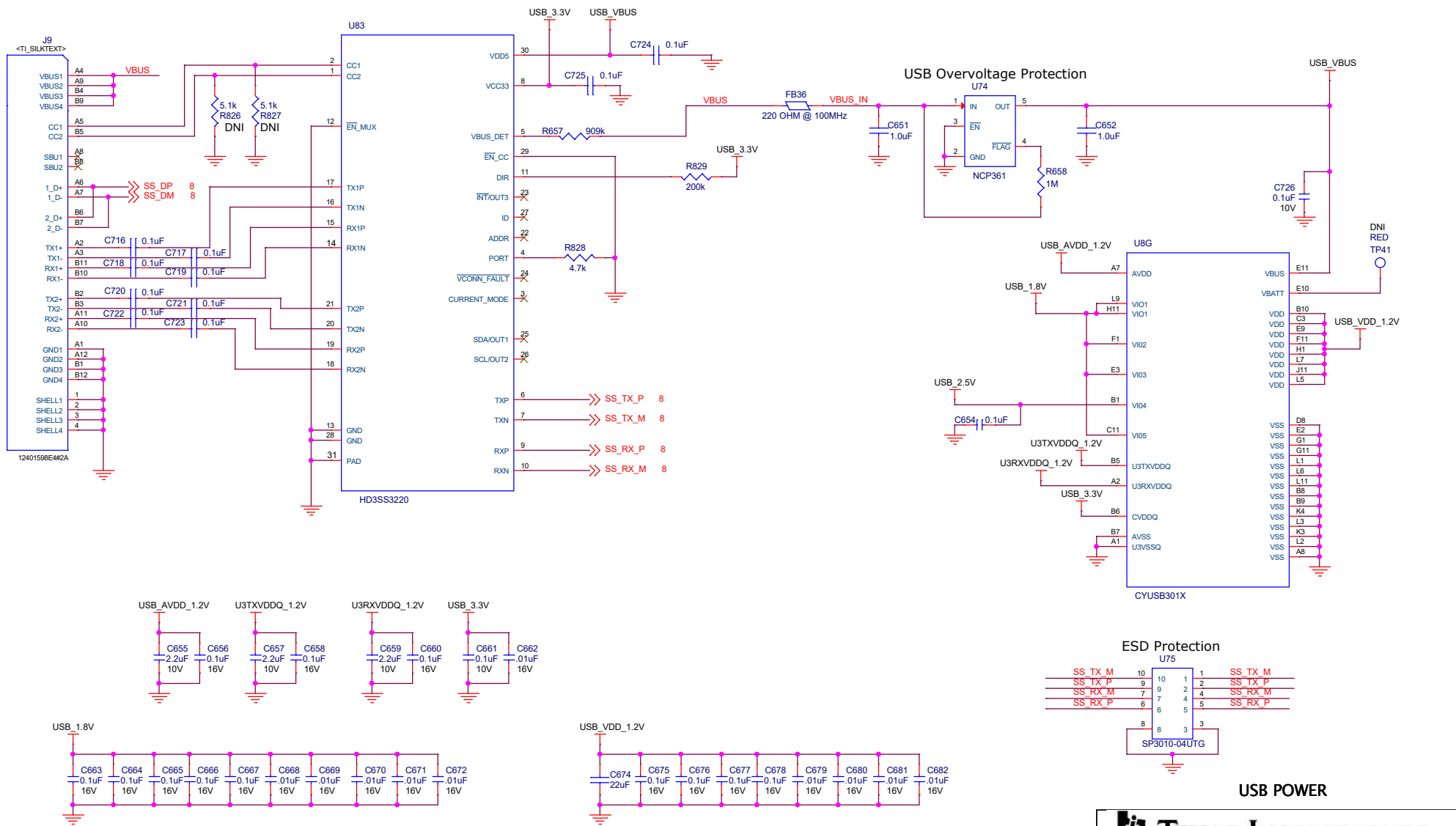


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TEXAS INSTRUMENTS

Title

Size B	Document Number TSW14J58EVM	Rev B
Date: Friday, August 21, 2020	Sheet 5 of 36	



USB POWER

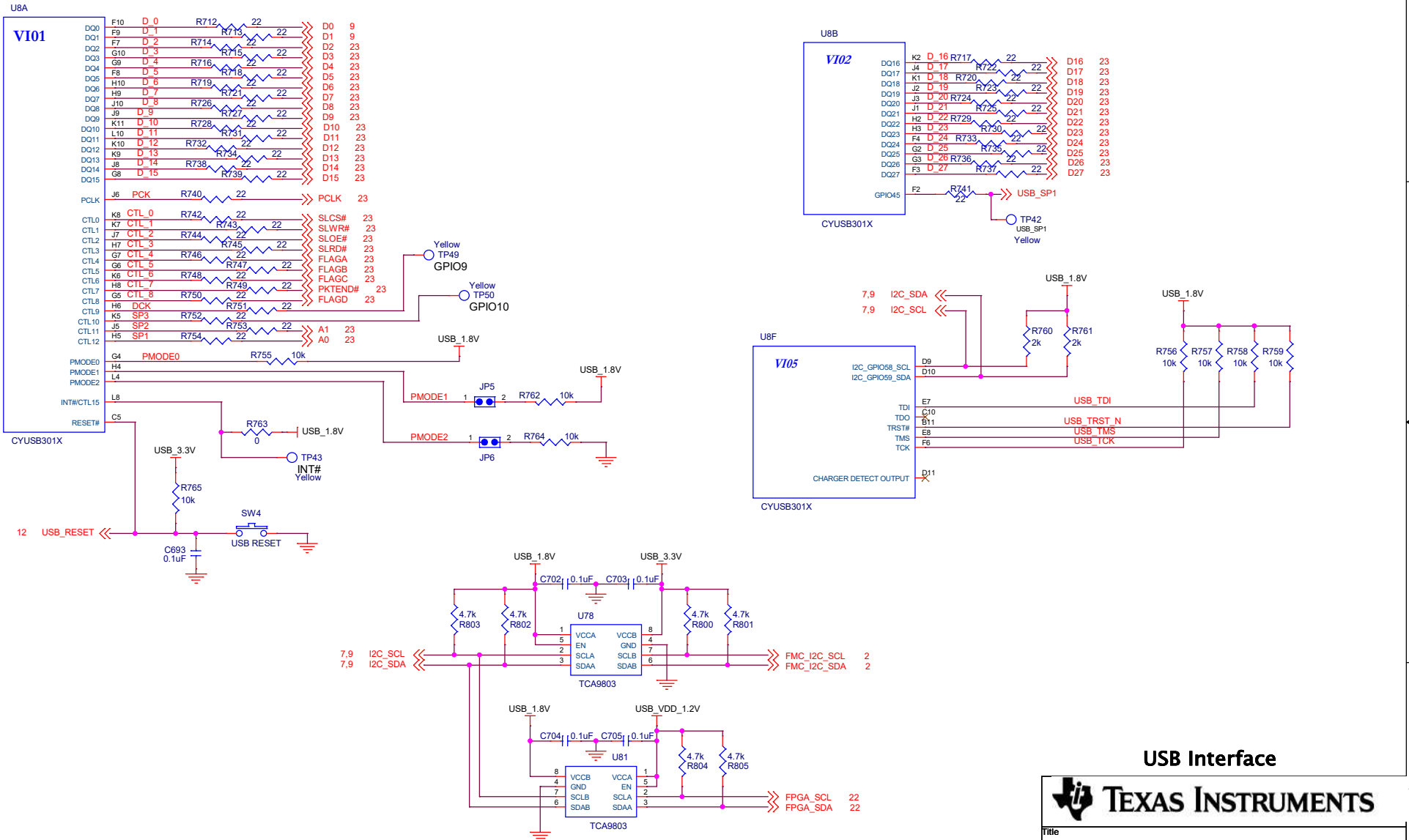
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Title

Size B Document Number **TSW14J58EVM** Rev B

Date: Friday, August 21, 2020 Sheet 6 of 36

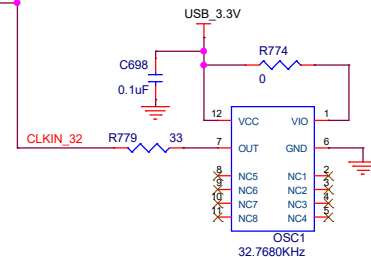
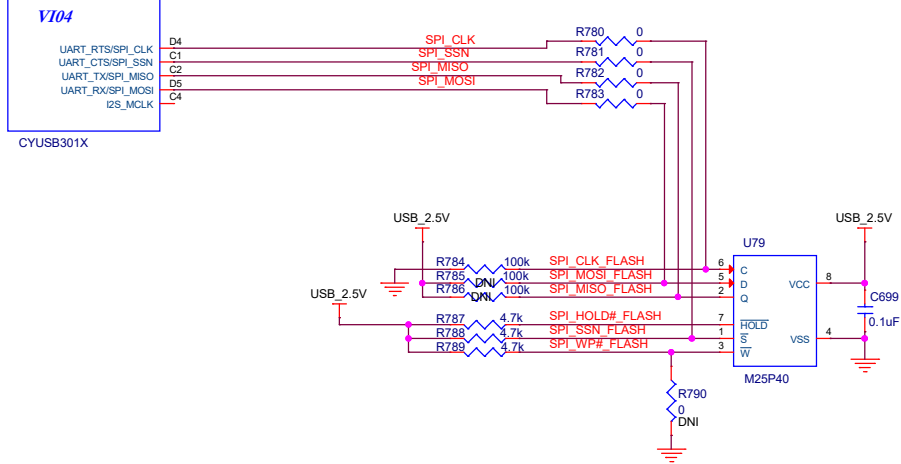
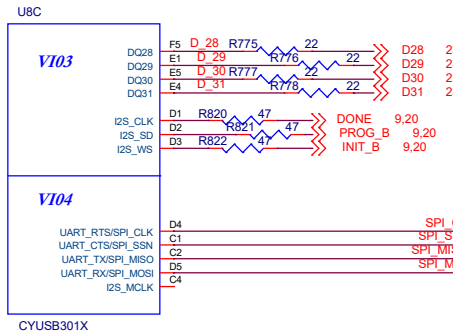
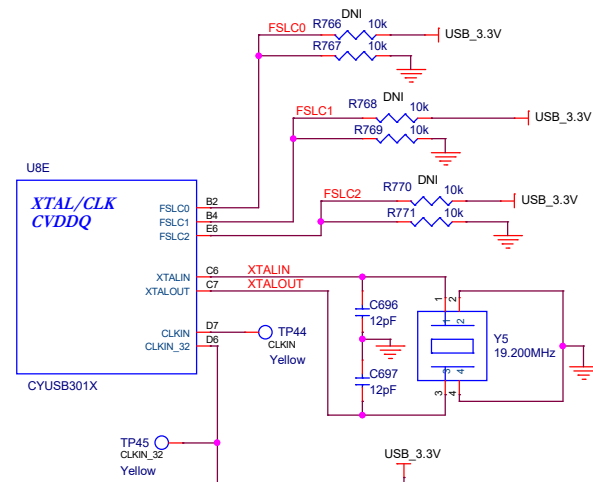
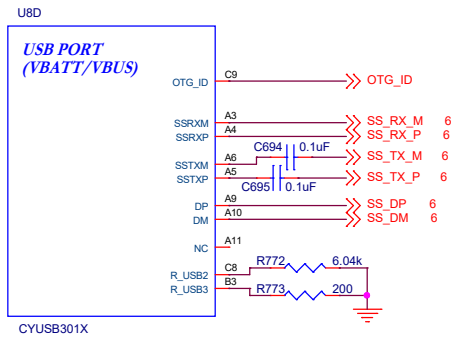
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USB Interface



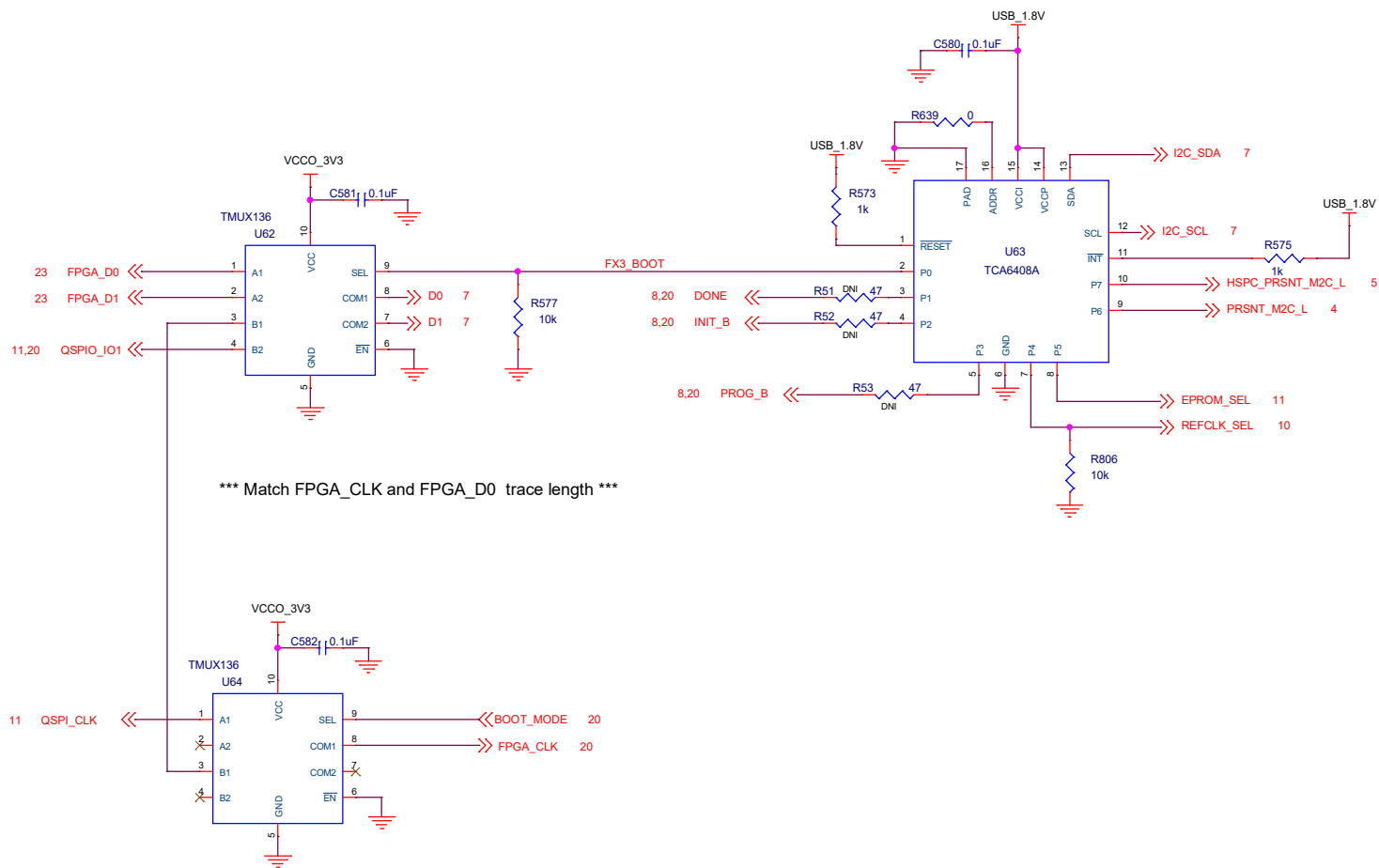
Title		
Size B	Document Number	Rev B
TSW14J58EVM		
Date:	Friday, August 21, 2020	Sheet 7 of 36



USB



Title		
Size B	Document Number	Rev B
TWS14J58EVM		
Date: Friday, August 21, 2020	Sheet 8 of 38	

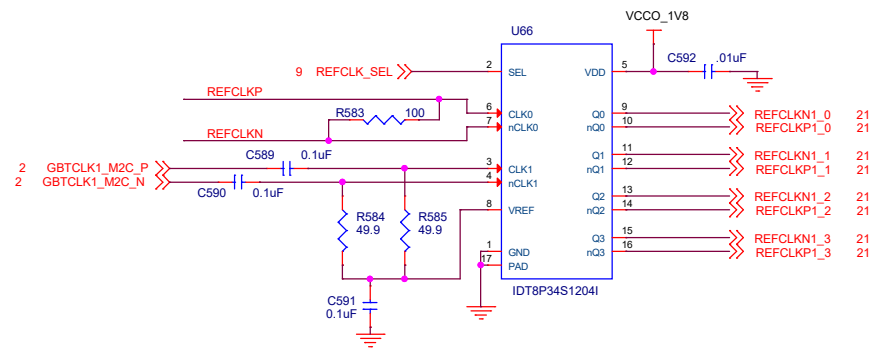
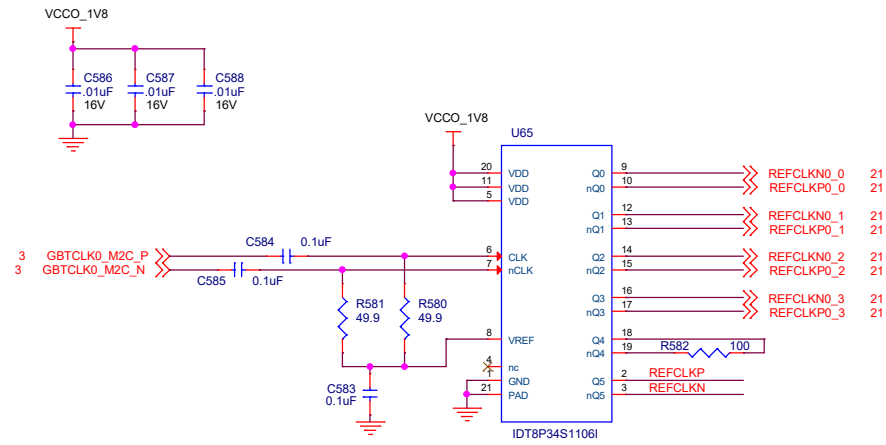


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TEXAS INSTRUMENTS

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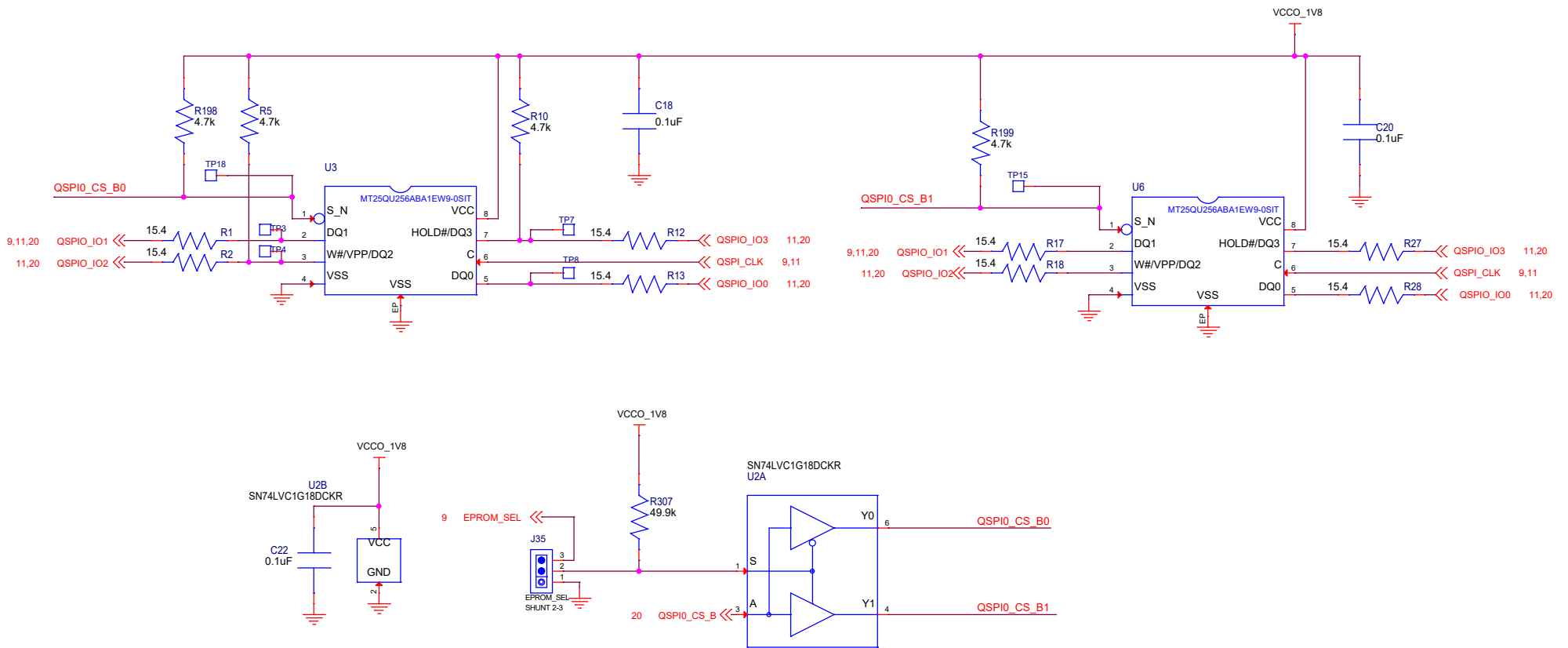
Size B	Document Number TSW14J58EVM	Rev B
Date: Friday, August 21, 2020	Sheet 9	of 36




CLOCK FANOUT

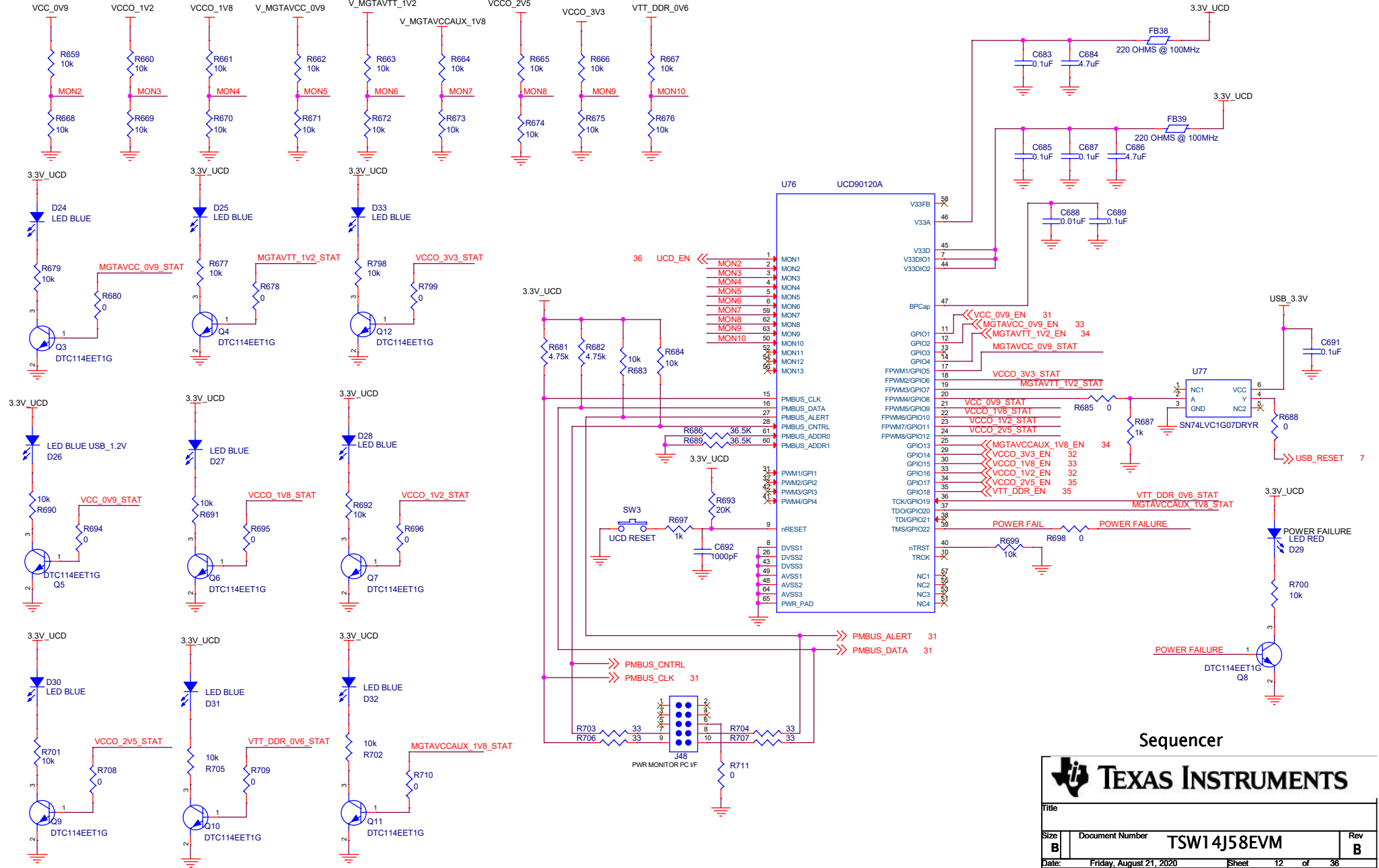


Title		
Size	Document Number	Rev
B	TSW14J58EVM	B
Date:	Friday, August 21, 2020	Sheet 10 of 38



PGM FLASH

 TEXAS INSTRUMENTS		
Title		
Size B	Document Number TSW14J58EVM	Rev B
Date: Friday, August 21, 2020	Sheet 11	of 36

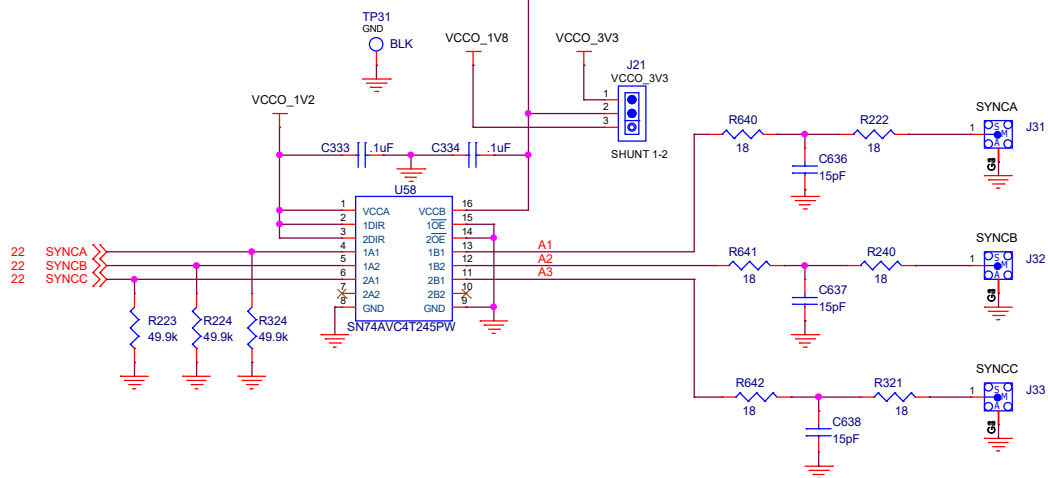
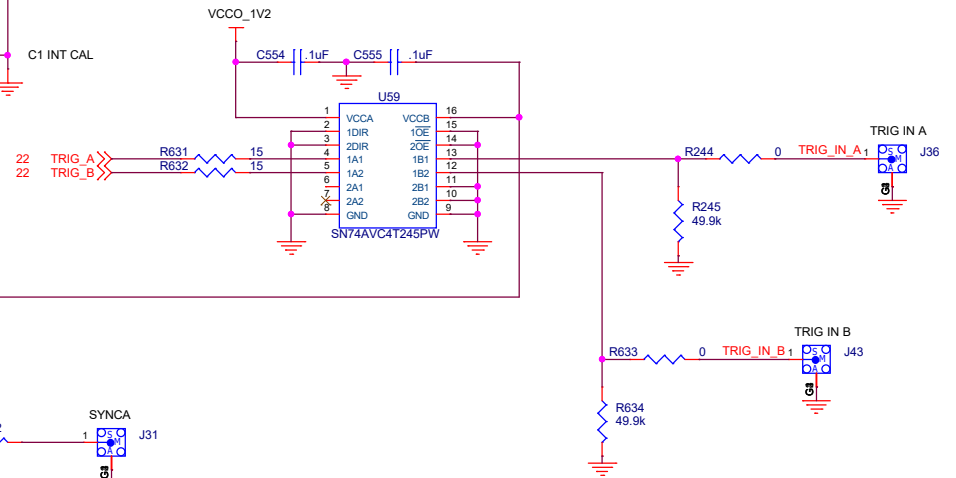
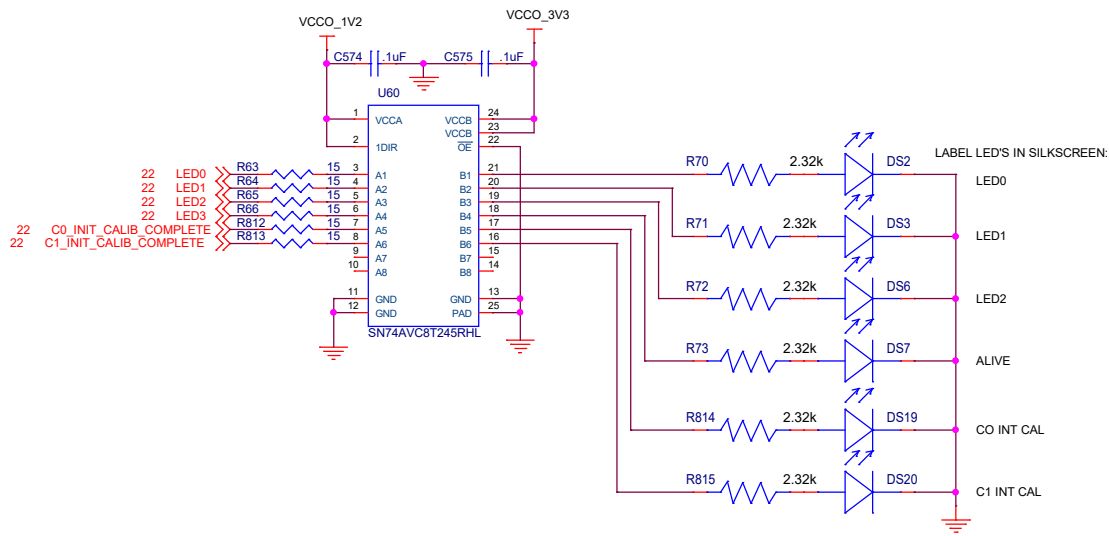


Sequencer

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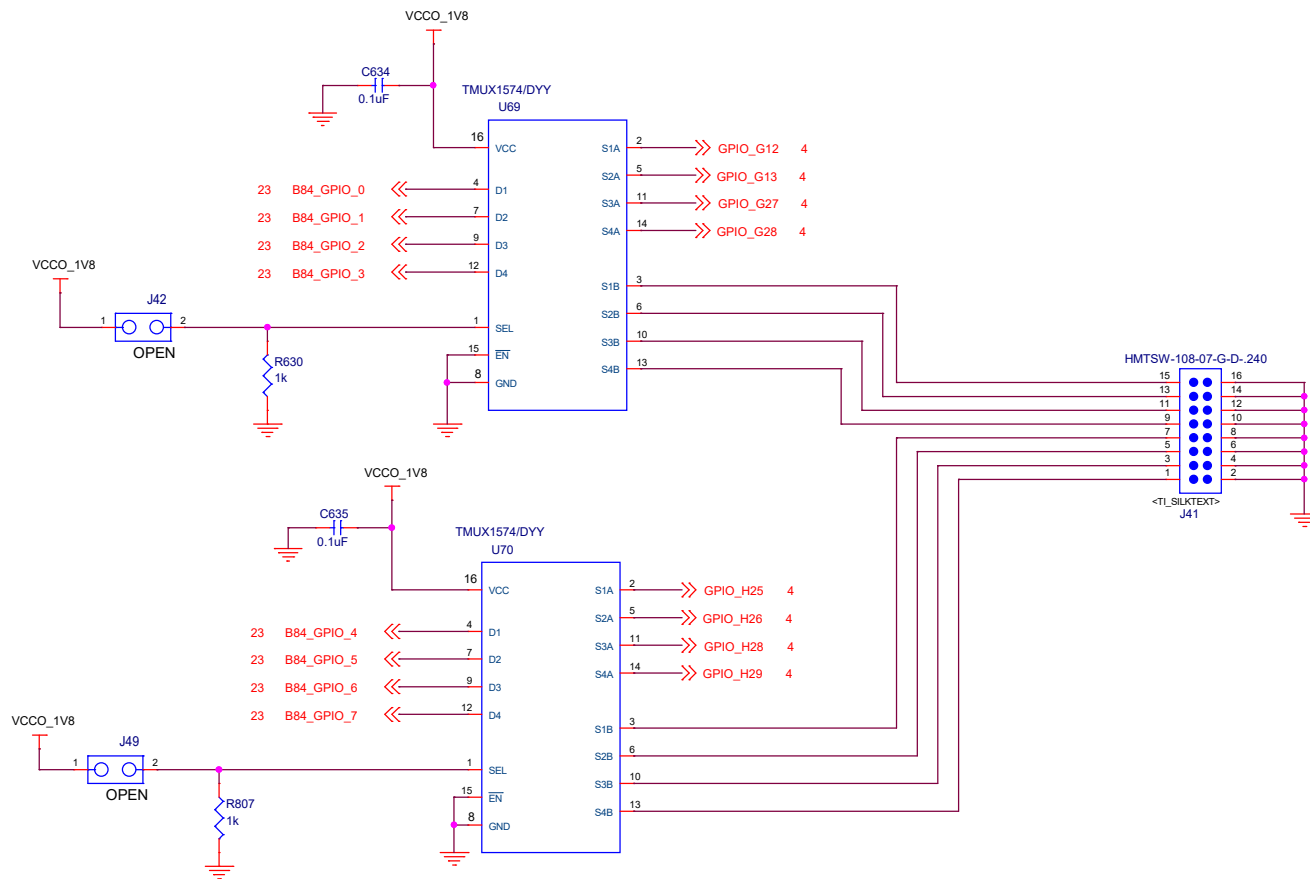
Size: B	Document Number: TSW14J58EVM	Rev: B
Date: Friday, August 21, 2020	Sheet: 12 of 36	

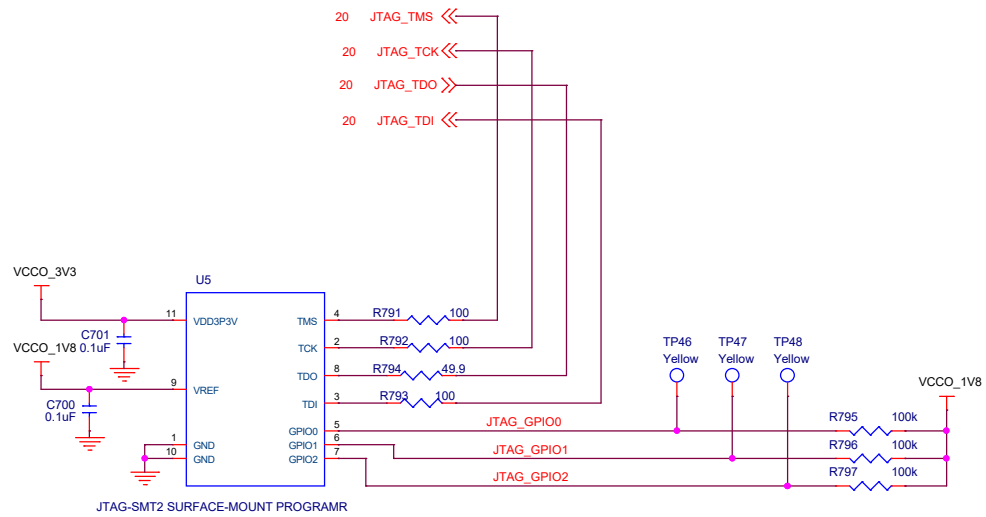


MISC IO



Title		
Size	Document Number	Rev
B	TSW14J58EVM	B
Date:	Monday, August 24, 2020	Sheet 13 of 38

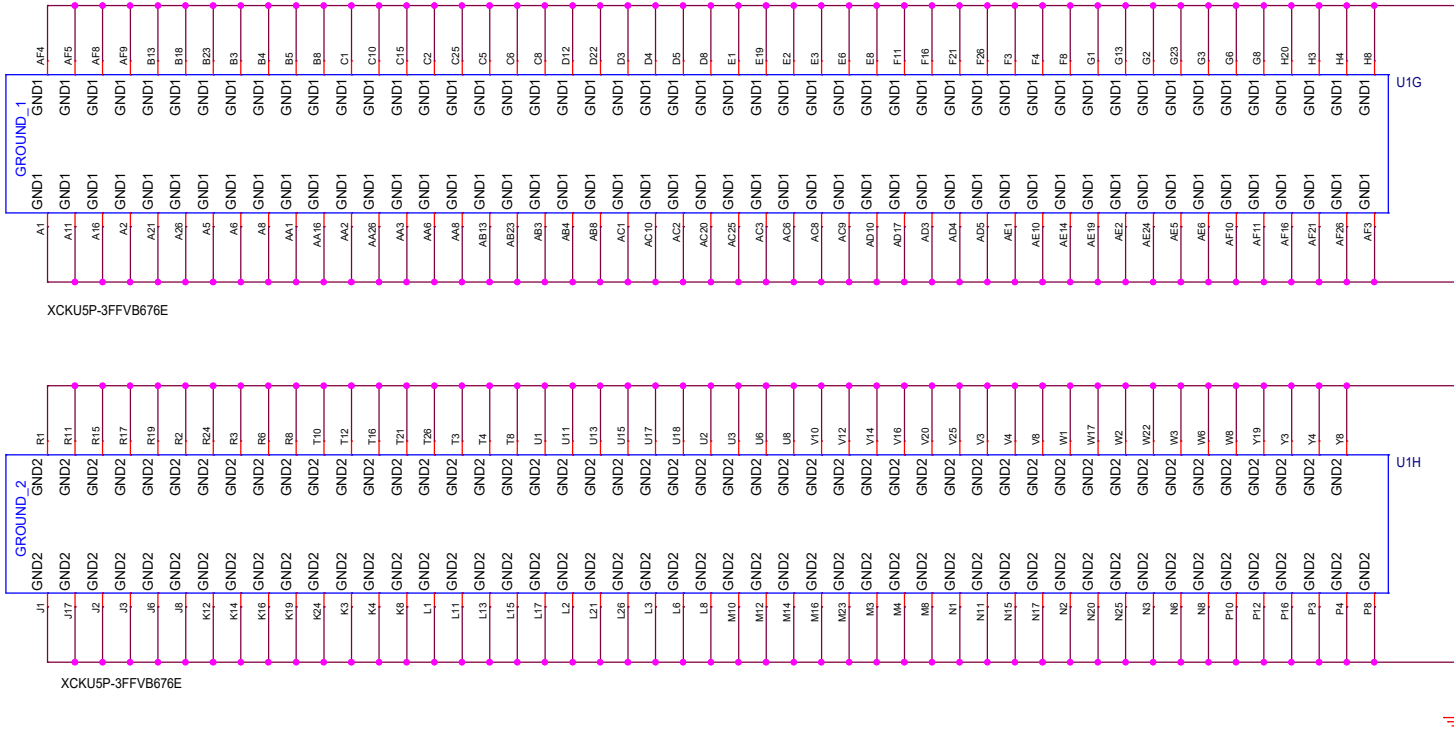




POWER SUPPLIES




Title		
Size B	Document Number TSW14J58EVM	Rev B
Date:	Friday, August 21, 2020	Sheet 15 of 36

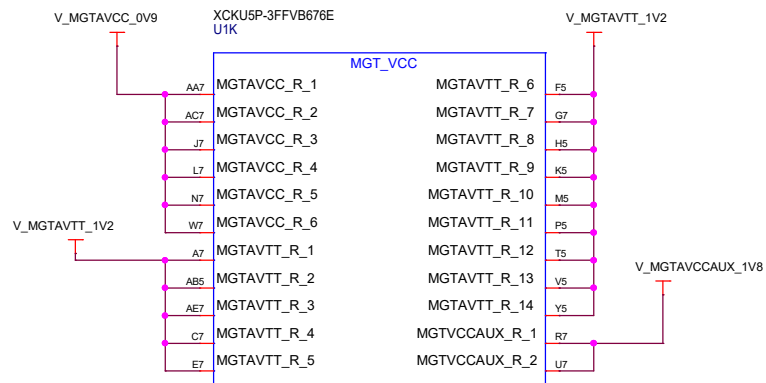
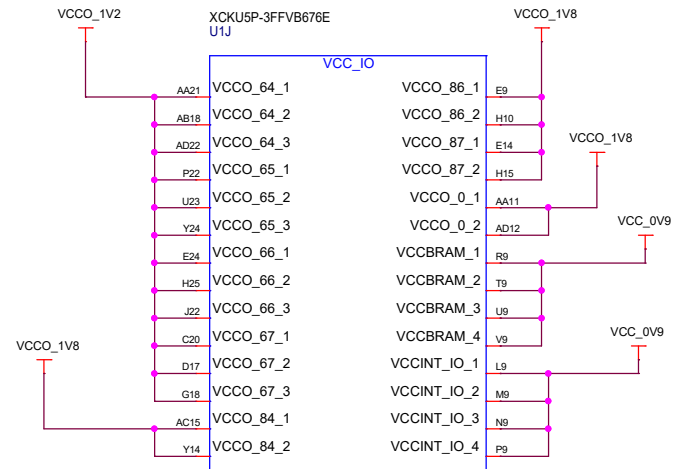
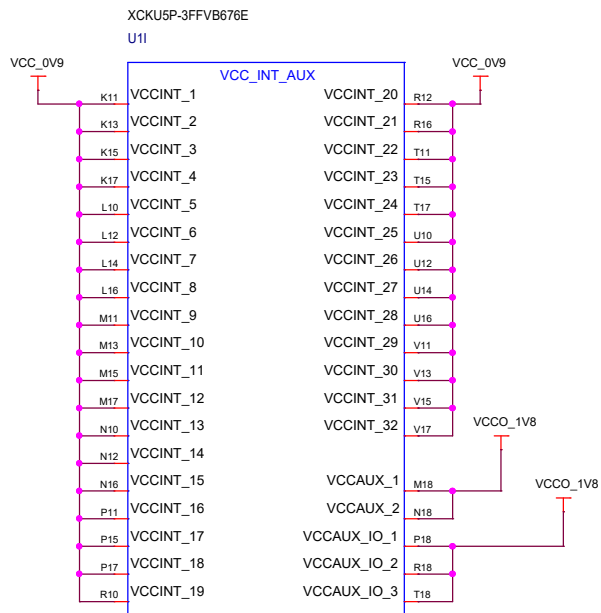


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XCKU5P-3FFVB676E

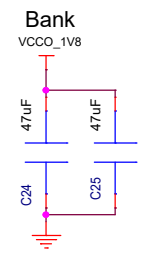
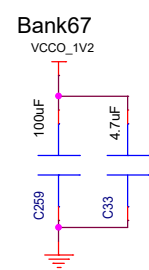
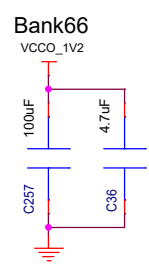
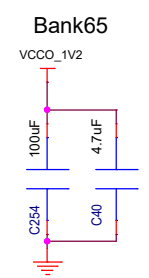
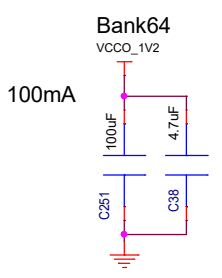
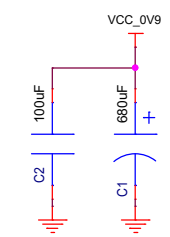
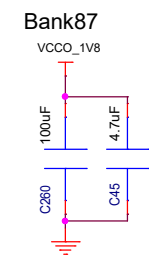
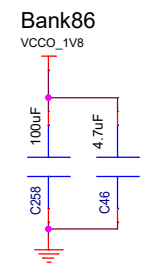
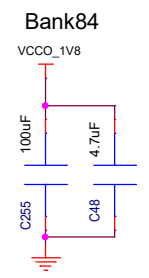
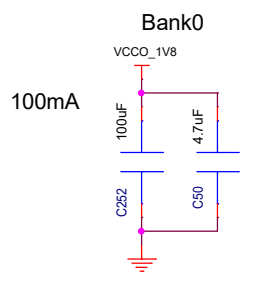
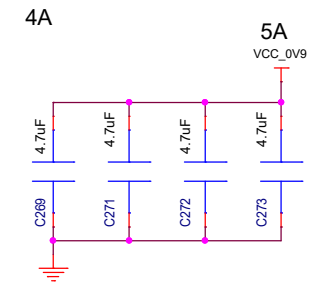
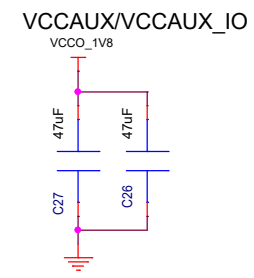
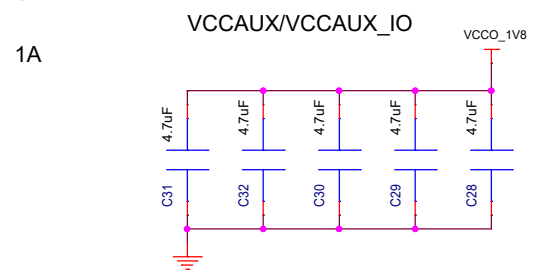
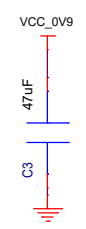
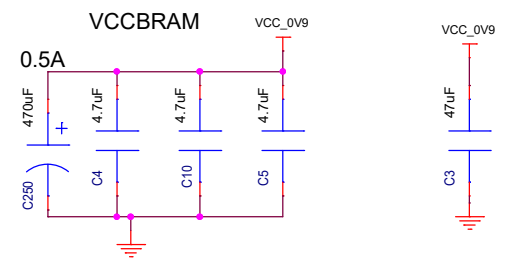
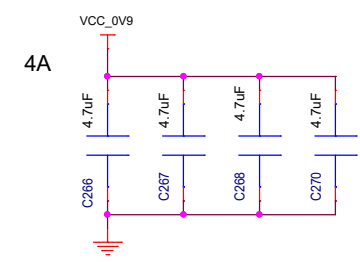
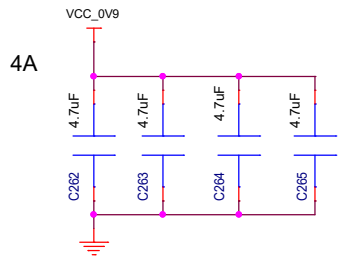
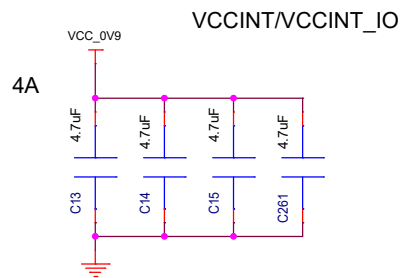
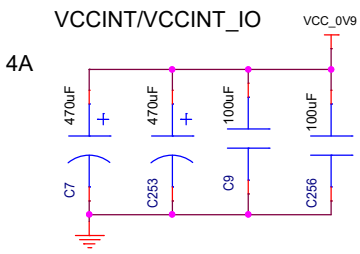
FPGA GND

 TEXAS INSTRUMENTS		
Title		
Size B	Document Number TSW14J58EVM	Rev B
Date: Friday, August 21, 2020	Sheet 16	of 36



FPGA PWR

 TEXAS INSTRUMENTS		
Title		
Size	Document Number	Rev
B	TSW14J58EVM	B
Date:	Friday, August 21, 2020	Sheet 17 of 36

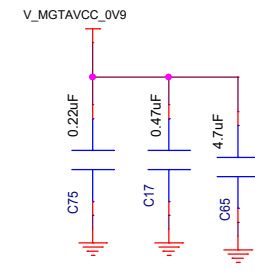
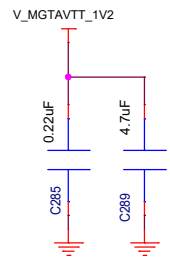
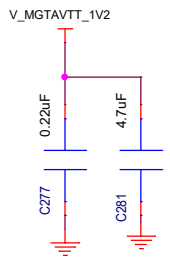
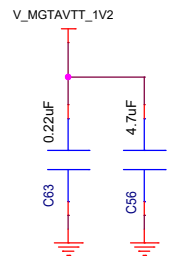
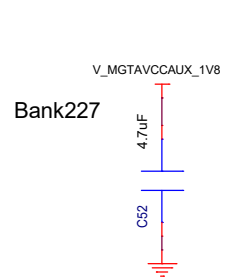
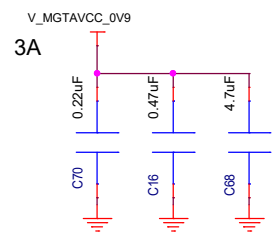
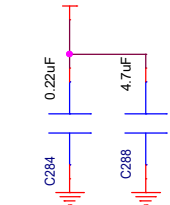
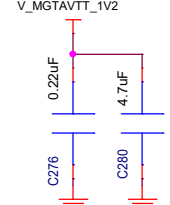
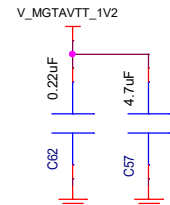
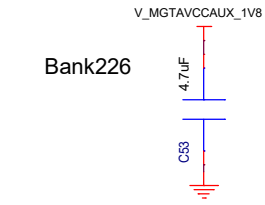
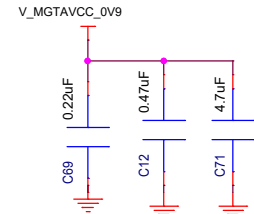
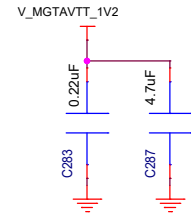
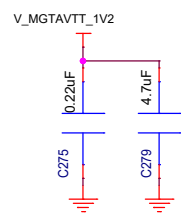
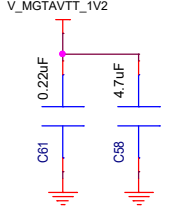
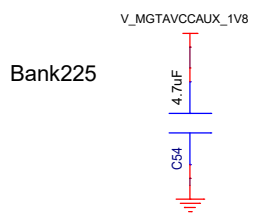
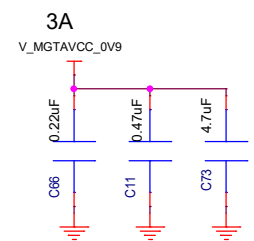
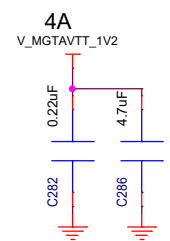
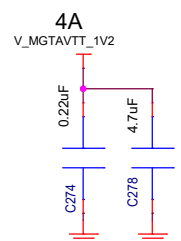
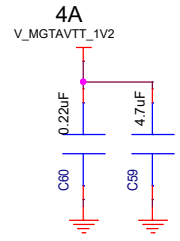
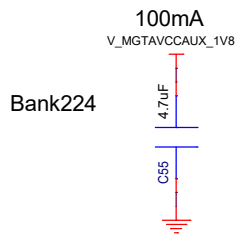


FPGA Decoupling

TEXAS INSTRUMENTS

Title

Size B	Document Number TSW14J58EVM	Rev B
Date: Friday, August 21, 2020	Sheet 18	of 36

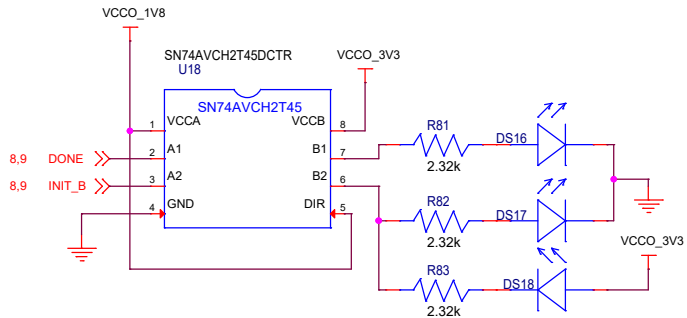
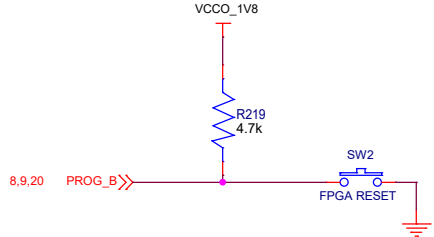
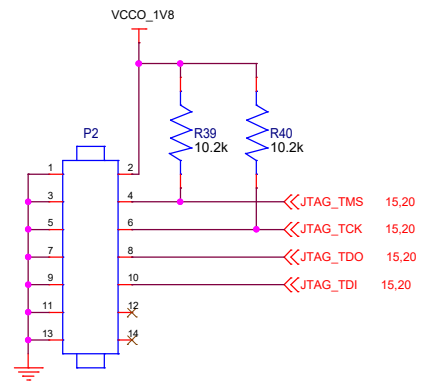
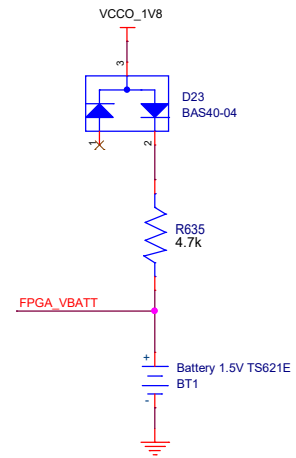
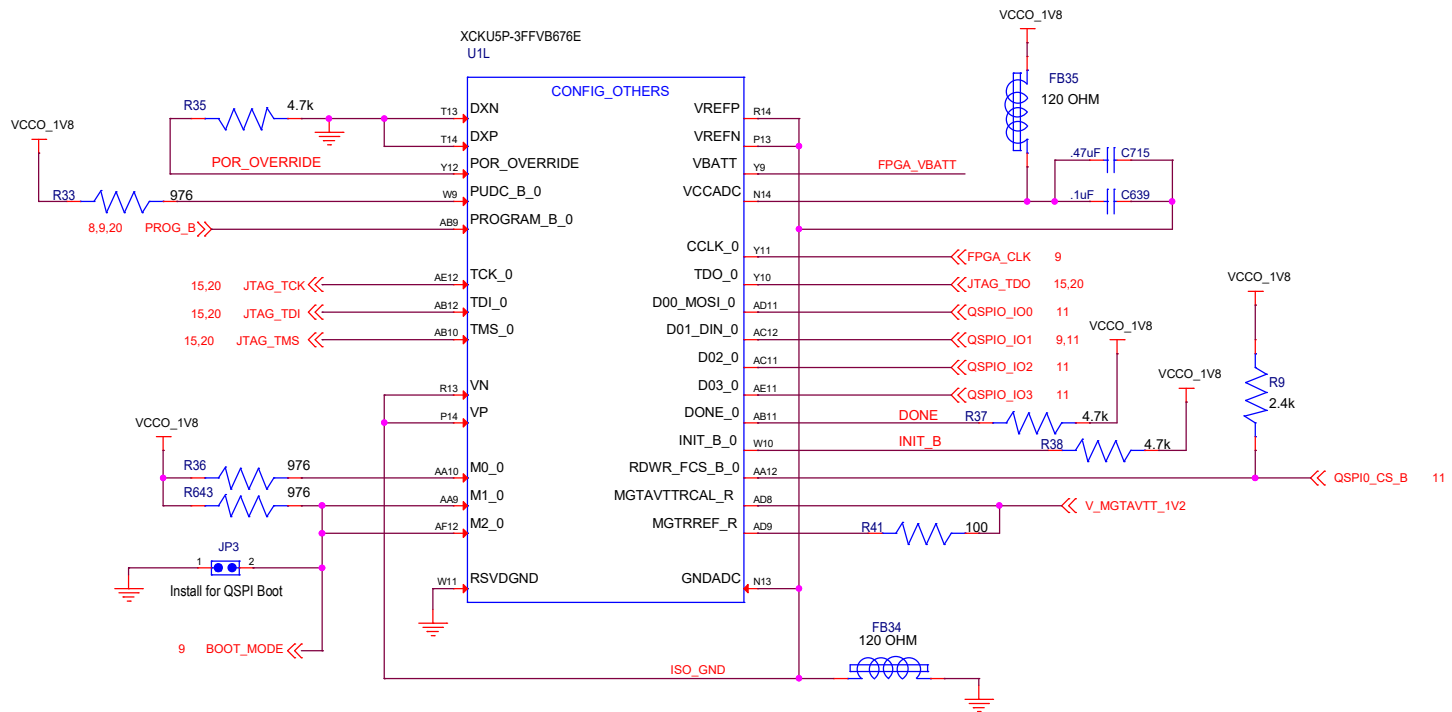


FPGA Decoupling

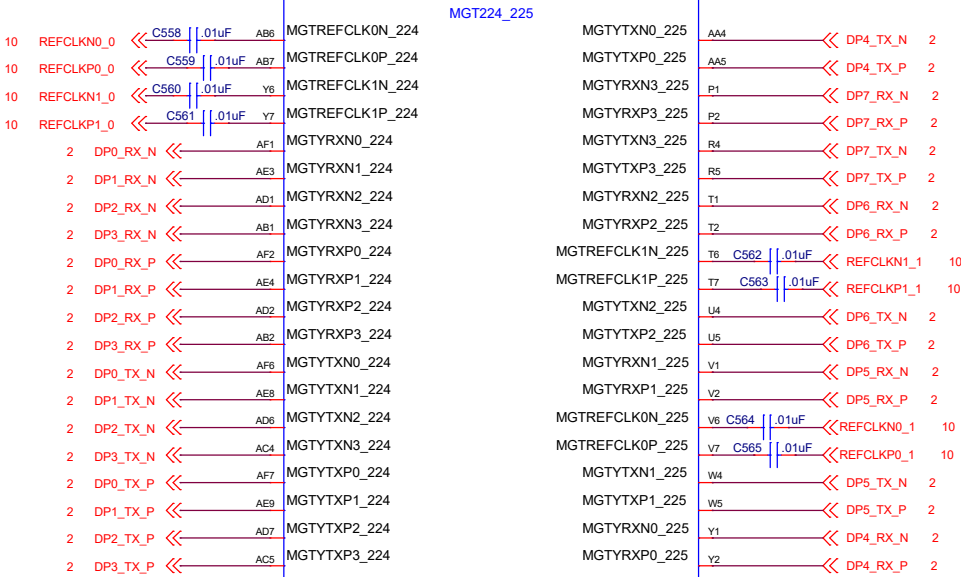
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Title

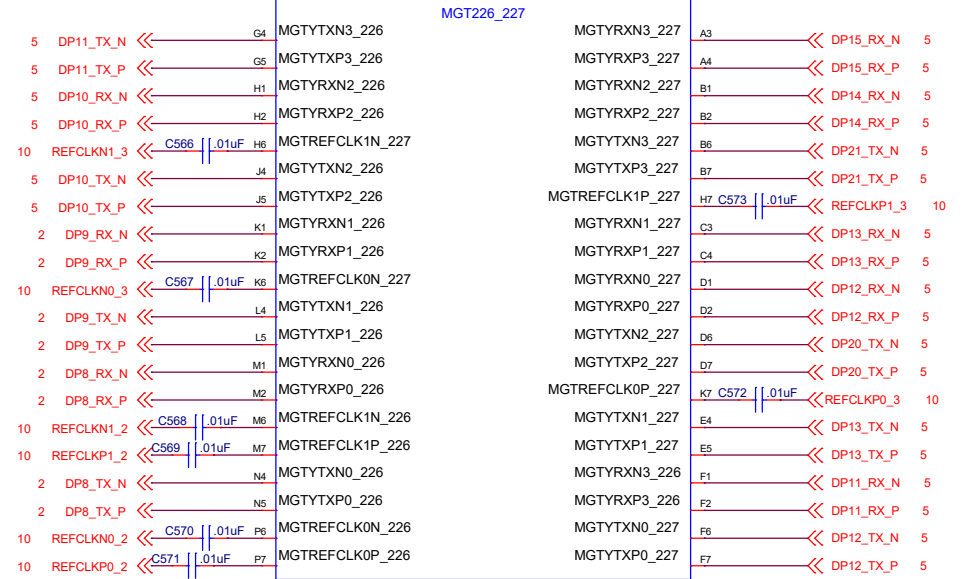
Size B	Document Number TSW14J58EVM	Rev B
Date: Friday, August 21, 2020	Sheet 19 of 36	



XCKU5P-3FFVB676E
U1A



XCKU5P-3FFVB676E
U1B



Ensure Clock and Signals are AC Coupled

FPGA GTY

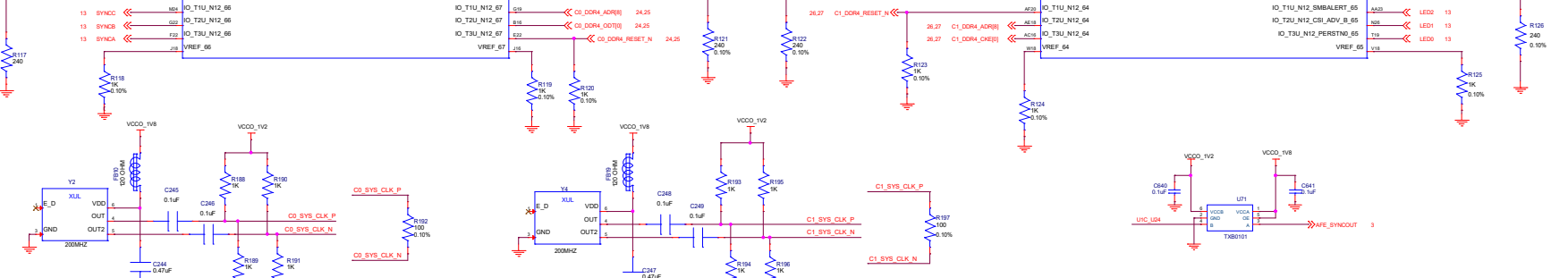


Title		
Size	Document Number	Rev
B	TSW14J58EVM	B
Date:	Friday, August 21, 2020	Sheet 21 of 38

Table listing connections for BANK_06_07, including signals like C0_D00A_D0G_Q0, C0_D00A_D0G_T0, and various IO signals.

Table listing connections for BANK_06_07, including signals like C0_D00A_CK_Q0, C0_D00A_CK_T0, and various IO signals.

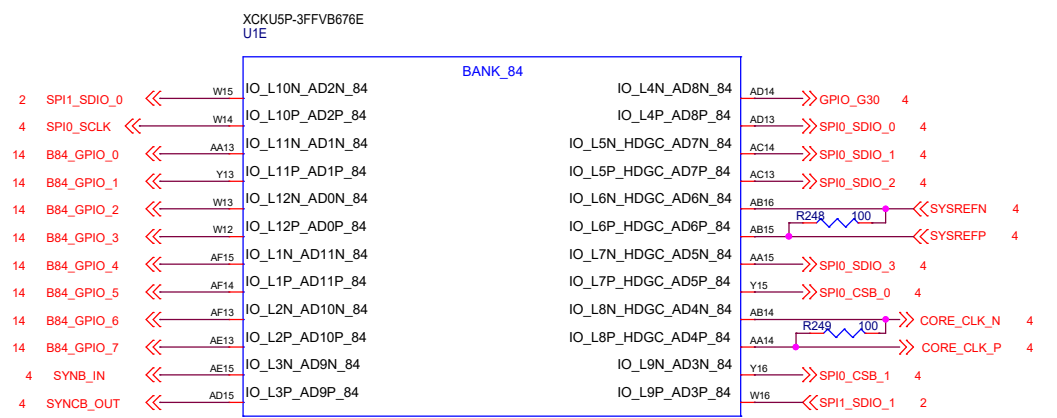
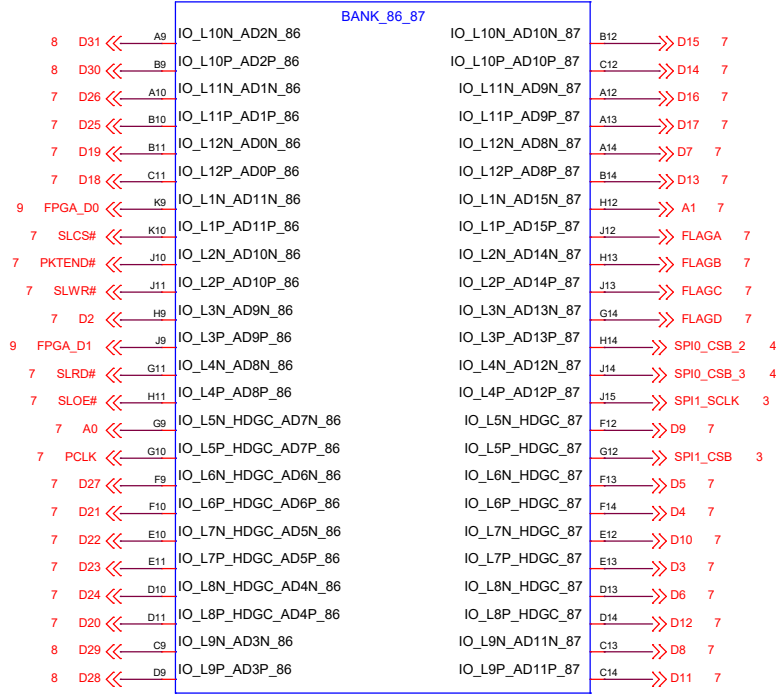
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FPGA DDR BANKS



Table with document information: Document Number TSW14J58EVM, Rev B, Date, and other metadata.



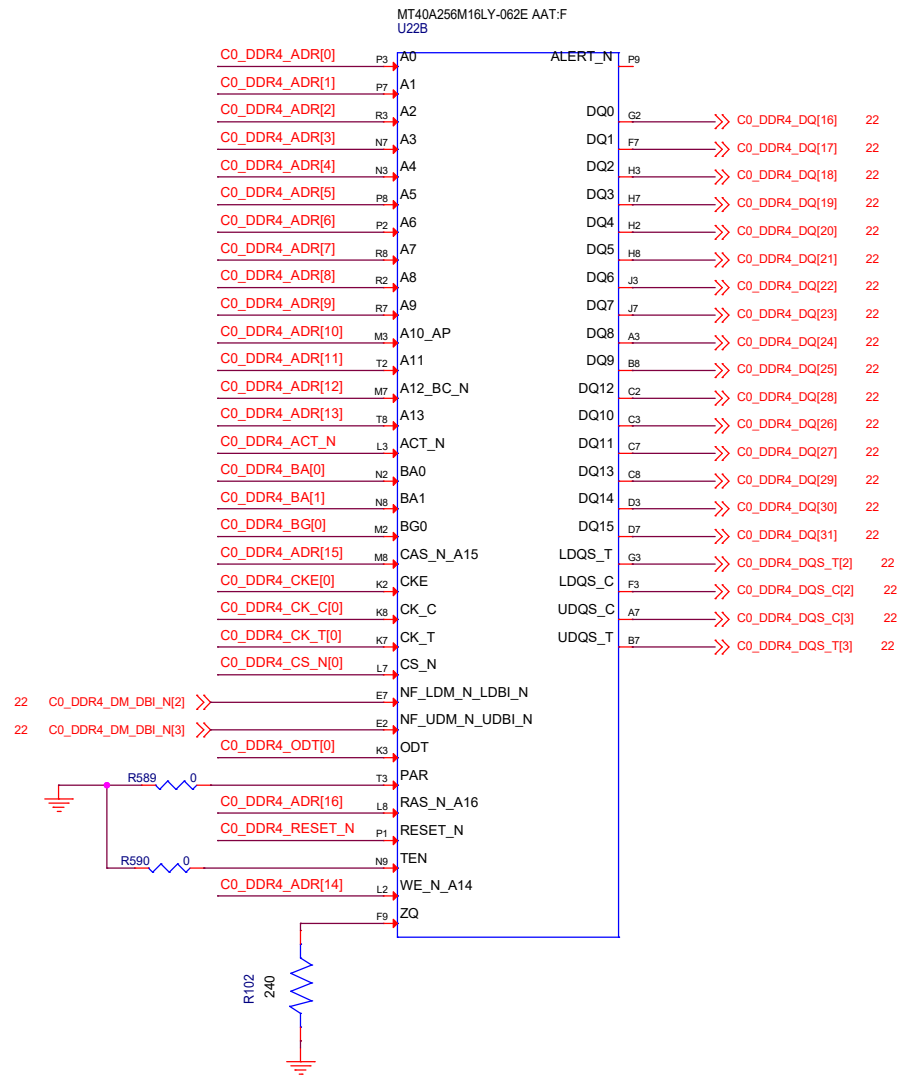
FPGA USB/IO BANK (2.5V Default)



TEXAS INSTRUMENTS

Title

Size	Document Number	Rev
B	TSW14J58EVM	B
Date:	Friday, August 21, 2020	Sheet 23 of 36



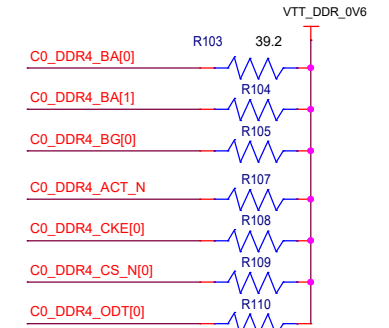
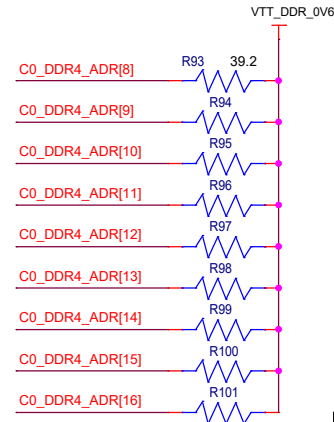
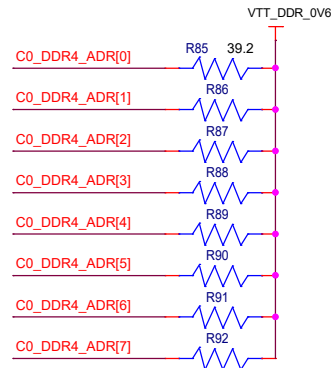
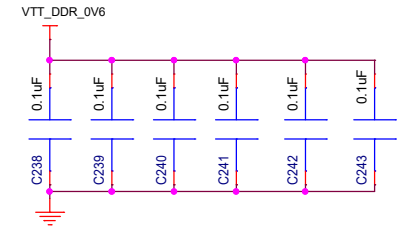
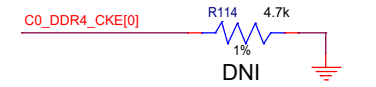
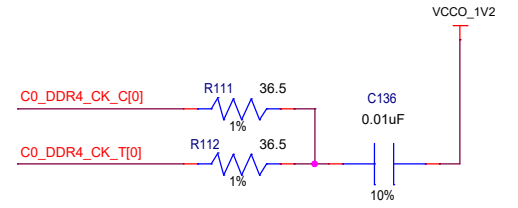
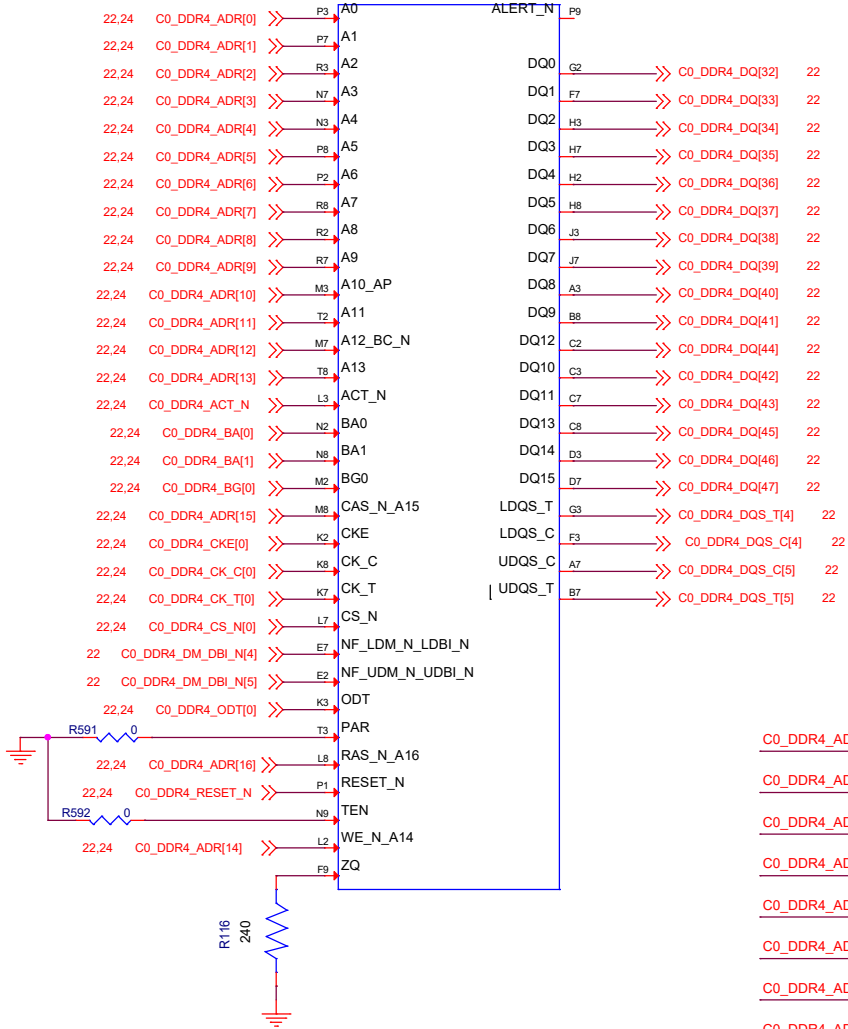
DDR0

TEXAS INSTRUMENTS


Title

Size B	Document Number TSW14J58EVM	Rev B
Date: Monday, August 24, 2020	Sheet 24	of 36

MT40A256M16LY-062E AAT:F
U21B

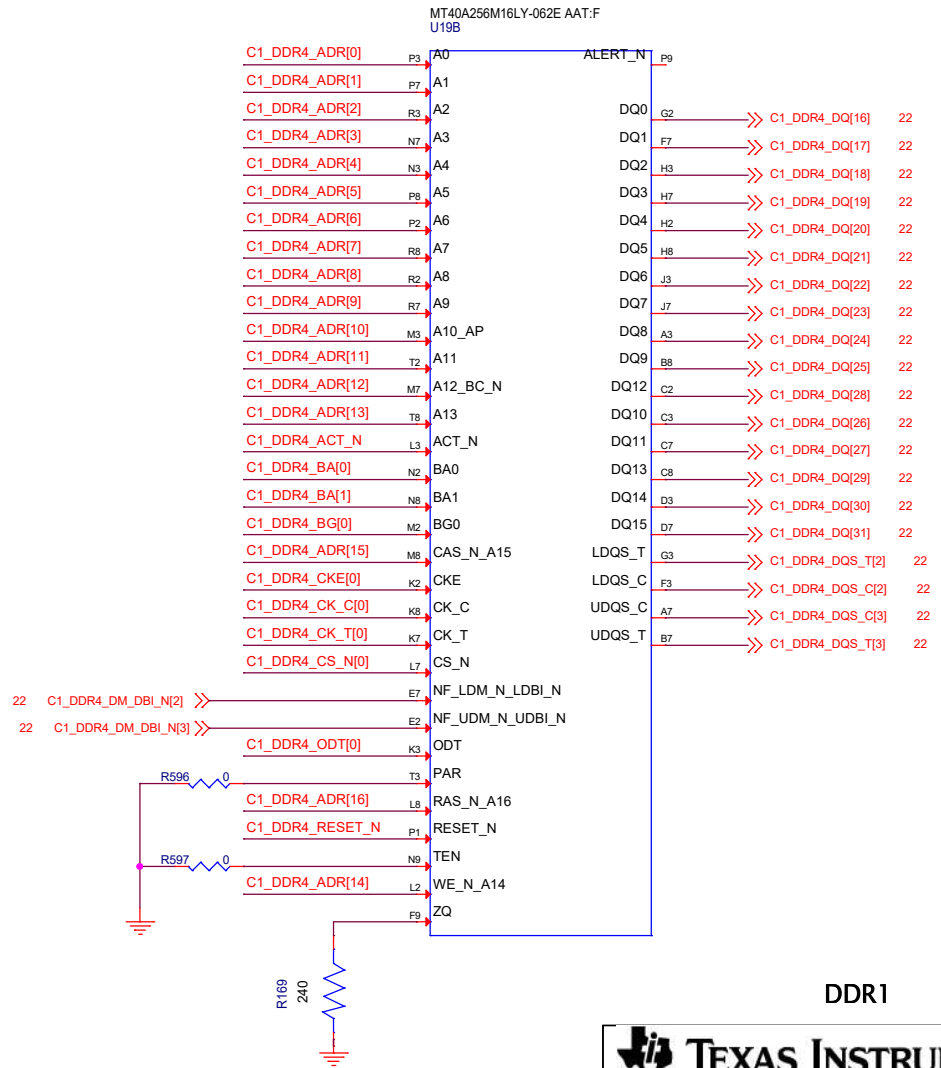
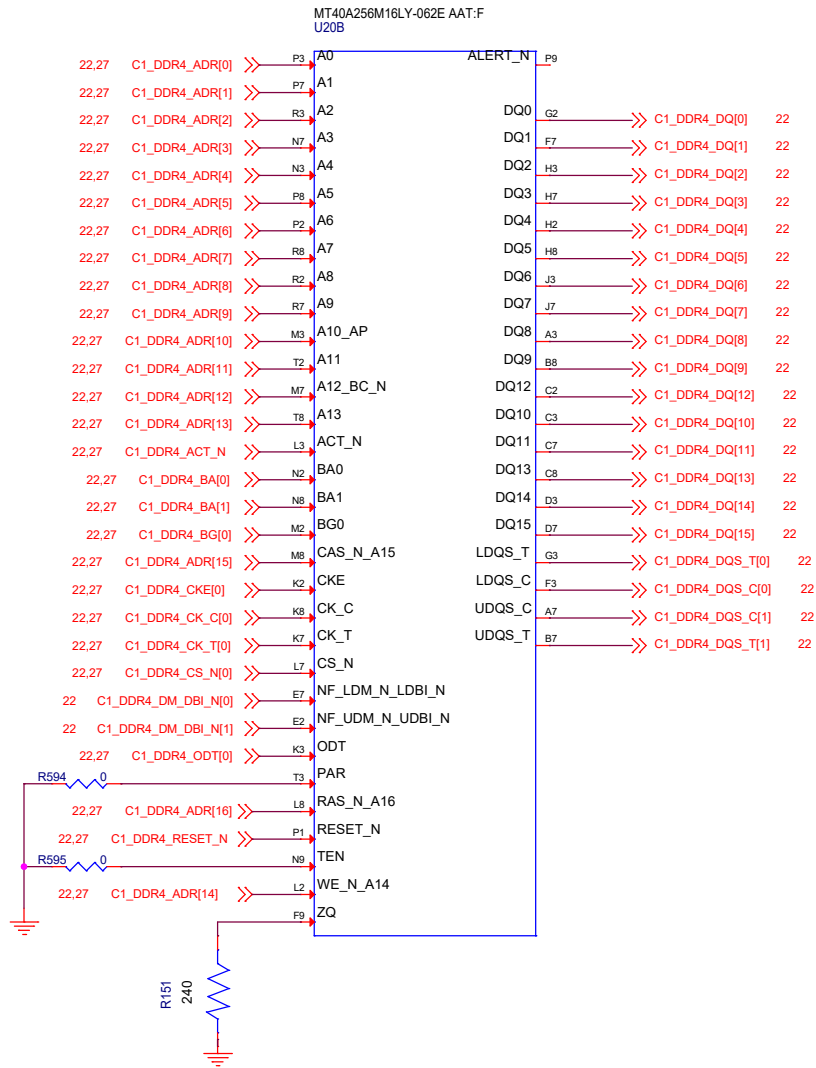


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 **TEXAS INSTRUMENTS**

Title: _____

Size: B	Document Number: TSW14J58EVM	Rev: B
Date: Monday, August 24, 2020	Sheet: 25	of 36

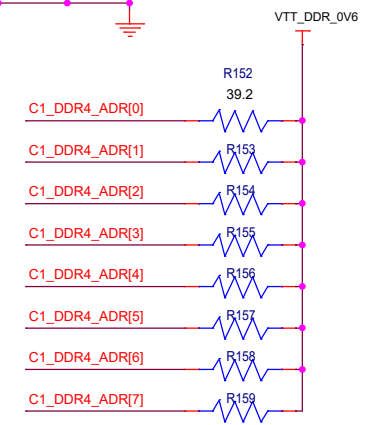
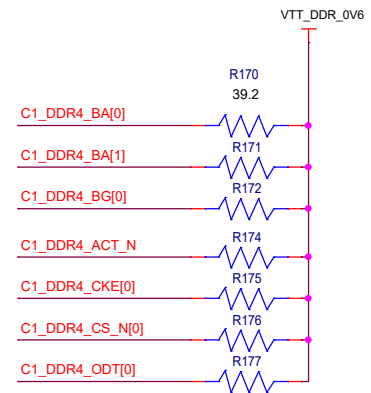
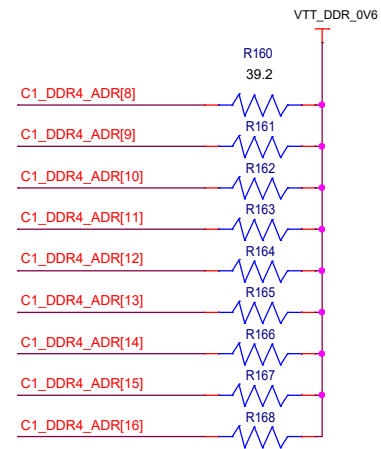
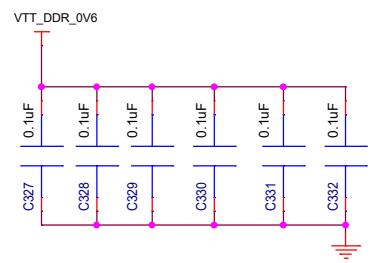
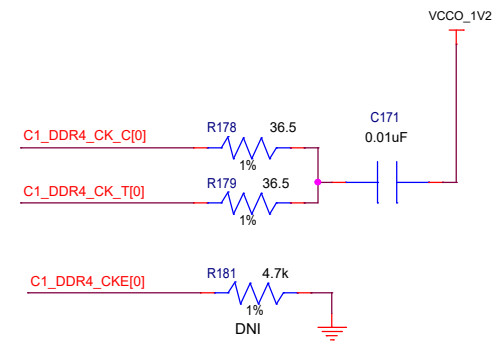
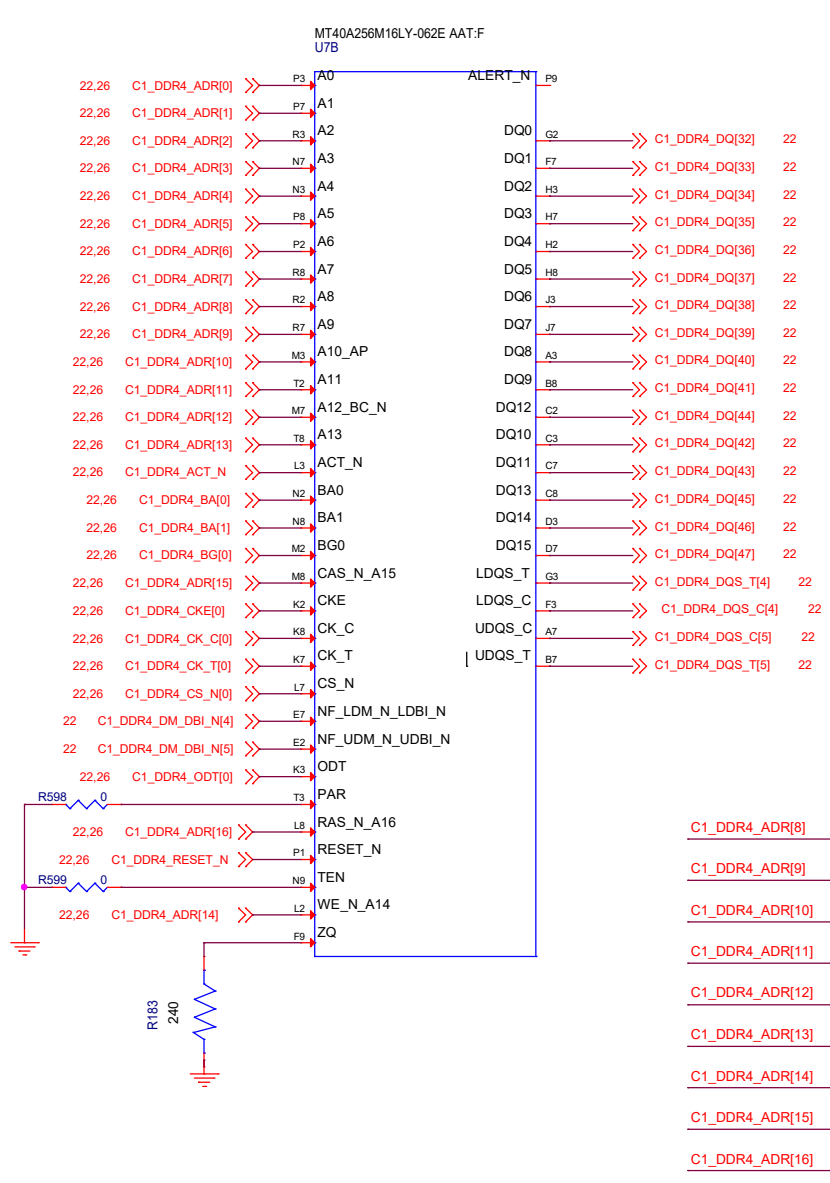


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TEXAS INSTRUMENTS

Title

Size B	Document Number TSW14J58EVM	Rev B
Date: Monday, August 24, 2020	Sheet 26	of 36



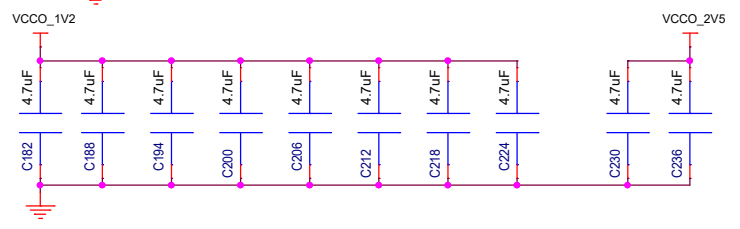
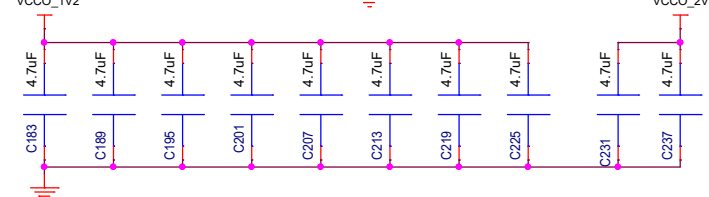
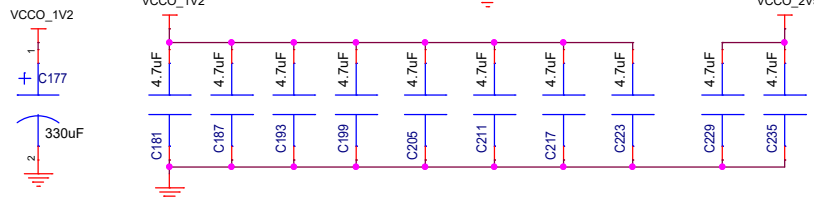
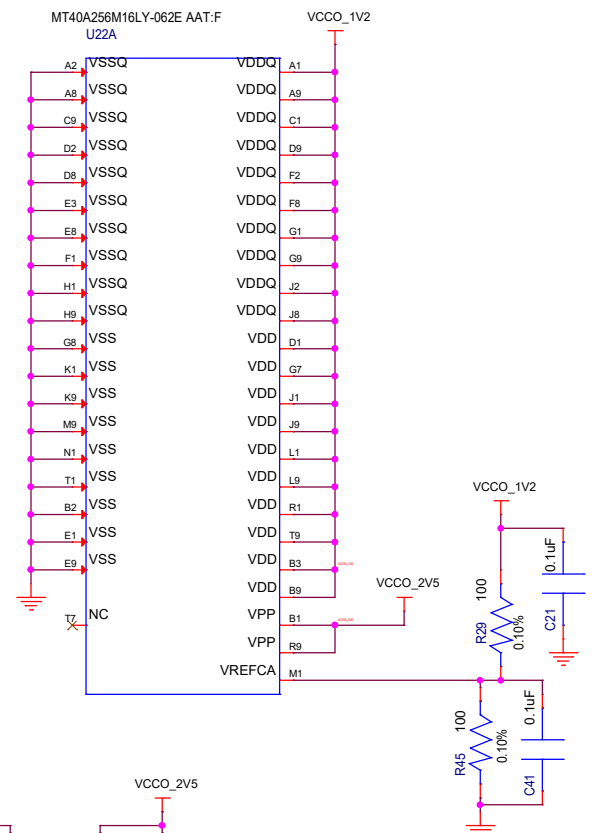
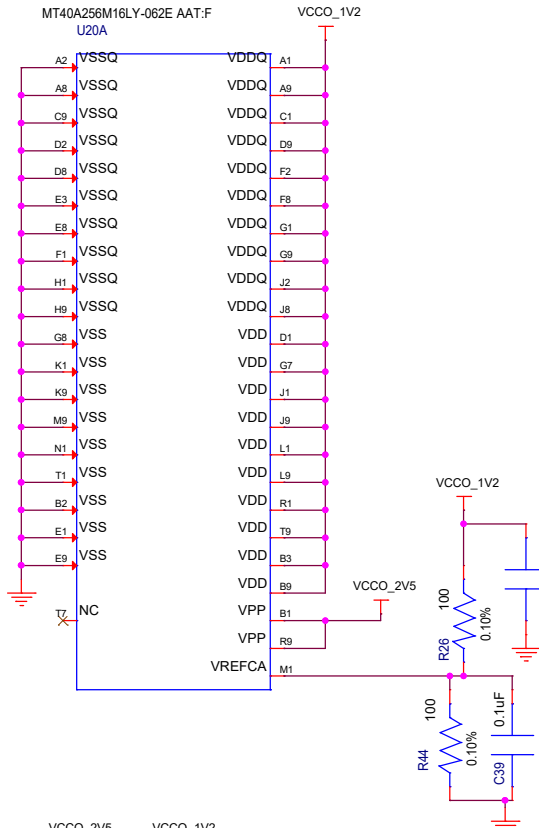
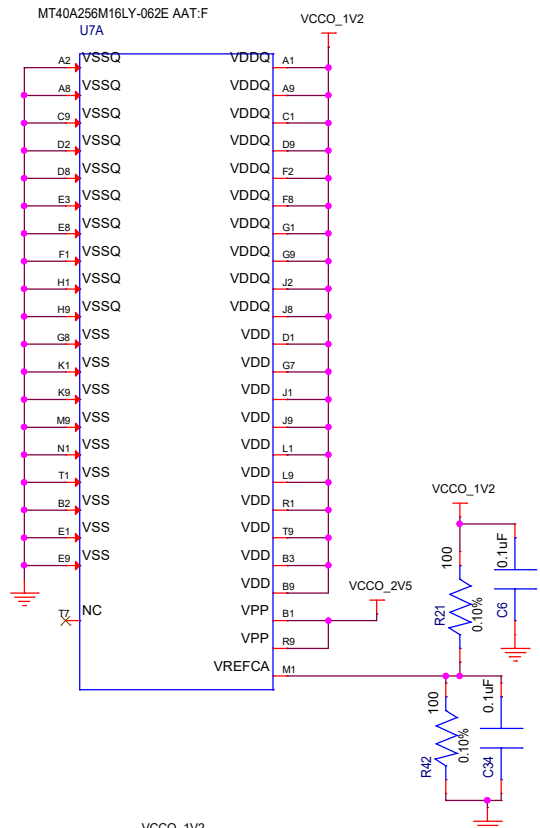
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TEXAS INSTRUMENTS

Title

Size **B** Document Number **TSW14J58EVM** Rev **B**

Date: Monday, August 24, 2020 Sheet 27 of 36



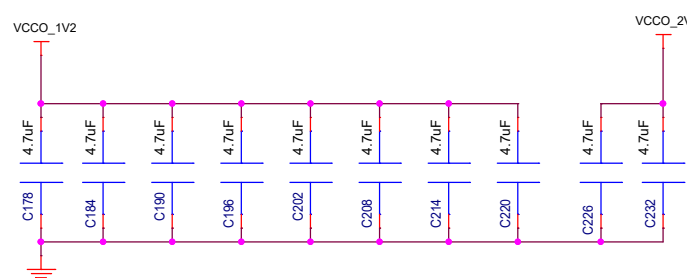
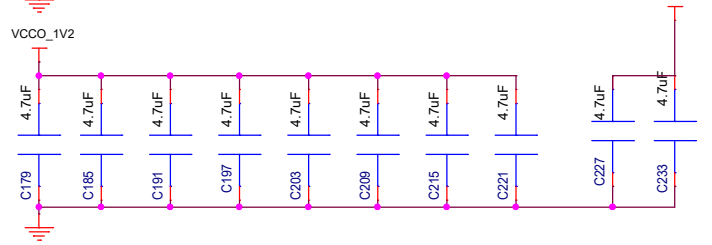
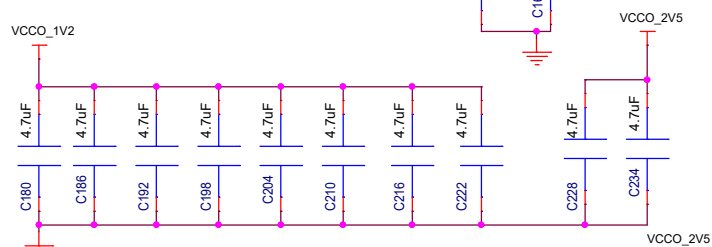
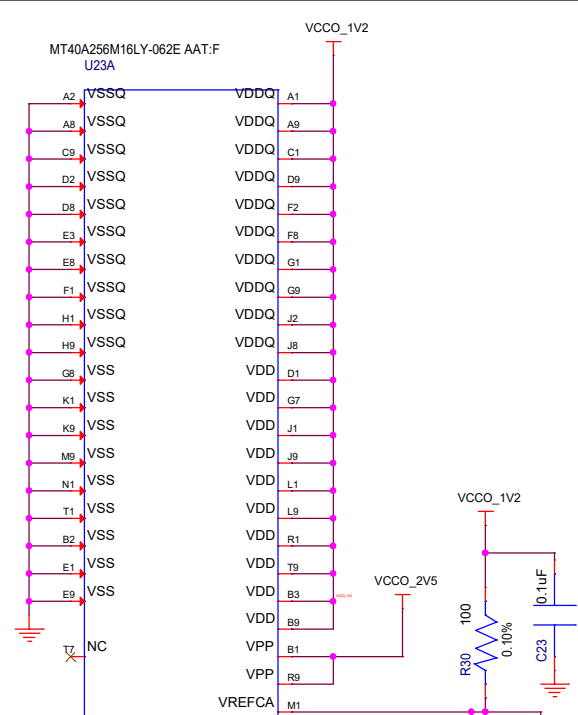
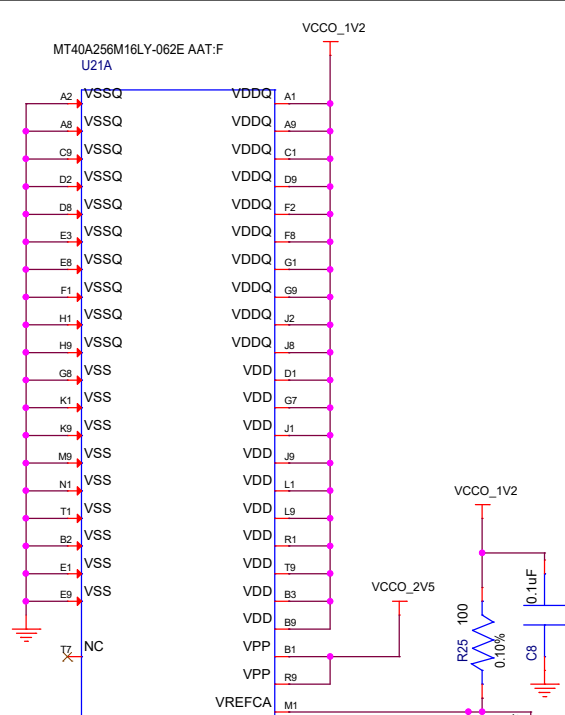
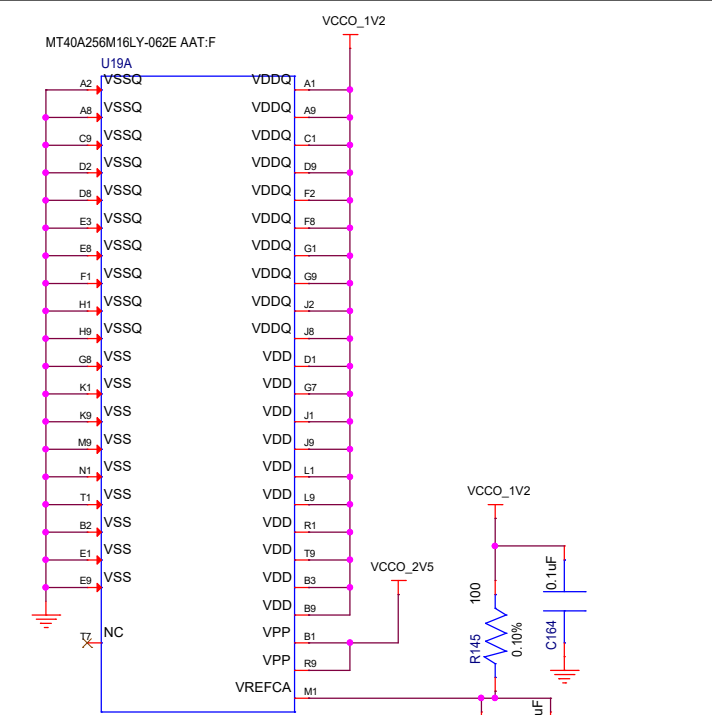
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TEXAS INSTRUMENTS

Title

Size **B** Document Number **TSW14J58EVM** Rev **B**

Date: Monday, August 24, 2020 Sheet 28 of 36



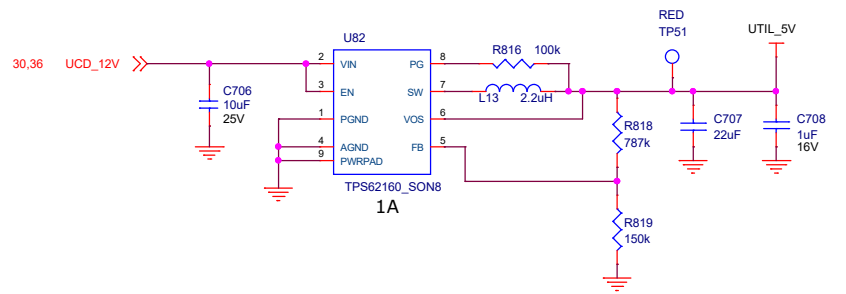
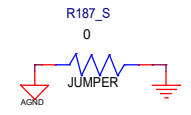
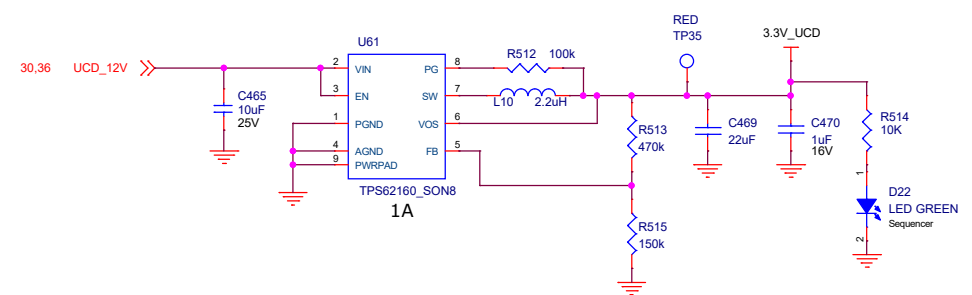
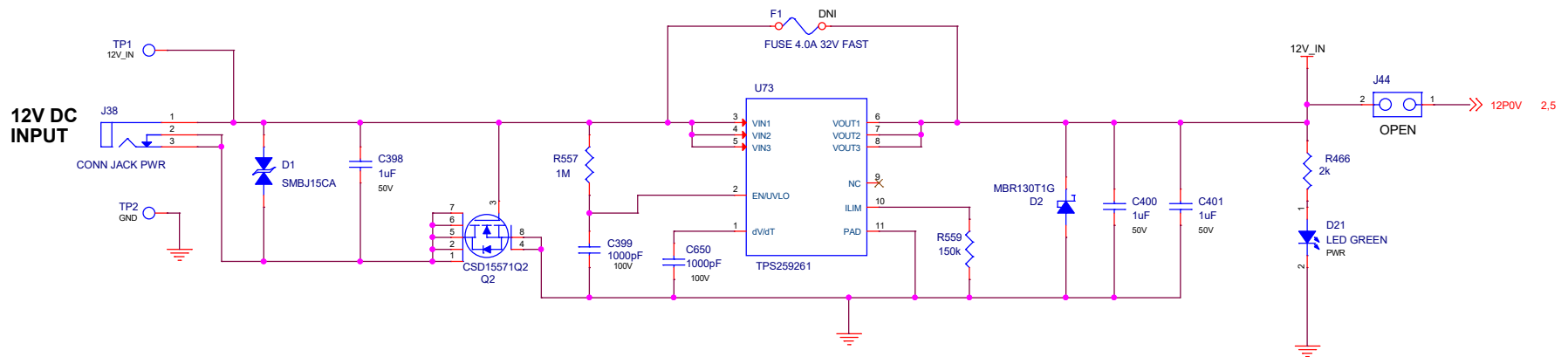
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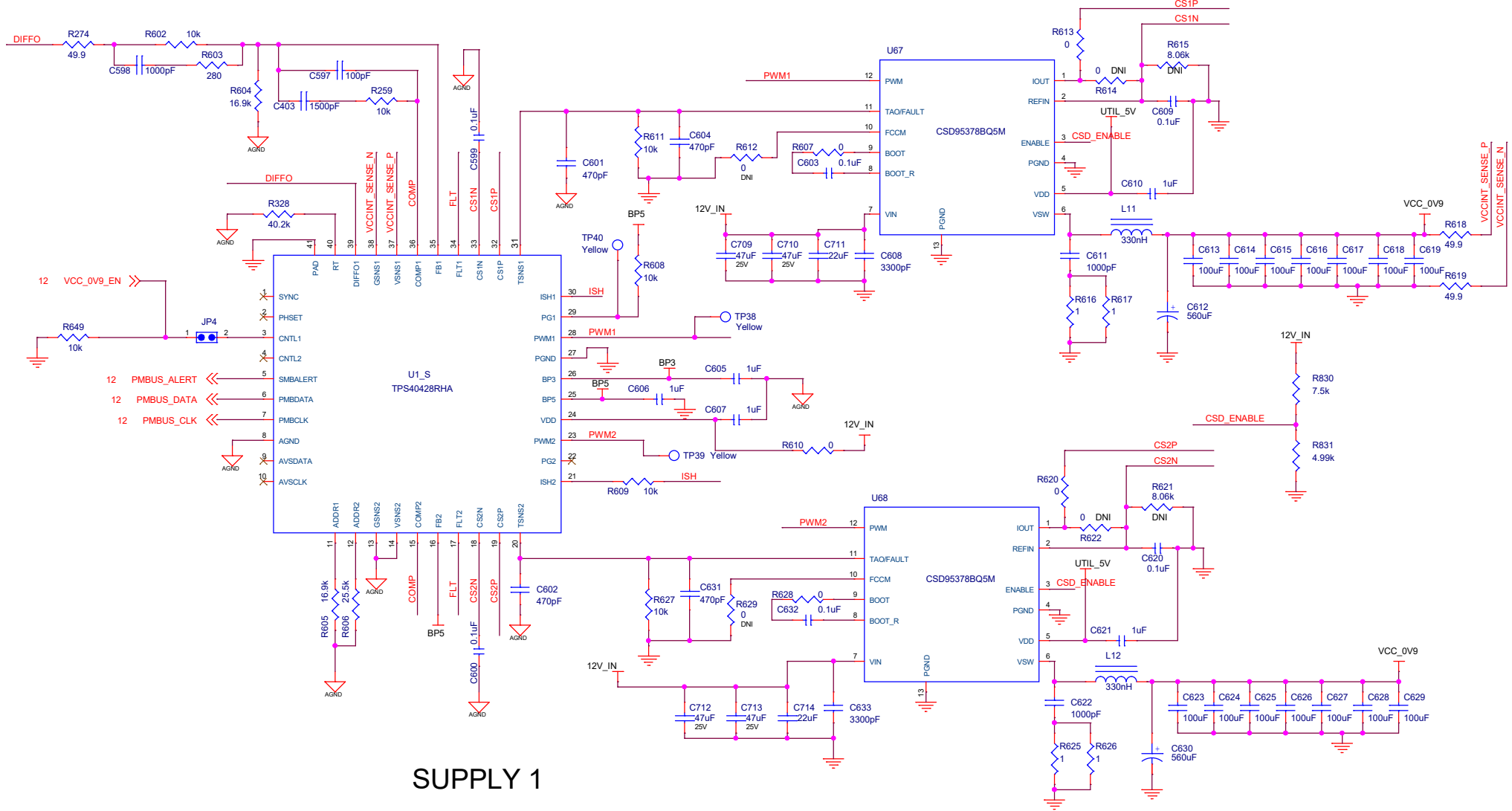
Date: **Monday, August 24, 2020** Sheet 29 of 36



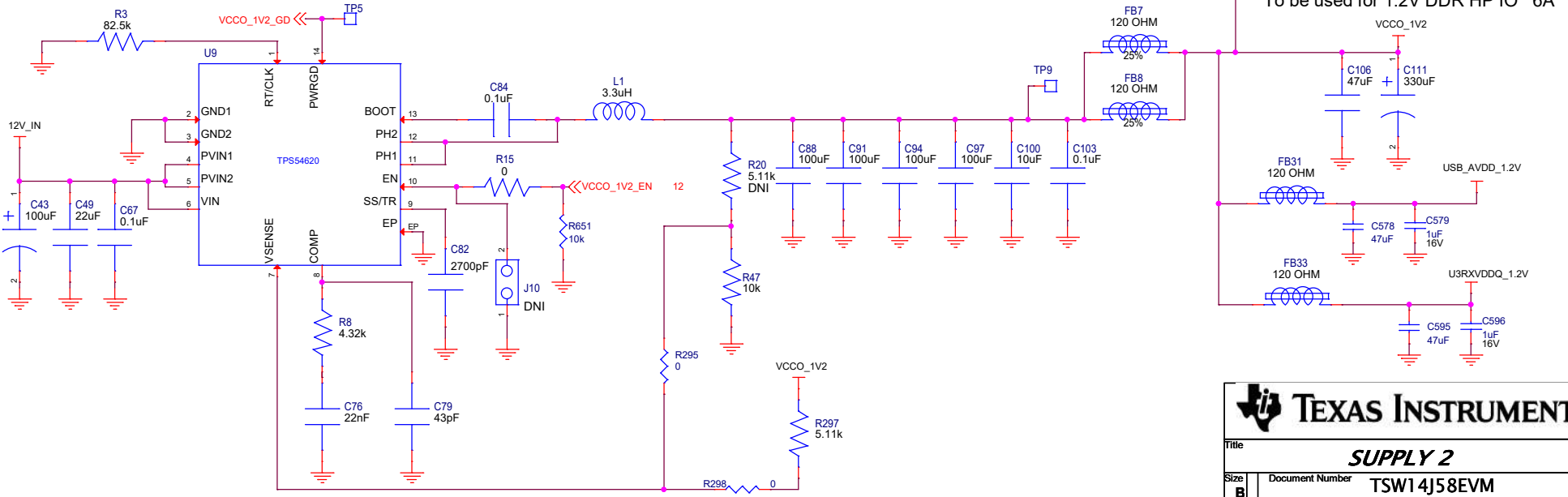
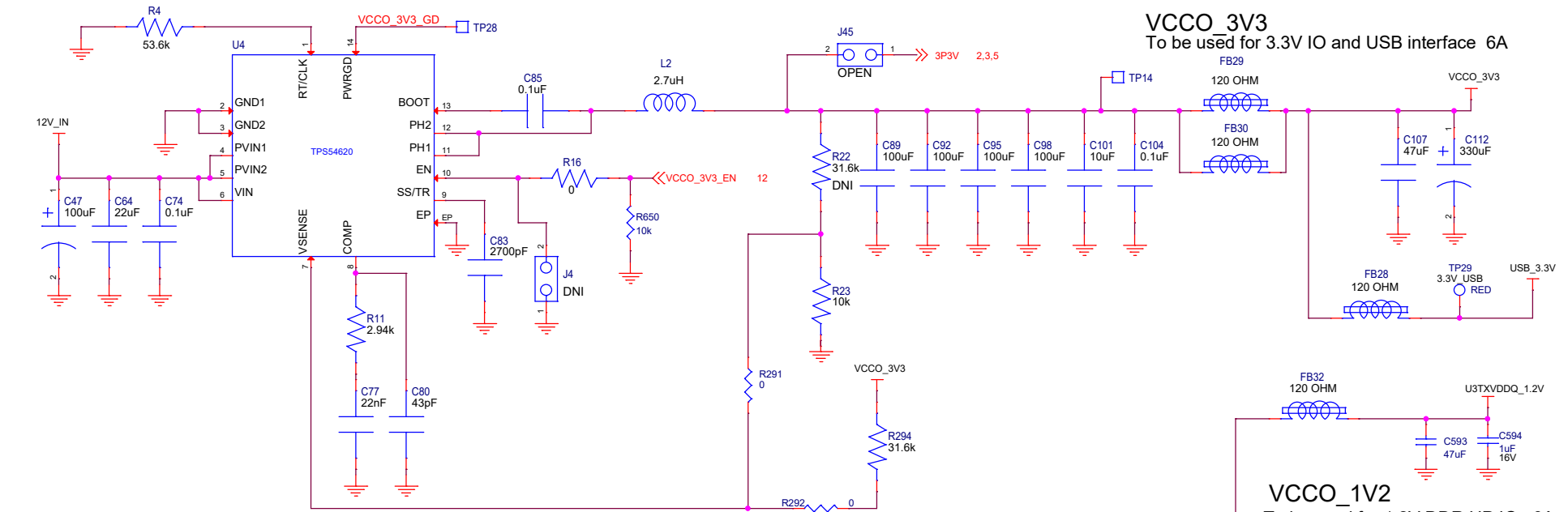
FPGA SUPPLY



Title		
Size B	Document Number TSW14J58EVM	Rev B
Date: Friday, August 21, 2020	Sheet 30	of 36



SUPPLY 1

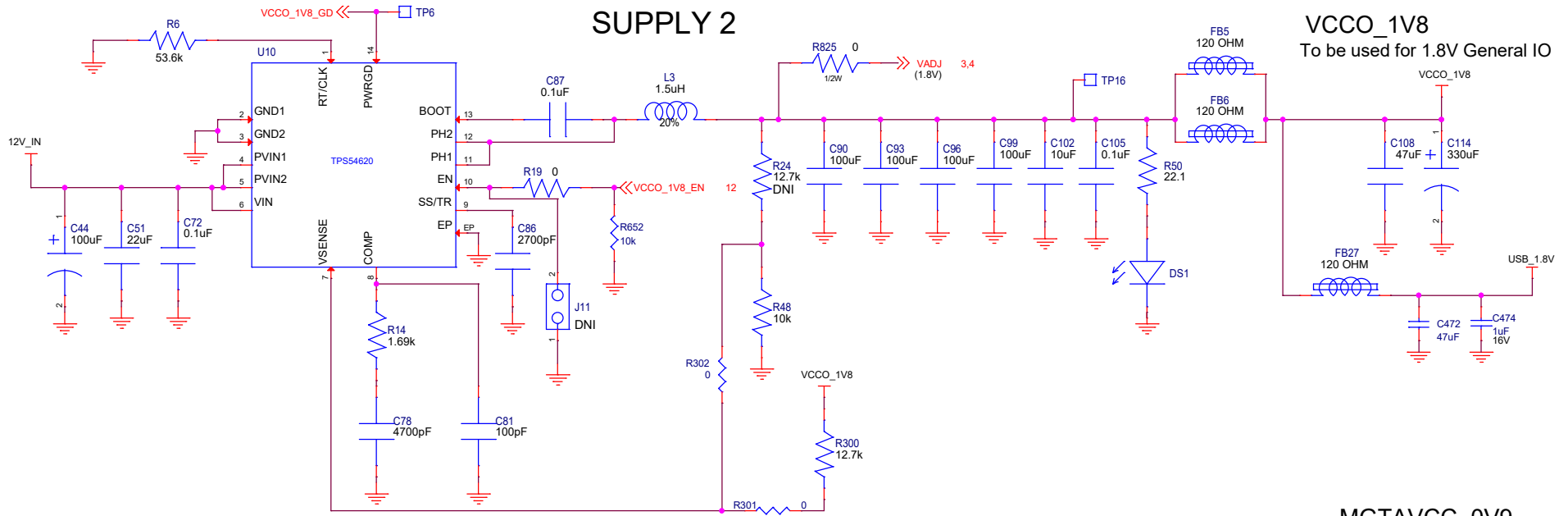


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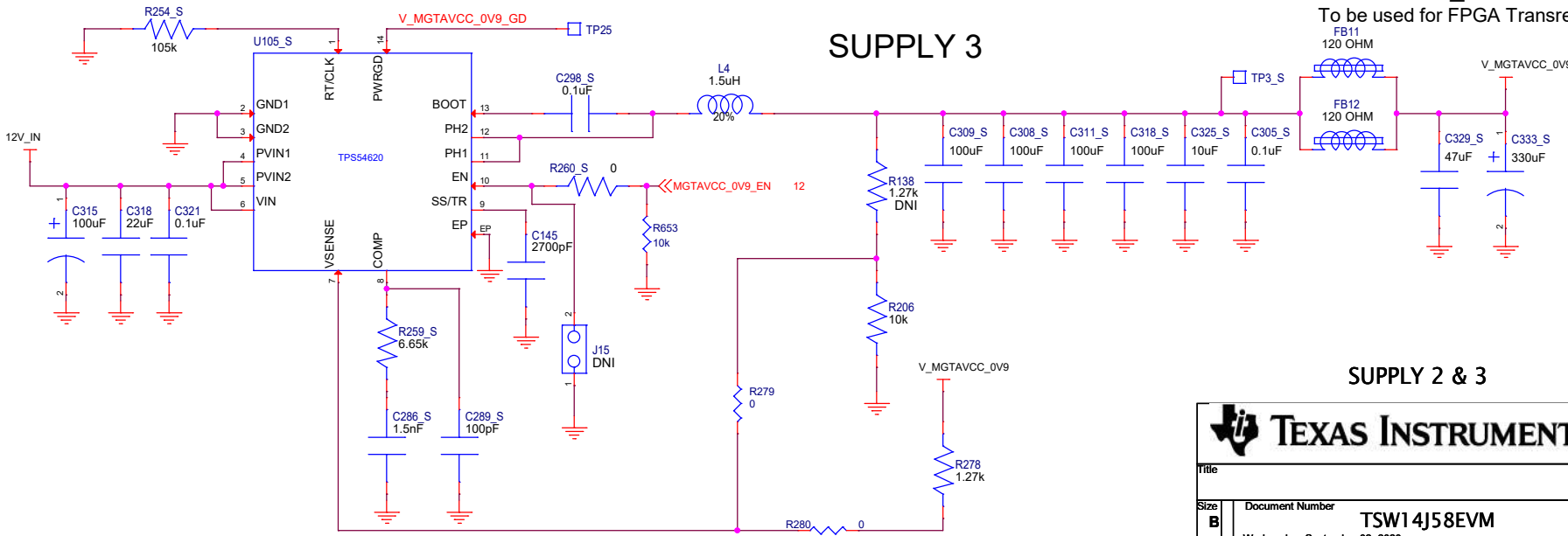
Size: B	Document Number: TSW14J58EVM	Rev: B
Date: Friday, August 21, 2020	Sheet: 32	of 36

SUPPLY 2




VCCO_1V8
To be used for 1.8V General IO

SUPPLY 3

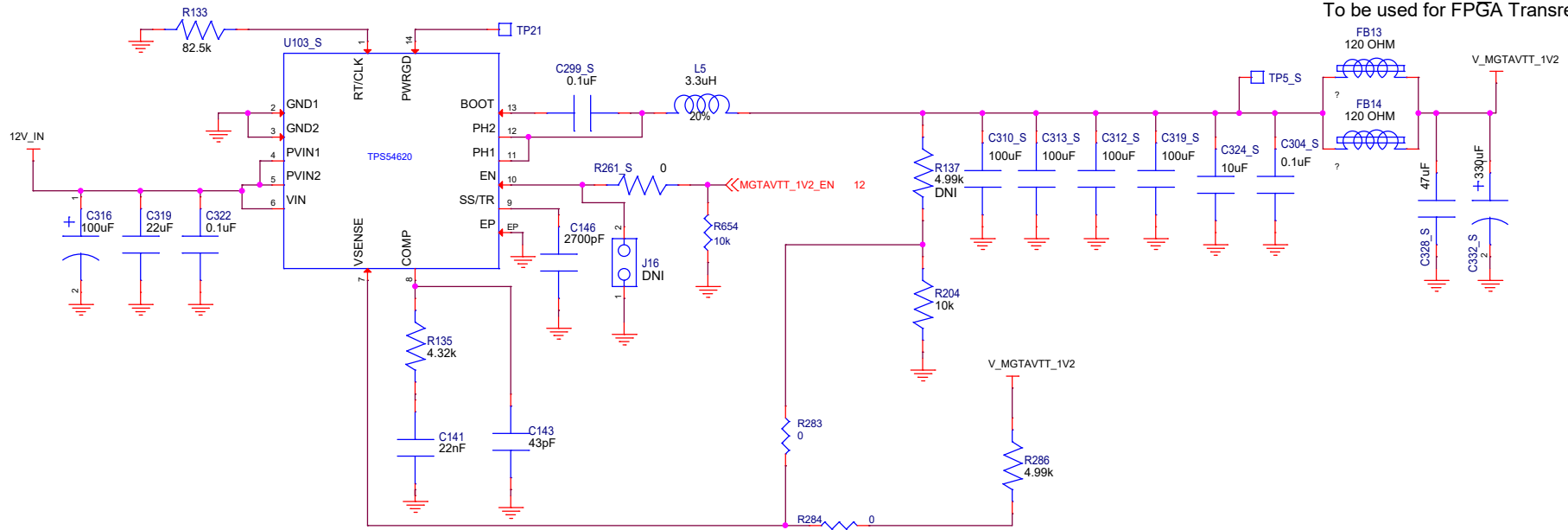


MGTAVCC_0V9
To be used for FPGA Transceiver

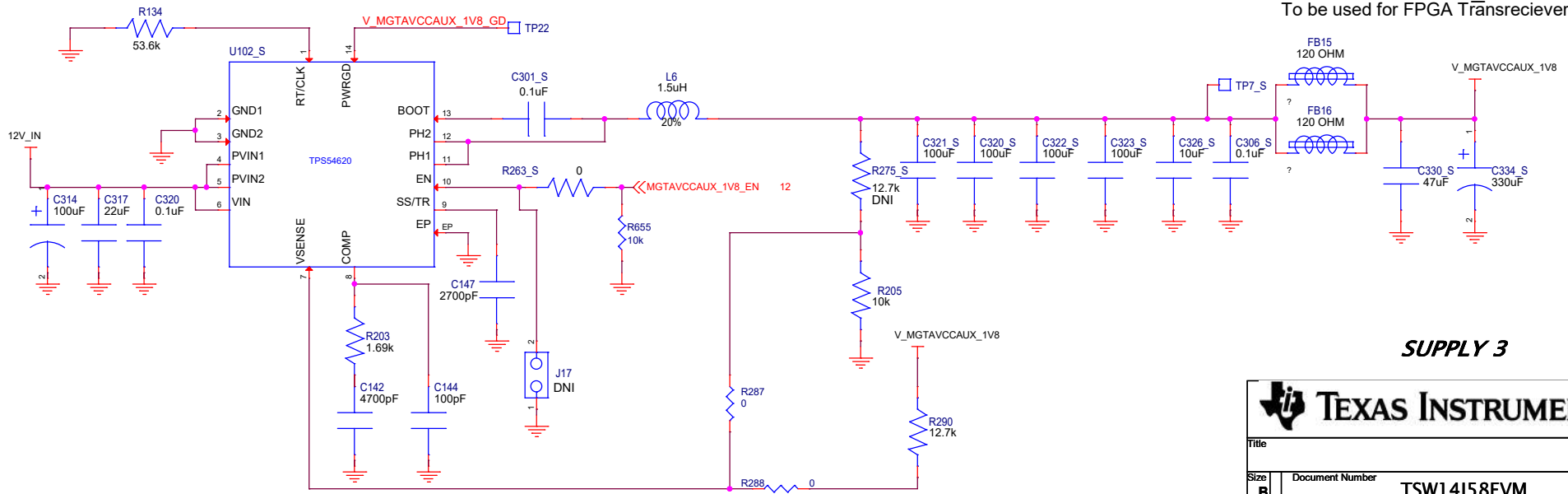
SUPPLY 2 & 3

 TEXAS INSTRUMENTS		
Title		
Size B	Document Number TSW14J58EVM	Rev B
Date: Wednesday, September 02, 2020	Sheet 33 of 36	

MGTAVTT_1V2
To be used for FPGA Transceiver



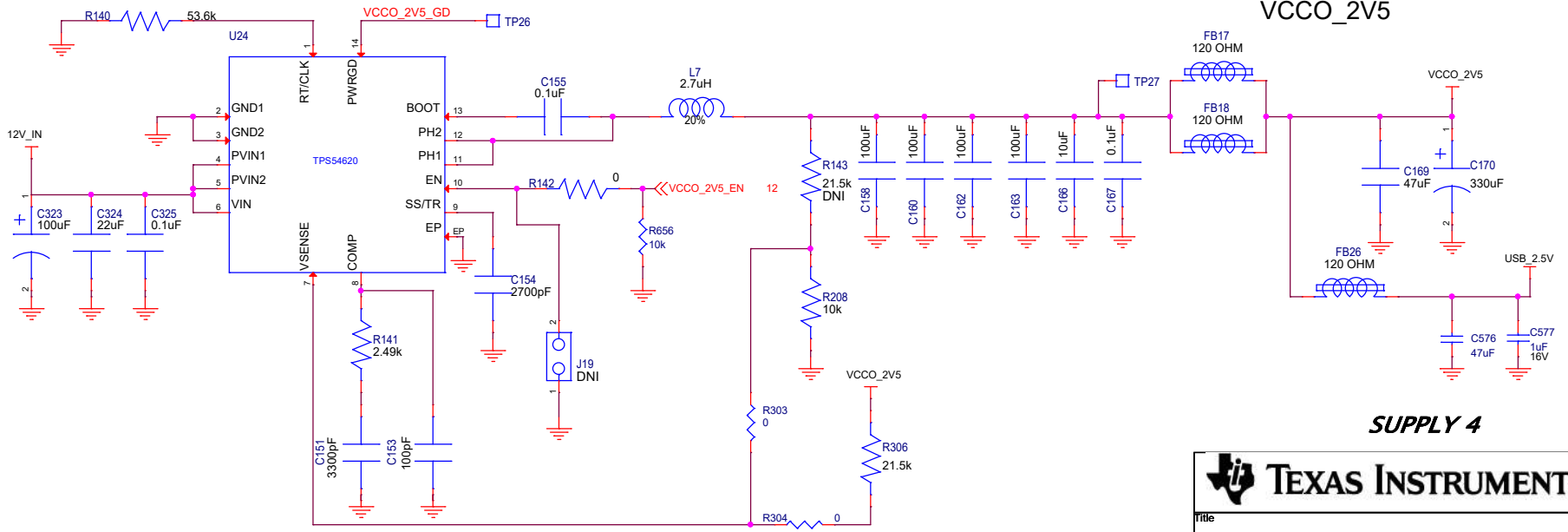
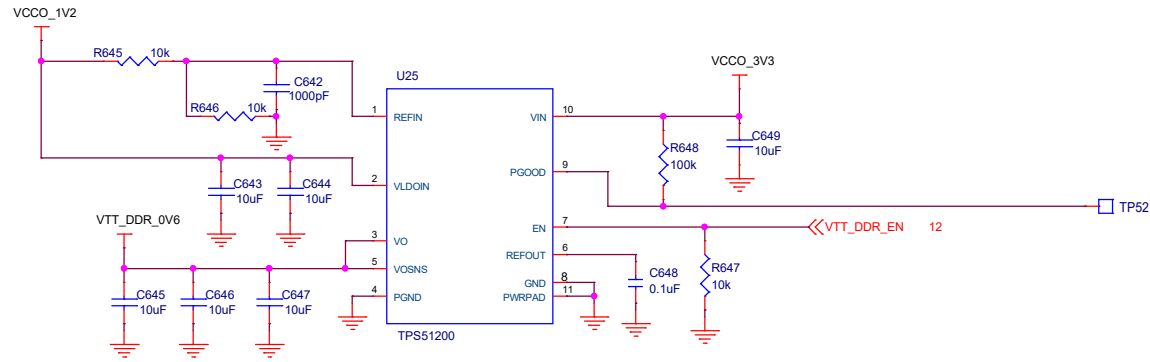
MGTAVCCAUX_1V8
To be used for FPGA Transceiver



SUPPLY 3

TEXAS INSTRUMENTS

Title		
Size B	Document Number TSW14J58EVM	Rev B
Date: Friday, August 21, 2020	Sheet 34	of 38



VCCO_2V5

SUPPLY 4

TEXAS INSTRUMENTS

Title		
Size B	Document Number TSW14J58EVM	Rev B
Date: Friday, August 21, 2020	Sheet 35	of 36

BARE BOARD, TSW14J58



Z_FAN1

FAN SINK, 27mm x 27mm
FIZ7

Z_LABEL1

TSW14J58EVM



STANDOFF ALUM HEX 2-56 x 3/4"



SCREW PANHEAD 2-56 x 1/4"



STANDOFF ALUM HEX 2-56 x 3/4"



SCREW PANHEAD 2-56 x 1/4"



STANDOFF ALUM HEX 2-56 x 3/4"



SCREW PANHEAD 2-56 x 1/4"



STANDOFF ALUM HEX 2-56 x 3/4"



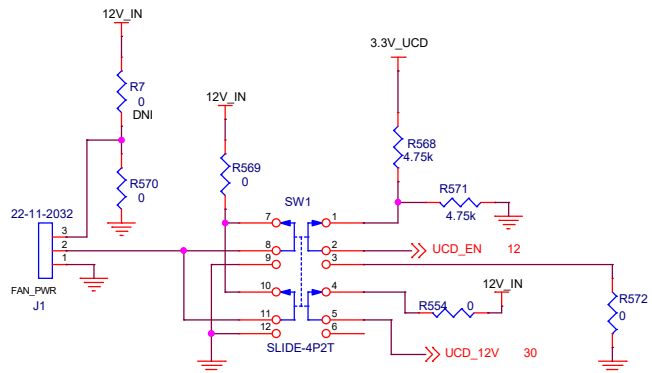
SCREW PANHEAD 2-56 x 1/4"



STANDOFF ALUM HEX 2-56 x 3/4"



SCREW PANHEAD 2-56 x 1/4"



Hardware



Title		
Size B	Document Number TSW14J58EVM	Rev B
Date:	Wednesday, August 26, 2020	Sheet 36 of 36