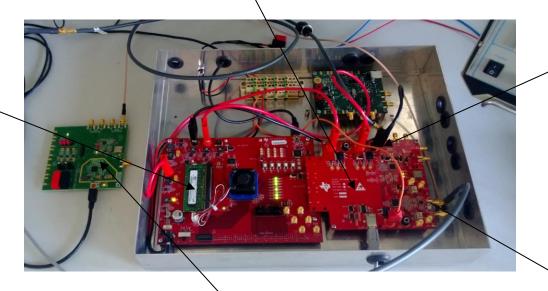
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DAC5682z EVM Contro			🐺 Texas Instruments
Menu	DAC5682z Register Configuration		version 3 functionality DAC5682z
DAC5682 Diagram Register Config TSW3100 Config Help Reset USB Port Readback Enabled	PLL Steep PLL reset VCO Frequency 1x M value LL Gain (MHz/V) 85 N value LL Range (MHz) 262 - 485)LL DAC mode Offset disable SLL dual DAC offset sync FIJ	Auto-DLL Swap data di Delay (deg) 90 same data di fixed current -3.43 m sy (ps/uA) normal FIFO offset FST error mask serial interface 3- FO error mask part our ourse hard 6-	ormal v interpolation 4x v isabled CM0 mode Bypass i sabled v CM0 mode Bypass i digital 0 0 clock 0 0 value software sync v sync v self test disable v
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Reg Value Hec 00 0100001 0.43 01 00010000 0.50 02 1110000 0.70 03 0110000 0.60 04 00000010 0.02 05 0010100 0.02 06 0101010 0.02 07 1111111 0.4F 08 00000000 0.00 0A 00000000 0.00 0B 000000000 </td <td>CDCM7005 Register Configuration M & N Selectio Auto Ref. Freq (MHL 10 © VCXO Freq (MH 983,04 © M Divider 125 © Output 983 Send All Load Reg Save Reg Save Reg</td> <td>YO Divider YO Level 3-trait 1 VD Level 3-trait 1 VD UPECL 3-trait 1 VI Output (SMA Outputs) 3-trait Phase Shift Divider YI Level 3-trait YO Divider YI Level 3-trait 3-trait YO Divider YI Level 3-trait 3-trait YO Divider YI Divider YI Level 3-trait YO Divider YI Output (DACSS2 4-trait YI Output (DACSS2 YI Output (DACSS2 3-trait YI Output (DACSS2 YI Output (DACSS2 3-trait YI Output (DACSS2 YI Output (DACSS2 3-trait</td> <td>• Y08 • Y14 • Y14 • Y15 • Y22 • Y28</td>	CDCM7005 Register Configuration M & N Selectio Auto Ref. Freq (MHL 10 © VCXO Freq (MH 983,04 © M Divider 125 © Output 983 Send All Load Reg Save Reg Save Reg	YO Divider YO Level 3-trait 1 VD Level 3-trait 1 VD UPECL 3-trait 1 VI Output (SMA Outputs) 3-trait Phase Shift Divider YI Level 3-trait YO Divider YI Level 3-trait 3-trait YO Divider YI Level 3-trait 3-trait YO Divider YI Divider YI Level 3-trait YO Divider YI Output (DACSS2 4-trait YI Output (DACSS2 YI Output (DACSS2 3-trait YI Output (DACSS2 YI Output (DACSS2 3-trait YI Output (DACSS2 YI Output (DACSS2 3-trait	• Y08 • Y14 • Y14 • Y15 • Y22 • Y28



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Registe	ers C80000	N 0	0000011	0	-42 0.		DD D U	95003C	0	
([Feedback signal: INT 400 + 0 2 MOD	PFD (MHz))x 10 / N = 400	2 = 20	(MHz) 00 Register 5	Divider Value CLK Div Mode le: Digital Lo	Clock Divider Off	•	onnected	I Autoset Div Freq≬	
	PFD Frequency: Prescaler:	10 8/9	MHz	Register 3					RF Output Enable: RF Output Power: Band Select Clock	
	1 7	Ref Doub			LDF:	FRAC-N -	Counter reset:	Disabled •		
	Output divider:	2	MHz		mp current:		CP 3-state:		Aux Output Enable:	
C	Channel spacing:	100	200 kł		Muxout:	3-state output	PD Polarity: Powerdown:		MTLD: Aux Output Select:	Disabled
R	RF Settings RF Frequency:	2000	VCO 4000 MI	Hz A	Spur Mode:	Low noise mode 💌	LDP:	10 ns 🔻	Register 4 VCO Powerdown:	

DAC5682z.ini

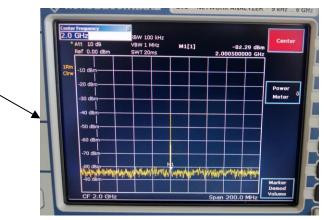
[DAC]

Interface name="DAC_SAMPLE_WISE" Number of channels=2 Number of Bits=16 Max sample Rate=1000000000 interp=4 Bus=16 dclkdly=0 pa_clks1=106 config1=16 config2=1 Format Pattern=-1,-2,1,2 //- for lsb //+ for msb //eg -1,-2,1,2= lsb of 1st channel data,lsb of 2nd channel data, msb of 1st channel data, msb of 2nd channel data. // Read EVM Setup Procedure="EVM Setup Procedure not available" \\use <> as delimiter for newline

Stabilock 4031

491,52 MHz 8,0 dBm

connected to DAC-Board J6 EXT_VCXO_P



connected to DAC-Board J16 RFOUT