Using the TI evaluation modules and software:

1. Connect 5V power and USB to both boards
2. Turn on power (using SW6) to data capture board
3. Turn on power (using S1) to ADC board
4. Start the ADC12J4000EVM GUI program
5. Select “EVM” tab on ADC12J4000EVM GUI
   1. Select clock source (On-board)
   2. Select Fs (FS=4000 Msps)
   3. Select decimation mode (Bypass Mode; DDR)
   4. Click “Program Clocks and ADC” button once
6. Select “Control” tab on ADC12J4000EVM GUI
   1. Click “ Excute Foreground CAL” button once
7. Start the HSDC Pro software
8. Select the ADC12J4000\_BYPASS device to upload FPGA firmware
9. Enter the “ADC Output Data Rate” (should match the Fs from above)
10. Select the number of samples to collect
11. Click the “Capture” button to acquire a set of samples

To use external trigger:

1. “Data Capture Options” => “Trigger Option”
2. Select “Trigger mode enable” then OK
3. Click the “Read DDR Memory” button. Samples will be acquired on external trigger event. This must occur within 12 seconds of clicking button. NOTE: if continuous triggers is applied to the trigger input, this seems to hang the board after the first successful trigger event.

Screen captures of setup:









