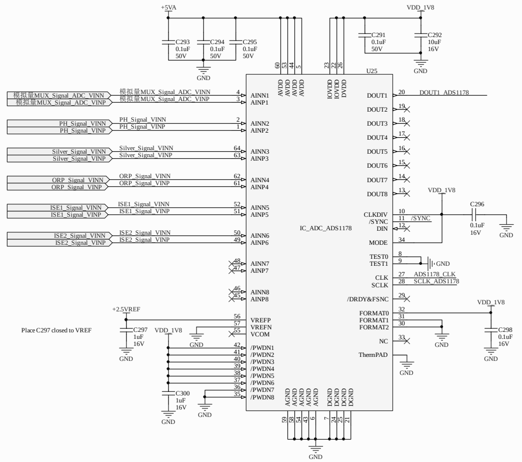
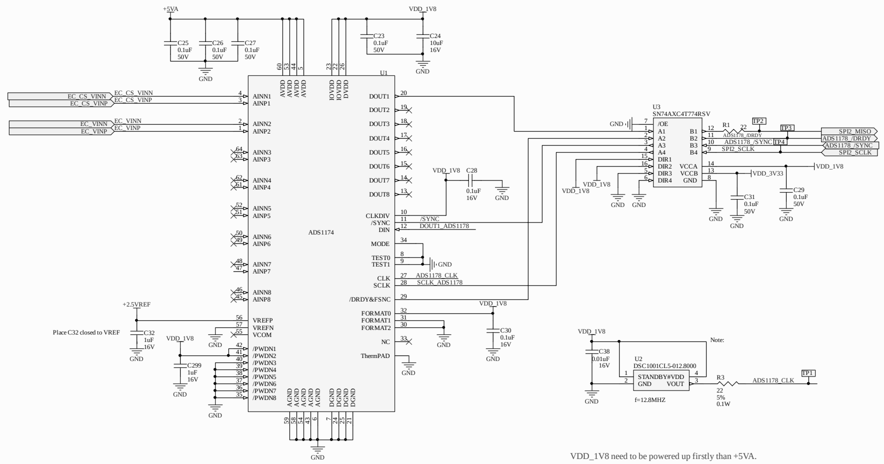

U25
IC_ADC_ADS1178
+5VA
VDD_1V8
+2.5VREF
Place C297 closed to VREF
模拟量MUX_Signal_ADC_VINN
模拟量MUX_Signal_ADC_VINP
PH_Signal_VINN
PH_Signal_VINP
Silver_Signal_VINN
Silver_Signal_VINP
ORP_Signal_VINN
ORP_Signal_VINP
ISE1_Signal_VINN
ISE1_Signal_VINP
ISE2_Signal_VINN
ISE2_Signal_VINP
DOUT1_ADS1178
/SYNC
ADS1178_CLK
SCLK_ADS1178
GND

Note:
1. master CLK to ADC is 12.8MHZ.
2. Set mode=high (low power mode);
3. fDATA=Fclk/2560=5Ksps; fMOD=1/40 of fCLK=320KHZ
4. Set CLK DIV=high to select fMOD=1/40 CLK=320KHZ
5. SCLK derived from MCU SPI1 SCLK. Set SCLK to 3.2MHZ.
6. Format[2:0]=001 select output format in SPI protocol and TDM Dout mode; data output in Dout1 only the channel position is fixed.
7. DIN connects to DOUT of the other ADS1178 for daisy chain operation.
8. Set /PWDN to high to disable power down mode as we need continuous sampling for vibration.
9. Set Test[1:0] to 00 to have the ADC always in normal operation.
10. the total data rate is 5K*16*6=480kbps=60KB
11.Power on sequence.

The internal digital filter helps to attenuate frequency above Nyquist sampling frequency.
fDATA=output data rate=sampling frequency
passband of digital filter is 0.453fDATA, help to attenuate all of unused frequency above 2.265KHZ
to avoid anit-aliasing issue.


U1
ADS1174
+5VA
VDD_1V8
+2.5VREF
Place C32 closed to VREF
EC_CS_VINN
EC_CS_VINP
EC_VINN
EC_VINP
/SYNC
DOUT1_ADS1178
ADS1178_CLK
SCLK_ADS1178
U3
SN74AXC4T774RSV
SPI2_MISO
ADS1178_/DRDY
ADS1178_/SYNC
SPI2_SCLK
VDD_3V33
U2
DSC1001CL5-012.8000
STANDBY#VDD
GND
VOUT
f=12.8MHZ
R3
22
5%
0.1W
TP1
GND

VDD_1V8 need to be powered up firstly than +5VA.

+5V is enabled by PGOOD_1.8V.

SPI clock and Dout need impedance control: 50 ohm+/-10%.
As IOVDD of ADS1178 is 1.8V while IO voltage potential of MCU is 3.3V, need bidirectional level shifter

Note:
1. master CLK to ADC is 12.8MHZ.
2. Set mode=low (high speed mode);
3. fDATA=Fclk/512=25Ksps; fMOD=64*fDATA=1/8 of fCLK=1.6MHZ
4. Set CLK DIV=high to select fMOD=1/8 CLK=1.6MHZ
5. SCLK derived from MCU SPI1 SCLK. Set SCLK to 3.2MHZ(1/4 of fCLK).
6. Format[2:0]=001 select output format in SPI protocol and TDM Dout mode; data output in Dout1 only the channel position is fixed.
7. DIN connects to DOUT of the other ADS1178 for daisy chain operation.
8. Set /PWDN to high to disable power down mode as we need continuous sampling for vibration.
9. Set Test[1:0] to 00 to have the ADC always in normal operation.
10. the total data rate is 25K*16*2+480K=1.28Mbps=160KB
11.Power on sequence.

The internal digital filter helps to attenuate frequency above Nyquist sampling frequency.
fDATA=output data rate=sampling frequency
passband of digital filter is 0.453fDATA, help to attenuate all of unused frequency above 11.325KHZ
to avoid anit-aliasing issue.

Title	模拟量&电极信号 ADC		
Size: A1	Number		Revision: A
Date:	2026/4/15	Sheet 9 of	17
File:	C:\Users\..\模拟量MUX信号ADC.SchDoc	Drawn By:	John Man