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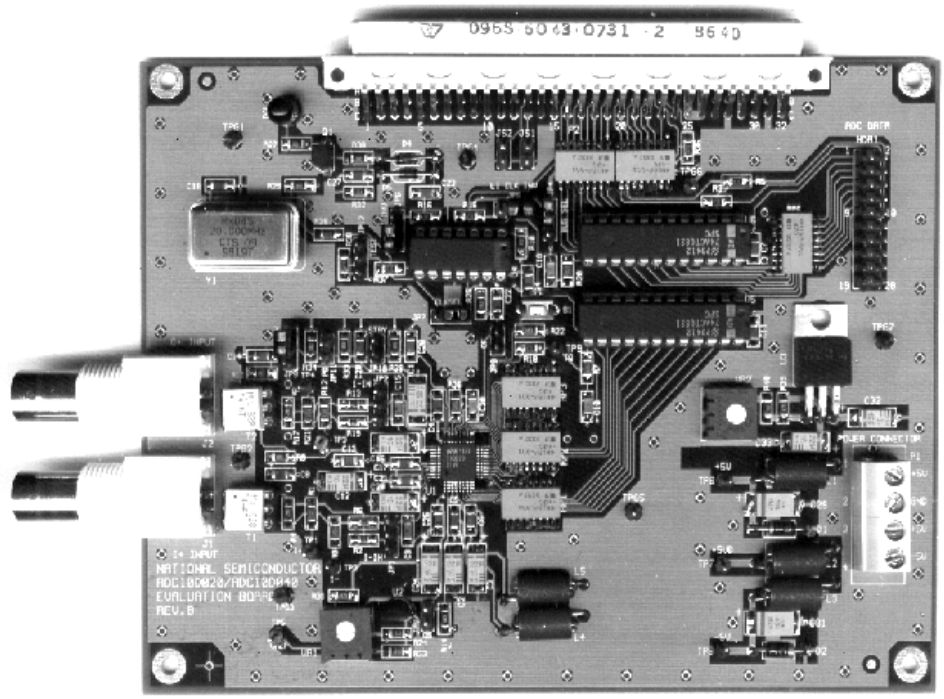
November 2001
Rev B

Evaluation Board Instruction Manual

ADC10D020 10-Bit, 20 MSPS, 3 Volt, 150mW A/D Converter with Internal Sample & Hold

and

ADC10D040 10-Bit, 20MSPS, 3 Volt, 240mW A/D Converter with Internal Sample-and-Hold



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1.0 Introduction

The ADC10D040EVAL Design Kit (consisting of the ADC10D040 Evaluation Board, National's WaveVision™ software and this manual) is designed to ease evaluation and design-in of National's ADC10D020 or ADC10D040 10-bit Analog-to-Digital Converter, which operate at speeds up to 20 MSPS and 40MSPS, respectively. Further reference in this manual to the ADC10D040 is meant to also include the ADC10D020, unless otherwise specified or implied.

The signal at the Analog Input is digitized and can be captured and displayed on a PC monitor as a dynamic waveform. The digitized output is also available at Euro connector P2 and 20-pin header HDR1.

The evaluation board can be used in either of two modes. In the Manual mode, suitable test equipment can be used with the board to evaluate the ADC10D040 performance.

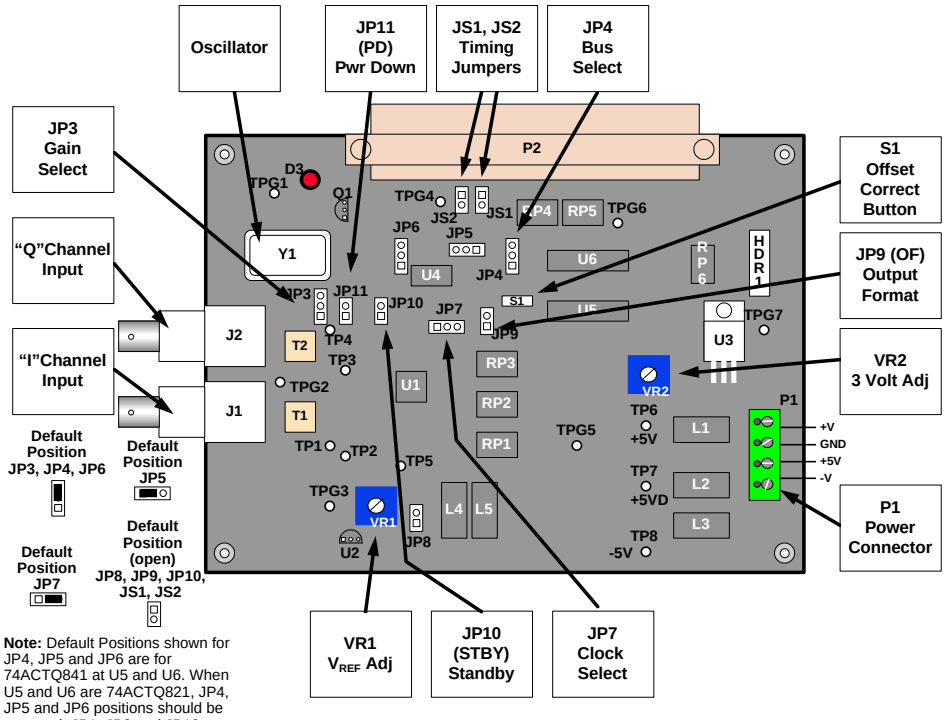
In the Computer mode, evaluation is simplified by connecting the board to the WaveVision™ Digital Interface Board (order number WAVEVSN BRD 3.0), which is connected to a personal computer through a serial communication port and running WaveVision™ software, operating under Microsoft Windows 95 or later. Use program WAVEVSN2.EXE.

The WaveVision™ software operates under Microsoft Windows and can perform an FFT on the captured data upon command and, with the frequency domain plot, shows dynamic performance in the form of SNR, SINAD, THD and SFDR.

The signal at the Analog Input to the board is digitized and is available at pins B16 through B21 and C16 through C21 of P2. Pins A16 through A21 of P2 are ground pins. The digitized signal is also available at 20-pin header HDR1. See the board schematic of *Figure 8* for more details.

2.0 Board Assembly

The ADC10D040 Evaluation Board may come pre-assembled or as a bare board that must be assembled. Refer to the Bill of Materials (Section 8.0) for a description of components, to *Figure 1* for major component placement and to *Figure 8* (in Section 8.0) for the Hardware schematic.



Note: Default Positions shown for JP4, JP5 and JP6 are for 74ACTQ841 at U5 and U6. When U5 and U6 are 74ACTQ821, JP4, JP5 and JP6 positions should be reversed. JP1, JP2 and JP12 are not needed or populated.

Figure 1. Component and Test Point Locations

3.0 Quick Start

Refer to *Figure 1* for locations of test points and major components. For Stand-Alone operation**:**

1. Install an appropriate crystal into socket Y1. While the oscillator may be soldered to the board, using a socket will allow you to easily change clock frequencies. Remove oscillator Y1 for Computer mode operation to minimize noise.
2. To use the crystal oscillator located at Y1 to clock the ADC, connect the jumper on JP7 to pins 1 and 2 (opposite from default position shown in *Figure 1*.).
3. Connect a jumper between pins 2 and 3 of JP3 (default position) to set ADC gain at 1.
4. Connect a jumper between pins 2 and 3 of JP4 (default position) to select the output of the I-channel bus (A jumper between pins 1 and 2 selects the Q-channel bus).
5. Connect a jumper between pins 1 and 2 of JP5 and of JP6 (default positions) if U5 and U6 are 74ACTQ841s. If U5 and U6 are 74ACTQ821s, connect jumpers between opposite pins described here.
6. Connect a clean power supply to Power Connector P1. Supply +5V at pins 1 and 3 of P1. Pin 2 is ground. No connection to pin 4 of P1 is needed.
7. Use VR2 to set the ADC10D040 supply voltage at either end of L4 or L5 to 3.0V ±0.05V.
8. Use VR1 to set the reference voltage (V_{REF}) for the ADC to 1.0V ±0.05V at TP5.
9. Remove any input signals from BNC connectors J1 and J2.
10. Press and release switch S1 to perform an offset correction.
11. Connect a signal of $1V_{P-P}$ amplitude from a 50-Ohm source to Analog Input BNC J1. The ADC differential input signal can be observed at TP1 and TP2 (near VR1). Because of isolation resistors R1 and R8 (see schematic, *Figure 8*) and the scope probe capacitance, the input signal at TP1 and TP2 will not have the same frequency response as the ADC input.
12. Adjust the input signal amplitude as needed to ensure that the signals at TP1 and TP2 remains below $1.0V_{P-P}$.
13. The digitized signal is available at pins B16 through B20 and C16 through C20 of P2.
14. Adjust the input level to get the desired output level.

For Computer mode operation:

1. Connect the evaluation board to the Digital Interface Board. See the Digital Interface Board Manual for operation of that board.
2. Connect a clean power supply to Power Connector P1. Supply +5V at pins 1 and 3 of P1. Pin 2 is ground. No connection to pin 4 of P1 is needed.
3. Connect the jumper at JP7 to pins 2 and 3 (default position) to use the clock signal from the Digital Interface Board.
4. Perform steps 3 through 12 of the Stand-Alone operation quick start, above.
5. See the Digital Interface Board Manual for instructions for setting the ADC clock frequency and for gathering data.
6. If the output level goes over range as seen on the data captured through WaveVision™, reduce the output level from the signal generator and capture data again. If the output level does not reach codes of 25 and 1000, increase the output level from the signal generator and capture data again.

To select the "Q" channel, and direct its output to the data bus, place the jumper on JP4 between pins 1 and 2 (opposite from default position shown in *Figure 1*).

4.0 Functional Description

The ADC10D040 Evaluation Board schematic is shown in *Figure 8*.

4.1 The Signal Input

This evaluation board is capable of accommodating two single-ended inputs. They can be quadrature signals or completely independent signals.

Signal transformers T1 and T2 provide single-ended to differential conversion. The common mode voltage at the ADC input on this board is equal to the common mode output voltage, V_{CM}, of the ADC, a nominal 1.5V.

The input signals to be digitized should be applied to BNC connector J1 for the I-channel and to BNC connector J2 for the Q-channel. These 50 Ohm inputs are intended to accept signals of 0.5V peak-to-peak amplitude with the GAIN pin at a logic low (pins 1 and 2 of JP3 shorted together, or no short on JP3) or signals of 1.0V peak-to-peak with the GAIN pin high (pins 2 and 3 of JP3 shorted together – the default position). An unused input (J1 or J2) may be left unconnected.

To accurately evaluate the ADC10D040 dynamic performance, the input test signal must be passed through a bandpass filter (See Section 4.1.2).

Data may be gathered on just one channel at a time.

> **NOTE:** If input frequency components above 20MHz are required, replace capacitors C9 and C12 at the ADC differential input pins with capacitors of 10pF.

4.1.1 Selecting the Conversion Channel

Data may be gathered on the selected channel with either of the set-ups indicated in *Table 1*:

CHAN BUS	Output Mode	JUMPER JP8 (OS) PINS SHORTED	JUMPER JP4 PINS SHORTED
I	Parallel	none	2 & 3
Q	Parallel	none	1 & 2
Q	Multiplexed	1 & 2	2 & 3
none	no output	1 & 2	1 & 2

Table 1. Selecting the output channel.

The ADC10D040 evaluation board can use either the 74ACTQ841 10-bit latch or the 74ACTQ821 10-bit buffer in positions U5 and U6. Both of these positions should have the same part type. *Table 2* indicates the shorted positions of JP5 and JP6 needed for the respective components at U5 and U6.

JUMPERs JP5 & JP6 PINS SHORTED	Clock Phase	Use when U5 & U6 are
1 & 2	Non-Inverted	74ACTQ821
2 & 3 (default)	Inverted	74ACTQ841

Table 2. Selecting the clock phase.

4.1.2 Evaluating the Converter

The output of just one converter of the dual ADC10D040 may be captured at a time. *Tables 1* and *2* show the jumper connections needed to select the converter to be evaluated.

It is important when evaluating the dynamic performance of the ADC10D040 (or any A/D converter), that a clean sine wave be presented to the converter. To do this it is necessary to use a bandpass filter between the signal source and the ADC10D040 evaluation board inputs J1 and J2. Even the best signal generators available do not provide adequate noise and distortion performance for proper evaluation of a 10-bit ADC. At each BNC connector use a high-quality bandpass filter with better than 12-bit equivalent noise characteristics and at least 80dB stop band attenuation. No scope or other test equipment should be connected to TP1, TP2, TP3, TP4, JP1 or to JP2 while gathering data.

4.1.3 Evaluating Crosstalk

Crosstalk can be evaluated with WaveVision™ by supplying full-scale input signals of different, non-harmonically related frequencies to inputs J1 and J2. Select the output of one of the converter channels and acquire data on that channel. Perform an FFT on that data and look for the output signal level of the frequency on the other channel. The frequency present at the input of the selected channel should be readily apparent, but the energy level of the frequency on the other channel will be very low or even in the noise floor, indicating excellent crosstalk performance.

4.2 Looking at Both Channels

This evaluation board is capable of gathering and uploading data on one channel at a time. To look at data from both channels, it is necessary to first gather data on one channel, then open another data window in WaveVision™, select the opposite channel (with JP4 or JP8) and gather data on the opposite channel.

Remember that, unless sampling is coherent, gathering repeated samples of the same signal will produce somewhat different results each time. The A/D converter performance is at least as good as the best sample taken. See Section 6.2 for information about coherent sampling.

4.3 ADC reference circuitry

An adjustable reference circuit is provided on the board. When using the resistor values shown in *Figure 1*, the reference circuit will generate a nominal reference voltage in the range of 0.4 to 1.2 Volts. The ADC10D040 is specified to operate with V_{REF} in the range of 0.8V to 1.2 V, with a nominal value of 1.0V when the GAIN pin is at a logic high, or half these values when the GAIN pin is at a logic low. The reference voltage can be monitored at test point TP5 and is set with VR1.

It is advisable to have no connection to TP5 while gathering data to ensure that no noise is injected into the reference.

A Common Mode voltage, V_{CM}, is provided by the ADC10D040. This voltage is nominally a stable 1.5V and can be used as the reference voltagesource for the ADC10D040. It is not used as the reference on this board, but is used as a common mode voltage for the two differential signal inputs. Be careful not to load the V_{CM} pin of the ADC10D040 with more than 1 mA.

4.4 ADC clock circuit

The clock signal applied to the ADC is selected with jumper JP7. A standard crystal oscillator can be installed at Y1 and selected with jumper JP7 pins 1 and 2 shorted together (opposite from default position). To use a different clock source, connect the clock signal to pin B23 of P2 and short pins 2 and 3 of jumper JP7 (default position). See Section 6.1 for cautions on using the oscillator at Y1 in the computer mode.

R36 and C30 are used for AC termination of the clock line. R36 should be the characteric impedance of the line and C30 is chosen to be twice the round trip delay

between the clock source and the ADC clock pin divided by the characteristic impedance of the clock line.

In the Computer mode of operation, using the Digital Interface Board, JP7 should be set to connect pins 2 and 3 together (default position) to use the clock from the Digital Interface Board and oscillator Y1 should be removed from its socket. Using an oscillator at Y1 for the ADC clock when using the Computer mode will result in data capture that is not synchronized with the operation of the Digital Interface Board, leading to corrupted data. See Section 6.1 for more information.

4.5 Digital Data Output.

The digital output data from the ADC10D040 is available at the 96-pin Euro connector P2. Series resistors RP1, RP2 and RP3 isolate the ADC output lines from board capacitances, reducing noise coupling back into the ADC that would result from the rapid charge and discharge of these capacitances. Series resistors RP4, RP5 and RP6 isolate latches U5 and U6 from their load circuit to reduce noise on the board.

4.6 ADC10D040 Control Pins.

The ADC10D040 has six control pins, making it a very versatile converter. They are Offset Correct (OC), GAIN, Output Bus Select (OS), Output Format (OF), Standby (STBY) and Power Down (PD).

4.6.1 The Offset Correct (OC) Pin

A low-to-high transition on this pin initiates an independent offset correction sequence for each converter, which takes 34 clock cycles to complete. During this time 32 conversions are taken and averaged. The result is subtracted from subsequent conversions. Each input pair should have 0V differential value during this entire 34 clock period.

4.6.2 The Gain Pin

This pin sets the internal signal gain at the inputs to the ADCs. With this pin at a logic low the full scale differential input peak-to-peak signal is equal to V_{REF}. With this pin at a logic high the full scale differential input peak-to-peak signal is equal to V_{REF} / 2. Default for this board is the GAIN pin at a logic high (pins 2 and 3 of JP3 shorted).

4.6.3 The Output Bus Select (OS) Pin

With this pin at a logic high, both the "I" and the "Q" data are present on their respective 10-bit output buses (parallel mode of operation). When this pin is at a logic low, the "I" and "Q" data are multiplexed onto the "I" output bus and the "Q" output lines all remain at a logic low (multiplexed mode). Default for this board is multiplexed mode (no connection at JP8).

4.6.4 The Output Forman (OF) pin

When this pin is LOW the output format is Straight Binary. When this pin is HIGH the output format is 2's complement. This pin may be changed "on the fly," but this will result in errors for one or two conversions after the logic level change at this pin. Default for this board is Straight Binary (no connection at JP9).

4.6.5 The Power Down (PD) Pin

With this pin at a logic high, the ADC10D040 is in the Power Down mode where it consumes less than 1mW of power. It takes 1ms to recover from this mode after the PD pin is brought low. If Both the STBY and PD pins are low simultaneously, the PD pin dominates.

4.6.6 The Standby (STBY) Pin

With this pin at a logic high and the PD pin is at a logic low, the ADC10D040 is in the standby mode where it consumes just 30mW of power. It takes just 800ns to come out of this mode after the STBY pin is brought low. The ADC10D040 operates normally with a logic low on this and the PD (Power Down) pins.

4.7 Power Supply Connections

Power to this board is supplied through power connector P1. The only supplies needed is +5V at pins 1 and 3 plus ground at pin 2. No connection to pin 4 of P1 is necessary.

When using the ADC10D040 Evaluation Board with the Digital Interface Board, the 5V logic power for it is supplied to it through pin 3 of P1. Accordingly, more power is consumed from the supply connected to this pin when the Digital Interface Board is used. The power is passed through P2 to the Digital Interface Board.

The 3 Volt supply for the ADC10D040 is provided by linear regulator U3, an LM1117 (or LM317). This voltage should be set with VR2 to 3.0V ±0.1V on either side of choke L4 or L5.

The supply voltages are protected by shunt diodes and can be measured at TP6, TP7 and TP8. The 3V supply can be measured on either end of chokes L4 and L5.

4.8 Power Requirements

Voltage and current requirements for the ADC10D040 Evaluation Board mode are:

- +5.0V at 100 mA [pin 1 of P1]
- +5.0V at 100mA (600mA when connected to the Digital Interface Board) [pin 3 of P1].

There is no need for a negative supply on this board.

5.0 Installing the ADC10D040 Evaluation Board

The evaluation board requires power supplies as described in Section 4.8. An appropriate signal source should be connected to the Analog Input BNC J1 (See Section 4.1.2). When evaluating dynamic performance (SINAD, SNR, THD, SFDR), an appropriate signal

generator (such as the HP3325B, HP4662A) with 50-Ohm source impedance should be connected to the Analog Input BNC J1 or J2 through an appropriate bandpass filter. Even the best signal generators available can not produce a signal pure enough to adequately evaluate the dynamic performance of an ADC.

If this board is used in conjunction with the Digital Interface Board and WaveVision™ software, a cable with a DB-9 connector must be connected between the Digital Interface Board and the host computer. See the Digital Interface Board manual for details.

6.0 Obtaining Best Results

Many factors go into reasonable data capture when evaluating an ADC. These include, but are not limited to, such things as PCB layout, clock timing, the ratio between the input frequency and sample rate and the FFT windowing technique.

Here we include very brief discussions on clock timing adjustments as it relates to the ADC10D040 and of sampling and FFT windowing.

6.1 Clock Timing

Because of differing delays in the clock signal and the data from the ADC, at some sample rates the data from the ADC may be latched as it is changing, leading to corrupted data, one example of which is seen in *Figure 2*, which shows the poor data capture of a 4.7MHz signal at 12.5Msps that results from poor timing of the clock and external latch signals relative to each other.

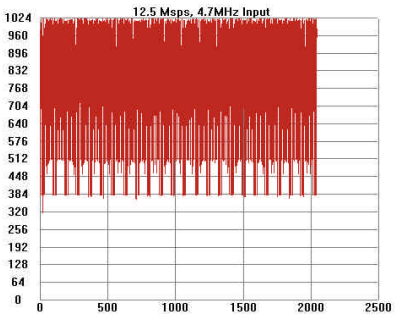


Figure 2. Bad data capture of a 4.7MHz input signal at 12.5Msps due to attempted capture at data transition.

Shorting jumpers JS1 and JS2 are provided to allow a change in the clock timing to avoid this problem. If the data seems corrupted, put a shorting jumper on JS1. If this does not improve the situation, move the shorting jumper to JS2. For some sample rates it may be necessary to put shorting jumpers on both JS1 and JS2.

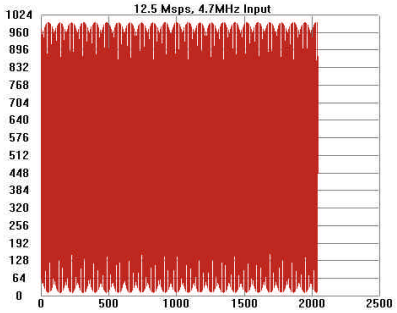


Figure 3. Good data capture of a 4.7MHz input signal at 12.5Msps

Figure 3 shows a good data capture of 4.7MHz input at 12.5Msps with a shorting jumper on JS1.

6.2 Coherent Sampling

Artifacts can result when we perform an FFT on a digitized waveform, producing inconsistent results when performing repeated testing. The presence of these artifacts means that the ADC under test may perform better than the measurements would indicate.

We can eliminate the need for windowing and get more consistent results if we observe the proper ratios between the input and sampling frequencies. This greatly increases the spectral resolution of the FFT, allowing us to more accurately evaluate the spectral response of the A/D converter. When we do this, however, we must be sure that the input signal has high spectral purity and stability and that the sampling clock signal is extremely stable with minimal jitter.

Coherent sampling of a periodic waveform occurs when a prime integer number of cycles exists in the sample window. The relationship between the number of cycles sampled (CY), the number of samples taken (SS), the signal input frequency (f_{in}) and the sample rate (f_S), for coherent sampling, is

$$\frac{CY}{SS} = \frac{f_{in}}{f_s}$$

CY, the number of cycles in the data record, must be a prime integer number and SS, the number of samples in the data record, must be a factor of 2 integer.

Further, f_{in} (signal input frequency) and f_S (sampling rate) should be locked to each other. If these frequencies are locked to each other, whatever frequency instability (jitter) is present in one of the signal is present in the other signal and these jitter terms will cancel each other.

Windowing (an FFT Option under WaveVision™) should be turned off for coherent sampling. The results of coherent sampling can be seen in the FFT plot seen in *Figure 4*. Note how narrow is the bin (how fine are the

lines) in this plot as compared with the flots of *Figures 5* thtoufh *7*.

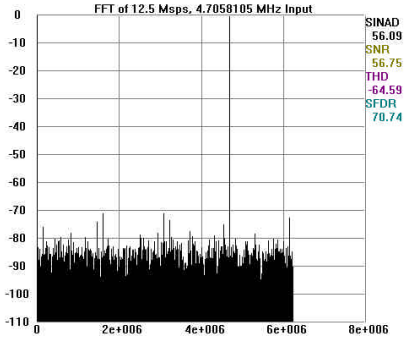


Figure 4. Coherent sampling will indicate accurate dynamic performance of the ADC

6.3 FFT Windowing Technique

The FFT assumes the waveform being evaluated is repetative and that it extends from -∞ to +∞ in time. In order to make the evaluated signal appear as though it extends from -∞ to +∞, FFT algorithms fold the signal such that the last point in the data record is followed by the first point. To the extent that this is true, there will be no discontinuities in the folded waveform.

However, folded waveforms often have a discontinuity and this leads to erroneous dynamic performance measurements. This is shown in *Figure 5*, where we see poor, inaccurate dynamic performance measurements at the upper right corner, as well as a spreading around the input frequency. This spreading is called "leakage".

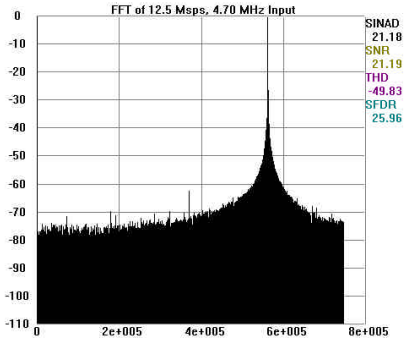


Figure 5. A discontinuity in the folded finite-time waveform leads to misleading results in the FFT.

There are many windowing techniques in use today to minimize this problem. *Figure 6* shows an FFT plot of the same data used in *Figure 5*, but using the Hanning windowing function. Note the improved dynamic performance over no windowing as in *Figure 5*.

The Flat-Top windowing function even yields similar dynamic performance measurements, as can be seen in *Figure 7*. Compare the dynamic performance parameters of *Figures 6 and 7* with those of coherent sampling (*Figure 4*).

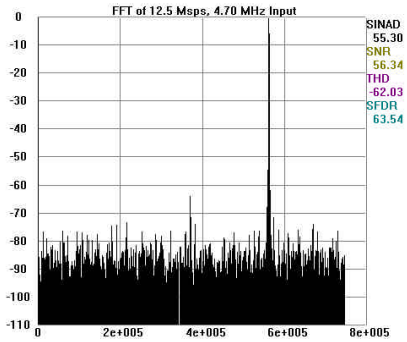


Figure 6. Windowing will reduce the effects of waveform folding. The Hanning windowing function is used here.

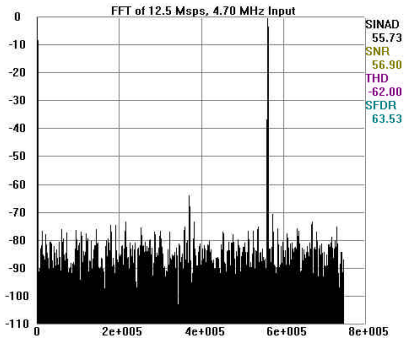


Figure 7. The Flat-Top windowing function yields slightly improved dynamic performance measurements over the Hanning function.

7.0 Evaluation Board Specifications

Board Size:	6.0" x 4.6" (15.2cm x 11.7cm)
Power Requirements:	+5.0V @ 100 mA
	+5V @ 100 mA / 600mA (see Section 4.8)
Clock Frequency Range:	1.0 MHz to 40 MHz
Analog Input	
Nominal Voltage:	$0.5V_{P-P}$, or $1V_{P-P}$
Impedance:	50 Ohms

8.0 Hardware Schematic

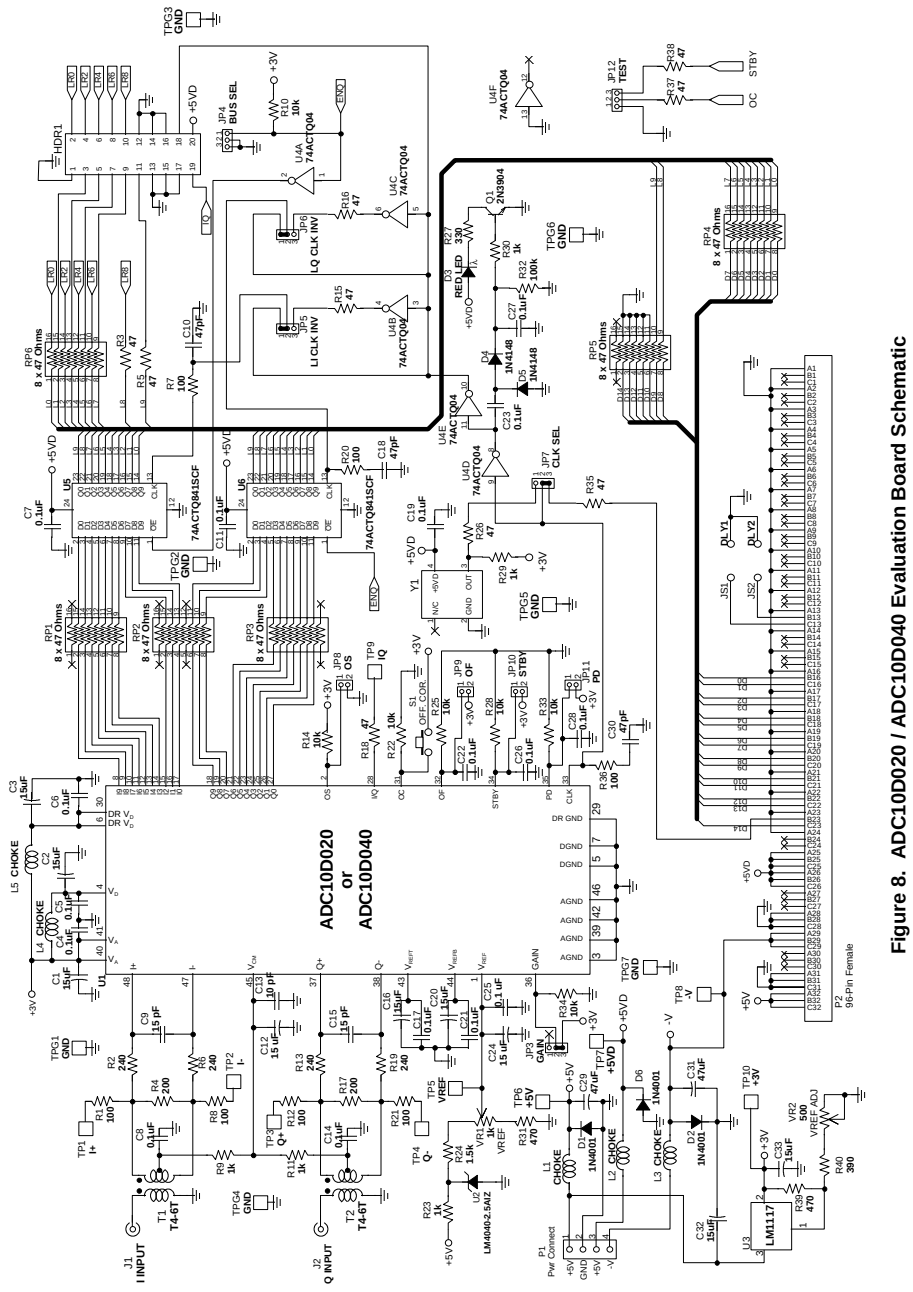


Figure 8. ADC10D020 / ADC10D040 Evaluation Board Schematic

9.0 Evaluation Board Bill of Materials

Item	Qty	Reference	Part	
1	9	C1, C2, C3, C12, C16, C20, C24, C32, C33	15uF, 6.3v	Type 7343 (D Size)
2	17	C4, C5, C6, C7, C8, C11, C13, C14, C17, C19, C21, C22, C23, C25, C26, C27, C28	0.1uF	Type 1206
3	2	C9, C15	15pF	Type 1206
4	3	C10, C18, C30	47pF	Type 1206
5	2	C29, C31	47uF, 6.3V	Type 7343 (D Size)
6	3	D1, D2, D6	1N4001	Various
7	1	D3	RED LED	DigiKey # 160-1124-ND
8	2	D4, D5	1N4148	Various
9	1	HDR1	2 X 10 Pin Post Header	DigiKey # S2012-10-ND
10	-	JP1, JP2, JP12	not used	n/a
11	5	JP3, JP4, JP5, JP6, JP7	3-Pin Post Headers	DigiKey # A19351-ND
12	6	JP8, JP9, JP10, JP11, JS1, JS2	2-Pin Post Headers	DigiKey # A19350-ND
13	2	J1, J2	BNC Connectors	DigiKey # ARF1177-ND
14	5	L1, L2, L3, L4, L5	CHOKE	DigiKey # M2204-ND
15	2	P1	Terminal Block	DigiKey # ED1609-ND
16	1	P2	96-Pin Female	DigiKey # H7096-ND
17	1	Q1	2N3904	Various
18	6	RP1, RP2, RP3, RP4, RP5, RP6	Resistor Pack - 8 x 47 Ohms	DigiKey # 766-163-R47-ND
19	2	R37, R38	not used	n/a
20	7	R3, R5, R15, R16, R18, R26, R35	47, 5%	Type 1206
21	7	R1, R7, R8, R12, R20, R21, R36	100, 5%	Type 1206
22	2	R4, R17	200, 5%	Type 1206
23	4	R2, R6, R13, R19	240, 5%	Type 1206
24	1	R27	330, 5%	Type 1206
25	1	R40	390, 5%	Type 1206
26	2	R31, R39	470, 5%	Type 1206
27	5	R9, R11, R23, R29, R30	1K, 5%	Type 1206
28	1	R24	1.5K, 5%	Type 1206
29	7	R10, R14, R22, R25, R28, R33, R34	10k, 5%	Type 1206
30	1	R32	100k, 5%	Type 1206
31	1	S1	n.o. SPST Switch	Key # CKN9016-ND or CKN9017-ND
32	1	VR1	1K	DigiKey # 3386F-102-ND
33	1	VR2	500	DigiKey # 3386F-501-ND
34	1	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TPG1, TPG2, TPG3, TPG4, TPG5, TPG6, TPG7	Breakable Header	DigiKey # S1012-36-ND
35	2	T1, T2	Signal Transformer	MiniCircuits type T4-6T
36	1	U1	ADC10D020CIVS or ADC10D040CIVS	National Semiconductor
37	1	U2	LM4040-2.5AIZ	National Semiconductor
38	1	U3	LM1117T	National Semiconductor
39	1	U4	74ACTQ04PC	various
41	2	U5, U6	74ACTQ841SPC	Fairchild Semiconductor
42	1	Y1	20MHz Oscillator (ADC10D020) **or** 40MHz Oscillator (ADC10D040)	DigiKey # CTX119-ND **or** DigiKey # CTX120-ND
43	1	Y1	6-pin Socket for Transformer	DigiKey # AE8906-ND

APPENDIX

A1.0 Operating in the Computer Mode

The ADC10D040 Evaluation Board is compatible with the WaveVision™ Digital Interface Board and WaveVision™ software. When connected to the Digital Interface Board, data capture is easily controlled from a personal computer operating in the Windows environment. The data samples that are captured can be observed on the PC video monitor in the time and frequency domains. The FFT analysis of the captured data yields insight into system noise and distortion sources and estimates of ADC dynamic performance such as SINAD, SNR and THD. A histogram of the data can also be displayed.

See the Digital Interface Board manual for more information.

A2.0 Summary Tables of Test Points and Connectors

Note: Pin 1 of jumpers can be identified by their square solder pad.

P1 Connector - Power Supply Connections

J1-1	+V	Positive Power Supply
J1-2	GND	Power Supply Ground
J1-3	+5V	+5.0V Logic Power Supply for Digital Interface Board
J1-4	-V	Optional Negative Power Supply for Breadboard Area

Test Points on the ADC10D040 Evaluation Board

TP1	I+ Input Test Point
TP2	I- Input Test Point
TP3	Q+ Input Test Point
TP4	Q- Input Test Point
TP5	Reference Voltage Test Point
TP6	+5V (analog) Test Point
TP7	+5VD (digital) Test Point
TP8	Negative supply Test Point (not needed for this board)
TP9	I/Q Signal Output Test Point
TPG1 - TPG7	Ground Test Points

JP1, JP2 and JP12 are not used.

JP3 Jumper - GAIN Select

Connect 1-2	Peak-to-Peak Input levels at J1 & J2 are $V_{REF}/2$ (0.5 V_{P-P} with V_{REF} = 1.0 V)
Connect 2-3	Peak-to-Peak Input levels at J1 & J2 are V_{REF} (1.0 V_{P-P} with V_{REF} = 1.0 V) [default]

JP4 Jumper - ADC Input Select

Connect 1-2	Select the ADC Q-Bus output
Connect 2-3	Select the ADC I-Bus output

JP5 & JP6 Jumpers - Latch Clock Sense (JP5 for I-Bus, JP6 for Q-Bus)

Connect 1-2	Clock not inverted
Connect 2-3	Clock inverted

JP7 Jumper - ADC Clock selection jumper settings

Connect 1-2	Use crystal oscillator Y1
Connect 2-3	Use Clock signal from P2 pin B23 (default)

JP8 Jumper - Output select (OS) Control.

No Connection	Parallel Mode - I-Channel and Q-Channel data on their respective buses
Connect 1-2	Multiplexed Mode - I-Channel and Q-Channel data multiplexed onto I-Bus

JP9 Jumper - Output Format (OF) Control.

No Connection	Binary output data format (default)
Connect 1-2	2' Complement output data format

JP10 Jumper - Standby Control.

No Connection	Normal Operation
Connect 1-2	ADC in Standby mode

JP11 Jumper - Power-Down Control.

No Connection	Normal Operation
Connect 1-2	ADC in Power-Down mode

P2 Connector - ADC Data Outputs - Connection to WaveVision™ Digital Interface Board

Signal	P2 pin number
ADC output D0	B16
ADC output D1	C16
ADC output D2	B17
ADC output D3	C17
ADC output D4	B18
ADC output D5	C18
ADC output D6	B19
ADC output D7	C19
ADC output D8	B20
ADC output D9	C20
ADC output D10	B21 (not used for this board)
ADC output D11	C21 (not used for this board)
GND	A1 thru A24, A28, B28, C28, A31, B31, C31
ADC Output Enable	C12 (not used)
External clock input	B23
Reserved, signal	B22, C22, C23
Reserved, power	A25, A26, B25, B26, C25, C26 (+5V Logic Power Supply to Digital Interface Board)
Reserved, power	A29, B29, C29
Reserved, power	A32, B32, C32

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