

# ADC12D1x00RF Reference Board

## REFERENCE DESIGN

### SPECIAL NOTES

These schematics reflect the current state of product development. This design had NOT yet been fully tested at the time these schematics were generated.

Since this product is in development, the user of this document is strongly advised to check for the latest revision.

National Semiconductor reserves the right to make changes to this product.

ALL parts labeled "NA" are NOT ASSEMBLED.


**Print Instructions:**

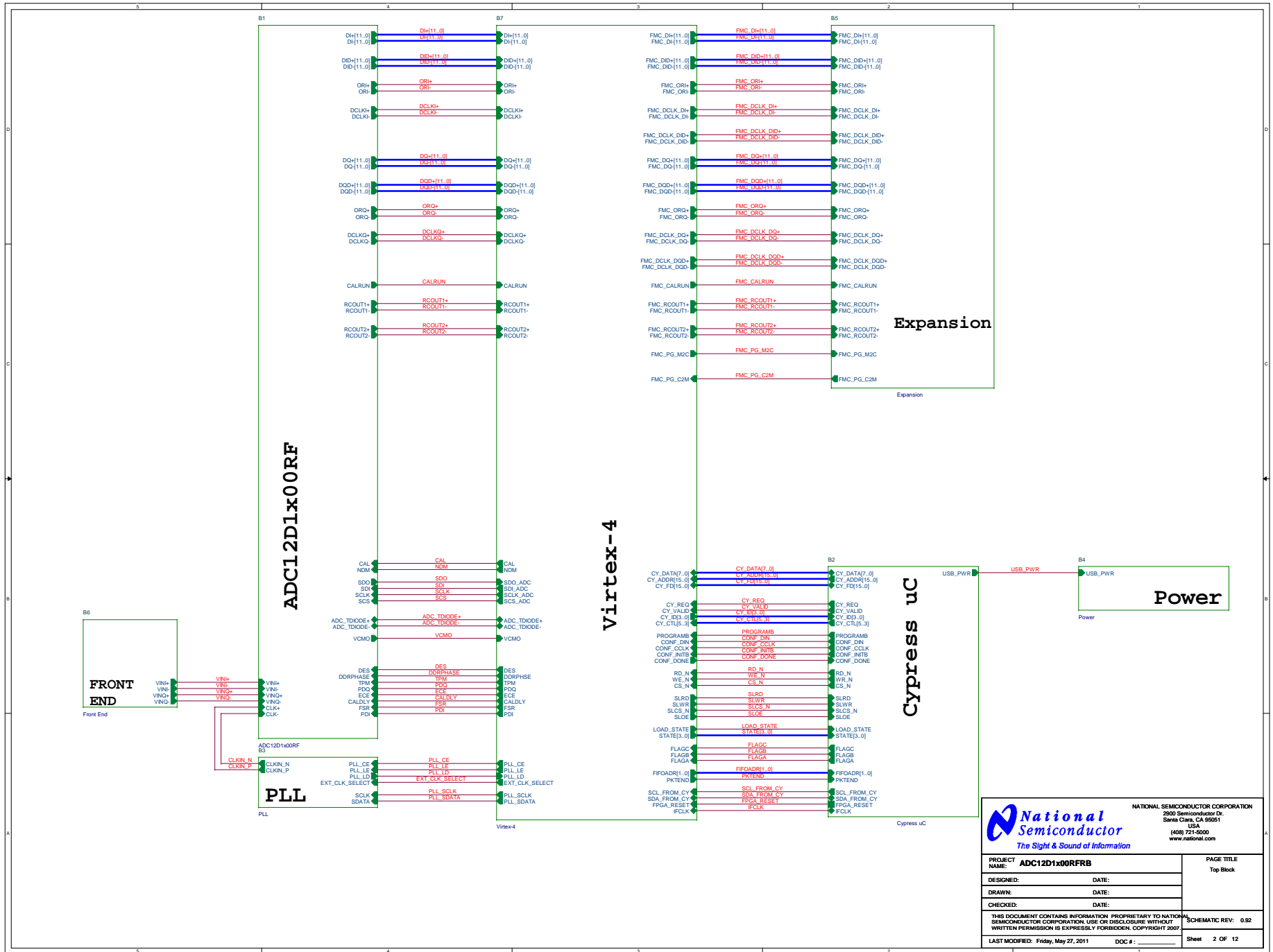
- To create a readable printout, we recommend to use A3 or 11x17" paper size.
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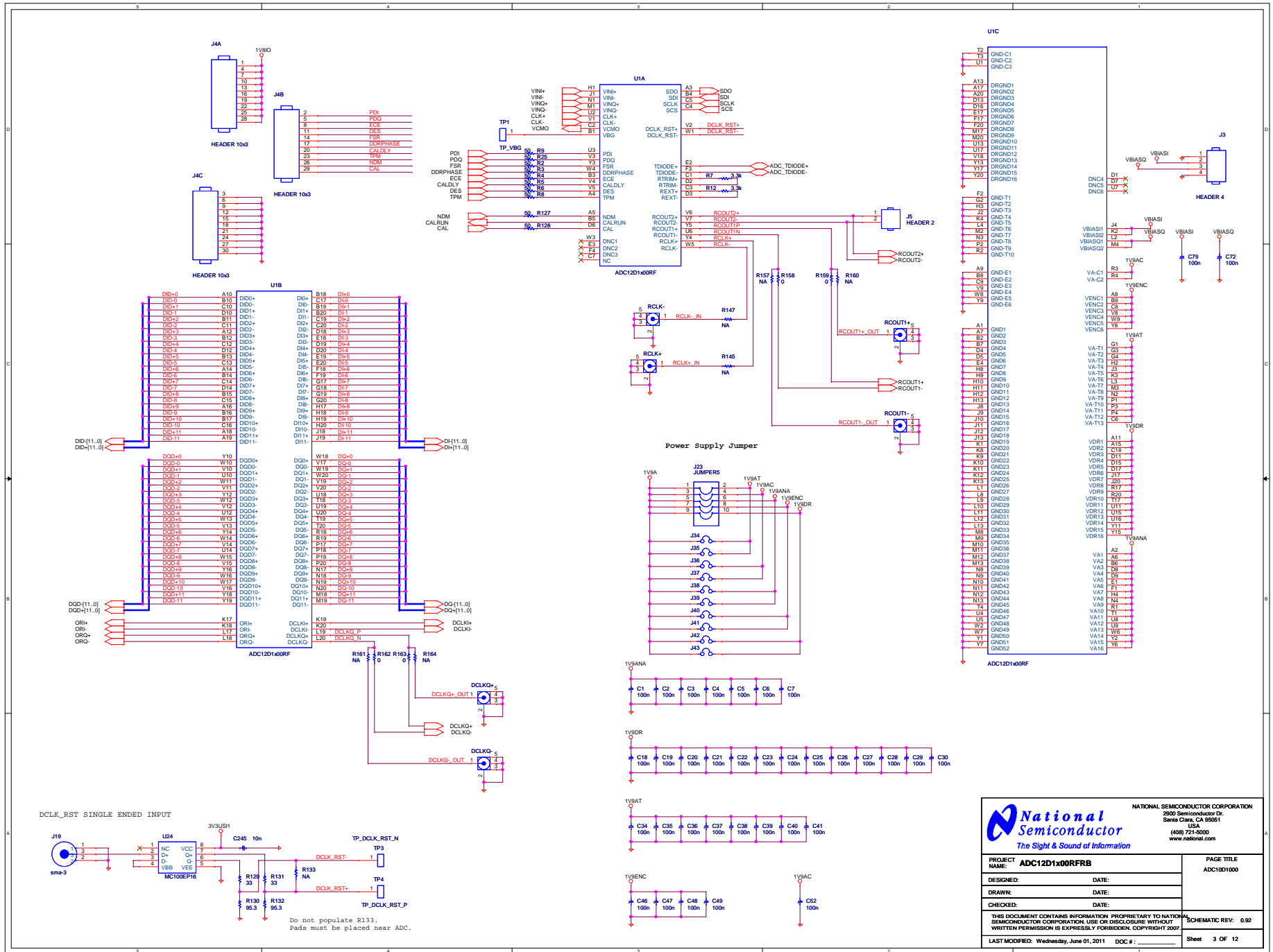
# PRELIMINARY

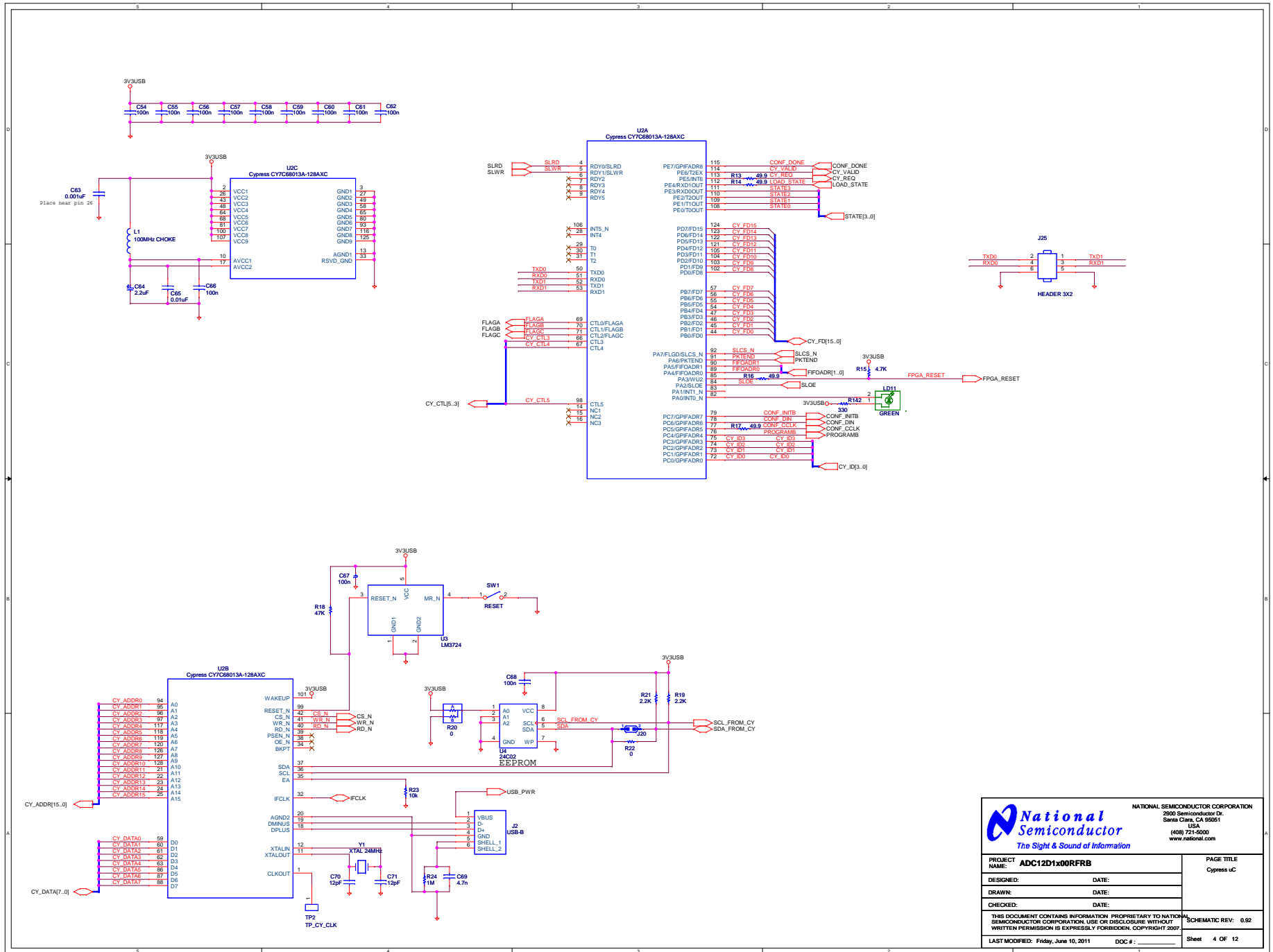
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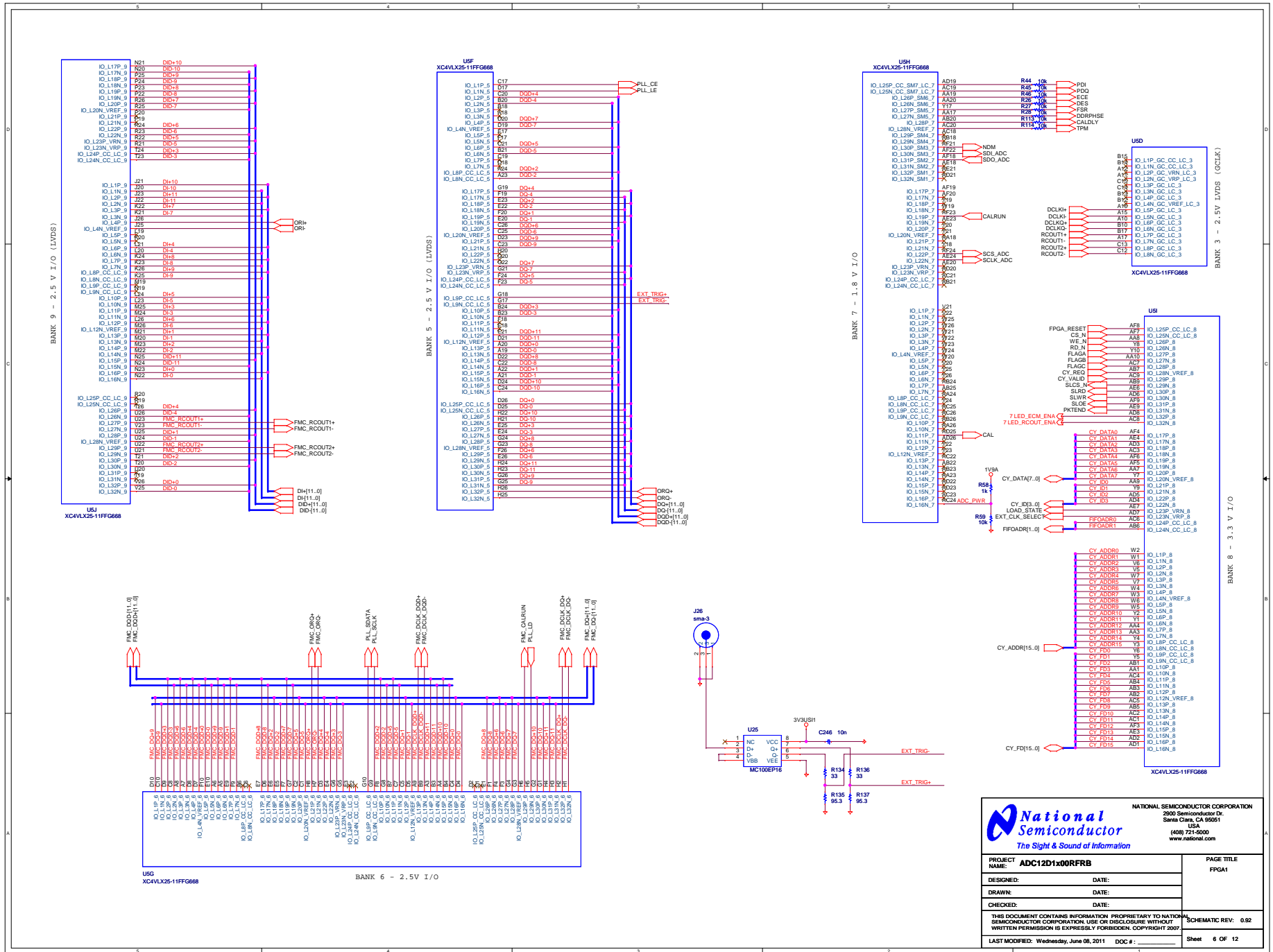


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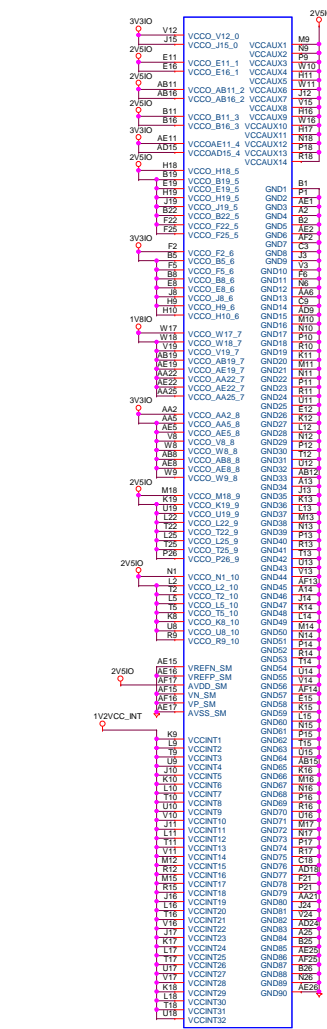
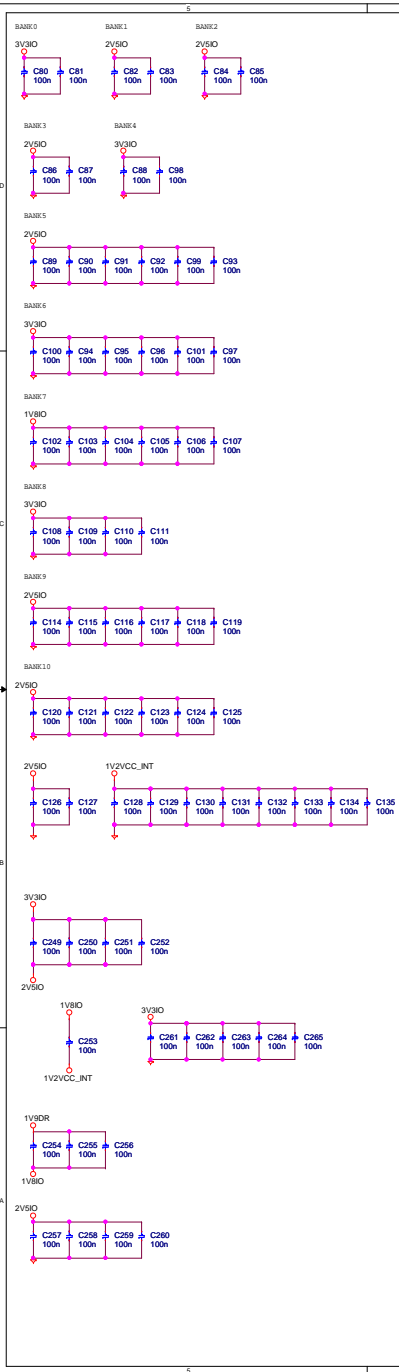




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USL  
XC4VLX25-11FFG668

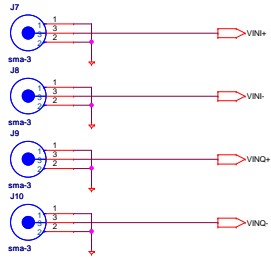
BANK #	BANK SUPPLY	INTERFACE
1	2V5IO	Clock Generator
2	2V5IO	Test Headers, Temp. Sensor
3	2V5IO	Cypress, LEDs, 100MHz Oscillator
4	3V3IO	ADC DCLK (LVDS)
5	2V5IO	ADC Q-Channel (LVDS)
6	3V3IO	USI-1 Header
7	1V8IO	ADC Control
8	3V3IO	Cypress, LEDs
9	2V5IO	ADC I-Channel (LVDS)
10	2V5IO	Logic Analyzer Header

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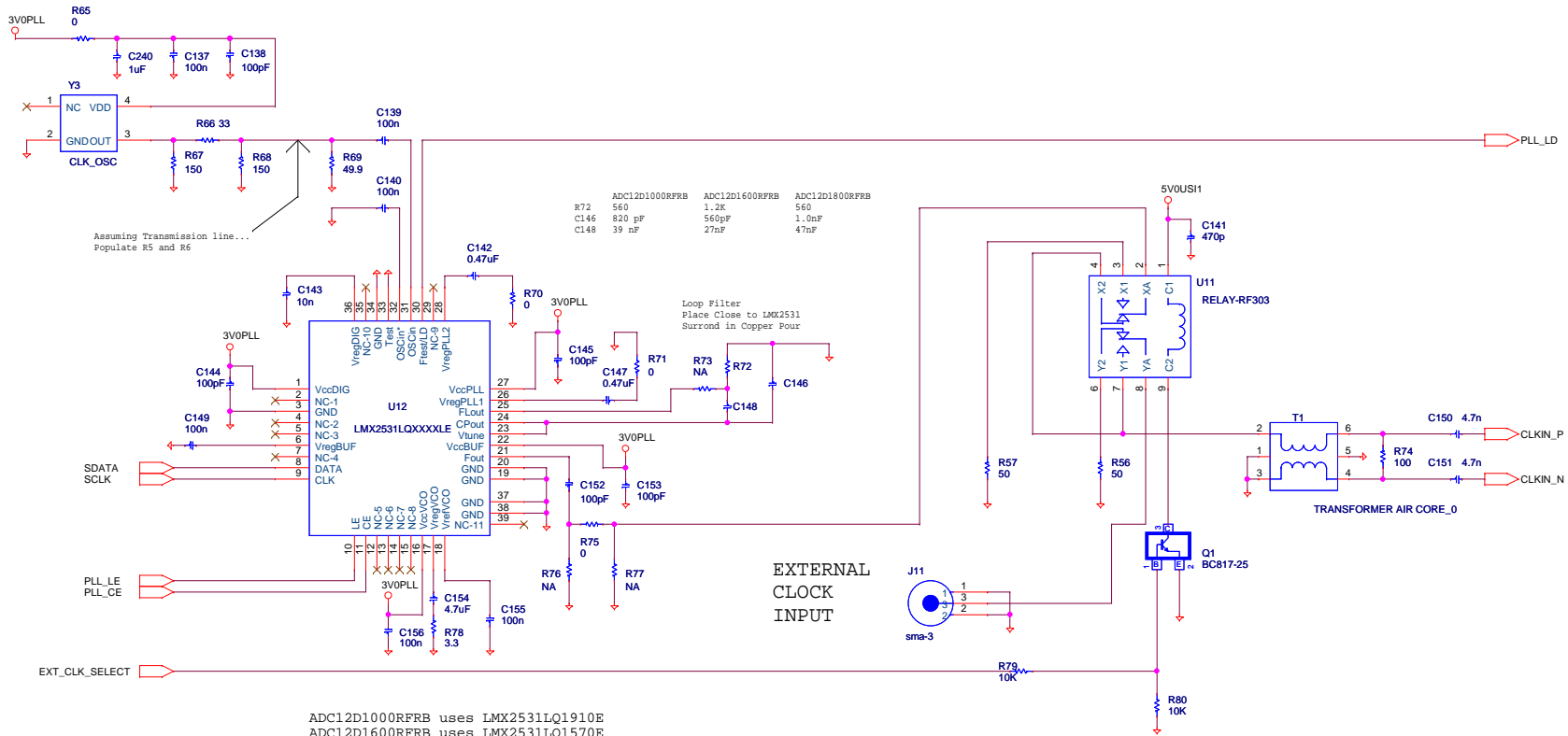
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Impedance test connectors

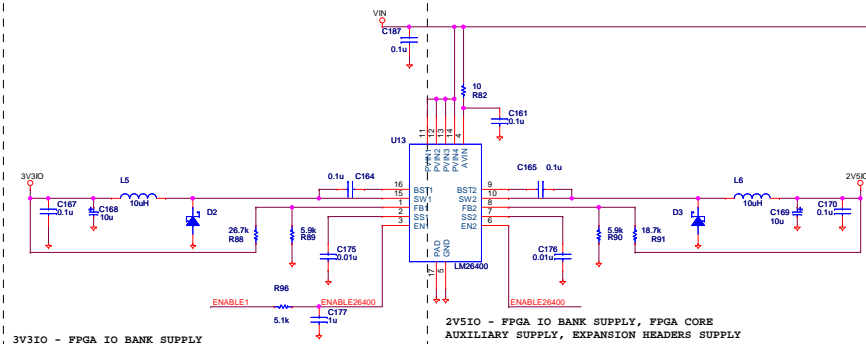
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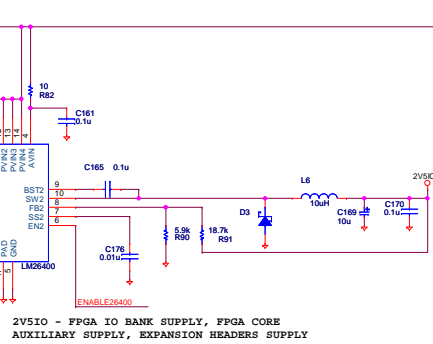
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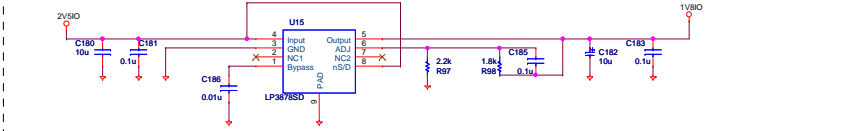
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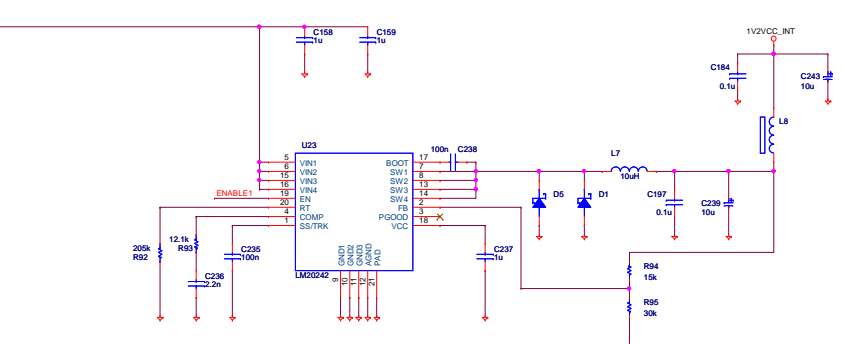
3V3IO - FPGA IO BANK SUPPLY



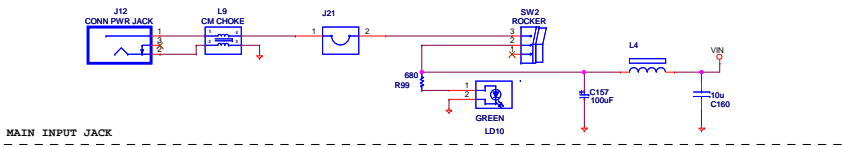
2V5IO - FPGA IO BANK SUPPLY, FPGA CORE AUXILIARY SUPPLY, EXPANSION HEADERS SUPPLY



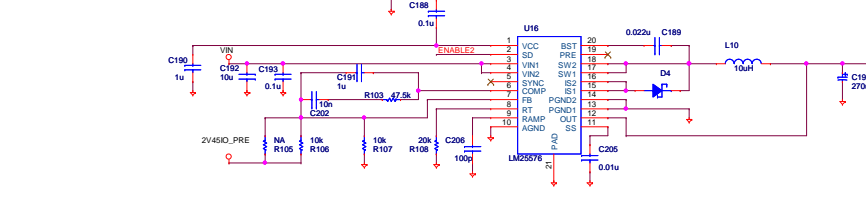
1V8IO - ADC IO SUPPLY, FPGA IO BANK SUPPLY



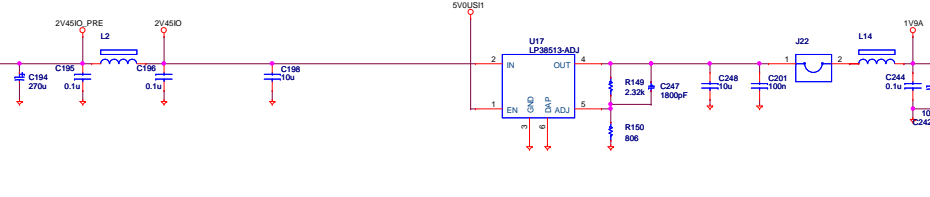
1V2VCC\_INT - FPGA CORE SUPPLY

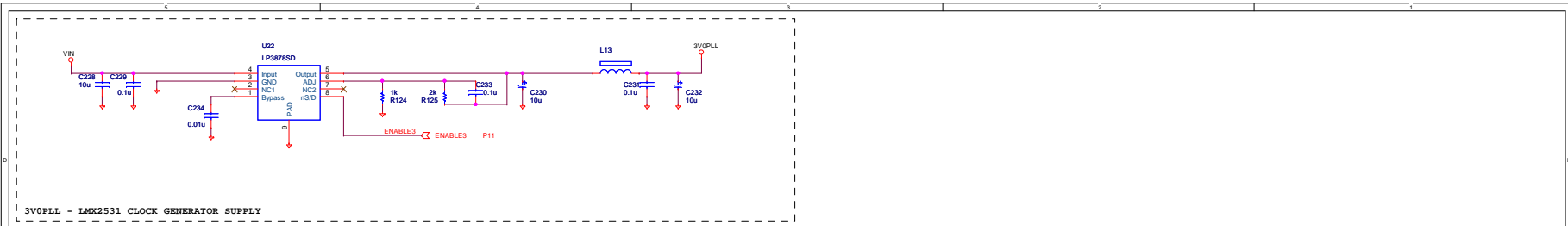


MAIN INPUT JACK

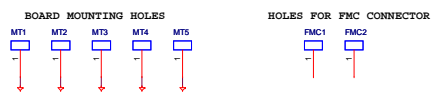



2V45IO/2V45\_PRE - NOT USED (INTERMEDIATE SUPPLY ONLY)





3V0PLL - LMX2531 CLOCK GENERATOR SUPPLY



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