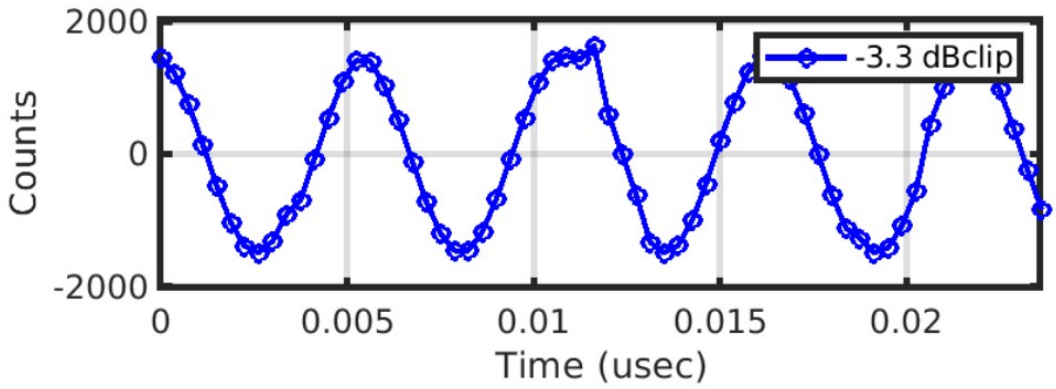
Hardware Setup:

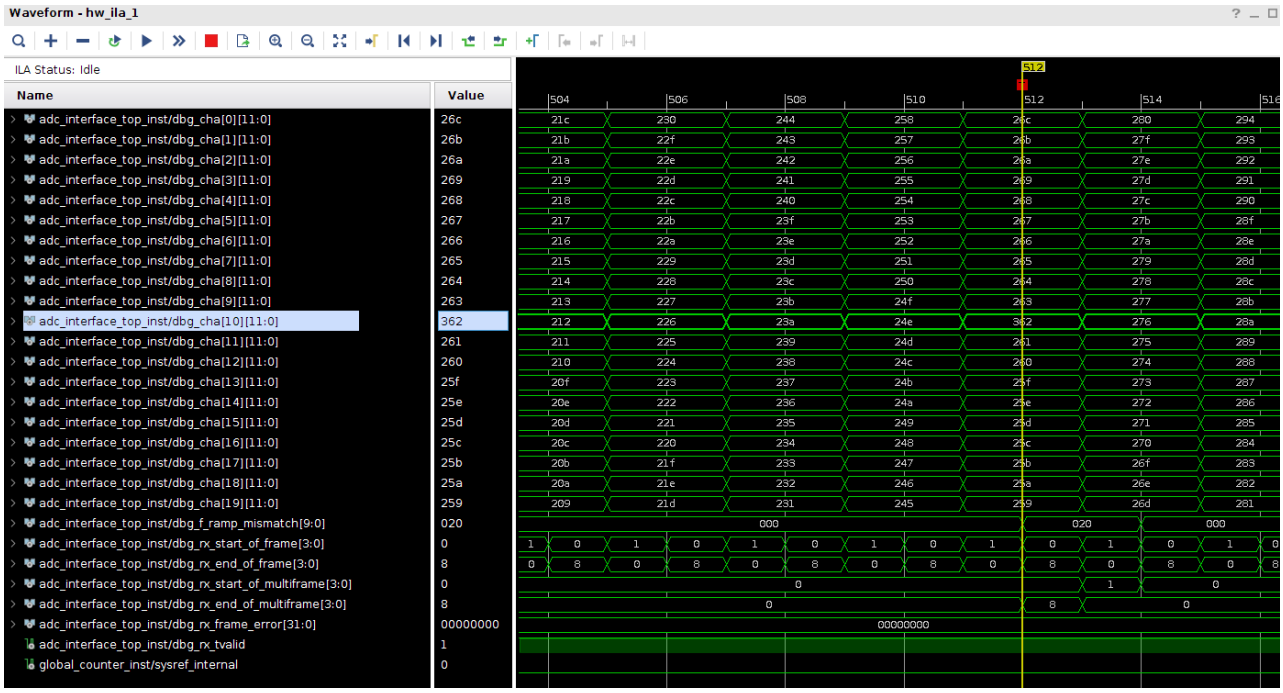
- ADC32RF45 is connected to a Xilinx Kintex Ultrascale FPGA on a custom PCB.
- Sampling frequency is 2666.667 MHz.
- ADC is set up in 82820 DDC bypass mode.
- JESD line rate is 10.667 Gbps.
- SYSREF frequency is 2.0833 MHz (FPGA is the source).
- Xilinx JESD204 Core was created using Vivado 2018.2.

Issue description:

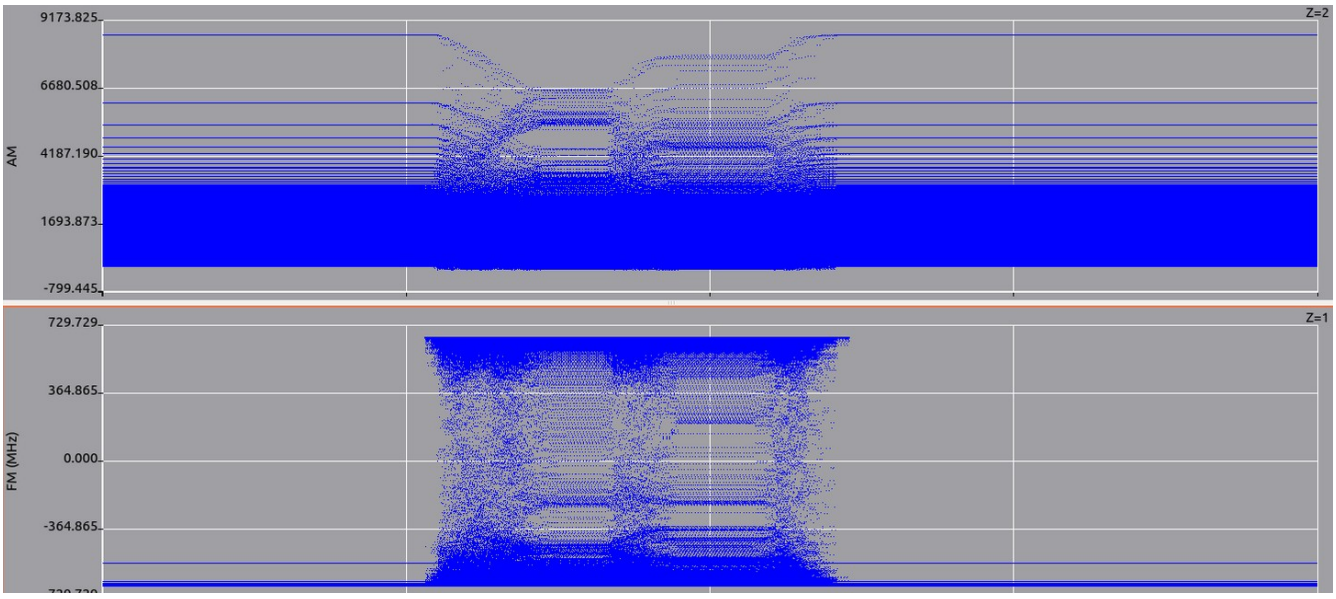
- Batch runs were created to sweep across ADC bandwidth at 5 MHz increments in an attempt to characterize the performance. At each frequency about 20,000 samples were collected for processing. On around 3% of the collects, errors were observed in the sinusoids. An example can be seen on the peak of the middle sinusoid below. The error occurrences were seemingly random and not frequency dependent.



- After placing the ADC in ramp mode, similar errors were observed. The ILA (Internal Logic Analyzer) capture below was triggered when the ramp mismatch checking logic asserted.



- No communication errors were reported by the JESD core, though an issue with the core has not been ruled out.
- 10 ms of ADC ramp data was collected, and a ~1068 us segment of bad ramp data was observed in the middle of the good ramp data. It was interesting to see that the ramp signal degrades for a while before recovering.



- Here is a list of tests that were performed in an attempt to fix this issue:
  - Altered JESD output voltage swing.
  - Altered de-emphasis settings.
  - Upgraded FPGA JESD core to latest revision.
  - Altered SYSREF generation logic to run off of JESD core clock output.
  - Altered SYSREF frequency to other frequencies supported by SBAA221 (ADC SYSREF Appnote).
  - Changed ADC configuration script to better follow Table 103 in SBAS747B (ADC spec).