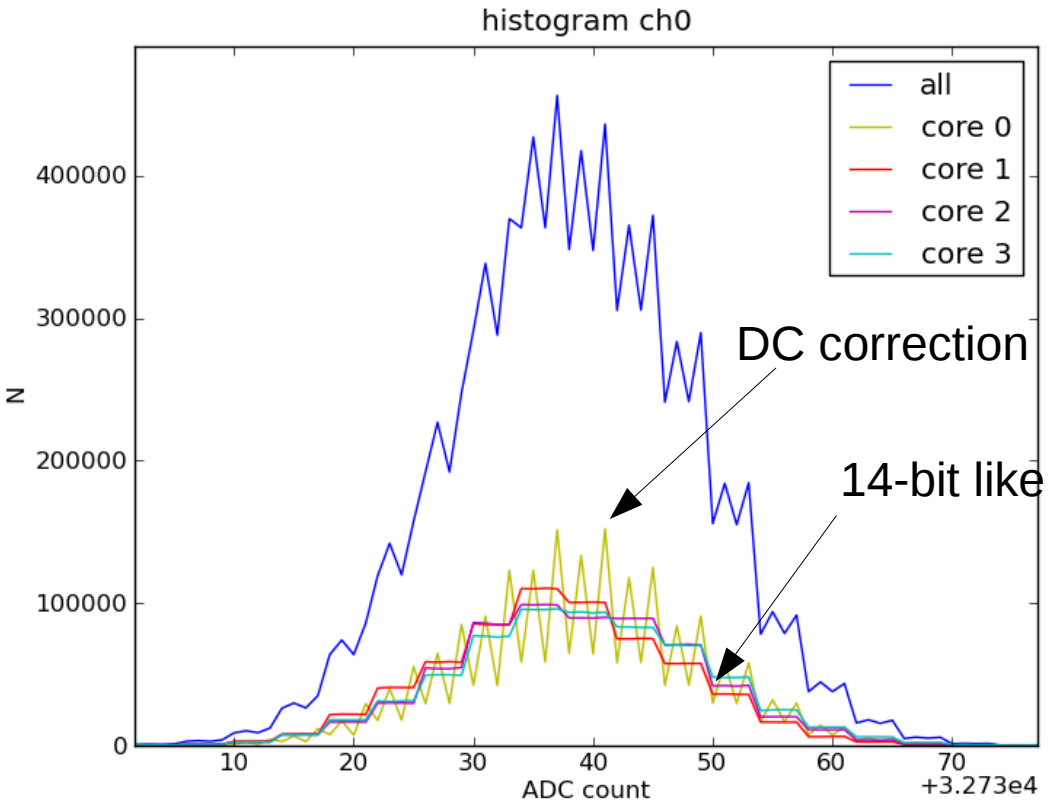
Problems with the ADS54J60

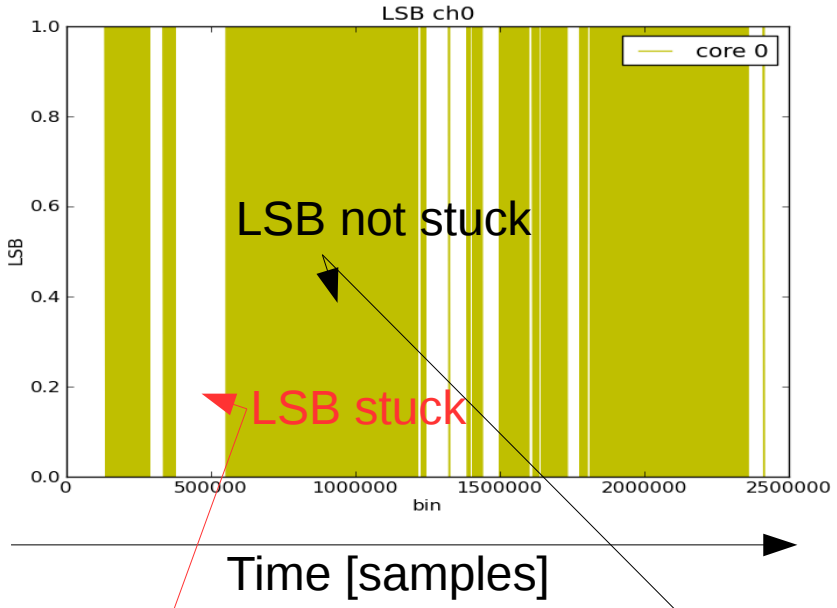
- 2 nested issues
- 1) DC correction infers strange behavior on **one** out of the 4 interleaving cores
- 2) The ADCs 2 LSB are random → 14-bit like

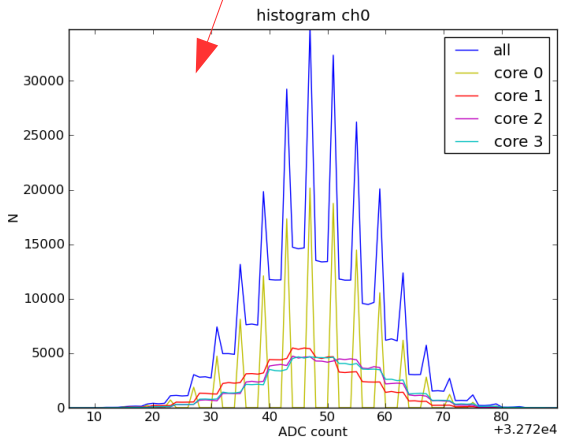
Histogram of ADC values on 50ohm terminated input

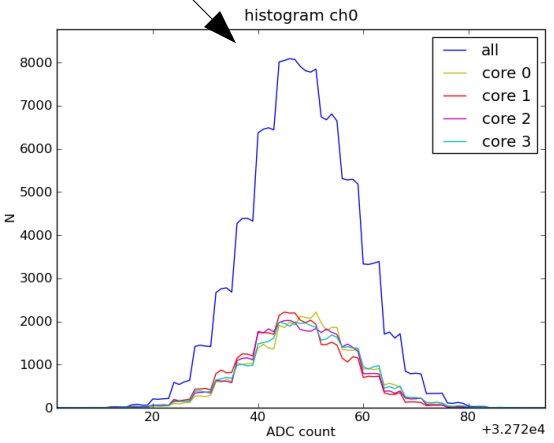


DC correction problem

LSB bit value on core 0
(out of 4 interleaving cores)





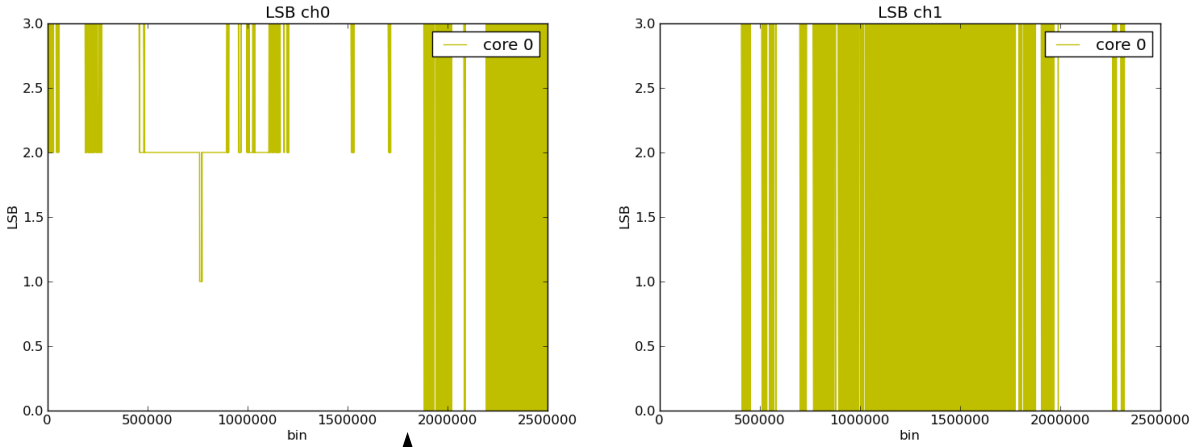


- Periods of LSB being stuck and not are interleaving rapidly
- 2 LSB of core 0 goes through large periods of being stuck at a constant value

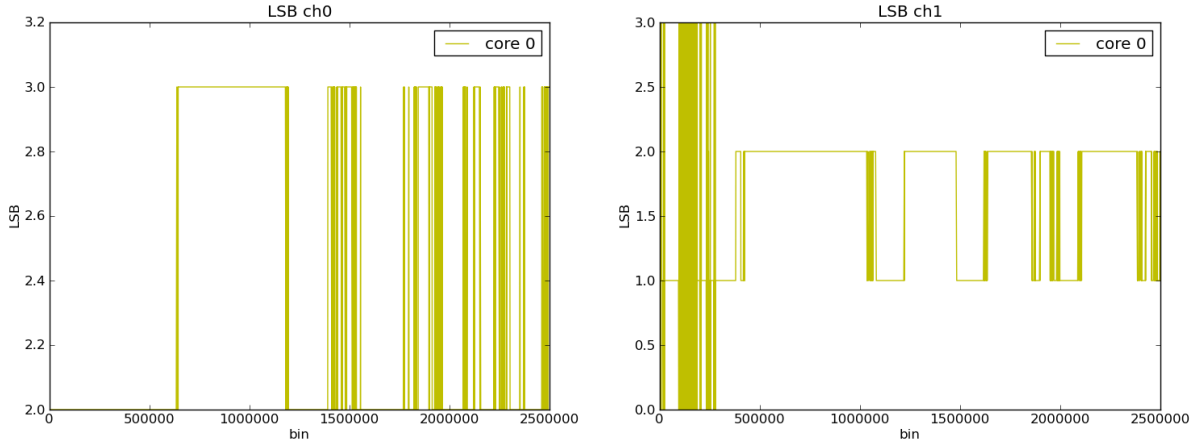
  11b in this case

DC correction problem

2 LSB bit value on core 0
(out of 4 interleaving cores)



2 consecutive power cycles

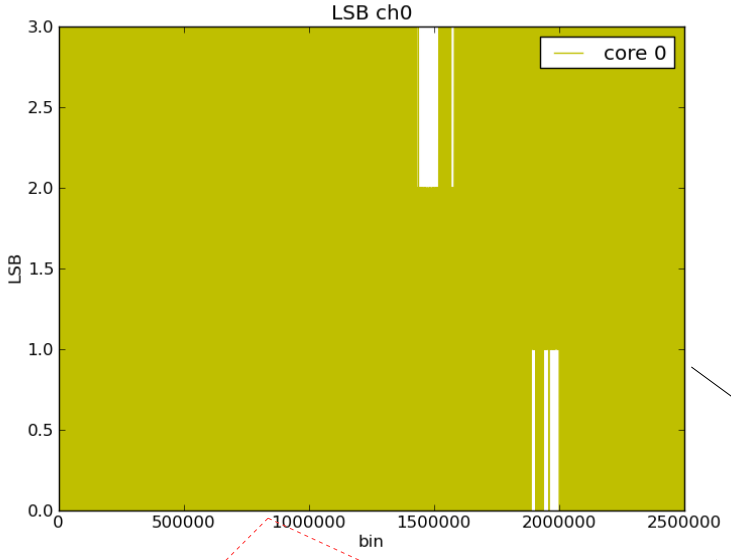


Core 0 of both ADS54J60 channels at the same time

- Other stuck values than 11 are also possible
- Changes from power cycle to power cycle

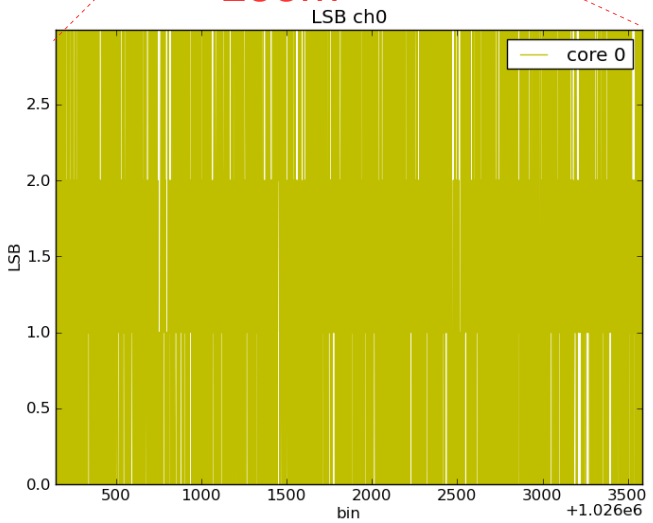
Digital gain

LSB bit value on core 0
(out of 4 interleaving cores)

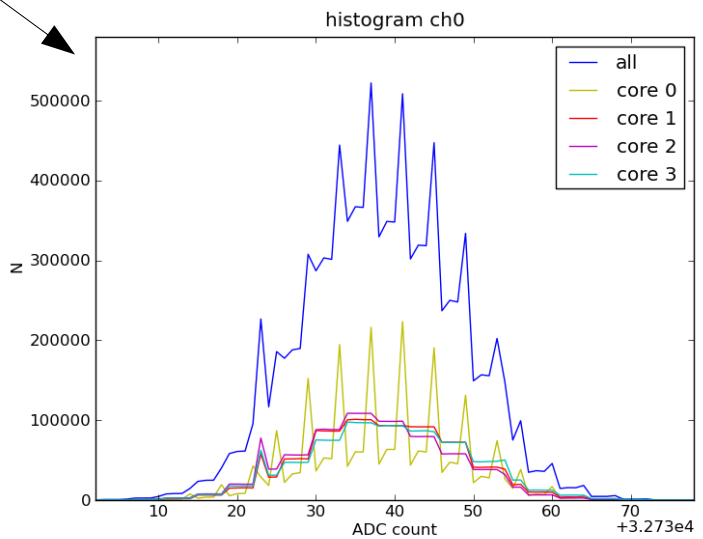


Time [samples]

zoom

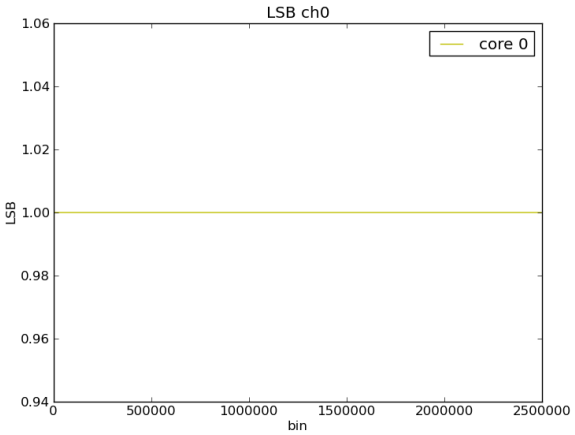


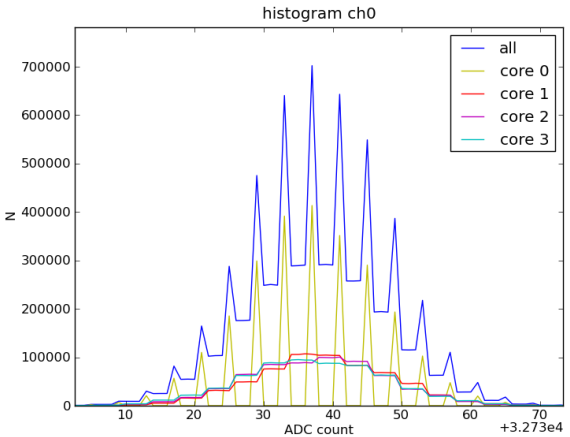
- Changing digital gain register to 0x1f changes the oscillation properties from “macroscopic” to “microscopic”



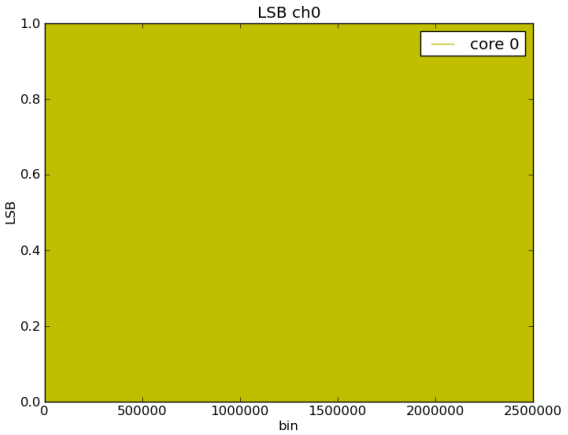
DC correction freeze

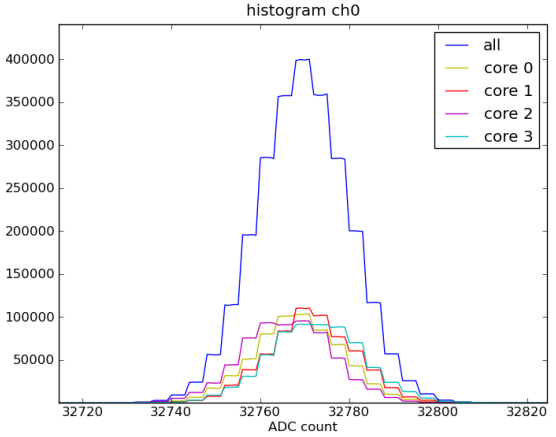
Sometimes freezes stuck





Sometimes freezes not stuck

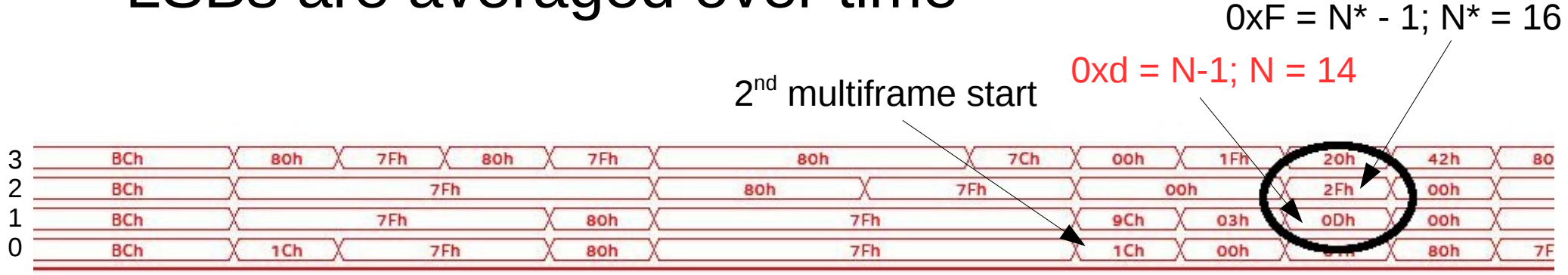




- Freezing the DC correction via **undocumented registers** results in stuck or not stuck state being conserved (which is probably dependent on when the DC correction is frozen)

14-bit problem

- ADS54J60 = 16-bit ADC
  - Die marking: AZ54J60 TI 614 ZFR7 G4
  - Page 0x61 reg 0xF read = 0x0
- JESD ILAS reports on **all** lanes N* = 16, **N = 14**!!!!!
- It is obvious from the preceding plots that the 2 LSBs are averaged over time



System description

- Abaco FMC-120 carrier (2x ADS54J60)
- DC coupled
- 650 MHz sampling clock, on-board
- 20.3125 MHz SYSREF
- Reception by Arria V JESD204B core
- LMFS = 4211 per ADS54J60, K = 32
- 50 Ohm terminated inputs (no signal, no offset)

Powerup sequence

- * power up (power to FMC, PG to FMC, ADC amp ON)
- * clock setup (650MHz sample,
- * continuous SYSREF
-
- * ADC hardware reset by toggling pin
- sleep 1s
- 0x0000 0x81 # soft reset ADC
- sleep 1s
- 0x0011 0x80 # select master page
- 0x004f 0x1 # DC coupling
- 0x4001 0x0 # erase page regs
- 0x4002 0x0 # erase page regs
- 0x4005 0x0 # erase page regs
- 0x4003 0x0 # select main digital
- 0x6004 0x68
- 0x60f7 0x1 # digital reset
- 0x6000 0x1 # pulse the apply bit
- 0x6000 0x0
- 0x0011 0x80 # select master page
- 0x0059 0x20 # must write 1
- 0x4003 0x0 # select JESD digital
- 0x4004 0x69
- 0x6000 0x80 # K sel enable
- 0x6001 0x04 # 4 lanes
- 0x6005 0x00 # no scrambler
- 0x4003 0x0 # select JESD analog
- 0x4004 0x6a
- 0x6012 0x2 # always write 1 to deemphasis
- 0x6016 0x2 # PLL 40x
- 0x6017 0x40 # PLL reset toggle
- 0x6017 0x0
- 0x4003 0x0 # select main digital
- 0x4004 0x68
- 0x6043 0x1 # offset binary format
- 0x604B 0x20 # offset sel enable
- #0x6052 0x1 # enable digital gain (optional)
- #0x6044 0x1f # dig gain set (optional)
- 0x60ab 0x1 # LSB select enable
- 0x60ad 0x0 # LSB data
- 0x6000 0x1 # pulse the apply bit
- 0x6000 0x0
- 0x4003 0x0 # select JESD digital
- 0x4004 0x69
- 0x6006 0x1f # set K = 32
-
- * disable continuous SYSREF
- * start JESD204B receiver core configuration
- * 2 SYSREF pulses during the CGS