



**Figure 61. Continuous SPI Read (RW\_CONT = 1, SPI\_REG\_READ = 1)**

The following lines show 20 consecutive responses of the AFE4410 chip to an attempt to read 6 registers in continuous mode via SPI. Responses are in hexadecimal format. The first 3 bytes should be ignored, because these are the bytes received when the master sends the address of the first read register. We left them, because they might be helpful in identifying the problem.

```
010F00 000002100002800003200003C00002B000032
003500 000002100002800003200003C00002B000032
003500 000002100002800003200003C00002B000032
003500 000002100002800003200003C00002B000032
003500 000002100002800003200003C00002B000032
003500 000002100002800003200003C00002B000032
003500 000002100002800003200003C00002B000032
003500 000002100002800003200003C00002B000032
003500 000002100002800003200003C00002B000032
003500 000002100002800003200003C00002B000032
003500 000002100002800003200003C00002B000032
350000 0002100002800003200003C00002B00003200
350000 0002100002800003200003C00002B00003200
350000 0002100002800003200003C00002B00003200
350000 0002100002800003200003C00002B00003200
350000 0002100002800003200003C00002B00003200
350000 0002100002800003200003C00002B00003200
350000 0002100002800003200003C00002B00003200
350000 0002100002800003200003C00002B00003200
350000 0002100002800003200003C00002B00003200
350000 0002100002800003200003C00002B00003200
```

The first register to read is LED2STC (01h). The value that was actually written to this register is bolded. The next bytes after bold are the values that were written to the next five registers.

There is no other SPI communication between readouts, and the SEN pin is pulled down for transmission, and pulled up between transmissions.

The question is - why that one-byte offset occurs? It would be easy to bypass, however the offset is not always present.