```
\\START: Doing Link up Sequence


\\START: Freeze RX IQMC/LO


\\START: Overriding TDD Pins internally

SPIWrite 0014,04,0,7    //PAGE: TIMING_CON=0x1;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0124,01,0,7    //use_reg_txon_AB=0x1;  Address(0x124[0:0],)
SPIWrite 0126,01,0,7    //use_reg_rxon_AB=0x1;  Address(0x124[16:16],)
SPIWrite 0128,01,0,7    //use_reg_fbon_AB=0x1;  Address(0x128[0:0],)
SPIWrite 012a,01,0,7    //use_reg_txon_CD=0x1;  Address(0x128[16:16],)
SPIWrite 012c,01,0,7    //use_reg_rxon_CD=0x1;  Address(0x12c[0:0],)
SPIWrite 012e,01,0,7    //use_reg_fbon_CD=0x1;  Address(0x12c[16:16],)
SPIWrite 0125,00,0,7    //reg_for_txon_AB=0x0;  Address(0x124[8:8],)
SPIWrite 0127,01,0,7    //reg_for_rxon_AB=0x1;  Address(0x124[24:24],)
SPIWrite 0129,00,0,7    //reg_for_fbon_AB=0x0;  Address(0x128[8:8],)
SPIWrite 012b,00,0,7    //reg_for_txon_CD=0x0;  Address(0x128[24:24],)
SPIWrite 012d,01,0,7    //reg_for_rxon_CD=0x1;  Address(0x12c[8:8],)
SPIWrite 012f,00,0,7    //reg_for_fbon_CD=0x0;  Address(0x12c[24:24],)

\\END: Done overriding TDD Pins internally


WAIT 0.0001

SPIWrite 0014,00,0,7    //PAGE: TIMING_CON=0x0;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0013,20,0,7    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIWrite 01a3,00,0,7
SPIWrite 01a2,0f,0,7
SPIWrite 01a1,00,0,7
SPIWrite 01a0,00,0,7
SPIWrite 01a3,11,0,7
SPIWrite 01a2,0f,0,7
SPIWrite 01a1,00,0,7
SPIWrite 01a0,00,0,7

WAIT 0.02

SPIWrite 0013,00,0,7    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
SPIWrite 0018,10,0,7    //PAGE: rx_iqmc=0x1;    Address(0x18[4:4],)
SPIWrite 00bc,00,0,7
SPIWrite 00bd,00,0,7
SPIWrite 0024,00,0,7
SPIWrite 0030,01,0,7
SPIWrite 0018,00,0,7    //PAGE: rx_iqmc=0x0;    Address(0x18[4:4],)
SPIWrite 0010,04,0,7    //PAGE: rx_top=0x1;     Address(0x10[3:2],)
SPIWrite 0a05,00,0,7    //op_clk_en_iqmc_clk_gen=0x0;(Meaning: );   Address(0xa04[8:8],)
SPIWrite 0010,08,0,7    //PAGE: rx_top=0x2;     Address(0x10[3:2],)
SPIWrite 0a05,00,0,7    //op_clk_en_iqmc_clk_gen=0x0;(Meaning: );   Address(0xa04[8:8],)

\\END: Done Freeze RX IQMC/LO


\\START: Freeze TX IQMC/LO

SPIWrite 0010,00,0,7    //PAGE: rx_top=0x0;     Address(0x10[3:2],)
SPIWrite 0013,10,0,7    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)
SPIWrite 00a3,00,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,ff,0,7
SPIWrite 00a0,06,0,7
SPIWrite 0193,35,0,7

WAIT 0.02


\\END: Done Freeze TX IQMC/LO
```

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SPIWrite 0013,00,0,7    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
\\ STEP: jesdLinkUpInit/step0

\\START: Clearing JESD TX Init States

SPIWrite 0015,01,0,7    //PAGE: rx_jesd=0x3;    Address(0x15[0:0],0x15[4:4],)
SPIWrite 0015,11,0,7
SPIWrite 0045,c0,0,7    //init_state=0x1;(Meaning: );   Address(0x44[15:15],)
SPIWrite 0045,c0,0,7    //fb_init_state=0x1;(Meaning: );    Address(0x44[14:14],)
SPIWrite 0045,40,0,7    //init_state=0x0;(Meaning: );   Address(0x44[15:15],)
SPIWrite 0045,00,0,7    //fb_init_state=0x0;(Meaning: );    Address(0x44[14:14],)
SPIWrite 0077,00,0,7    //sysref_to_ddc_jesd_clk_div_override=0x0;  Address(0x74[26:26],)

\\END: Done clearing JESD TX Init States


\\START: Clearing JESD RX Init States

SPIWrite 0015,10,0,7    //PAGE: rx_jesd=0x0;    Address(0x15[0:0],0x15[4:4],)
SPIWrite 0015,00,0,7
SPIWrite 0015,02,0,7    //PAGE: tx_jesd=0x3;    Address(0x15[1:1],0x15[5:5],)
SPIWrite 0015,22,0,7
SPIWrite 0020,01,0,7    //init_state_tx0=0x1;(Meaning: );   Address(0x20[0:0],)
SPIWrite 0020,00,0,7    //init_state_tx0=0x0;(Meaning: );   Address(0x20[0:0],)
SPIWrite 0134,00,0,7    //sysref_to_dac_jesd_clk_div_override=0x0;  Address(0x134[2:2],)

\\END: Done clearing JESD RX Init States

SPIWrite 0015,20,0,7    //PAGE: tx_jesd=0x0;    Address(0x15[1:1],0x15[5:5],)
SPIWrite 0015,00,0,7
\\ STEP: jesdLinkUpInit/step1

\\START: Clearing Sysref Flags

SPIWrite 0015,01,0,7    //PAGE: rx_jesd=0x1;    Address(0x15[0:0],0x15[4:4],)
SPIWrite 0015,01,0,7
SPIWrite 00a8,f1,0,7    //clear_rx_root_clk_monitor_flag=0x1;   Address(0xa8[0:0],)
SPIWrite 00a8,f3,0,7    //clear_rx_root_sysref_monitor_flag=0x1;    Address(0xa8[1:1],)
SPIWrite 00a8,f7,0,7    //clear_fb_root_clk_monitor_flag=0x1;   Address(0xa8[2:2],)
SPIWrite 00a8,ff,0,7    //clear_fb_root_sysref_monitor_flag=0x1;    Address(0xa8[3:3],)
SPIWrite 00a8,fe,0,7    //clear_rx_root_clk_monitor_flag=0x0;   Address(0xa8[0:0],)
SPIWrite 00a8,fc,0,7    //clear_rx_root_sysref_monitor_flag=0x0;    Address(0xa8[1:1],)
SPIWrite 00a8,f8,0,7    //clear_fb_root_clk_monitor_flag=0x0;   Address(0xa8[2:2],)
SPIWrite 00a8,f0,0,7    //clear_fb_root_sysref_monitor_flag=0x0;    Address(0xa8[3:3],)
SPIWrite 0015,00,0,7    //PAGE: rx_jesd=0x0;    Address(0x15[0:0],0x15[4:4],)
SPIWrite 0015,00,0,7
SPIWrite 0011,f0,0,7    //PAGE: rx_ec_q=0xf;    Address(0x11[7:4],)
SPIWrite 053f,ff,0,7
SPIWrite 053e,ff,0,7
SPIWrite 053f,00,0,7
SPIWrite 053e,00,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,0f,0,7    //PAGE: rx_ec_i=0xf;    Address(0x11[3:0],)
SPIWrite 053f,ff,0,7
SPIWrite 053e,ff,0,7
SPIWrite 053f,00,0,7
SPIWrite 053e,00,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0017,01,0,7    //PAGE: dac_1t=0x1;     Address(0x17[3:0],)
SPIWrite 0050,00,0,7
SPIWrite 0050,80,0,7
SPIWrite 0050,00,0,7
SPIWrite 0017,00,0,7    //PAGE: dac_1t=0x0;     Address(0x17[3:0],)
SPIWrite 0017,10,0,7    //PAGE: dac_2t=0x1;     Address(0x17[5:4],)
SPIWrite 0030,00,0,7
SPIWrite 0030,08,0,7
SPIWrite 0030,00,0,7
SPIWrite 0017,20,0,7    //PAGE: dac_2t=0x2;     Address(0x17[5:4],)
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SPIWrite 0030,00,0,7
SPIWrite 0030,08,0,7
SPIWrite 0030,00,0,7
SPIWrite 0017,00,0,7    //PAGE: dac_2t=0x0;     Address(0x17[5:4],)
SPIWrite 0017,40,0,7    //PAGE: ana_2r=0x1;     Address(0x17[7:6],)
SPIWrite 002b,00,0,7
SPIWrite 002b,08,0,7
SPIWrite 002b,00,0,7
SPIWrite 0017,80,0,7    //PAGE: ana_2r=0x2;     Address(0x17[7:6],)
SPIWrite 002b,00,0,7
SPIWrite 002b,08,0,7
SPIWrite 002b,00,0,7
SPIWrite 0017,40,0,7    //PAGE: ana_2r=0x1;     Address(0x17[7:6],)
SPIWrite 002e,00,0,7
SPIWrite 002e,08,0,7
SPIWrite 002e,00,0,7
SPIWrite 0017,80,0,7    //PAGE: ana_2r=0x2;     Address(0x17[7:6],)
SPIWrite 002e,00,0,7
SPIWrite 002e,08,0,7
SPIWrite 002e,00,0,7
SPIWrite 0118,07,0,7
SPIWrite 0119,7f,0,7
SPIWrite 0117,10,0,7
SPIWrite 0116,00,0,7

\\END: Done clearing Sysref Flags

SPIWrite 0017,00,0,7    //PAGE: ana_2r=0x0;     Address(0x17[7:6],)
\\ STEP: jesdLinkUpInit/step2

\\START: Sending Sysref to device from Pin/SPI


\\START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 01d4,01,0,7    //pll_reg_spi_req_a=0x1;    Address(0x1d4[0:0],)
SPIWrite 0374,00,0,7    //pll_reg_spi_req_b1=0x0;(Meaning: );   Address(0x374[0:0],)

SPIPoll 01d5,0,0,1


\\Read  pll_reg_spi_a_ack=0x1;  Address(0x1d4[8:8],)


\\END: Done requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0014,01,0,7    //PAGE: clktop_2t=0x1;  Address(0x14[1:0],)
SPIWrite 002c,00,0,7    //TRIM_100N_INT_TXCMLLDOVREF1=0x0;  Address(0x2c[7:5],)

WAIT 0.001

SPIWrite 0014,00,0,7    //PAGE: clktop_2t=0x0;  Address(0x14[1:0],)
SPIWrite 0014,04,0,7    //PAGE: TIMING_CON=0x1;(Meaning: );     Address(0x14[2:2],)
SPIWrite 04d1,00,0,7    //count_len_sysref=0xbf;    Address(0x4d0[15:0],)
SPIWrite 04d0,bf,0,7
SPIWrite 0717,00,0,7    //spare_reg_port=0x0;   Address(0x714[31:0],)
SPIWrite 0716,00,0,7
SPIWrite 0715,00,0,7
SPIWrite 0714,00,0,7
SPIWrite 0717,00,0,7    //spare_reg_port=0x101;     Address(0x714[31:0],)
SPIWrite 0716,00,0,7
SPIWrite 0715,01,0,7
SPIWrite 0714,01,0,7
SPIWrite 0717,00,0,7    //spare_reg_port=0x0;   Address(0x714[31:0],)
SPIWrite 0716,00,0,7
SPIWrite 0715,00,0,7
SPIWrite 0714,00,0,7
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SPIWrite 0014,00,0,7    //PAGE: TIMING_CON=0x0;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0014,08,0,7    //PAGE: pll=0x1;    Address(0x14[7:3],)
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 0051,86,0,7    //SYS_REF_FROM_PIN_BYPAS=0x1;   Address(0x50[15:15],)
SPIWrite 0051,8e,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x1;    Address(0x50[11:11],)
SPIWrite 0014,10,0,7    //PAGE: pll=0x2;    Address(0x14[7:3],)
SPIWrite 004e,30,0,7    //lcmgen_usespisysref=0x0;  Address(0x4c[18:18],)
SPIWrite 0014,08,0,7    //PAGE: pll=0x1;    Address(0x14[7:3],)
SPIWrite 004e,30,0,7    //lcmgen_div=0xbf;  Address(0x4c[17:2],)
SPIWrite 004d,02,0,7
SPIWrite 004c,fc,0,7
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 004c,fd,0,7    //lcmgen_sync_ena=0x1;  Address(0x4c[0:0],)
SPIWrite 0014,10,0,7    //PAGE: pll=0x2;    Address(0x14[7:3],)
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 0051,84,0,7    //SYS_REF_FROM_PIN_BYPAS=0x1;   Address(0x50[15:15],)
SPIWrite 0051,8c,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x1;    Address(0x50[11:11],)
SPIWrite 004e,30,0,7    //lcmgen_usespisysref=0x0;  Address(0x4c[18:18],)
SPIWrite 004e,30,0,7    //lcmgen_div=0xbf;  Address(0x4c[17:2],)
SPIWrite 004d,02,0,7
SPIWrite 004c,fc,0,7
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 004c,fd,0,7    //lcmgen_sync_ena=0x1;  Address(0x4c[0:0],)
SPIWrite 0014,20,0,7    //PAGE: pll=0x4;    Address(0x14[7:3],)
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 0051,86,0,7    //SYS_REF_FROM_PIN_BYPAS=0x1;   Address(0x50[15:15],)
SPIWrite 0051,8e,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x1;    Address(0x50[11:11],)
SPIWrite 0014,10,0,7    //PAGE: pll=0x2;    Address(0x14[7:3],)
SPIWrite 004e,30,0,7    //lcmgen_usespisysref=0x0;  Address(0x4c[18:18],)
SPIWrite 0014,20,0,7    //PAGE: pll=0x4;    Address(0x14[7:3],)
SPIWrite 004e,30,0,7    //lcmgen_div=0xbf;  Address(0x4c[17:2],)
SPIWrite 004d,02,0,7
SPIWrite 004c,fc,0,7
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 004c,fd,0,7    //lcmgen_sync_ena=0x1;  Address(0x4c[0:0],)
SPIWrite 0014,40,0,7    //PAGE: pll=0x8;    Address(0x14[7:3],)
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 0051,86,0,7    //SYS_REF_FROM_PIN_BYPAS=0x1;   Address(0x50[15:15],)
SPIWrite 0051,8e,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x1;    Address(0x50[11:11],)
SPIWrite 0014,10,0,7    //PAGE: pll=0x2;    Address(0x14[7:3],)
SPIWrite 004e,30,0,7    //lcmgen_usespisysref=0x0;  Address(0x4c[18:18],)
SPIWrite 0014,40,0,7    //PAGE: pll=0x8;    Address(0x14[7:3],)
SPIWrite 004e,30,0,7    //lcmgen_div=0xbf;  Address(0x4c[17:2],)
SPIWrite 004d,02,0,7
SPIWrite 004c,fc,0,7
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 004c,fd,0,7    //lcmgen_sync_ena=0x1;  Address(0x4c[0:0],)
SPIWrite 0014,80,0,7    //PAGE: pll=0x10;   Address(0x14[7:3],)
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 0051,86,0,7    //SYS_REF_FROM_PIN_BYPAS=0x1;   Address(0x50[15:15],)
SPIWrite 0051,8e,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x1;    Address(0x50[11:11],)
SPIWrite 0014,10,0,7    //PAGE: pll=0x2;    Address(0x14[7:3],)
SPIWrite 004e,30,0,7    //lcmgen_usespisysref=0x0;  Address(0x4c[18:18],)
SPIWrite 0014,80,0,7    //PAGE: pll=0x10;   Address(0x14[7:3],)
SPIWrite 004e,30,0,7    //lcmgen_div=0xbf;  Address(0x4c[17:2],)
SPIWrite 004d,02,0,7
SPIWrite 004c,fc,0,7
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 004c,fd,0,7    //lcmgen_sync_ena=0x1;  Address(0x4c[0:0],)

\\Give Sysref Here.


WAIT 0.001

SPIWrite 0014,08,0,7    //PAGE: pll=0x1;    Address(0x14[7:3],)
SPIWrite 0051,0e,0,7    //SYS_REF_FROM_PIN_BYPAS=0x0;   Address(0x50[15:15],)
SPIWrite 0051,06,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x0;    Address(0x50[11:11],)
SPIWrite 0014,10,0,7    //PAGE: pll=0x2;    Address(0x14[7:3],)
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SPIWrite 0051,0c,0,7    //SYS_REF_FROM_PIN_BYPAS=0x0;   Address(0x50[15:15],)
SPIWrite 0051,04,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x0;    Address(0x50[11:11],)
SPIWrite 0014,20,0,7    //PAGE: pll=0x4;    Address(0x14[7:3],)
SPIWrite 0051,0e,0,7    //SYS_REF_FROM_PIN_BYPAS=0x0;   Address(0x50[15:15],)
SPIWrite 0051,06,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x0;    Address(0x50[11:11],)
SPIWrite 0014,40,0,7    //PAGE: pll=0x8;    Address(0x14[7:3],)
SPIWrite 0051,0e,0,7    //SYS_REF_FROM_PIN_BYPAS=0x0;   Address(0x50[15:15],)
SPIWrite 0051,06,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x0;    Address(0x50[11:11],)
SPIWrite 0014,80,0,7    //PAGE: pll=0x10;   Address(0x14[7:3],)
SPIWrite 0051,0e,0,7    //SYS_REF_FROM_PIN_BYPAS=0x0;   Address(0x50[15:15],)
SPIWrite 0051,06,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x0;    Address(0x50[11:11],)
SPIWrite 0014,00,0,7    //PAGE: pll=0x0;    Address(0x14[7:3],)
SPIWrite 0014,01,0,7    //PAGE: clktop_2t=0x1;  Address(0x14[1:0],)
SPIWrite 002c,00,0,7    //TRIM_100N_INT_TXCMLLDOVREF1=0x0;  Address(0x2c[7:5],)

\\START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0014,00,0,7    //PAGE: clktop_2t=0x0;  Address(0x14[1:0],)
SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 01d4,00,0,7    //pll_reg_spi_req_a=0x0;    Address(0x1d4[0:0],)
SPIWrite 0374,00,0,7    //pll_reg_spi_req_b1=0x0;(Meaning: );   Address(0x374[0:0],)

WAIT 0.01


\\END: Done requesting/releasing SPI Access to PLL Pages


\\END: Done sending Sysref to device from Pin/SPI


\\START: Staggered TDD Toggle

SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0014,04,0,7    //PAGE: TIMING_CON=0x1;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0124,01,0,7    //use_reg_txon_AB=0x1;  Address(0x124[0:0],)
SPIWrite 0126,01,0,7    //use_reg_rxon_AB=0x1;  Address(0x124[16:16],)
SPIWrite 0128,01,0,7    //use_reg_fbon_AB=0x1;  Address(0x128[0:0],)
SPIWrite 012a,01,0,7    //use_reg_txon_CD=0x1;  Address(0x128[16:16],)
SPIWrite 012c,01,0,7    //use_reg_rxon_CD=0x1;  Address(0x12c[0:0],)
SPIWrite 012e,01,0,7    //use_reg_fbon_CD=0x1;  Address(0x12c[16:16],)
SPIWrite 0127,00,0,7    //reg_for_rxon_AB=0x0;  Address(0x124[24:24],)
SPIWrite 012d,00,0,7    //reg_for_rxon_CD=0x0;  Address(0x12c[8:8],)
SPIWrite 0127,01,0,7    //reg_for_rxon_AB=0x1;  Address(0x124[24:24],)
SPIWrite 012d,01,0,7    //reg_for_rxon_CD=0x1;  Address(0x12c[8:8],)
SPIWrite 0127,00,0,7    //reg_for_rxon_AB=0x0;  Address(0x124[24:24],)
SPIWrite 012d,00,0,7    //reg_for_rxon_CD=0x0;  Address(0x12c[8:8],)
SPIWrite 0125,00,0,7    //reg_for_txon_AB=0x0;  Address(0x124[8:8],)
SPIWrite 012b,00,0,7    //reg_for_txon_CD=0x0;  Address(0x128[24:24],)
SPIWrite 0129,00,0,7    //reg_for_fbon_AB=0x0;  Address(0x128[8:8],)
SPIWrite 012f,00,0,7    //reg_for_fbon_CD=0x0;  Address(0x12c[24:24],)
SPIWrite 0125,01,0,7    //reg_for_txon_AB=0x1;  Address(0x124[8:8],)
SPIWrite 012b,01,0,7    //reg_for_txon_CD=0x1;  Address(0x128[24:24],)
SPIWrite 0129,01,0,7    //reg_for_fbon_AB=0x1;  Address(0x128[8:8],)
SPIWrite 012f,01,0,7    //reg_for_fbon_CD=0x1;  Address(0x12c[24:24],)

\\END: Done Staggered TDD Toggle

SPIWrite 0014,00,0,7    //PAGE: TIMING_CON=0x0;(Meaning: );     Address(0x14[2:2],)
\\ STEP: jesdLinkUpInit/step3

\\START: Checking Sysref Flags

SPIWrite 0017,40,0,7    //PAGE: ana_2r=0x1;     Address(0x17[7:6],)
SPIReadCheck 0049,0,1,03

\\Read  pi_from_rx_2r_rxab_ro_bits_0=0xf;   Address(0x48[15:8],)

SPIWrite 0017,80,0,7    //PAGE: ana_2r=0x2;     Address(0x17[7:6],)
```

```
SPIReadCheck 0049,0,1,03

\\Read  pi_from_rx_2r_rxab_ro_bits_0=0xf;   Address(0x48[15:8],)

SPIWrite 0017,40,0,7    //PAGE: ana_2r=0x1;     Address(0x17[7:6],)
SPIReadCheck 0049,3,3,08

\\Read  pi_from_rx_2r_rxab_ro_bits_0=0xf;   Address(0x48[15:8],)

SPIWrite 0017,80,0,7    //PAGE: ana_2r=0x2;     Address(0x17[7:6],)
SPIReadCheck 0049,3,3,08

\\Read  pi_from_rx_2r_rxab_ro_bits_0=0xf;   Address(0x48[15:8],)

SPIWrite 0017,00,0,7    //PAGE: ana_2r=0x0;     Address(0x17[7:6],)
SPIWrite 0017,10,0,7    //PAGE: dac_2t=0x1;     Address(0x17[5:4],)
SPIReadCheck 003c,0,2,07

\\Read  pi_from_2t_txab_ro0=0x7;    Address(0x3c[7:0],)

SPIWrite 0017,20,0,7    //PAGE: dac_2t=0x2;     Address(0x17[5:4],)
SPIReadCheck 003c,0,2,07

\\Read  pi_from_2t_txab_ro0=0x7;    Address(0x3c[7:0],)

SPIWrite 0017,00,0,7    //PAGE: dac_2t=0x0;     Address(0x17[5:4],)
SPIWrite 0015,01,0,7    //PAGE: rx_jesd=0x1;    Address(0x15[0:0],0x15[4:4],)
SPIWrite 0015,01,0,7
SPIReadCheck 00a8,4,4,10

\\Read  rx_root_clk_monitor_flag=0x1;   Address(0xa8[4:4],)

SPIReadCheck 00a8,5,5,20

\\Read  rx_root_sysref_monitor_flag=0x1;    Address(0xa8[5:5],)

SPIWrite 0015,00,0,7    //PAGE: rx_jesd=0x0;    Address(0x15[0:0],0x15[4:4],)
SPIWrite 0015,00,0,7
SPIWrite 0011,01,0,7    //PAGE: rx_ec_i=0x1;    Address(0x11[3:0],)
SPIReadCheck 053d,0,2,00
SPIReadCheck 053c,0,7,07

\\Read  read_flags=0x7;     Address(0x53c[15:0],)


\\END: Done checking Sysref Flags

SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
\\ STEP: jesdLinkUpInit/step4
\\ STEP: dacJesdLinkUp/step0

\\START: Reading the JESD RX states to check if link is established


\\START: Clearing JESD RX Data and alarms

SPIWrite 0015,02,0,7    //PAGE: tx_jesd=0x1;    Address(0x15[1:1],0x15[5:5],)
SPIWrite 0015,02,0,7
SPIWrite 0081,ff,0,7    //jesd_clear_data=0xff;     Address(0x80[15:8],)
SPIWrite 0081,00,0,7    //jesd_clear_data=0x0;  Address(0x80[15:8],)
SPIWrite 002d,db,0,7    //serdes_fifo_err_clear=0x1;    Address(0x2c[14:14],)
SPIWrite 002d,9b,0,7    //serdes_fifo_err_clear=0x0;    Address(0x2c[14:14],)
SPIWrite 0190,01,0,7    //clear_all_alarms=0x1;     Address(0x190[0:0],)
SPIWrite 0190,00,0,7    //clear_all_alarms=0x0;     Address(0x190[0:0],)
SPIWrite 0190,04,0,7    //clear_all_alarms_to_pap=0x1;  Address(0x190[2:2],)
SPIWrite 0190,00,0,7    //clear_all_alarms_to_pap=0x0;  Address(0x190[2:2],)

\\END: Done clearing JESD RX Data and alarms
```

```
WAIT 0.001

SPIReadCheck 0163,0,7,00
SPIReadCheck 0162,0,7,00
SPIReadCheck 0161,0,7,00

SPIReadCheck 0167,0,7,00
SPIReadCheck 0166,0,7,00
SPIReadCheck 0165,0,7,00
SPIReadCheck 0164,0,7,00

\\Read  alarms=0x8;     Address(0x160[31:0],0x164[31:0],)

SPIReadCheck 0135,4,4,10

\\Read  comma_align_lock_lane0_monitor_flag=0x1;    Address(0x134[12:12],)

SPIReadCheck 012a,0,7,02

\\Read  jesd_cs_state_tx0=0x2;  Address(0x128[23:16],)

SPIReadCheck 012e,0,7,03

\\Read  jesd_buf_state_tx0=0x3;     Address(0x12c[23:16],)


\\END: Done reading the JESD RX states to check if link is established


\\START: Reading the JESD RX states to check if link is established


\\START: Clearing JESD RX Data and alarms

SPIWrite 0015,00,0,7    //PAGE: tx_jesd=0x2;    Address(0x15[1:1],0x15[5:5],)
SPIWrite 0015,20,0,7
SPIWrite 0081,ff,0,7    //jesd_clear_data=0xff;     Address(0x80[15:8],)
SPIWrite 0081,00,0,7    //jesd_clear_data=0x0;  Address(0x80[15:8],)
SPIWrite 002d,db,0,7    //serdes_fifo_err_clear=0x1;    Address(0x2c[14:14],)
SPIWrite 002d,9b,0,7    //serdes_fifo_err_clear=0x0;    Address(0x2c[14:14],)
SPIWrite 0190,01,0,7    //clear_all_alarms=0x1;     Address(0x190[0:0],)
SPIWrite 0190,00,0,7    //clear_all_alarms=0x0;     Address(0x190[0:0],)
SPIWrite 0190,04,0,7    //clear_all_alarms_to_pap=0x1;  Address(0x190[2:2],)
SPIWrite 0190,00,0,7    //clear_all_alarms_to_pap=0x0;  Address(0x190[2:2],)

\\END: Done clearing JESD RX Data and alarms


WAIT 0.001

SPIReadCheck 0163,0,7,00
SPIReadCheck 0162,0,7,00
SPIReadCheck 0161,0,7,00

SPIReadCheck 0167,0,7,00
SPIReadCheck 0166,0,7,00
SPIReadCheck 0165,0,7,00
SPIReadCheck 0164,0,7,00

\\Read  alarms=0x0;     Address(0x160[31:0],0x164[31:0],)

SPIReadCheck 0135,4,4,10

\\Read  comma_align_lock_lane0_monitor_flag=0x1;    Address(0x134[12:12],)

SPIReadCheck 012a,0,7,02

\\Read  jesd_cs_state_tx0=0x2;  Address(0x128[23:16],)
```

```
SPIReadCheck 012e,0,7,03

\\Read  jesd_buf_state_tx0=0x3;     Address(0x12c[23:16],)


\\END: Done reading the JESD RX states to check if link is established

SPIWrite 0015,20,0,7    //PAGE: tx_jesd=0x0;    Address(0x15[1:1],0x15[5:5],)
SPIWrite 0015,00,0,7
\\ STEP: dacJesdLinkUp/step1

\\START: Writing Post Link up SERDES writes

SPIWrite 0015,04,0,7    //PAGE: SERDES=0x1;     Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,04,0,7
SPIWrite 41fb,02,0,7
SPIWrite 41fa,6e,0,7
SPIWrite 43fb,02,0,7
SPIWrite 43fa,6e,0,7
SPIWrite 45fb,02,0,7
SPIWrite 45fa,6e,0,7
SPIWrite 47fb,02,0,7
SPIWrite 47fa,6e,0,7

\\END: Done writing Post Link up SERDES writes


\\START: Writing Post Link up SERDES writes

SPIWrite 0015,00,0,7    //PAGE: SERDES=0x2;     Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,40,0,7
SPIWrite 41fb,02,0,7
SPIWrite 41fa,6e,0,7
SPIWrite 43fb,02,0,7
SPIWrite 43fa,6e,0,7
SPIWrite 45fb,02,0,7
SPIWrite 45fa,6e,0,7
SPIWrite 47fb,02,0,7
SPIWrite 47fa,6e,0,7

\\END: Done writing Post Link up SERDES writes


\\START: Unfreeze TX IQMC/LO

SPIWrite 0015,40,0,7    //PAGE: SERDES=0x0;     Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,00,0,7
SPIWrite 0013,10,0,7    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)
SPIWrite 00a3,00,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,ff,0,7
SPIWrite 00a0,07,0,7
SPIWrite 0193,35,0,7

\\END: Done Unfreeze TX IQMC/LO


\\START: Unfreeze RX IQMC/LO


\\START: Overriding TDD Pins internally

SPIWrite 0013,00,0,7    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0014,04,0,7    //PAGE: TIMING_CON=0x1;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0124,01,0,7    //use_reg_txon_AB=0x1;  Address(0x124[0:0],)
SPIWrite 0126,01,0,7    //use_reg_rxon_AB=0x1;  Address(0x124[16:16],)
SPIWrite 0128,01,0,7    //use_reg_fbon_AB=0x1;  Address(0x128[0:0],)
SPIWrite 012a,01,0,7    //use_reg_txon_CD=0x1;  Address(0x128[16:16],)
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```
SPIWrite 012c,01,0,7    //use_reg_rxon_CD=0x1;  Address(0x12c[0:0],)
SPIWrite 012e,01,0,7    //use_reg_fbon_CD=0x1;  Address(0x12c[16:16],)
SPIWrite 0125,00,0,7    //reg_for_txon_AB=0x0;  Address(0x124[8:8],)
SPIWrite 0127,01,0,7    //reg_for_rxon_AB=0x1;  Address(0x124[24:24],)
SPIWrite 0129,00,0,7    //reg_for_fbon_AB=0x0;  Address(0x128[8:8],)
SPIWrite 012b,00,0,7    //reg_for_txon_CD=0x0;  Address(0x128[24:24],)
SPIWrite 012d,01,0,7    //reg_for_rxon_CD=0x1;  Address(0x12c[8:8],)
SPIWrite 012f,00,0,7    //reg_for_fbon_CD=0x0;  Address(0x12c[24:24],)

\\END: Done overriding TDD Pins internally


WAIT 0.0001

SPIWrite 0014,00,0,7    //PAGE: TIMING_CON=0x0;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0010,04,0,7    //PAGE: rx_top=0x1;     Address(0x10[3:2],)
SPIWrite 0a05,01,0,7    //op_clk_en_iqmc_clk_gen=0x1;(Meaning: );   Address(0xa04[8:8],)
SPIWrite 0010,08,0,7    //PAGE: rx_top=0x2;     Address(0x10[3:2],)
SPIWrite 0a05,01,0,7    //op_clk_en_iqmc_clk_gen=0x1;(Meaning: );   Address(0xa04[8:8],)
SPIWrite 0010,00,0,7    //PAGE: rx_top=0x0;     Address(0x10[3:2],)
SPIWrite 0013,20,0,7    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIWrite 01a3,00,0,7
SPIWrite 01a2,0f,0,7
SPIWrite 01a1,00,0,7
SPIWrite 01a0,00,0,7
SPIWrite 01a3,17,0,7
SPIWrite 01a2,0f,0,7
SPIWrite 01a1,00,0,7
SPIWrite 01a0,00,0,7
SPIWrite 01a3,00,0,7
SPIWrite 01a2,0f,0,7
SPIWrite 01a1,00,0,7
SPIWrite 01a0,00,0,7
SPIWrite 01a3,12,0,7
SPIWrite 01a2,0f,0,7
SPIWrite 01a1,00,0,7
SPIWrite 01a0,00,0,7

\\END: Done Unfreeze RX IQMC/LO

SPIWrite 0013,00,0,7    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
SPIWrite 0014,04,0,7    //PAGE: TIMING_CON=0x1;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0124,01,0,7    //use_reg_txon_AB=0x1;  Address(0x124[0:0],)
SPIWrite 0126,01,0,7    //use_reg_rxon_AB=0x1;  Address(0x124[16:16],)
SPIWrite 0128,00,0,7    //use_reg_fbon_AB=0x0;  Address(0x128[0:0],)
SPIWrite 012a,01,0,7    //use_reg_txon_CD=0x1;  Address(0x128[16:16],)
SPIWrite 012c,01,0,7    //use_reg_rxon_CD=0x1;  Address(0x12c[0:0],)
SPIWrite 012e,00,0,7    //use_reg_fbon_CD=0x0;  Address(0x12c[16:16],)
SPIWrite 0125,01,0,7    //reg_for_txon_AB=0x1;  Address(0x124[8:8],)
SPIWrite 0127,01,0,7    //reg_for_rxon_AB=0x1;  Address(0x124[24:24],)
SPIWrite 0129,00,0,7    //reg_for_fbon_AB=0x0;  Address(0x128[8:8],)
SPIWrite 012b,01,0,7    //reg_for_txon_CD=0x1;  Address(0x128[24:24],)
SPIWrite 012d,01,0,7    //reg_for_rxon_CD=0x1;  Address(0x12c[8:8],)
SPIWrite 012f,00,0,7    //reg_for_fbon_CD=0x0;  Address(0x12c[24:24],)

\\START: Clearing All Alarms

SPIWrite 001a,ff,0,7    //alarms_clear=0x1ff;   Address(0x1a[7:0],0x1b[0:0],)
SPIWrite 001b,01,0,7
SPIWrite 001a,00,0,7    //alarms_clear=0x0;     Address(0x1a[7:0],0x1b[0:0],)
SPIWrite 001b,00,0,7
SPIWrite 0014,00,0,7    //PAGE: TIMING_CON=0x0;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0013,20,0,7    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIWrite 02e5,20,0,7
SPIWrite 02e5,00,0,7

\\START: Clearing JESD RX Data and alarms

SPIWrite 0013,00,0,7    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
```

```
SPIWrite 0015,02,0,7    //PAGE: tx_jesd=0x3;    Address(0x15[1:1],0x15[5:5],)
SPIWrite 0015,22,0,7
SPIWrite 0081,ff,0,7    //jesd_clear_data=0xff;     Address(0x80[15:8],)
SPIWrite 0081,00,0,7    //jesd_clear_data=0x0;  Address(0x80[15:8],)
SPIWrite 002d,db,0,7    //serdes_fifo_err_clear=0x1;    Address(0x2c[14:14],)
SPIWrite 002d,9b,0,7    //serdes_fifo_err_clear=0x0;    Address(0x2c[14:14],)
SPIWrite 0190,01,0,7    //clear_all_alarms=0x1;     Address(0x190[0:0],)
SPIWrite 0190,00,0,7    //clear_all_alarms=0x0;     Address(0x190[0:0],)
SPIWrite 0190,04,0,7    //clear_all_alarms_to_pap=0x1;  Address(0x190[2:2],)
SPIWrite 0190,00,0,7    //clear_all_alarms_to_pap=0x0;  Address(0x190[2:2],)

\\END: Done clearing JESD RX Data and alarms


\\START: Clearing JESD TX Data and alarms

SPIWrite 0015,20,0,7    //PAGE: tx_jesd=0x0;    Address(0x15[1:1],0x15[5:5],)
SPIWrite 0015,00,0,7
SPIWrite 0015,01,0,7    //PAGE: rx_jesd=0x3;    Address(0x15[0:0],0x15[4:4],)
SPIWrite 0015,11,0,7
SPIWrite 00b1,0f,0,7    //alarms_serdes_fifo_errors_clear=0xf;  Address(0xb0[11:8],)
SPIWrite 00b1,00,0,7    //alarms_serdes_fifo_errors_clear=0x0;  Address(0xb0[11:8],)
SPIWrite 0026,0f,0,7    //jesd_clear_data=0xf;  Address(0x24[19:16],)
SPIWrite 0026,00,0,7    //jesd_clear_data=0x0;  Address(0x24[19:16],)
SPIWrite 0045,00,0,7    //fifo_init_state=0x0;  Address(0x44[13:13],)

\\END: Done clearing JESD TX Data and alarms


\\START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,10,0,7    //PAGE: rx_jesd=0x0;    Address(0x15[0:0],0x15[4:4],)
SPIWrite 0015,00,0,7
SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 01d4,01,0,7    //pll_reg_spi_req_a=0x1;    Address(0x1d4[0:0],)
SPIWrite 0374,00,0,7    //pll_reg_spi_req_b1=0x0;(Meaning: );   Address(0x374[0:0],)

SPIPoll 01d5,0,0,1


\\Read  pll_reg_spi_a_ack=0x1;  Address(0x1d4[8:8],)


\\END: Done requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0014,f8,0,7    //PAGE: pll=0x1f;   Address(0x14[7:3],)
SPIWrite 0066,08,0,7    //lock_lost_rst=0x1;    Address(0x64[19:19],)
SPIWrite 0066,00,0,7    //lock_lost_rst=0x0;    Address(0x64[19:19],)

\\START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0014,00,0,7    //PAGE: pll=0x0;    Address(0x14[7:3],)
SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 01d4,00,0,7    //pll_reg_spi_req_a=0x0;    Address(0x1d4[0:0],)
SPIWrite 0374,00,0,7    //pll_reg_spi_req_b1=0x0;(Meaning: );   Address(0x374[0:0],)

WAIT 0.01


\\END: Done requesting/releasing SPI Access to PLL Pages

SPIWrite 064a,0f,0,7    //pap_alarm_clear=0xf;  Address(0x648[19:16],)
SPIWrite 064a,00,0,7    //pap_alarm_clear=0x0;  Address(0x648[19:16],)

\\END: Done clearing All Alarms

SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
```

\\END: Completed Link up Sequence