

\\START: Doing AFE Config

\\Library Version: 2.21

\\ STEP: rstDevice/step0

\\EXTERNAL-ACTION: Toggle HW Reset

\\START: Resetting the Device

```
SPIWrite 0000,30,0,7    //global_soft_reset=0x0;    Address(0x0[7:7],)
SPIWrite 0000,b0,0,7    //global_soft_reset=0x1;    Address(0x0[7:7],)
SPIWrite 0000,30,0,7    //global_soft_reset=0x0;    Address(0x0[7:7],)
SPIWrite 0000,30,0,7    //global_4pin=0x1;    Address(0x0[4:4],)
SPIWrite 0000,30,0,7    //global_ascend=0x1;    Address(0x0[5:5],)
SPIReadCheck 0003,0,7,0a
```

\\Read chip_type=0xa; Address(0x3[7:0],)

```
SPIReadCheck 0004,0,7,77
SPIReadCheck 0005,0,7,00
```

\\Read chip_id=0x77; Address(0x4[7:0],0x5[7:0],)

```
SPIReadCheck 0006,0,7,11
```

\\Read chip_ver=0x11; Address(0x6[7:0],)

\\Read vendor_id=0x451; Address(0x7[7:0],0x8[7:0],)

\\END: Done resetting the Device

\\The list of parameters. In the arrays of 2 elements, each value corresponds to one 2T2R1F.
// jesdKfb: [32, 32]; agcRegConfigParams: [{'coarseIndexBits': 3, 'dgcMode': 0, 'windowLenSa': 256, 'thresholdSd': -7, 'stepSizeSa': 1, 'thresholdBa': -2, 'thresholdLowSd': 0, 'numHitsSa': 32, 'stepSizePa': 1, 'numHitsSd': 32, 'thresholdLowSa': -3.0, 'thresholdPd': -18.0, 'coarseStep': 6, 'enablePd': False, 'enablePa': True, 'windowLenBa': 128, 'enableEl': 1, 'stepSizePd': 1, 'windowLenBd': 256, 'thresholdSa': -3, 'fdsaOffset': 0, 'regFreeze': 0, 'thresholdPa': -9.0, 'windowLenPd': 32768, 'floatingPointMode': 0, 'windowLenPa': 6, 'enableBd': 0, 'dgcEnable': 0, 'stepSizeBa': 3, 'enableSd': 1, 'enableBa': 0, 'gainControl': 0, 'pinFreezeEn': 0, 'freeze': 0, 'floatingPointFormat': 1, 'numHitsBd': 32, 'enableIa': 0, 'stepSizeSd': 1, 'thresholdLowBd': -12.0, 'modePd': 0, 'thresholdLowBa': -1.0, 'gainMargin': 2, 'modePa': 0, 'enableSa': 1, 'numHitsBa': 32, 'thresholdBd': -6, 'lnabypassGain': 16, 'windowLenSd': 512, 'phmOvrEn': 0, 'stepSizeBd': 3}, {'coarseIndexBits': 3, 'dgcMode': 0, 'windowLenSa': 256, 'thresholdSd': -7, 'stepSizeSa': 1, 'thresholdBa': -2, 'thresholdLowSd': 0, 'numHitsSa': 32, 'stepSizePa': 1, 'numHitsSd': 32, 'thresholdLowSa': -3.0, 'thresholdPd': -18.0, 'coarseStep': 6, 'enablePd': False, 'enablePa': True, 'windowLenBa': 128, 'enableEl': 1, 'stepSizePd': 1, 'windowLenBd': 256, 'thresholdSa': -3, 'fdsaOffset': 0, 'regFreeze': 0, 'thresholdPa': -9.0, 'windowLenPd': 32768, 'floatingPointMode': 0, 'windowLenPa': 6, 'enableBd': 0, 'dgcEnable': 0, 'stepSizeBa': 3, 'enableSd': 1, 'enableBa': 0, 'gainControl': 0, 'pinFreezeEn': 0, 'freeze': 0, 'floatingPointFormat': 1, 'numHitsBd': 32, 'enableIa': 0, 'stepSizeSd': 1, 'thresholdLowBd': -12.0, 'modePd': 0, 'thresholdLowBa': -1.0, 'gainMargin': 2, 'modePa': 0, 'enableSa': 1, 'numHitsBa': 32, 'thresholdBd': -6, 'lnabypassGain': 16, 'windowLenSd': 512, 'phmOvrEn': 0, 'stepSizeBd': 3}, {'coarseIndexBits': 3, 'dgcMode': 0, 'windowLenSa': 256, 'thresholdSd': -7, 'stepSizeSa': 1, 'thresholdBa': -2, 'thresholdLowSd': 0, 'numHitsSa': 32, 'stepSizePa': 1, 'numHitsSd': 32, 'thresholdLowSa': -3.0, 'thresholdPd': -18.0, 'coarseStep': 6, 'enablePd': False, 'enablePa': True, 'windowLenBa': 128, 'enableEl': 1, 'stepSizePd': 1, 'windowLenBd': 256, 'thresholdSa': -3, 'fdsaOffset': 0, 'regFreeze': 0, 'thresholdPa': -9.0, 'windowLenPd': 32768, 'floatingPointMode': 0, 'windowLenPa': 6, 'enableBd': 0, 'dgcEnable': 0, 'stepSizeBa': 3, 'enableSd': 1, 'enableBa': 0, 'gainControl': 0, 'pinFreezeEn': 0, 'freeze': 0, 'floatingPointFormat': 1, 'numHitsBd': 32, 'enableIa': 0, 'stepSizeSd': 1, 'thresholdLowBd': -12.0, 'modePd': 0, 'thresholdLowBa': -1.0, 'gainMargin': 2, 'modePa': 0, 'enableSa': 1, 'numHitsBa': 32, 'thresholdBd': -6, 'lnabypassGain': 16,

```

>windowLenSd': 512, 'phmOvrEn': 0, 'stepSizeBd': 3}, {'coarseIndexBits': 3, 'dgcMode': 0,
>windowLenSa': 256, 'thresholdSd': -7, 'stepSizeSa': 1, 'thresholdBa': -2, 'thresholdLowSd': 0,
>numHitsSa': 32, 'stepSizePa': 1, 'numHitsSd': 32, 'thresholdLowSa': -3.0, 'thresholdPd':
>-18.0, 'coarseStep': 6, 'enablePd': False, 'enablePa': True, 'windowLenBa': 128, 'enableEl': 1,
>stepSizePd': 1, 'windowLenBd': 256, 'thresholdSa': -3, 'fdsaOffset': 0, 'regFreeze': 0,
>thresholdPa': -9.0, 'windowLenPd': 32768, 'floatingPointMode': 0, 'windowLenPa': 6,
>enableBd': 0, 'dgcEnable': 0, 'stepSizeBa': 3, 'enableSd': 1, 'enableBa': 0, 'gainControl': 0,
>pinFreezeEn': 0, 'freeze': 0, 'floatingPointFormat': 1, 'numHitsBd': 32, 'enableIa': 0,
>stepSizeSd': 1, 'thresholdLowBd': -12.0, 'modePd': 0, 'thresholdLowBa': -1.0, 'gainMargin': 2,
>modePa': 0, 'enableSa': 1, 'numHitsBa': 32, 'thresholdBd': -6, 'lnabypassGain': 16,
>windowLenSd': 512, 'phmOvrEn': 0, 'stepSizeBd': 3}}; useDifferentKforRxFbTx: False;
jesdProtocol: 0; fbNco: [778.0, 778.0];
// usePllExternalLoClock: [False, False]; enableTxIqmcLolHostUpdateMode: False;
txDsaCalibMode: 0; enableReliabilityDetector: True; jesdRxDsaLaneMux: [2, 3, 4, 5, 0, 1, 6, 7];
// fbDsaPerTx: [0, 0, 0, 0]; LMFShdTxFb: ['48410', '48410']; X: 61.44; serdesManualCTLEn:
False; halfRateModeRx: 0;
// lowIfNcoTx: [0.0, 0.0]; serdesTxLanePolarity: [False, False, False, False, False, False, False,
False, False]; txIqmcExternalDelayValue: [0, 0, 0, 0]; txDsaGainStepDelay: 5;
pdnUnusedLanes: 1;
// dedicatedLaneMode: [1, 1]; chipType: 16; txIqmcCalibMode: 0; pllLoopBw: 1; chipVersion:
17;
// intPinsParams: [{'JESD': True, 'SPI': 0, 'SRTXA': True, 'SRTXB': True, 'SRTXC': True,
>SRTXD': True, 'PLL4': True, 'PLL0': True, 'PLL1': True, 'PLL2': True, 'PLL3': True}, {'JESD':
0, 'SPI': True, 'SRTXA': 0, 'SRTXB': 0, 'SRTXC': 0, 'SRTXD': 0, 'PLL4': 0, 'PLL0': 0, 'PLL1':
0, 'PLL2': 0, 'PLL3': 0}]; LMFShdFb: ['12410', '12410']; enableTxIqmcLolPowerUpCorr: False;
defaultRxDsa: [0, 0, 0, 0]; enableRxIqmcLolPowerUpCorr: False;
// defaultTxDsa: [13, 13, 13, 13]; jesdLoopbackEn: 0; ddcFactorRx: [16, 16]; syncLoopBack:
True; jesdTxFBCDSyncMux: 3;
// enableTxJesdLinks: [1, 0]; pllMuxModes: 0; enableTxIqmcDelayChar: False; halfRateModeTx:
0; lowIfNcoRx: [-55.0, -55.0];
// fbDsaPerTxEn: False; jesdRxBd: [31, 31]; FRef: 491.52; lowIfNcoFb: [0.0, 0.0];
simulationMode: False;
// lmfcOffset: 0; rxDsaPacketFilePath: ; setLoForCoherence: True; gpioMapping: {'D14':
>u'tdd_2t_en_cd', 'U5': 'u'adc_sync_n_cd_0', 'U6': 'u'fspic_data_in', 'E17': 'u'alarm_2', 'E16':
>u'global_pdn', 'T13': 'u'tdd_1f_en_ab', 'C13': 'u'tdd_2r_en_cd', 'U10': 'u'fspia_clk', 'C10':
>u'fspib_clk', 'C17': 'u'alarm_1', 'U14': 'u'tdd_2t_en_ab', 'U16': 'u'spib1_clk', 'C8':
>u'fspib_data_in', 'A5': 'u'dac_sync_n_cd_0', 'V5': 'u'adc_sync_n_ab_0', 'V6': 'u'fspic_clk', 'V8':
>u'fspia_data_in', 'C6': 'u'fspid_clk', 'C5': 'u'adc_sync_n_ab_1', 'V13': 'u'tdd_2r_en_ab', 'V16':
>u'intbipi_spib1_sdi', 'V14': 'u'spib1_cs_n', 'V15': 'u'spib1_sdo', 'D6': 'u'fspid_data_in', 'D5':
>u'adc_sync_n_cd_1', 'Y5': 'u'dac_sync_n_ab_0'}; Fs: 2949.12;
// pllLo: [778.0, 2949.12, 2139.84, 1747.44, 1950.0]; txIqmcFullBandEstimation: False;
txDsaPacketFilePath: ; srConfigParams: [{'enable': True, 'amplMode': 1, 'GainStepSize': 38,
>AttnStepSize': 38, 'alarmMask': 4060, 'AmplRampGainDly': 0, 'mode': 0, 'threshold': 30,
>AmplRampAttnDly': 0, 'AmplUpdateCycles': 6}, {'enable': True, 'amplMode': 1, 'GainStepSize':
38, 'AttnStepSize': 38, 'alarmMask': 4060, 'AmplRampGainDly': 0, 'mode': 0, 'threshold': 30,
>AmplRampAttnDly': 0, 'AmplUpdateCycles': 6}, {'enable': True, 'amplMode': 1, 'GainStepSize':
38, 'AttnStepSize': 38, 'alarmMask': 4060, 'AmplRampGainDly': 0, 'mode': 0, 'threshold': 30,
>AmplRampAttnDly': 0, 'AmplUpdateCycles': 6}, {'enable': True, 'amplMode': 1, 'GainStepSize':
38, 'AttnStepSize': 38, 'alarmMask': 4060, 'AmplRampGainDly': 0, 'mode': 0, 'threshold': 30,
>AmplRampAttnDly': 0, 'AmplUpdateCycles': 6}]; jesdAlarmPinMask: [1519143632681832447L,
18446744073709551615L];
// serdesFirmware: True; fbNcoBand1: [778, 2139.84]; jesdABLvdsSync: 0;
serdesRxDsaLanePolarity: [False, False, False, False, False, False, False, False, False]; useMacros:
True;
// rxDsaCalibMode: 0; jesdK: [32, 32]; sampDropByFb: [1, 1]; enableTxDsaFactoryCal: False;
halfRateModeFb: 0;
// jesdScr: [False, False]; releaseTxMuxControlToPins: False; jesdKTx: [32, 32];
jesdAlarmPdpMask: [1519143632681832447L, 18446744073709551615L]; latteLibVersion: 2.21;
// jesdTxFBABSyncMux: 2; ducFactorTx: [8, 8]; jesdRxBABSyncMux: 0; customerConfig: True;
jesdTxRxBABSyncMux: 0;
// serdesTxPostCursor: [0, 0, 0, 0, 0, 0, 0, 0]; enableRxFbJesdLinks: [1, 0]; chipId: 119;
defaultFbDsa: [12, 12]; serdesTxMainCursor: [7, 7, 7, 7, 7, 7, 7, 7];
// executeLinkUpSequenceSeparately: True; sampDropByRx: [1, 1]; enableRxDsaFactoryCal:
False; enableAuxAdc: True; ddcFactorFb: [8, 8];
// serdesManualCTLE: [6, 6, 6, 6, 6, 6, 6, 6]; enableTxIqmcLolTrackingCorr: False;
jesdRxCDSyncMux: 2; useSpiSysref: False; sysrefFreqDiv: 256;
// jesdTxRxCDSyncMux: 1; enableRxIqmcLolTrackingCorr: True; systemMode: [1, 1]; enableFbCd:
False; setTxLoFbNcoFreqForTxCalib: True;
// enableTxSigGen: False; mode2t2r: 1; jesdKRx: [32, 32]; rxAdcBw: 100; jesdTxLaneMux: [4,

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3, 0, 2, 1, 6, 5, 7];
// txDsaUpdateMode: 0;  LMFShdRx: ['28810', '28810'];  txDigDelay: [0, 0, 0, 0];
serdesTxPreCursor: [0, 0, 0, 0, 0, 0, 0, 0];  gpioConfigMode: 3;
// jesdCDLvdsSync: 0;

\\Doing LMK config

\\Doing LMK config

\\ STEP: wakeUp/step0

\\START: Waking up device

SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1; (Meaning: );    Address(0x15[7:7],)
SPIWrite 0600,03,0,7    //misc_spi_global_pdn_ctrl=0x1;    Address(0x600[0:0],)
SPIWrite 0600,01,0,7    //misc_spi_global_pdn_sig=0x0;    Address(0x600[1:1],)

\\END: Done waking up device

\\START: Loading Efuse Chain

SPIWrite 07f0,00,0,7    //spi_ovr_sys_autoload_chain=0x0;    Address(0x7f0[5:2],)
SPIWrite 0804,00,0,7    //spi_ovr_sys_autoload_chain=0x0;    Address(0x804[5:2],)
SPIWrite 07f0,3c,0,7    //spi_ovr_sys_autoload_chain=0xf;    Address(0x7f0[5:2],)
SPIWrite 0804,3c,0,7    //spi_ovr_sys_autoload_chain=0xf;    Address(0x804[5:2],)
SPIWrite 07f0,3c,0,7    //spi_sys_rstn_ctrl=0x0;    Address(0x7f0[1:0],)
SPIWrite 07f0,3d,0,7    //spi_sys_rstn_ctrl=0x1;    Address(0x7f0[1:0],)
SPIWrite 07f0,3f,0,7    //spi_sys_rstn_ctrl=0x3;    Address(0x7f0[1:0],)
SPIWrite 07f0,3c,0,7    //spi_sys_rstn_ctrl=0x0;    Address(0x7f0[1:0],)
SPIWrite 0804,3c,0,7    //spi_sys_rstn_ctrl=0x0;    Address(0x804[1:0],)
SPIWrite 0804,3d,0,7    //spi_sys_rstn_ctrl=0x1;    Address(0x804[1:0],)
SPIWrite 0804,3f,0,7    //spi_sys_rstn_ctrl=0x3;    Address(0x804[1:0],)
SPIWrite 0804,3c,0,7    //spi_sys_rstn_ctrl=0x0;    Address(0x804[1:0],)
SPIWrite 07f0,00,0,7    //spi_ovr_sys_autoload_chain=0x0;    Address(0x7f0[5:2],)
SPIWrite 0804,00,0,7    //spi_ovr_sys_autoload_chain=0x0;    Address(0x804[5:2],)

WAIT 0.01

\\END: Done loading Efuse Chain

\\START: Checking Efuse Chain

\\Read  obs_func_spi_chain_autoload_done=0xf;    Address(0x138[3:0],)

\\Read  obs_func_spi_chain_autoload_error=0x0;    Address(0x138[7:4],)

\\END: Done checking Efuse Chain

\\START: Enabling/Disabling Efuse Clock

SPIWrite 0135,01,0,7    //spi_ovr_sys_clk_gate=0x1;    Address(0x134[8:8],)
SPIWrite 0131,01,0,7    //spi_ovr_sys_clk_gate=0x1;    Address(0x130[8:8],)

\\END: Done enabling/Disabling Efuse Clock

SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0; (Meaning: );    Address(0x15[7:7],)
\\ STEP: rstMCU/step0

\\START: Resetting Top MC

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```
SPIWrite 0013,10,0,7    //PAGE: customer_macro=0x1;(Meaning: );    Address(0x13[4:4],)
SPIWrite 0140,01,0,7
```

```
\\END: Done resetting Top MC
```

```
\\START: Resetting Top MC
```

```
SPIWrite 0140,00,0,7
```

```
\\END: Done resetting Top MC
```

```
WAIT 0.1
```

```
SPIWrite 0013,00,0,7    //PAGE: customer_macro=0x0;(Meaning: );    Address(0x13[4:4],)
\\ STEP: rstMCU/step1
SPIWrite 0012,10,4,4    //PAGE: sys_calib_macro_memory=0x1;(Meaning: );    Address(0x12[4:4],)
SPIWrite 0040,00,0,7
SPIWrite 0020,00,0,7
SPIWrite 0021,00,0,7
SPIWrite 0022,00,0,7
SPIWrite 0023,00,0,7
SPIWrite 0024,75,0,7
SPIWrite 0025,8a,0,7
SPIWrite 0026,02,0,7
SPIWrite 0027,00,0,7
SPIWrite 0028,b5,0,7
SPIWrite 0029,a4,0,7
SPIWrite 002a,6d,0,7
SPIWrite 002b,ea,0,7
SPIWrite 002c,7d,0,7
SPIWrite 002d,19,0,7
SPIWrite 002e,ce,0,7
SPIWrite 002f,ca,0,7
SPIWrite 0030,10,0,7
SPIWrite 0031,00,0,7
SPIWrite 0032,99,0,7
SPIWrite 0033,10,0,7
SPIWrite 0034,0a,0,7
SPIWrite 0035,01,0,7
SPIWrite 0036,12,0,7
SPIWrite 0037,00,0,7
SPIWrite 0038,11,0,7
SPIWrite 0039,00,0,7
SPIWrite 003a,9e,0,7
SPIWrite 003b,11,0,7
SPIWrite 003c,05,0,7
SPIWrite 003d,06,0,7
SPIWrite 003e,12,0,7
SPIWrite 003f,00,0,7
SPIWrite 0040,00,0,7
SPIWrite 0041,00,0,7
SPIWrite 0042,00,0,7
SPIWrite 0043,05,0,7
SPIWrite 0044,09,0,7
SPIWrite 0045,08,0,7
SPIWrite 0046,17,0,7
SPIWrite 0047,00,0,7
SPIWrite 0048,00,0,7
SPIWrite 0049,00,0,7
SPIWrite 004a,00,0,7
SPIWrite 004b,00,0,7
SPIWrite 004c,00,0,7
SPIWrite 004d,00,0,7
SPIWrite 004e,00,0,7
SPIWrite 004f,00,0,7
SPIWrite 0050,ad,0,7
SPIWrite 0051,f1,0,7
```

SPIWrite 0052,08,0,7
SPIWrite 0053,0d,0,7
SPIWrite 0054,00,0,7
SPIWrite 0055,21,0,7
SPIWrite 0056,7f,0,7
SPIWrite 0057,4a,0,7
SPIWrite 0058,00,0,7
SPIWrite 0059,91,0,7
SPIWrite 005a,50,0,7
SPIWrite 005b,7d,0,7
SPIWrite 005c,00,0,7
SPIWrite 005d,90,0,7
SPIWrite 005e,00,0,7
SPIWrite 005f,98,0,7
SPIWrite 0060,c0,0,7
SPIWrite 0061,b1,0,7
SPIWrite 0062,10,0,7
SPIWrite 0063,46,0,7
SPIWrite 0064,81,0,7
SPIWrite 0065,75,0,7
SPIWrite 0066,00,0,7
SPIWrite 0067,bf,0,7
SPIWrite 0068,0a,0,7
SPIWrite 0069,46,0,7
SPIWrite 006a,01,0,7
SPIWrite 006b,92,0,7
SPIWrite 006c,82,0,7
SPIWrite 006d,7d,0,7
SPIWrite 006e,01,0,7
SPIWrite 006f,92,0,7
SPIWrite 0070,01,0,7
SPIWrite 0071,9a,0,7
SPIWrite 0072,01,0,7
SPIWrite 0073,2a,0,7
SPIWrite 0074,0d,0,7
SPIWrite 0075,d0,0,7
SPIWrite 0076,01,0,7
SPIWrite 0077,23,0,7
SPIWrite 0078,20,0,7
SPIWrite 0079,22,0,7
SPIWrite 007a,c0,0,7
SPIWrite 007b,f2,0,7
SPIWrite 007c,00,0,7
SPIWrite 007d,02,0,7
SPIWrite 007e,52,0,7
SPIWrite 007f,1e,0,7
SPIWrite 0080,fd,0,7
SPIWrite 0081,d1,0,7
SPIWrite 0082,00,0,7
SPIWrite 0083,bf,0,7
SPIWrite 0084,00,0,7
SPIWrite 0085,bf,0,7
SPIWrite 0086,c3,0,7
SPIWrite 0087,75,0,7
SPIWrite 0088,82,0,7
SPIWrite 0089,7d,0,7
SPIWrite 008a,01,0,7
SPIWrite 008b,92,0,7
SPIWrite 008c,01,0,7
SPIWrite 008d,9a,0,7
SPIWrite 008e,01,0,7
SPIWrite 008f,2a,0,7
SPIWrite 0090,f2,0,7
SPIWrite 0091,d1,0,7
SPIWrite 0092,c1,0,7
SPIWrite 0093,75,0,7
SPIWrite 0094,02,0,7
SPIWrite 0095,b0,0,7
SPIWrite 0096,70,0,7

SPIWrite 0097,47,0,7
SPIWrite 0098,2d,0,7
SPIWrite 0099,e9,0,7
SPIWrite 009a,f0,0,7
SPIWrite 009b,47,0,7
SPIWrite 009c,6d,0,7
SPIWrite 009d,4c,0,7
SPIWrite 009e,21,0,7
SPIWrite 009f,79,0,7
SPIWrite 00a0,60,0,7
SPIWrite 00a1,79,0,7
SPIWrite 00a2,08,0,7
SPIWrite 00a3,43,0,7
SPIWrite 00a4,65,0,7
SPIWrite 00a5,d0,0,7
SPIWrite 00a6,dc,0,7
SPIWrite 00a7,48,0,7
SPIWrite 00a8,df,0,7
SPIWrite 00a9,f8,0,7
SPIWrite 00aa,68,0,7
SPIWrite 00ab,a3,0,7
SPIWrite 00ac,22,0,7
SPIWrite 00ad,88,0,7
SPIWrite 00ae,00,0,7
SPIWrite 00af,88,0,7
SPIWrite 00b0,da,0,7
SPIWrite 00b1,f8,0,7
SPIWrite 00b2,08,0,7
SPIWrite 00b3,14,0,7
SPIWrite 00b4,50,0,7
SPIWrite 00b5,43,0,7
SPIWrite 00b6,c0,0,7
SPIWrite 00b7,10,0,7
SPIWrite 00b8,88,0,7
SPIWrite 00b9,47,0,7
SPIWrite 00ba,20,0,7
SPIWrite 00bb,79,0,7
SPIWrite 00bc,58,0,7
SPIWrite 00bd,b3,0,7
SPIWrite 00be,4f,0,7
SPIWrite 00bf,f0,0,7
SPIWrite 00c0,78,0,7
SPIWrite 00c1,47,0,7
SPIWrite 00c2,01,0,7
SPIWrite 00c3,20,0,7
SPIWrite 00c4,4f,0,7
SPIWrite 00c5,f0,0,7
SPIWrite 00c6,2f,0,7
SPIWrite 00c7,46,0,7
SPIWrite 00c8,97,0,7
SPIWrite 00c9,f8,0,7
SPIWrite 00ca,39,0,7
SPIWrite 00cb,91,0,7
SPIWrite 00cc,87,0,7
SPIWrite 00cd,f8,0,7
SPIWrite 00ce,39,0,7
SPIWrite 00cf,01,0,7
SPIWrite 00d0,d6,0,7
SPIWrite 00d1,f8,0,7
SPIWrite 00d2,00,0,7
SPIWrite 00d3,81,0,7
SPIWrite 00d4,d6,0,7
SPIWrite 00d5,f8,0,7
SPIWrite 00d6,00,0,7
SPIWrite 00d7,11,0,7
SPIWrite 00d8,41,0,7
SPIWrite 00d9,f0,0,7
SPIWrite 00da,80,0,7
SPIWrite 00db,71,0,7

SPIWrite 00dc,c6,0,7
SPIWrite 00dd,f8,0,7
SPIWrite 00de,00,0,7
SPIWrite 00df,11,0,7
SPIWrite 00e0,00,0,7
SPIWrite 00e1,25,0,7
SPIWrite 00e2,86,0,7
SPIWrite 00e3,f8,0,7
SPIWrite 00e4,02,0,7
SPIWrite 00e5,51,0,7
SPIWrite 00e6,e3,0,7
SPIWrite 00e7,7a,0,7
SPIWrite 00e8,86,0,7
SPIWrite 00e9,f8,0,7
SPIWrite 00ea,01,0,7
SPIWrite 00eb,31,0,7
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SPIWrite 0d2a,84,0,7
SPIWrite 0d2b,f8,0,7
SPIWrite 0d2c,70,0,7
SPIWrite 0d2d,00,0,7
SPIWrite 0d2e,4f,0,7
SPIWrite 0d2f,f0,0,7
SPIWrite 0d30,b0,0,7
SPIWrite 0d31,41,0,7
SPIWrite 0d32,81,0,7
SPIWrite 0d33,f8,0,7
SPIWrite 0d34,3e,0,7
SPIWrite 0d35,51,0,7
SPIWrite 0d36,81,0,7
SPIWrite 0d37,f8,0,7
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SPIWrite 0d39,51,0,7
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SPIWrite 0d3c,70,0,7
SPIWrite 0d3d,b5,0,7
SPIWrite 0d3e,0e,0,7
SPIWrite 0d3f,4c,0,7
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SPIWrite 0d41,f1,0,7

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SPIWrite 0d43,00,0,7
SPIWrite 0d44,00,0,7
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SPIWrite 0d4d,f8,0,7
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SPIWrite 0d53,f8,0,7
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SPIWrite 0d55,00,0,7
SPIWrite 0d56,f1,0,7
SPIWrite 0d57,f7,0,7
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SPIWrite 0d59,f8,0,7
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SPIWrite 0d5c,b0,0,7
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SPIWrite 0f85,00,0,7
SPIWrite 0f86,00,0,7
SPIWrite 0f87,00,0,7
SPIWrite 0f88,00,0,7
SPIWrite 0f89,00,0,7
SPIWrite 0f8a,00,0,7
SPIWrite 0f8b,00,0,7
SPIWrite 0f8c,00,0,7
SPIWrite 0f8d,00,0,7
SPIWrite 0f8e,00,0,7
SPIWrite 0f8f,00,0,7
SPIWrite 0f90,00,0,7
SPIWrite 0f91,00,0,7
SPIWrite 0f92,00,0,7
SPIWrite 0f93,00,0,7
SPIWrite 0f94,00,0,7
SPIWrite 0f95,00,0,7
SPIWrite 0f96,00,0,7
SPIWrite 0f97,00,0,7
SPIWrite 0f98,00,0,7
SPIWrite 0f99,00,0,7
SPIWrite 0f9a,00,0,7
SPIWrite 0f9b,00,0,7
SPIWrite 0f9c,00,0,7
SPIWrite 0f9d,00,0,7
SPIWrite 0f9e,00,0,7
SPIWrite 0f9f,00,0,7
SPIWrite 0fa0,00,0,7
SPIWrite 0fa1,00,0,7
SPIWrite 0fa2,00,0,7
SPIWrite 0fa3,00,0,7
SPIWrite 0fa4,00,0,7
SPIWrite 0fa5,00,0,7
SPIWrite 0fa6,00,0,7
SPIWrite 0fa7,00,0,7
SPIWrite 0fa8,00,0,7
SPIWrite 0fa9,00,0,7
SPIWrite 0faa,00,0,7
SPIWrite 0fab,00,0,7
SPIWrite 0fac,00,0,7
SPIWrite 0fad,00,0,7
SPIWrite 0fae,00,0,7

SPIWrite 0faf,00,0,7
SPIWrite 0fb0,00,0,7
SPIWrite 0fb1,00,0,7
SPIWrite 0fb2,00,0,7
SPIWrite 0fb3,00,0,7
SPIWrite 0fb4,00,0,7
SPIWrite 0fb5,00,0,7
SPIWrite 0fb6,00,0,7
SPIWrite 0fb7,00,0,7
SPIWrite 0fb8,00,0,7
SPIWrite 0fb9,00,0,7
SPIWrite 0fba,00,0,7
SPIWrite 0fbb,00,0,7
SPIWrite 0fbc,00,0,7
SPIWrite 0fbd,00,0,7
SPIWrite 0fbe,00,0,7
SPIWrite 0fbf,00,0,7
SPIWrite 0fc0,00,0,7
SPIWrite 0fc1,00,0,7
SPIWrite 0fc2,00,0,7
SPIWrite 0fc3,00,0,7
SPIWrite 0fc4,00,0,7
SPIWrite 0fc5,00,0,7
SPIWrite 0fc6,00,0,7
SPIWrite 0fc7,00,0,7
SPIWrite 0fc8,00,0,7
SPIWrite 0fc9,00,0,7
SPIWrite 0fca,00,0,7
SPIWrite 0fcb,00,0,7
SPIWrite 0fcc,00,0,7
SPIWrite 0fcd,00,0,7
SPIWrite 0fce,00,0,7
SPIWrite 0fcf,00,0,7
SPIWrite 0fd0,00,0,7
SPIWrite 0fd1,00,0,7
SPIWrite 0fd2,00,0,7
SPIWrite 0fd3,00,0,7
SPIWrite 0fd4,00,0,7
SPIWrite 0fd5,00,0,7
SPIWrite 0fd6,00,0,7
SPIWrite 0fd7,00,0,7
SPIWrite 0fd8,00,0,7
SPIWrite 0fd9,00,0,7
SPIWrite 0fda,00,0,7
SPIWrite 0fdb,00,0,7
SPIWrite 0fdc,00,0,7
SPIWrite 0fdd,00,0,7
SPIWrite 0fde,00,0,7
SPIWrite 0fdf,00,0,7
SPIWrite 0fe0,00,0,7
SPIWrite 0fe1,00,0,7
SPIWrite 0fe2,00,0,7
SPIWrite 0fe3,00,0,7
SPIWrite 0fe4,00,0,7
SPIWrite 0fe5,00,0,7
SPIWrite 0fe6,00,0,7
SPIWrite 0fe7,00,0,7
SPIWrite 0fe8,00,0,7
SPIWrite 0fe9,00,0,7
SPIWrite 0fea,00,0,7
SPIWrite 0feb,00,0,7
SPIWrite 0fec,00,0,7
SPIWrite 0fed,00,0,7
SPIWrite 0fee,00,0,7
SPIWrite 0fef,00,0,7
SPIWrite 0ff0,00,0,7
SPIWrite 0ff1,00,0,7
SPIWrite 0ff2,00,0,7
SPIWrite 0ff3,00,0,7

SPIWrite 0ff4,00,0,7
SPIWrite 0ff5,00,0,7
SPIWrite 0ff6,00,0,7
SPIWrite 0ff7,00,0,7
SPIWrite 0ff8,00,0,7
SPIWrite 0ff9,00,0,7
SPIWrite 0ffa,00,0,7
SPIWrite 0ffb,00,0,7
SPIWrite 0ffc,00,0,7
SPIWrite 0ffd,00,0,7
SPIWrite 0ffe,00,0,7
SPIWrite 0fff,00,0,7
SPIWrite 1000,00,0,7
SPIWrite 1001,00,0,7
SPIWrite 1002,00,0,7
SPIWrite 1003,00,0,7
SPIWrite 1004,00,0,7
SPIWrite 1005,00,0,7
SPIWrite 1006,00,0,7
SPIWrite 1007,00,0,7
SPIWrite 1008,00,0,7
SPIWrite 1009,00,0,7
SPIWrite 100a,00,0,7
SPIWrite 100b,00,0,7
SPIWrite 100c,00,0,7
SPIWrite 100d,00,0,7
SPIWrite 100e,00,0,7
SPIWrite 100f,00,0,7
SPIWrite 1010,00,0,7
SPIWrite 1011,00,0,7
SPIWrite 1012,00,0,7
SPIWrite 1013,00,0,7
SPIWrite 1014,00,0,7
SPIWrite 1015,00,0,7
SPIWrite 1016,00,0,7
SPIWrite 1017,00,0,7
SPIWrite 1018,00,0,7
SPIWrite 1019,00,0,7
SPIWrite 101a,00,0,7
SPIWrite 101b,00,0,7
SPIWrite 101c,00,0,7
SPIWrite 101d,00,0,7
SPIWrite 101e,00,0,7
SPIWrite 101f,00,0,7

WAIT 0.5

SPIWrite 0012,00,4,4 //PAGE: sys_calib_macro_memory=0x0;(Meaning:); Address(0x12[4:4],)
SPIWrite 0013,10,4,4 //PAGE: customer_macro=0x1;(Meaning:); Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,10,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,81,0,7

SPIPoll 00f0,1,1,1

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4 //PAGE: customer_macro=0x0;(Meaning:); Address(0x13[4:4],)
SPIWrite 0013,20,5,5 //PAGE: cm4_macro=0x1; Address(0x13[5:5],)

\\Read MACRO_READY=0x1; Address(0x20[0:0],)

\\Read MACRO_ACK=0x1; Address(0x20[1:1],)

\\Read MACRO_DONE=0x1; Address(0x20[2:2],)

SPIReadCheck 0020,3,3,00

\\Read MACRO_ERROR=0x0; Address(0x20[3:3],)

SPIWrite 0013,00,5,5 //PAGE: cm4_macro=0x0; Address(0x13[5:5],)

SPIWrite 0012,10,4,4 //PAGE: sys_calib_macro_memory=0x1;(Meaning:); Address(0x12[4:4],)

SPIWrite 0040,00,0,7

SPIWrite 0020,00,0,7

SPIWrite 0021,7c,0,7

SPIWrite 0022,01,0,7

SPIWrite 0023,20,0,7

SPIWrite 0024,91,0,7

SPIWrite 0025,00,0,7

SPIWrite 0026,00,0,7

SPIWrite 0027,00,0,7

SPIWrite 0028,cd,0,7

SPIWrite 0029,d3,0,7

SPIWrite 002a,01,0,7

SPIWrite 002b,00,0,7

SPIWrite 002c,e9,0,7

SPIWrite 002d,d3,0,7

SPIWrite 002e,01,0,7

SPIWrite 002f,00,0,7

SPIWrite 0030,db,0,7

SPIWrite 0031,d3,0,7

SPIWrite 0032,01,0,7

SPIWrite 0033,00,0,7

SPIWrite 0034,05,0,7

SPIWrite 0035,d4,0,7

SPIWrite 0036,01,0,7

SPIWrite 0037,00,0,7

SPIWrite 0038,a3,0,7

SPIWrite 0039,d3,0,7

SPIWrite 003a,01,0,7

SPIWrite 003b,00,0,7

SPIWrite 003c,00,0,7

SPIWrite 003d,00,0,7

SPIWrite 003e,00,0,7

SPIWrite 003f,00,0,7

SPIWrite 0040,00,0,7

SPIWrite 0041,00,0,7

SPIWrite 0042,00,0,7

SPIWrite 0043,00,0,7

SPIWrite 0044,00,0,7

SPIWrite 0045,00,0,7

SPIWrite 0046,00,0,7

SPIWrite 0047,00,0,7

SPIWrite 0048,00,0,7

SPIWrite 0049,00,0,7

SPIWrite 004a,00,0,7

SPIWrite 004b,00,0,7

SPIWrite 004c,b1,0,7

SPIWrite 004d,d3,0,7

SPIWrite 004e,01,0,7

SPIWrite 004f,00,0,7

SPIWrite 0050,f7,0,7

SPIWrite 0051,d3,0,7

SPIWrite 0052,01,0,7

SPIWrite 0053,00,0,7

SPIWrite 0054,00,0,7

SPIWrite 0055,00,0,7
SPIWrite 0056,00,0,7
SPIWrite 0057,00,0,7
SPIWrite 0058,bf,0,7
SPIWrite 0059,d3,0,7
SPIWrite 005a,01,0,7
SPIWrite 005b,00,0,7
SPIWrite 005c,af,0,7
SPIWrite 005d,d3,0,7
SPIWrite 005e,01,0,7
SPIWrite 005f,00,0,7
SPIWrite 0060,9f,0,7
SPIWrite 0061,d5,0,7
SPIWrite 0062,01,0,7
SPIWrite 0063,00,0,7
SPIWrite 0064,57,0,7
SPIWrite 0065,d4,0,7
SPIWrite 0066,01,0,7
SPIWrite 0067,00,0,7
SPIWrite 0068,61,0,7
SPIWrite 0069,d4,0,7
SPIWrite 006a,01,0,7
SPIWrite 006b,00,0,7
SPIWrite 006c,31,0,7
SPIWrite 006d,d4,0,7
SPIWrite 006e,01,0,7
SPIWrite 006f,00,0,7
SPIWrite 0070,43,0,7
SPIWrite 0071,d4,0,7
SPIWrite 0072,01,0,7
SPIWrite 0073,00,0,7
SPIWrite 0074,55,0,7
SPIWrite 0075,d4,0,7
SPIWrite 0076,01,0,7
SPIWrite 0077,00,0,7
SPIWrite 0078,21,0,7
SPIWrite 0079,d4,0,7
SPIWrite 007a,01,0,7
SPIWrite 007b,00,0,7
SPIWrite 007c,55,0,7
SPIWrite 007d,d4,0,7
SPIWrite 007e,01,0,7
SPIWrite 007f,00,0,7
SPIWrite 0080,15,0,7
SPIWrite 0081,ff,0,7
SPIWrite 0082,00,0,7
SPIWrite 0083,00,0,7
SPIWrite 0084,55,0,7
SPIWrite 0085,d4,0,7
SPIWrite 0086,01,0,7
SPIWrite 0087,00,0,7
SPIWrite 0088,79,0,7
SPIWrite 0089,80,0,7
SPIWrite 008a,02,0,7
SPIWrite 008b,00,0,7
SPIWrite 008c,55,0,7
SPIWrite 008d,d4,0,7
SPIWrite 008e,01,0,7
SPIWrite 008f,00,0,7
SPIWrite 0090,55,0,7
SPIWrite 0091,d4,0,7
SPIWrite 0092,01,0,7
SPIWrite 0093,00,0,7
SPIWrite 0094,57,0,7
SPIWrite 0095,81,0,7
SPIWrite 0096,02,0,7
SPIWrite 0097,00,0,7
SPIWrite 0098,55,0,7
SPIWrite 0099,d4,0,7

SPIWrite 009a,01,0,7
SPIWrite 009b,00,0,7
SPIWrite 009c,55,0,7
SPIWrite 009d,d4,0,7
SPIWrite 009e,01,0,7
SPIWrite 009f,00,0,7
SPIWrite 00a0,6d,0,7
SPIWrite 00a1,d4,0,7
SPIWrite 00a2,01,0,7
SPIWrite 00a3,00,0,7
SPIWrite 00a4,55,0,7
SPIWrite 00a5,d4,0,7
SPIWrite 00a6,01,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a8,55,0,7
SPIWrite 00a9,d4,0,7
SPIWrite 00aa,01,0,7
SPIWrite 00ab,00,0,7
SPIWrite 00ac,79,0,7
SPIWrite 00ad,fd,0,7
SPIWrite 00ae,00,0,7
SPIWrite 00af,00,0,7
SPIWrite 00b0,55,0,7
SPIWrite 00b1,d4,0,7
SPIWrite 00b2,01,0,7
SPIWrite 00b3,00,0,7
SPIWrite 00b4,55,0,7
SPIWrite 00b5,d4,0,7
SPIWrite 00b6,01,0,7
SPIWrite 00b7,00,0,7
SPIWrite 00b8,5d,0,7
SPIWrite 00b9,8d,0,7
SPIWrite 00ba,02,0,7
SPIWrite 00bb,00,0,7
SPIWrite 00bc,00,0,7
SPIWrite 00bd,00,0,7
SPIWrite 00be,00,0,7
SPIWrite 00bf,00,0,7
SPIWrite 00c0,00,0,7
SPIWrite 00c1,00,0,7
SPIWrite 00c2,00,0,7
SPIWrite 00c3,00,0,7
SPIWrite 00c4,00,0,7
SPIWrite 00c5,00,0,7
SPIWrite 00c6,00,0,7
SPIWrite 00c7,00,0,7
SPIWrite 00c8,00,0,7
SPIWrite 00c9,00,0,7
SPIWrite 00ca,00,0,7
SPIWrite 00cb,00,0,7
SPIWrite 00cc,00,0,7
SPIWrite 00cd,00,0,7
SPIWrite 00ce,00,0,7
SPIWrite 00cf,00,0,7
SPIWrite 00d0,00,0,7
SPIWrite 00d1,00,0,7
SPIWrite 00d2,00,0,7
SPIWrite 00d3,00,0,7
SPIWrite 00d4,00,0,7
SPIWrite 00d5,00,0,7
SPIWrite 00d6,00,0,7
SPIWrite 00d7,00,0,7
SPIWrite 00d8,00,0,7
SPIWrite 00d9,00,0,7
SPIWrite 00da,00,0,7
SPIWrite 00db,00,0,7
SPIWrite 00dc,00,0,7
SPIWrite 00dd,00,0,7
SPIWrite 00de,00,0,7

SPIWrite 00df,00,0,7
SPIWrite 00e0,00,0,7
SPIWrite 00e1,00,0,7
SPIWrite 00e2,00,0,7
SPIWrite 00e3,00,0,7
SPIWrite 00e4,00,0,7
SPIWrite 00e5,00,0,7
SPIWrite 00e6,00,0,7
SPIWrite 00e7,00,0,7
SPIWrite 00e8,00,0,7
SPIWrite 00e9,00,0,7
SPIWrite 00ea,00,0,7
SPIWrite 00eb,00,0,7
SPIWrite 00ec,00,0,7
SPIWrite 00ed,00,0,7
SPIWrite 00ee,00,0,7
SPIWrite 00ef,00,0,7
SPIWrite 00f0,00,0,7
SPIWrite 00f1,00,0,7
SPIWrite 00f2,00,0,7
SPIWrite 00f3,00,0,7
SPIWrite 00f4,00,0,7
SPIWrite 00f5,00,0,7
SPIWrite 00f6,00,0,7
SPIWrite 00f7,00,0,7
SPIWrite 00f8,00,0,7
SPIWrite 00f9,00,0,7
SPIWrite 00fa,00,0,7
SPIWrite 00fb,00,0,7
SPIWrite 00fc,00,0,7
SPIWrite 00fd,00,0,7
SPIWrite 00fe,00,0,7
SPIWrite 00ff,00,0,7
SPIWrite 0100,00,0,7
SPIWrite 0101,00,0,7
SPIWrite 0102,00,0,7
SPIWrite 0103,00,0,7
SPIWrite 0104,00,0,7
SPIWrite 0105,00,0,7
SPIWrite 0106,00,0,7
SPIWrite 0107,00,0,7
SPIWrite 0108,00,0,7
SPIWrite 0109,00,0,7
SPIWrite 010a,00,0,7
SPIWrite 010b,00,0,7
SPIWrite 010c,00,0,7
SPIWrite 010d,00,0,7
SPIWrite 010e,00,0,7
SPIWrite 010f,00,0,7
SPIWrite 0110,00,0,7
SPIWrite 0111,00,0,7
SPIWrite 0112,00,0,7
SPIWrite 0113,00,0,7
SPIWrite 0114,00,0,7
SPIWrite 0115,00,0,7
SPIWrite 0116,00,0,7
SPIWrite 0117,00,0,7
SPIWrite 0118,00,0,7
SPIWrite 0119,00,0,7
SPIWrite 011a,00,0,7
SPIWrite 011b,00,0,7
SPIWrite 011c,00,0,7
SPIWrite 011d,00,0,7
SPIWrite 011e,00,0,7
SPIWrite 011f,00,0,7
SPIWrite 0120,00,0,7
SPIWrite 0121,00,0,7
SPIWrite 0122,00,0,7
SPIWrite 0123,00,0,7

SPIWrite 0124,00,0,7
SPIWrite 0125,00,0,7
SPIWrite 0126,00,0,7
SPIWrite 0127,00,0,7
SPIWrite 0128,00,0,7
SPIWrite 0129,00,0,7
SPIWrite 012a,00,0,7
SPIWrite 012b,00,0,7
SPIWrite 012c,00,0,7
SPIWrite 012d,00,0,7
SPIWrite 012e,00,0,7
SPIWrite 012f,00,0,7
SPIWrite 0130,00,0,7
SPIWrite 0131,00,0,7
SPIWrite 0132,00,0,7
SPIWrite 0133,00,0,7
SPIWrite 0134,00,0,7
SPIWrite 0135,00,0,7
SPIWrite 0136,00,0,7
SPIWrite 0137,00,0,7
SPIWrite 0138,00,0,7
SPIWrite 0139,00,0,7
SPIWrite 013a,00,0,7
SPIWrite 013b,00,0,7
SPIWrite 013c,00,0,7
SPIWrite 013d,00,0,7
SPIWrite 013e,00,0,7
SPIWrite 013f,00,0,7
SPIWrite 0140,00,0,7
SPIWrite 0141,00,0,7
SPIWrite 0142,00,0,7
SPIWrite 0143,00,0,7
SPIWrite 0144,00,0,7
SPIWrite 0145,00,0,7
SPIWrite 0146,00,0,7
SPIWrite 0147,00,0,7
SPIWrite 0148,00,0,7
SPIWrite 0149,00,0,7
SPIWrite 014a,00,0,7
SPIWrite 014b,00,0,7
SPIWrite 014c,00,0,7
SPIWrite 014d,00,0,7
SPIWrite 014e,00,0,7
SPIWrite 014f,00,0,7
SPIWrite 0150,00,0,7
SPIWrite 0151,00,0,7
SPIWrite 0152,00,0,7
SPIWrite 0153,00,0,7
SPIWrite 0154,00,0,7
SPIWrite 0155,00,0,7
SPIWrite 0156,00,0,7
SPIWrite 0157,00,0,7
SPIWrite 0158,00,0,7
SPIWrite 0159,00,0,7
SPIWrite 015a,00,0,7
SPIWrite 015b,00,0,7
SPIWrite 015c,00,0,7
SPIWrite 015d,00,0,7
SPIWrite 015e,00,0,7
SPIWrite 015f,00,0,7
SPIWrite 0160,00,0,7
SPIWrite 0161,00,0,7
SPIWrite 0162,00,0,7
SPIWrite 0163,00,0,7
SPIWrite 0164,00,0,7
SPIWrite 0165,00,0,7
SPIWrite 0166,00,0,7
SPIWrite 0167,00,0,7
SPIWrite 0168,00,0,7

SPIWrite 0169,00,0,7
SPIWrite 016a,00,0,7
SPIWrite 016b,00,0,7
SPIWrite 016c,00,0,7
SPIWrite 016d,00,0,7
SPIWrite 016e,00,0,7
SPIWrite 016f,00,0,7
SPIWrite 0170,00,0,7
SPIWrite 0171,00,0,7
SPIWrite 0172,00,0,7
SPIWrite 0173,00,0,7
SPIWrite 0174,00,0,7
SPIWrite 0175,00,0,7
SPIWrite 0176,00,0,7
SPIWrite 0177,00,0,7
SPIWrite 0178,00,0,7
SPIWrite 0179,00,0,7
SPIWrite 017a,00,0,7
SPIWrite 017b,00,0,7
SPIWrite 017c,00,0,7
SPIWrite 017d,00,0,7
SPIWrite 017e,00,0,7
SPIWrite 017f,00,0,7
SPIWrite 0180,00,0,7
SPIWrite 0181,00,0,7
SPIWrite 0182,00,0,7
SPIWrite 0183,00,0,7
SPIWrite 0184,00,0,7
SPIWrite 0185,00,0,7
SPIWrite 0186,00,0,7
SPIWrite 0187,00,0,7
SPIWrite 0188,00,0,7
SPIWrite 0189,00,0,7
SPIWrite 018a,00,0,7
SPIWrite 018b,00,0,7
SPIWrite 018c,00,0,7
SPIWrite 018d,00,0,7
SPIWrite 018e,00,0,7
SPIWrite 018f,00,0,7
SPIWrite 0190,00,0,7
SPIWrite 0191,00,0,7
SPIWrite 0192,00,0,7
SPIWrite 0193,00,0,7
SPIWrite 0194,00,0,7
SPIWrite 0195,00,0,7
SPIWrite 0196,00,0,7
SPIWrite 0197,00,0,7
SPIWrite 0198,00,0,7
SPIWrite 0199,00,0,7
SPIWrite 019a,00,0,7
SPIWrite 019b,00,0,7
SPIWrite 019c,00,0,7
SPIWrite 019d,00,0,7
SPIWrite 019e,00,0,7
SPIWrite 019f,00,0,7
SPIWrite 01a0,00,0,7
SPIWrite 01a1,00,0,7
SPIWrite 01a2,00,0,7
SPIWrite 01a3,00,0,7
SPIWrite 01a4,00,0,7
SPIWrite 01a5,00,0,7
SPIWrite 01a6,00,0,7
SPIWrite 01a7,00,0,7
SPIWrite 01a8,00,0,7
SPIWrite 01a9,00,0,7
SPIWrite 01aa,00,0,7
SPIWrite 01ab,00,0,7
SPIWrite 01ac,00,0,7
SPIWrite 01ad,00,0,7

SPIWrite 01ae,00,0,7
SPIWrite 01af,00,0,7
SPIWrite 01b0,00,0,7
SPIWrite 01b1,00,0,7
SPIWrite 01b2,00,0,7
SPIWrite 01b3,00,0,7
SPIWrite 01b4,00,0,7
SPIWrite 01b5,00,0,7
SPIWrite 01b6,00,0,7
SPIWrite 01b7,00,0,7
SPIWrite 01b8,00,0,7
SPIWrite 01b9,00,0,7
SPIWrite 01ba,00,0,7
SPIWrite 01bb,00,0,7
SPIWrite 01bc,00,0,7
SPIWrite 01bd,00,0,7
SPIWrite 01be,00,0,7
SPIWrite 01bf,00,0,7
SPIWrite 01c0,00,0,7
SPIWrite 01c1,00,0,7
SPIWrite 01c2,00,0,7
SPIWrite 01c3,00,0,7
SPIWrite 01c4,00,0,7
SPIWrite 01c5,00,0,7
SPIWrite 01c6,00,0,7
SPIWrite 01c7,00,0,7
SPIWrite 01c8,00,0,7
SPIWrite 01c9,00,0,7
SPIWrite 01ca,00,0,7
SPIWrite 01cb,00,0,7
SPIWrite 01cc,00,0,7
SPIWrite 01cd,00,0,7
SPIWrite 01ce,00,0,7
SPIWrite 01cf,00,0,7
SPIWrite 01d0,00,0,7
SPIWrite 01d1,00,0,7
SPIWrite 01d2,00,0,7
SPIWrite 01d3,00,0,7
SPIWrite 01d4,00,0,7
SPIWrite 01d5,00,0,7
SPIWrite 01d6,00,0,7
SPIWrite 01d7,00,0,7
SPIWrite 01d8,00,0,7
SPIWrite 01d9,00,0,7
SPIWrite 01da,00,0,7
SPIWrite 01db,00,0,7
SPIWrite 01dc,00,0,7
SPIWrite 01dd,00,0,7
SPIWrite 01de,00,0,7
SPIWrite 01df,00,0,7
SPIWrite 01e0,00,0,7
SPIWrite 01e1,00,0,7
SPIWrite 01e2,00,0,7
SPIWrite 01e3,00,0,7
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SPIWrite 06ff,00,0,7
SPIWrite 0700,00,0,7
SPIWrite 0701,00,0,7
SPIWrite 0702,00,0,7
SPIWrite 0703,00,0,7
SPIWrite 0704,00,0,7
SPIWrite 0705,00,0,7
SPIWrite 0706,00,0,7
SPIWrite 0707,00,0,7
SPIWrite 0708,00,0,7
SPIWrite 0709,00,0,7
SPIWrite 070a,00,0,7
SPIWrite 070b,00,0,7
SPIWrite 070c,00,0,7
SPIWrite 070d,00,0,7
SPIWrite 070e,00,0,7
SPIWrite 070f,00,0,7
SPIWrite 0710,00,0,7
SPIWrite 0711,00,0,7

SPIWrite 0712,00,0,7
SPIWrite 0713,00,0,7
SPIWrite 0714,00,0,7
SPIWrite 0715,00,0,7
SPIWrite 0716,00,0,7
SPIWrite 0717,00,0,7
SPIWrite 0718,00,0,7
SPIWrite 0719,00,0,7
SPIWrite 071a,00,0,7
SPIWrite 071b,00,0,7
SPIWrite 071c,00,0,7
SPIWrite 071d,00,0,7
SPIWrite 071e,00,0,7
SPIWrite 071f,00,0,7
SPIWrite 0720,00,0,7
SPIWrite 0721,00,0,7
SPIWrite 0722,00,0,7
SPIWrite 0723,00,0,7
SPIWrite 0724,00,0,7
SPIWrite 0725,00,0,7
SPIWrite 0726,00,0,7
SPIWrite 0727,00,0,7
SPIWrite 0728,00,0,7
SPIWrite 0729,00,0,7
SPIWrite 072a,00,0,7
SPIWrite 072b,00,0,7
SPIWrite 072c,00,0,7
SPIWrite 072d,00,0,7
SPIWrite 072e,00,0,7
SPIWrite 072f,00,0,7
SPIWrite 0730,00,0,7
SPIWrite 0731,00,0,7
SPIWrite 0732,00,0,7
SPIWrite 0733,00,0,7
SPIWrite 0734,00,0,7
SPIWrite 0735,00,0,7
SPIWrite 0736,00,0,7
SPIWrite 0737,00,0,7
SPIWrite 0738,00,0,7
SPIWrite 0739,00,0,7
SPIWrite 073a,00,0,7
SPIWrite 073b,00,0,7
SPIWrite 073c,00,0,7
SPIWrite 073d,00,0,7
SPIWrite 073e,00,0,7
SPIWrite 073f,00,0,7
SPIWrite 0740,00,0,7
SPIWrite 0741,00,0,7
SPIWrite 0742,00,0,7
SPIWrite 0743,00,0,7
SPIWrite 0744,00,0,7
SPIWrite 0745,00,0,7
SPIWrite 0746,00,0,7
SPIWrite 0747,00,0,7
SPIWrite 0748,00,0,7
SPIWrite 0749,00,0,7
SPIWrite 074a,00,0,7
SPIWrite 074b,00,0,7
SPIWrite 074c,00,0,7
SPIWrite 074d,00,0,7
SPIWrite 074e,00,0,7
SPIWrite 074f,00,0,7
SPIWrite 0750,00,0,7
SPIWrite 0751,00,0,7
SPIWrite 0752,00,0,7
SPIWrite 0753,00,0,7
SPIWrite 0754,00,0,7
SPIWrite 0755,00,0,7
SPIWrite 0756,00,0,7

SPIWrite 0757,00,0,7
SPIWrite 0758,00,0,7
SPIWrite 0759,00,0,7
SPIWrite 075a,00,0,7
SPIWrite 075b,00,0,7
SPIWrite 075c,00,0,7
SPIWrite 075d,00,0,7
SPIWrite 075e,00,0,7
SPIWrite 075f,00,0,7
SPIWrite 0760,00,0,7
SPIWrite 0761,00,0,7
SPIWrite 0762,00,0,7
SPIWrite 0763,00,0,7
SPIWrite 0764,00,0,7
SPIWrite 0765,00,0,7
SPIWrite 0766,00,0,7
SPIWrite 0767,00,0,7
SPIWrite 0768,00,0,7
SPIWrite 0769,00,0,7
SPIWrite 076a,00,0,7
SPIWrite 076b,00,0,7
SPIWrite 076c,00,0,7
SPIWrite 076d,00,0,7
SPIWrite 076e,00,0,7
SPIWrite 076f,00,0,7
SPIWrite 0770,00,0,7
SPIWrite 0771,00,0,7
SPIWrite 0772,00,0,7
SPIWrite 0773,00,0,7
SPIWrite 0774,00,0,7
SPIWrite 0775,00,0,7
SPIWrite 0776,00,0,7
SPIWrite 0777,00,0,7
SPIWrite 0778,00,0,7
SPIWrite 0779,00,0,7
SPIWrite 077a,00,0,7
SPIWrite 077b,00,0,7
SPIWrite 077c,00,0,7
SPIWrite 077d,00,0,7
SPIWrite 077e,00,0,7
SPIWrite 077f,00,0,7
SPIWrite 0780,00,0,7
SPIWrite 0781,00,0,7
SPIWrite 0782,00,0,7
SPIWrite 0783,00,0,7
SPIWrite 0784,00,0,7
SPIWrite 0785,00,0,7
SPIWrite 0786,00,0,7
SPIWrite 0787,00,0,7
SPIWrite 0788,00,0,7
SPIWrite 0789,00,0,7
SPIWrite 078a,00,0,7
SPIWrite 078b,00,0,7
SPIWrite 078c,00,0,7
SPIWrite 078d,00,0,7
SPIWrite 078e,00,0,7
SPIWrite 078f,00,0,7
SPIWrite 0790,00,0,7
SPIWrite 0791,00,0,7
SPIWrite 0792,00,0,7
SPIWrite 0793,00,0,7
SPIWrite 0794,00,0,7
SPIWrite 0795,00,0,7
SPIWrite 0796,00,0,7
SPIWrite 0797,00,0,7
SPIWrite 0798,00,0,7
SPIWrite 0799,00,0,7
SPIWrite 079a,00,0,7
SPIWrite 079b,00,0,7

SPIWrite 079c,00,0,7
SPIWrite 079d,00,0,7
SPIWrite 079e,00,0,7
SPIWrite 079f,00,0,7
SPIWrite 07a0,00,0,7
SPIWrite 07a1,00,0,7
SPIWrite 07a2,00,0,7
SPIWrite 07a3,00,0,7
SPIWrite 07a4,00,0,7
SPIWrite 07a5,00,0,7
SPIWrite 07a6,00,0,7
SPIWrite 07a7,00,0,7
SPIWrite 07a8,00,0,7
SPIWrite 07a9,00,0,7
SPIWrite 07aa,00,0,7
SPIWrite 07ab,00,0,7
SPIWrite 07ac,00,0,7
SPIWrite 07ad,00,0,7
SPIWrite 07ae,00,0,7
SPIWrite 07af,00,0,7
SPIWrite 07b0,00,0,7
SPIWrite 07b1,00,0,7
SPIWrite 07b2,00,0,7
SPIWrite 07b3,00,0,7
SPIWrite 07b4,00,0,7
SPIWrite 07b5,00,0,7
SPIWrite 07b6,00,0,7
SPIWrite 07b7,00,0,7
SPIWrite 07b8,00,0,7
SPIWrite 07b9,00,0,7
SPIWrite 07ba,00,0,7
SPIWrite 07bb,00,0,7
SPIWrite 07bc,00,0,7
SPIWrite 07bd,00,0,7
SPIWrite 07be,00,0,7
SPIWrite 07bf,00,0,7
SPIWrite 07c0,00,0,7
SPIWrite 07c1,00,0,7
SPIWrite 07c2,00,0,7
SPIWrite 07c3,00,0,7
SPIWrite 07c4,00,0,7
SPIWrite 07c5,00,0,7
SPIWrite 07c6,00,0,7
SPIWrite 07c7,00,0,7
SPIWrite 07c8,00,0,7
SPIWrite 07c9,00,0,7
SPIWrite 07ca,00,0,7
SPIWrite 07cb,00,0,7
SPIWrite 07cc,00,0,7
SPIWrite 07cd,00,0,7
SPIWrite 07ce,00,0,7
SPIWrite 07cf,00,0,7
SPIWrite 07d0,00,0,7
SPIWrite 07d1,00,0,7
SPIWrite 07d2,00,0,7
SPIWrite 07d3,00,0,7
SPIWrite 07d4,00,0,7
SPIWrite 07d5,00,0,7
SPIWrite 07d6,00,0,7
SPIWrite 07d7,00,0,7
SPIWrite 07d8,00,0,7
SPIWrite 07d9,00,0,7
SPIWrite 07da,00,0,7
SPIWrite 07db,00,0,7
SPIWrite 07dc,00,0,7
SPIWrite 07dd,00,0,7
SPIWrite 07de,00,0,7
SPIWrite 07df,00,0,7
SPIWrite 07e0,00,0,7

```
SPIWrite 07e1,00,0,7
SPIWrite 07e2,00,0,7
SPIWrite 07e3,00,0,7
SPIWrite 07e4,00,0,7
SPIWrite 07e5,00,0,7
SPIWrite 07e6,00,0,7
SPIWrite 07e7,00,0,7
SPIWrite 07e8,00,0,7
SPIWrite 07e9,00,0,7
SPIWrite 07ea,00,0,7
SPIWrite 07eb,00,0,7
SPIWrite 07ec,00,0,7
SPIWrite 07ed,00,0,7
SPIWrite 07ee,00,0,7
SPIWrite 07ef,00,0,7
SPIWrite 07f0,00,0,7
SPIWrite 07f1,00,0,7
SPIWrite 07f2,00,0,7
SPIWrite 07f3,00,0,7
SPIWrite 07f4,00,0,7
SPIWrite 07f5,00,0,7
SPIWrite 07f6,00,0,7
SPIWrite 07f7,00,0,7
SPIWrite 07f8,00,0,7
SPIWrite 07f9,00,0,7
SPIWrite 07fa,00,0,7
SPIWrite 07fb,00,0,7
SPIWrite 07fc,00,0,7
SPIWrite 07fd,00,0,7
SPIWrite 07fe,00,0,7
SPIWrite 07ff,00,0,7
SPIWrite 0800,00,0,7
SPIWrite 0801,00,0,7
SPIWrite 0802,00,0,7
SPIWrite 0803,00,0,7
SPIWrite 0804,00,0,7
SPIWrite 0805,00,0,7
SPIWrite 0806,00,0,7
SPIWrite 0807,00,0,7
SPIWrite 0808,00,0,7
SPIWrite 0809,00,0,7
SPIWrite 080a,00,0,7
SPIWrite 080b,00,0,7
SPIWrite 080c,00,0,7
SPIWrite 080d,00,0,7
SPIWrite 080e,00,0,7
SPIWrite 080f,00,0,7
SPIWrite 0810,00,0,7
SPIWrite 0811,00,0,7
SPIWrite 0812,00,0,7
SPIWrite 0813,00,0,7
SPIWrite 0814,00,0,7
SPIWrite 0815,00,0,7
SPIWrite 0816,00,0,7
SPIWrite 0817,00,0,7
SPIWrite 0818,00,0,7
SPIWrite 0819,00,0,7
SPIWrite 081a,00,0,7
SPIWrite 081b,00,0,7
SPIWrite 081c,00,0,7
SPIWrite 081d,00,0,7
SPIWrite 081e,00,0,7
SPIWrite 081f,00,0,7
SPIWrite 0012,00,4,4 //PAGE: sys_calib_macro_memory=0x0; (Meaning: ); Address(0x12[4:4],)
SPIWrite 0013,10,4,4 //PAGE: customer_macro=0x1; (Meaning: ); Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,10,0,7
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SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,10,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,81,0,7

SPIPoll 00f0,1,1,1

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0; (Meaning: );    Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;    Address(0x13[5:5],)

\\Read  MACRO_READY=0x1;    Address(0x20[0:0],)

\\Read  MACRO_ACK=0x1;    Address(0x20[1:1],)

\\Read  MACRO_DONE=0x1;    Address(0x20[2:2],)

SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)

SPIWrite 0013,00,5,5    //PAGE: cm4_macro=0x0;    Address(0x13[5:5],)
SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1; (Meaning: );    Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,10,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,81,0,7

SPIPoll 00f0,1,1,1

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0; (Meaning: );    Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;    Address(0x13[5:5],)

\\Read  MACRO_READY=0x1;    Address(0x20[0:0],)

\\Read  MACRO_ACK=0x1;    Address(0x20[1:1],)

\\Read  MACRO_DONE=0x1;    Address(0x20[2:2],)

SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)

SPIWrite 0013,00,0,7    //PAGE: cm4_macro=0x0;    Address(0x13[5:5],)
\\ STEP: rstMCU/step2

\\START: Loading PLL EFuse trims
```

```

SPIWrite 0013,10,0,7    //PAGE: customer_macro=0x1;(Meaning: );    Address(0x13[4:4],)
SPIWrite 0144,00,0,7
SPIWrite 0144,00,0,7
SPIWrite 0013,00,0,7    //PAGE: customer_macro=0x0;(Meaning: );    Address(0x13[4:4],)
SPIWrite 0013,02,0,7    //PAGE: cm4top_dram=0x1;(Meaning: );    Address(0x13[1:1],)
SPIWrite 3f10,20,0,7
SPIWrite 3f12,ce,0,7
SPIWrite 3f13,ff,0,7
SPIWrite 3f14,7f,0,7
SPIWrite 3f15,00,0,7
SPIWrite 3ee6,01,0,7
SPIWrite 3f64,00,0,7
SPIWrite 3f65,00,0,7
SPIWrite 3f66,00,0,7
SPIWrite 3f67,01,0,7
SPIWrite 0013,00,0,7    //PAGE: cm4top_dram=0x0;(Meaning: );    Address(0x13[1:1],)
SPIWrite 0013,10,0,7    //PAGE: customer_macro=0x1;(Meaning: );    Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0193,25,0,7

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,0,7    //PAGE: customer_macro=0x0;(Meaning: );    Address(0x13[4:4],)
SPIWrite 0013,20,0,7    //PAGE: cm4_macro=0x1;    Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)

SPIWrite 0013,00,0,7    //PAGE: cm4_macro=0x0;    Address(0x13[5:5],)
SPIWrite 0013,10,0,7    //PAGE: customer_macro=0x1;(Meaning: );    Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,12,0,7

SPIPoll 00f0,0,7,7

\\END: Done Loading PLL EFuse trims

\\START: Configuring TOP parameters for MCU

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,03,0,7
SPIWrite 00a1,1f,0,7
SPIWrite 00a0,1f,0,7
SPIWrite 0193,21,0,7

\\Read  macro_opcode_operand=0x21000000;    Address(0x190[31:0],)

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```
SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );    Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;    Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)

\\Read  MACRO_ERROR_IN_OPCODE=0x0;    Address(0x20[4:4],)

\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;    Address(0x20[5:5],)

\\Read  MACRO_ERROR_IN_OPERAND=0x0;    Address(0x20[6:6],)

\\Read  MACRO_ERROR_IN_EXECUTION=0x0;    Address(0x20[7:7],)

SPIWrite 0013,00,5,5    //PAGE: cm4_macro=0x0;    Address(0x13[5:5],)
SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );    Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0193,25,0,7

\\Read  macro_opcode_operand=0x25000000;    Address(0x190[31:0],)

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );    Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;    Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)

\\Read  MACRO_ERROR_IN_OPCODE=0x0;    Address(0x20[4:4],)

\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;    Address(0x20[5:5],)

\\Read  MACRO_ERROR_IN_OPERAND=0x0;    Address(0x20[6:6],)

\\Read  MACRO_ERROR_IN_EXECUTION=0x0;    Address(0x20[7:7],)

SPIWrite 0013,00,5,5    //PAGE: cm4_macro=0x0;    Address(0x13[5:5],)
SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );    Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,04,0,7
SPIWrite 00a2,03,0,7
SPIWrite 00a1,04,0,7
SPIWrite 00a0,03,0,7
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SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,03,0,7
SPIWrite 00a4,03,0,7
SPIWrite 0193,26,0,7

\\Read macro_opcode_operand=0x26000000; Address(0x190[31:0],)

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4 //PAGE: customer_macro=0x0; (Meaning:); Address(0x13[4:4],)
SPIWrite 0013,20,5,5 //PAGE: cm4_macro=0x1; Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read MACRO_ERROR=0x0; Address(0x20[3:3],)

\\Read MACRO_ERROR=0x0; Address(0x20[3:3],)

\\Read MACRO_ERROR_IN_OPCODE=0x0; Address(0x20[4:4],)

\\Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0x20[5:5],)

\\Read MACRO_ERROR_IN_OPERAND=0x0; Address(0x20[6:6],)

\\Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0x20[7:7],)

SPIWrite 0013,00,5,5 //PAGE: cm4_macro=0x0; Address(0x13[5:5],)
SPIWrite 0013,10,4,4 //PAGE: customer_macro=0x1; (Meaning:); Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,1f,0,7
SPIWrite 00a2,03,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,03,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,06,0,7
SPIWrite 00a4,06,0,7
SPIWrite 00ab,00,0,7
SPIWrite 00aa,00,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00a8,03,0,7
SPIWrite 0193,2a,0,7

\\Read macro_opcode_operand=0x2a000000; Address(0x190[31:0],)

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4 //PAGE: customer_macro=0x0; (Meaning:); Address(0x13[4:4],)
SPIWrite 0013,20,5,5 //PAGE: cm4_macro=0x1; Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read MACRO_ERROR=0x0; Address(0x20[3:3],)

\\Read MACRO_ERROR=0x0; Address(0x20[3:3],)

\\Read MACRO_ERROR_IN_OPCODE=0x0; Address(0x20[4:4],)

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\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0x20[5:5],)

\\Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0x20[6:6],)

\\Read  MACRO_ERROR_IN_EXECUTION=0x0;      Address(0x20[7:7],)

SPIWrite 0013,00,5,5      //PAGE: cm4_macro=0x0; Address(0x13[5:5],)
SPIWrite 0013,10,4,4      //PAGE: customer_macro=0x1; (Meaning: );      Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,ff,0,7
SPIWrite 00a2,fa,0,7
SPIWrite 00a1,60,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,ff,0,7
SPIWrite 00a6,fa,0,7
SPIWrite 00a5,60,0,7
SPIWrite 00a4,00,0,7
SPIWrite 00ab,00,0,7
SPIWrite 00aa,04,0,7
SPIWrite 00a9,c9,0,7
SPIWrite 00a8,28,0,7
SPIWrite 00af,00,0,7
SPIWrite 00ae,04,0,7
SPIWrite 00ad,c9,0,7
SPIWrite 00ac,28,0,7
SPIWrite 00b3,ff,0,7
SPIWrite 00b2,fa,0,7
SPIWrite 00b1,60,0,7
SPIWrite 00b0,00,0,7
SPIWrite 00b7,ff,0,7
SPIWrite 00b6,fa,0,7
SPIWrite 00b5,60,0,7
SPIWrite 00b4,00,0,7
SPIWrite 0193,29,0,7

\\Read  macro_opcode_operand=0x29000000;      Address(0x190[31:0],)

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4      //PAGE: customer_macro=0x0; (Meaning: );      Address(0x13[4:4],)
SPIWrite 0013,20,5,5      //PAGE: cm4_macro=0x1; Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;      Address(0x20[3:3],)

\\Read  MACRO_ERROR=0x0;      Address(0x20[3:3],)

\\Read  MACRO_ERROR_IN_OPCODE=0x0;      Address(0x20[4:4],)

\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0x20[5:5],)

\\Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0x20[6:6],)

\\Read  MACRO_ERROR_IN_EXECUTION=0x0;      Address(0x20[7:7],)

SPIWrite 0013,00,5,5      //PAGE: cm4_macro=0x0; Address(0x13[5:5],)
SPIWrite 0013,10,4,4      //PAGE: customer_macro=0x1; (Meaning: );      Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

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SPIWrite 00a3,00,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 00ab,00,0,7
SPIWrite 00aa,00,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00a8,00,0,7
SPIWrite 00af,00,0,7
SPIWrite 00ae,00,0,7
SPIWrite 00ad,00,0,7
SPIWrite 00ac,00,0,7
SPIWrite 00b3,00,0,7
SPIWrite 00b2,0b,0,7
SPIWrite 00b1,df,0,7
SPIWrite 00b0,10,0,7
SPIWrite 00b7,00,0,7
SPIWrite 00b6,0b,0,7
SPIWrite 00b5,df,0,7
SPIWrite 00b4,10,0,7
SPIWrite 00bb,00,0,7
SPIWrite 00ba,0b,0,7
SPIWrite 00b9,df,0,7
SPIWrite 00b8,10,0,7
SPIWrite 00bf,00,0,7
SPIWrite 00be,20,0,7
SPIWrite 00bd,a6,0,7
SPIWrite 00bc,c0,0,7
SPIWrite 0193,24,0,7
```

```
\\Read macro_opcode_operand=0x24000000; Address(0x190[31:0],)
```

```
SPIPoll 00f0,0,7,7
```

```
SPIWrite 0013,00,4,4 //PAGE: customer_macro=0x0;(Meaning: ); Address(0x13[4:4],)
SPIWrite 0013,20,5,5 //PAGE: cm4_macro=0x1; Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00
```

```
\\Read MACRO_ERROR=0x0; Address(0x20[3:3],)
```

```
\\Read MACRO_ERROR=0x0; Address(0x20[3:3],)
```

```
\\Read MACRO_ERROR_IN_OPCODE=0x0; Address(0x20[4:4],)
```

```
\\Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0x20[5:5],)
```

```
\\Read MACRO_ERROR_IN_OPERAND=0x0; Address(0x20[6:6],)
```

```
\\Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0x20[7:7],)
```

```
\\END: Done configuring TOP parameters for MCU
```

```
SPIWrite 0013,00,0,7 //PAGE: cm4_macro=0x0; Address(0x13[5:5],)
\\ STEP: efusebyMCU/step0
```

```
\\START: Loading PLL EFuse trims
```

SPIWrite 0013,10,0,7 //PAGE: customer_macro=0x1; (Meaning:); Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7

SPIWrite 00a2,1f,0,7

SPIWrite 00a1,7c,0,7

SPIWrite 00a0,00,0,7

SPIWrite 00a7,09,0,7

SPIWrite 00a6,08,0,7

SPIWrite 00a5,02,0,7

SPIWrite 00a4,00,0,7

SPIWrite 0193,12,0,7

SPIPoll 00f0,0,7,7

\\END: Done Loading PLL EFuse trims

SPIWrite 0013,00,0,7 //PAGE: customer_macro=0x0; (Meaning:); Address(0x13[4:4],)

SPIWrite 0014,04,0,7 //PAGE: TIMING_CON=0x1; (Meaning:); Address(0x14[2:2],)

SPIWrite 0717,00,0,7 //spare_reg_port=0x101; Address(0x714[31:0],)

SPIWrite 0716,00,0,7

SPIWrite 0715,01,0,7

SPIWrite 0714,01,0,7

SPIWrite 0014,00,0,7 //PAGE: TIMING_CON=0x0; (Meaning:); Address(0x14[2:2],)

\\ STEP: pll0Config/step0

\\START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,80,0,7 //PAGE: DIGTOP_MISC=0x1; (Meaning:); Address(0x15[7:7],)

SPIWrite 01d4,01,0,7 //pll_reg_spi_req_a=0x1; Address(0x1d4[0:0],)

SPIWrite 0374,00,0,7 //pll_reg_spi_req_b1=0x0; (Meaning:); Address(0x374[0:0],)

SPIPoll 01d5,0,0,1

\\Read pll_reg_spi_a_ack=0x1; Address(0x1d4[8:8],)

\\END: Done requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7 //PAGE: DIGTOP_MISC=0x0; (Meaning:); Address(0x15[7:7],)

\\ STEP: pll0Config/step1

\\START: Configure PLL

SPIWrite 0014,08,0,7 //PAGE: pll=0x1; Address(0x14[7:3],)

SPIWrite 004b,33,0,7 //PLL_SPARE0=0xcc000; Address(0x48[31:10],)

SPIWrite 004a,00,0,7

SPIWrite 0049,00,0,7

SPIWrite 005e,97,0,7 //EN_VCO=0x1; Address(0x5c[23:23],)

SPIWrite 0028,0c,0,7 //N=0xc; Address(0x28[7:0],)

SPIWrite 0036,0c,0,7 //N_to_CAL=0xc; Address(0x34[23:16],)

SPIWrite 0035,08,0,7 //CAL_CONTROL=0x8; Address(0x34[12:8],)

SPIWrite 0051,06,0,7 //CTL_REF_DIV=0x1; (Meaning:); Address(0x50[8:6],)

SPIWrite 0050,40,0,7

SPIWrite 0051,06,0,7 //EN_DIV8_CLK_TO_PLLDIG=0x1; Address(0x50[9:9],)

SPIWrite 0051,06,0,7 //EN_CLK_TO_PLLDIG=0x1; Address(0x50[10:10],)

SPIWrite 0051,0e,0,7 //EN_SYNC_TO_PLLDIG_DIV=0x1; Address(0x50[11:11],)

SPIWrite 003c,41,0,7 //CTL_DIV_23_45=0x1; Address(0x3c[0:0],)

SPIWrite 005e,97,0,7 //EN_FRAC_N_MODE=0x1; Address(0x5c[16:16],)

SPIWrite 0033,03,0,7 //EN_FRAC_MODE=0x1; Address(0x30[24:24],)

SPIWrite 003f,0c,0,7 //CTL_TEST_MUX=0x0; Address(0x3c[31:30],)

SPIWrite 0049,01,0,7 //EN_VCO_PKDET=0x1; Address(0x48[8:8],)

SPIWrite 0048,2f,0,7 //VCO_PKDET_BIAS=0x7; Address(0x48[2:0],)

SPIWrite 0044,27,0,7 //CTL_VCO_IB_GM=0x7; Address(0x44[2:0],)

SPIWrite 0043,4c,0,7 //CTL_VCO_IB_TAIL=0xc; Address(0x40[27:24],)

SPIWrite 0043,0c,0,7 //CTL_VCO_IB_GM_SLOPE=0x0; Address(0x40[30:28],)

```

SPIWrite 0042,04,0,7 //CTL_VCO_IB_TAIL_SLOPE=0x0; Address(0x40[22:19],)
SPIWrite 0046,00,0,7 //CTL_VCO_IB_GM1=0x0; Address(0x44[22:21],)
SPIWrite 0040,28,0,7 //CTL_VB_VAR_SLOPE=0x0; Address(0x40[2:0],)
SPIWrite 002e,02,0,7 //F=0x27c40; Address(0x2c[19:0],)
SPIWrite 002d,7c,0,7
SPIWrite 002c,40,0,7
SPIWrite 0032,03,0,7 //D=0x3c000; Address(0x30[19:0],)
SPIWrite 0031,c0,0,7
SPIWrite 0030,00,0,7
SPIWrite 0033,03,0,7 //F_order=0x1; Address(0x30[27:25],)
SPIWrite 0039,40,0,7 //EN_LOCK_DETECT=0x1; Address(0x38[14:14],)
SPIWrite 003f,14,0,7 //CTL_PFD_DEL=0x2; Address(0x3c[29:27],)
SPIWrite 003f,14,0,7 //CTL_OUT_DIV=0x4; Address(0x3c[26:24],)
SPIWrite 003c,41,0,7 //CTL_LDO_ANA=0x4; Address(0x3c[6:4],)
SPIWrite 003d,24,0,7 //CTL_LDO_RF=0x4; Address(0x3c[10:8],)
SPIWrite 0052,10,0,7 //CTL_FBDIV_LDO_PROG=0x8; Address(0x50[20:17],)
SPIWrite 003a,08,0,7 //CTL_CP_IREF=0x2; Address(0x38[20:18],)
SPIWrite 003b,30,0,7 //CTL_CP_IOUT=0x3; Address(0x38[29:28],)
SPIWrite 0034,03,0,7 //lock_acc=0x3; Address(0x34[1:0],)
SPIWrite 0034,0f,0,7 //lock_cnt=0x3; Address(0x34[3:2],)
SPIWrite 0034,1f,0,7 //lock_err=0x1; Address(0x34[5:4],)
SPIWrite 0066,04,0,7 //lock_rst=0x1; Address(0x64[18:18],)
SPIWrite 0066,00,0,7 //lock_rst=0x0; Address(0x64[18:18],)
SPIWrite 0066,08,0,7 //lock_lost_rst=0x1; Address(0x64[19:19],)
SPIWrite 0066,00,0,7 //lock_lost_rst=0x0; Address(0x64[19:19],)
SPIWrite 0034,1f,0,7 //EN_CAL=0x0; Address(0x34[6:6],)
SPIWrite 0034,5f,0,7 //EN_CAL=0x1; Address(0x34[6:6],)
SPIWrite 003c,45,0,7 //CTL_I_OFFSET=0x1; Address(0x3c[3:2],)

```

WAIT 0.01

```

SPIWrite 005e,9f,0,7 //EN_I_OFFSET=0x1; Address(0x5c[19:19],)
SPIWrite 003c,45,0,7 //CTL_I_OFST_UP_DN=0x0; Address(0x3c[1:1],)
SPIWrite 0065,10,0,7 //CTL_I_OFST_REF=0x1; Address(0x64[14:12],)

```

SPIPoll 0062,7,7,1

SPIReadCheck 0062,7,7,80

\\Read lock=0x1; Address(0x60[23:23],)

\\END: Done configuring PLL

```

SPIWrite 0014,00,0,7 //PAGE: pll=0x0; Address(0x14[7:3],)
\\ STEP: pll1Config/step0

```

\\START: Configure PLL

```

SPIWrite 0014,10,0,7 //PAGE: pll=0x2; Address(0x14[7:3],)
SPIWrite 005e,97,0,7 //EN_VCO=0x1; Address(0x5c[23:23],)
SPIWrite 0028,12,0,7 //N=0x12; Address(0x28[7:0],)
SPIWrite 0036,12,0,7 //N_to_CAL=0x12; Address(0x34[23:16],)
SPIWrite 0035,08,0,7 //CAL_CONTROL=0x8; Address(0x34[12:8],)
SPIWrite 0051,06,0,7 //CTL_REF_DIV=0x1; (Meaning: ); Address(0x50[8:6],)
SPIWrite 0050,40,0,7
SPIWrite 0051,06,0,7 //EN_DIV8_CLK_TO_PLLDIG=0x1; Address(0x50[9:9],)
SPIWrite 0051,06,0,7 //EN_CLK_TO_PLLDIG=0x1; Address(0x50[10:10],)
SPIWrite 0051,0e,0,7 //EN_SYNC_TO_PLLDIG_DIV=0x1; Address(0x50[11:11],)
SPIWrite 003c,40,0,7 //CTL_DIV_23_45=0x0; Address(0x3c[0:0],)
SPIWrite 005e,96,0,7 //EN_FRAC_N_MODE=0x0; Address(0x5c[16:16],)
SPIWrite 0033,02,0,7 //EN_FRAC_MODE=0x0; Address(0x30[24:24],)
SPIWrite 003f,0c,0,7 //CTL_TEST_MUX=0x0; Address(0x3c[31:30],)
SPIWrite 0049,01,0,7 //EN_VCO_PKDET=0x1; Address(0x48[8:8],)
SPIWrite 0048,2f,0,7 //VCO_PKDT_BIAS=0x7; Address(0x48[2:0],)
SPIWrite 0044,27,0,7 //CTL_VCO_IB_GM=0x7; Address(0x44[2:0],)
SPIWrite 0043,4c,0,7 //CTL_VCO_IB_TAIL=0xc; Address(0x40[27:24],)
SPIWrite 0043,0c,0,7 //CTL_VCO_IB_GM_SLOPE=0x0; Address(0x40[30:28],)
SPIWrite 0042,04,0,7 //CTL_VCO_IB_TAIL_SLOPE=0x0; Address(0x40[22:19],)

```

```

SPIWrite 0046,00,0,7 //CTL_VCO_IB_GM1=0x0; Address(0x44[22:21],)
SPIWrite 0040,28,0,7 //CTL_VB_VAR_SLOPE=0x0; Address(0x40[2:0],)
SPIWrite 002e,00,0,7 //F=0x0; Address(0x2c[19:0],)
SPIWrite 002d,00,0,7
SPIWrite 002c,00,0,7
SPIWrite 0032,02,0,7 //D=0x20000; Address(0x30[19:0],)
SPIWrite 0031,00,0,7
SPIWrite 0030,00,0,7
SPIWrite 0033,02,0,7 //F_order=0x1; Address(0x30[27:25],)
SPIWrite 0039,40,0,7 //EN_LOCK_DETECT=0x1; Address(0x38[14:14],)
SPIWrite 003f,14,0,7 //CTL_PFD_DEL=0x2; Address(0x3c[29:27],)
SPIWrite 003f,13,0,7 //CTL_OUT_DIV=0x3; Address(0x3c[26:24],)
SPIWrite 003c,40,0,7 //CTL_LDO_ANA=0x4; Address(0x3c[6:4],)
SPIWrite 003d,24,0,7 //CTL_LDO_RF=0x4; Address(0x3c[10:8],)
SPIWrite 0052,10,0,7 //CTL_FBDIV_LDO_PROG=0x8; Address(0x50[20:17],)
SPIWrite 003a,08,0,7 //CTL_CP_IREF=0x2; Address(0x38[20:18],)
SPIWrite 003b,30,0,7 //CTL_CP_IOUT=0x3; Address(0x38[29:28],)
SPIWrite 0034,03,0,7 //lock_acc=0x3; Address(0x34[1:0],)
SPIWrite 0034,0f,0,7 //lock_cnt=0x3; Address(0x34[3:2],)
SPIWrite 0034,1f,0,7 //lock_err=0x1; Address(0x34[5:4],)
SPIWrite 0066,04,0,7 //lock_rst=0x1; Address(0x64[18:18],)
SPIWrite 0066,00,0,7 //lock_rst=0x0; Address(0x64[18:18],)
SPIWrite 0066,08,0,7 //lock_lost_rst=0x1; Address(0x64[19:19],)
SPIWrite 0066,00,0,7 //lock_lost_rst=0x0; Address(0x64[19:19],)
SPIWrite 0034,1f,0,7 //EN_CAL=0x0; Address(0x34[6:6],)
SPIWrite 0034,5f,0,7 //EN_CAL=0x1; Address(0x34[6:6],)

WAIT 0.01

SPIWrite 005e,96,0,7 //EN_I_OFFSET=0x0; Address(0x5c[19:19],)

SPIPoll 0062,7,7,1

SPIReadCheck 0062,7,7,80

\\Read lock=0x1; Address(0x60[23:23],)

SPIWrite 0051,0c,0,7 //EN_DIV8_CLK_TO_PLLDIG=0x0; Address(0x50[9:9],)

\\END: Done configuring PLL

SPIWrite 0014,00,0,7 //PAGE: pll=0x0; Address(0x14[7:3],)
\\ STEP: pll2PowerDown/step0

\\START: Powers up/down the PLL

SPIWrite 0014,20,0,7 //PAGE: pll=0x4; Address(0x14[7:3],)
SPIWrite 005e,17,0,7 //EN_VCO=0x0; Address(0x5c[23:23],)
SPIWrite 0014,00,0,7 //PAGE: pll=0x0; Address(0x14[7:3],)
\\ STEP: pll3PowerDown/step0

\\START: Powers up/down the PLL

SPIWrite 0014,40,0,7 //PAGE: pll=0x8; Address(0x14[7:3],)
SPIWrite 005e,17,0,7 //EN_VCO=0x0; Address(0x5c[23:23],)
SPIWrite 0014,00,0,7 //PAGE: pll=0x0; Address(0x14[7:3],)
\\ STEP: pll4PowerDown/step0

\\START: Powers up/down the PLL

SPIWrite 0014,80,0,7 //PAGE: pll=0x10; Address(0x14[7:3],)
SPIWrite 005e,17,0,7 //EN_VCO=0x0; Address(0x5c[23:23],)
SPIWrite 0014,00,0,7 //PAGE: pll=0x0; Address(0x14[7:3],)
\\ STEP: pll4PowerDown/step1

\\START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,80,0,7 //PAGE: DIGTOP_MISC=0x1; (Meaning: ); Address(0x15[7:7],)
SPIWrite 01d4,00,0,7 //pll_reg_spi_req_a=0x0; Address(0x1d4[0:0],)

```

SPIWrite 0374,00,0,7 //pll_reg_spi_req_b1=0x0; (Meaning:); Address(0x374[0:0],)

WAIT 0.01

\\END: Done requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7 //PAGE: DIGTOP_MISC=0x0; (Meaning:); Address(0x15[7:7],)

\\ STEP: efuseToAnalog/step0

SPIWrite 0013,20,0,7 //PAGE: cm4_macro=0x1; Address(0x13[5:5],)

SPIWrite 0084,21,0,7

SPIWrite 0084,61,0,7

SPIWrite 0084,21,0,7

SPIWrite 0084,21,0,7

SPIWrite 0084,01,0,7

SPIWrite 0088,01,0,7

SPIWrite 0013,00,0,7 //PAGE: cm4_macro=0x0; Address(0x13[5:5],)

\\ STEP: efuseToAnalog/step1

\\START: Loading EFuse Packets

SPIWrite 0013,10,0,7 //PAGE: customer_macro=0x1; (Meaning:); Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7

SPIWrite 00a2,00,0,7

SPIWrite 00a1,00,0,7

SPIWrite 00a0,00,0,7

SPIWrite 00a7,04,0,7

SPIWrite 00a6,00,0,7

SPIWrite 00a5,07,0,7

SPIWrite 00a4,00,0,7

SPIWrite 00ab,11,0,7

SPIWrite 00aa,0b,0,7

SPIWrite 00a9,0a,0,7

SPIWrite 00a8,07,0,7

SPIWrite 00af,00,0,7

SPIWrite 00ae,00,0,7

SPIWrite 00ad,00,0,7

SPIWrite 00ac,14,0,7

SPIWrite 0193,12,0,7

SPIPoll 00f0,0,7,7

\\END: Done Loading Efuse packets

SPIWrite 0013,00,0,7 //PAGE: customer_macro=0x0; (Meaning:); Address(0x13[4:4],)

\\ STEP: topConfig/step0

\\START: Doing Top & DSA initialization

SPIWrite 0015,80,0,7 //PAGE: DIGTOP_MISC=0x1; (Meaning:); Address(0x15[7:7],)

SPIWrite 0649,80,0,7 //dsa_abcd_addr_range=0x1; Address(0x648[15:15],)

\\Disabling FB CD

SPIWrite 0015,00,0,7 //PAGE: DIGTOP_MISC=0x0; (Meaning:); Address(0x15[7:7],)

SPIWrite 0018,01,0,7 //PAGE: ana_4t4r=0x1; (Meaning:); Address(0x18[0:0],)

SPIWrite 002c,02,0,7

SPIWrite 0018,00,0,7 //PAGE: ana_4t4r=0x0; (Meaning:); Address(0x18[0:0],)

SPIWrite 0014,01,0,7 //PAGE: clktop_2t=0x1; Address(0x14[1:0],)

SPIWrite 006c,08,0,7 //MASK_PDN_SYNC_TXCML_L=0x1; Address(0x6c[3:3],)

SPIWrite 006c,18,0,7 //MASK_PDN_SYNC_TXCML_R=0x1; Address(0x6c[4:4],)

SPIWrite 006c,1c,0,7 //MASK_PDN_FAST_TXCML_R=0x1; Address(0x6c[2:2],)

SPIWrite 006c,1e,0,7 //MASK_PDN_FAST_TXCML_L=0x1; Address(0x6c[1:1],)

SPIWrite 0014,00,0,7 //PAGE: clktop_2t=0x0; Address(0x14[1:0],)

SPIWrite 0018,01,0,7 //PAGE: ana_4t4r=0x1; (Meaning:); Address(0x18[0:0],)

```
SPIWrite 0050,00,0,7
SPIWrite 0054,00,0,7
SPIWrite 0050,00,0,7
SPIWrite 0054,00,0,7
SPIWrite 0018,00,0,7 //PAGE: ana_4t4r=0x0;(Meaning: ); Address(0x18[0:0],)
SPIWrite 0014,04,0,7 //PAGE: TIMING_CON=0x1;(Meaning: ); Address(0x14[2:2],)
SPIWrite 0105,02,0,7 //map_invalid_settings=0x2; Address(0x104[9:8],)
SPIWrite 0014,00,0,7 //PAGE: TIMING_CON=0x0;(Meaning: ); Address(0x14[2:2],)
SPIWrite 0015,80,0,7 //PAGE: DIGTOP_MISC=0x1;(Meaning: ); Address(0x15[7:7],)
SPIWrite 039c,00,0,7 //sync_lvds_mode_ab=0x0;(Meaning: ); Address(0x39c[0:0],)
SPIWrite 039c,00,0,7 //sync_lvds_mode_cd=0x0;(Meaning: ); Address(0x39c[1:1],)
SPIWrite 0330,00,0,7 //pull_ctrl_gpio_76=0x0; Address(0x330[2:0],)
SPIWrite 02e4,00,0,7 //pull_ctrl_gpio_57=0x0; Address(0x2e4[2:0],)
SPIWrite 02f4,00,0,7 //pull_ctrl_gpio_61=0x0; Address(0x2f4[2:0],)
SPIWrite 02c0,00,0,7 //pull_ctrl_gpio_48=0x0; Address(0x2c0[2:0],)
SPIWrite 0015,00,0,7 //PAGE: DIGTOP_MISC=0x0;(Meaning: ); Address(0x15[7:7],)
SPIWrite 0016,30,0,7 //PAGE: dsa=0x3; Address(0x16[5:4],)
SPIWrite 0180,01,0,7
SPIWrite 02fb,00,0,7
SPIWrite 065b,00,0,7
SPIWrite 02fd,00,0,7
SPIWrite 065d,00,0,7
SPIWrite 02fe,00,0,7
SPIWrite 0305,00,0,7
SPIWrite 030e,00,0,7
SPIWrite 065e,00,0,7
SPIWrite 0665,00,0,7
SPIWrite 066e,00,0,7
SPIWrite 0040,03,0,7
SPIWrite 0311,00,0,7
SPIWrite 0671,00,0,7
SPIWrite 02c8,01,0,7
SPIWrite 02d0,01,0,7
SPIWrite 0630,01,0,7
SPIWrite 0051,00,0,7
SPIWrite 00b1,00,0,7
SPIWrite 0677,01,0,7
SPIWrite 0676,f0,0,7
SPIWrite 0675,03,0,7
SPIWrite 0674,e0,0,7
SPIWrite 067b,01,0,7
SPIWrite 067a,f0,0,7
SPIWrite 0679,03,0,7
SPIWrite 0678,21,0,7
SPIWrite 067f,01,0,7
SPIWrite 067e,f0,0,7
SPIWrite 067d,02,0,7
SPIWrite 067c,82,0,7
SPIWrite 0683,01,0,7
SPIWrite 0682,f0,0,7
SPIWrite 0681,02,0,7
SPIWrite 0680,23,0,7
SPIWrite 0687,01,0,7
SPIWrite 0686,f0,0,7
SPIWrite 0685,01,0,7
SPIWrite 0684,c4,0,7
SPIWrite 068b,01,0,7
SPIWrite 068a,f0,0,7
SPIWrite 0689,01,0,7
SPIWrite 0688,85,0,7
SPIWrite 068f,01,0,7
SPIWrite 068e,f0,0,7
SPIWrite 068d,01,0,7
SPIWrite 068c,46,0,7
SPIWrite 0693,01,0,7
SPIWrite 0692,f0,0,7
SPIWrite 0691,01,0,7
SPIWrite 0690,27,0,7
SPIWrite 0697,01,0,7
```

SPIWrite 0696,e0,0,7
SPIWrite 0695,01,0,7
SPIWrite 0694,08,0,7
SPIWrite 069b,01,0,7
SPIWrite 069a,e0,0,7
SPIWrite 0699,00,0,7
SPIWrite 0698,e9,0,7
SPIWrite 069f,01,0,7
SPIWrite 069e,f0,0,7
SPIWrite 069d,00,0,7
SPIWrite 069c,ca,0,7
SPIWrite 06a3,01,0,7
SPIWrite 06a2,f0,0,7
SPIWrite 06a1,00,0,7
SPIWrite 06a0,ab,0,7
SPIWrite 06a7,01,0,7
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SPIWrite 0cde,00,0,7
SPIWrite 0cdd,00,0,7
SPIWrite 0cdc,00,0,7
SPIWrite 0ce7,00,0,7
SPIWrite 0ce6,00,0,7
SPIWrite 0ce5,00,0,7
SPIWrite 0ce4,00,0,7
SPIWrite 0cef,00,0,7
SPIWrite 0cee,00,0,7
SPIWrite 0ced,00,0,7
SPIWrite 0cec,00,0,7
SPIWrite 0cf7,00,0,7
SPIWrite 0cf6,00,0,7
SPIWrite 0cf5,00,0,7
SPIWrite 0cf4,00,0,7
SPIWrite 0cff,00,0,7
SPIWrite 0cfe,00,0,7
SPIWrite 0cfd,00,0,7
SPIWrite 0cfc,00,0,7
SPIWrite 0d07,00,0,7
SPIWrite 0d06,00,0,7
SPIWrite 0d05,00,0,7
SPIWrite 0d04,00,0,7
SPIWrite 09a2,00,0,7
SPIWrite 09a2,01,0,7
SPIWrite 09a2,00,0,7
SPIWrite 0bc2,00,0,7
SPIWrite 0bc2,01,0,7
SPIWrite 0bc2,00,0,7
SPIWrite 0101,18,0,7
SPIWrite 0121,18,0,7
SPIWrite 0103,01,0,7
SPIWrite 0123,01,0,7
SPIWrite 0100,01,0,7
SPIWrite 0102,00,0,7
SPIWrite 0102,01,0,7
SPIWrite 0102,00,0,7
SPIWrite 0100,00,0,7
SPIWrite 0102,00,0,7
SPIWrite 0102,01,0,7
SPIWrite 0102,00,0,7
SPIWrite 0120,01,0,7
SPIWrite 0122,00,0,7
SPIWrite 0122,01,0,7
SPIWrite 0122,00,0,7
SPIWrite 0120,00,0,7
SPIWrite 0122,00,0,7
SPIWrite 0122,01,0,7
SPIWrite 0122,00,0,7
SPIWrite 0103,00,0,7

SPIWrite 0123,00,0,7
SPIWrite 0155,0f,0,7
SPIWrite 0994,01,0,7
SPIWrite 0bb4,01,0,7
SPIWrite 0df2,00,0,7
SPIWrite 0df1,00,0,7
SPIWrite 0df0,00,0,7
SPIWrite 0df6,00,0,7
SPIWrite 0df5,84,0,7
SPIWrite 0df4,88,0,7
SPIWrite 0dfa,01,0,7
SPIWrite 0df9,10,0,7
SPIWrite 0df8,a0,0,7
SPIWrite 0dfe,02,0,7
SPIWrite 0dfd,98,0,7
SPIWrite 0dfc,b9,0,7
SPIWrite 0e02,04,0,7
SPIWrite 0e01,20,0,7
SPIWrite 0e00,df,0,7
SPIWrite 0e06,06,0,7
SPIWrite 0e05,25,0,7
SPIWrite 0e04,12,0,7
SPIWrite 0e0a,08,0,7
SPIWrite 0e09,a9,0,7
SPIWrite 0e08,41,0,7
SPIWrite 0e0e,0b,0,7
SPIWrite 0e0d,31,0,7
SPIWrite 0e0c,5e,0,7
SPIWrite 0e12,0f,0,7
SPIWrite 0e11,31,0,7
SPIWrite 0e10,92,0,7
SPIWrite 0e16,15,0,7
SPIWrite 0e15,b5,0,7
SPIWrite 0e14,98,0,7
SPIWrite 0e1a,20,0,7
SPIWrite 0e19,ba,0,7
SPIWrite 0e18,de,0,7
SPIWrite 0e1e,25,0,7
SPIWrite 0e1d,42,0,7
SPIWrite 0e1c,c0,0,7
SPIWrite 0e22,25,0,7
SPIWrite 0e21,4a,0,7
SPIWrite 0e20,d8,0,7
SPIWrite 0e26,25,0,7
SPIWrite 0e25,4b,0,7
SPIWrite 0e24,00,0,7
SPIWrite 0e2a,25,0,7
SPIWrite 0e29,53,0,7
SPIWrite 0e28,15,0,7
SPIWrite 0e2e,25,0,7
SPIWrite 0e2d,57,0,7
SPIWrite 0e2c,2b,0,7
SPIWrite 0e32,25,0,7
SPIWrite 0e31,5b,0,7
SPIWrite 0e30,40,0,7
SPIWrite 0e36,25,0,7
SPIWrite 0e35,5f,0,7
SPIWrite 0e34,53,0,7
SPIWrite 0e3a,25,0,7
SPIWrite 0e39,63,0,7
SPIWrite 0e38,64,0,7
SPIWrite 0e3e,25,0,7
SPIWrite 0e3d,67,0,7
SPIWrite 0e3c,74,0,7
SPIWrite 0e42,25,0,7
SPIWrite 0e41,6b,0,7
SPIWrite 0e40,81,0,7
SPIWrite 0e46,25,0,7
SPIWrite 0e45,6b,0,7

```
SPIWrite 0e44,81,0,7
SPIWrite 0e4a,25,0,7
SPIWrite 0e49,6b,0,7
SPIWrite 0e48,81,0,7
SPIWrite 0e4e,25,0,7
SPIWrite 0e4d,6b,0,7
SPIWrite 0e4c,81,0,7
SPIWrite 0e52,25,0,7
SPIWrite 0e51,6b,0,7
SPIWrite 0e50,81,0,7
SPIWrite 0e56,25,0,7
SPIWrite 0e55,6b,0,7
SPIWrite 0e54,81,0,7
SPIWrite 0e5a,25,0,7
SPIWrite 0e59,6b,0,7
SPIWrite 0e58,81,0,7
SPIWrite 0e5e,25,0,7
SPIWrite 0e5d,6b,0,7
SPIWrite 0e5c,81,0,7
SPIWrite 0e62,25,0,7
SPIWrite 0e61,6b,0,7
SPIWrite 0e60,81,0,7
SPIWrite 0e66,25,0,7
SPIWrite 0e65,6b,0,7
SPIWrite 0e64,81,0,7
SPIWrite 0e6a,25,0,7
SPIWrite 0e69,6b,0,7
SPIWrite 0e68,81,0,7
SPIWrite 0e6e,25,0,7
SPIWrite 0e6d,6b,0,7
SPIWrite 0e6c,81,0,7
SPIWrite 0dd1,01,0,7
```

\\END: Done Top & DSA initialization

```
SPIWrite 0016,00,0,7    //PAGE: dsa=0x0;    Address(0x16[5:4],)
\\ STEP: clkMuxConfig/step0
```

\\START: Configuring PLL Mux

```
SPIWrite 0014,01,0,7    //PAGE: clktop_2t=0x1;  Address(0x14[1:0],)
SPIWrite 0064,00,0,7    //CTL_SEL_CLK_MUX_CROSS_PLL_TOP_1P8_L=0x0; (Meaning: );
Address(0x64[0:0],)
SPIWrite 0064,00,0,7    //CTL_SEL_CLK_MUX_CROSS_PLL_TOP_1P8_R=0x0; (Meaning: );
Address(0x64[1:1],)
SPIWrite 0062,01,0,7    //CTL_SEL_CLK_MUX_CROSS_PLL_BOT_L=0x1; (Meaning: );  Address(0x60[16:16],)
SPIWrite 0062,03,0,7    //CTL_SEL_CLK_MUX_CROSS_PLL_BOT_R=0x1; (Meaning: );  Address(0x60[17:17],)
SPIWrite 0071,00,0,7    //SEL_CLK_MUX_RX_1P8_L=0x0; (Meaning: );    Address(0x70[8:8],)
SPIWrite 0071,00,0,7    //SEL_CLK_MUX_RX_1P8_R=0x0; (Meaning: );    Address(0x70[9:9],)
SPIWrite 0071,00,0,7    //SEL_CLK_MUX_TX_1P8_L=0x0; (Meaning: );    Address(0x70[10:10],)
SPIWrite 0071,00,0,7    //SEL_CLK_MUX_TX_1P8_R=0x0; (Meaning: );    Address(0x70[11:11],)
SPIWrite 0060,01,0,7    //CTL_EN_CROSS_PLL_BLOCK_1P8=0x1; (Meaning: );  Address(0x60[0:0],)
SPIWrite 0060,01,0,7    //CTL_SEL_CROSS_PLL_DIR_1P8=0x0; (Meaning: );  Address(0x60[1:1],)
SPIWrite 0014,00,0,7    //PAGE: clktop_2t=0x0;  Address(0x14[1:0],)
SPIWrite 0011,10,0,7    //PAGE: rx_ec_q=0x1;    Address(0x11[7:4],)
SPIWrite 0f0d,00,0,7
SPIWrite 0011,20,0,7    //PAGE: rx_ec_q=0x2;    Address(0x11[7:4],)
SPIWrite 0f0d,00,0,7
SPIWrite 0011,40,0,7    //PAGE: rx_ec_q=0x4;    Address(0x11[7:4],)
SPIWrite 0f0d,00,0,7
SPIWrite 0011,80,0,7    //PAGE: rx_ec_q=0x8;    Address(0x11[7:4],)
SPIWrite 0f0d,00,0,7
```

\\END: Done configuring PLL Mux

```
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
\\ STEP: serdesConfig/step0
```

\\START: Enabling access to SERDES

```

SPIWrite 0015,08,0,7 //PAGE: jesd_subchip=0x1; (Meaning: ); Address(0x15[3:3],)
SPIWrite 0020,07,0,7
SPIWrite 0020,07,0,7
SPIWrite 0021,12,0,7
SPIWrite 0022,12,0,7
SPIWrite 0021,12,0,7
SPIWrite 0022,12,0,7
SPIWrite 0021,12,0,7
SPIWrite 0022,12,0,7
SPIWrite 0015,00,0,7 //PAGE: jesd_subchip=0x0; (Meaning: ); Address(0x15[3:3],)
SPIWrite 0015,04,0,7 //PAGE: SERDES=0x1; Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,04,0,7
SPIWrite 7007,00,0,7 //BUS_WIDTH_LANE3=0x0; Address(0x9803[3:3],)
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7 //BUS_WIDTH_LANE2=0x0; Address(0x9803[2:2],)
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7 //BUS_WIDTH_LANE1=0x0; Address(0x9803[1:1],)
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7 //BUS_WIDTH_LANE0=0x0; Address(0x9803[0:0],)
SPIWrite 7006,00,0,7
SPIWrite 0015,00,0,7 //PAGE: SERDES=0x2; Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,40,0,7
SPIWrite 7007,00,0,7 //BUS_WIDTH_LANE3=0x0; Address(0x9803[3:3],)
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7 //BUS_WIDTH_LANE2=0x0; Address(0x9803[2:2],)
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7 //BUS_WIDTH_LANE1=0x0; Address(0x9803[1:1],)
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7 //BUS_WIDTH_LANE0=0x0; Address(0x9803[0:0],)
SPIWrite 7006,00,0,7

```

\\END: Done enabling access to SERDES

\\Forcing the sync pins to high to ensure random data for SERDES adaptation.

```

SPIWrite 0015,40,0,7 //PAGE: SERDES=0x0; Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,00,0,7
SPIWrite 0015,80,0,7 //PAGE: DIGTOP_MISC=0x1; (Meaning: ); Address(0x15[7:7],)
SPIWrite 0520,02,0,7 //buf_dir_ctrl_gpio_72=0x2; Address(0x520[1:0],)
SPIWrite 0520,02,0,7 //preferred_input_sel_gpio_72=0x0; Address(0x520[4:2],)
SPIWrite 0520,22,0,7 //preferred_output_sel_gpio_72=0x1; Address(0x520[7:5],)
SPIWrite 0521,00,0,7 //crossbar_sel_input_gpio_72=0x0; Address(0x520[15:8],)
SPIWrite 0522,00,0,7 //crossbar_sel_output_gpio_72=0x0; Address(0x520[23:16],)
SPIWrite 0523,00,0,7 //activ_bir_dir_ctrl_gpio_72=0x0; Address(0x520[27:25],)
SPIWrite 0528,02,0,7 //buf_dir_ctrl_gpio_74=0x2; Address(0x528[1:0],)
SPIWrite 0528,02,0,7 //preferred_input_sel_gpio_74=0x0; Address(0x528[4:2],)
SPIWrite 0528,22,0,7 //preferred_output_sel_gpio_74=0x1; Address(0x528[7:5],)
SPIWrite 0529,00,0,7 //crossbar_sel_input_gpio_74=0x0; Address(0x528[15:8],)
SPIWrite 052a,00,0,7 //crossbar_sel_output_gpio_74=0x0; Address(0x528[23:16],)
SPIWrite 052b,00,0,7 //activ_bir_dir_ctrl_gpio_74=0x0; Address(0x528[27:25],)
SPIWrite 04bc,02,0,7 //buf_dir_ctrl_gpio_47=0x2; Address(0x4bc[1:0],)
SPIWrite 04bc,02,0,7 //preferred_input_sel_gpio_47=0x0; Address(0x4bc[4:2],)
SPIWrite 04bc,22,0,7 //preferred_output_sel_gpio_47=0x1; Address(0x4bc[7:5],)
SPIWrite 04bd,00,0,7 //crossbar_sel_input_gpio_47=0x0; Address(0x4bc[15:8],)
SPIWrite 04be,00,0,7 //crossbar_sel_output_gpio_47=0x0; Address(0x4bc[23:16],)
SPIWrite 04bf,00,0,7 //activ_bir_dir_ctrl_gpio_47=0x0; Address(0x4bc[27:25],)
SPIWrite 04c4,02,0,7 //buf_dir_ctrl_gpio_49=0x2; Address(0x4c4[1:0],)
SPIWrite 04c4,02,0,7 //preferred_input_sel_gpio_49=0x0; Address(0x4c4[4:2],)
SPIWrite 04c4,22,0,7 //preferred_output_sel_gpio_49=0x1; Address(0x4c4[7:5],)
SPIWrite 04c5,00,0,7 //crossbar_sel_input_gpio_49=0x0; Address(0x4c4[15:8],)
SPIWrite 04c6,00,0,7 //crossbar_sel_output_gpio_49=0x0; Address(0x4c4[23:16],)
SPIWrite 04c7,00,0,7 //activ_bir_dir_ctrl_gpio_49=0x0; Address(0x4c4[27:25],)
SPIWrite 039c,00,0,7 //sync_lvds_mode_ab=0x0; (Meaning: ); Address(0x39c[0:0],)
SPIWrite 039c,00,0,7 //sync_lvds_mode_cd=0x0; (Meaning: ); Address(0x39c[1:1],)
SPIWrite 0555,02,0,7 //ovr_sel_intpo_dac_sync_n_ab_0=0x1; Address(0x554[9:9],)
SPIWrite 0555,0a,0,7 //ovr_sel_intpo_dac_sync_n_ab_1=0x1; Address(0x554[11:11],)
SPIWrite 0555,2a,0,7 //ovr_sel_intpo_dac_sync_n_cd_0=0x1; Address(0x554[13:13],)

```

```
SPIWrite 0555,aa,0,7 //ovr_sel_intpo_dac_sync_n_cd_1=0x1; Address(0x554[15:15],)
SPIWrite 0555,ba,0,7 //ovr_intpo_dac_sync_n_cd_0=0x1; Address(0x554[12:12],)
SPIWrite 0555,bb,0,7 //ovr_intpo_dac_sync_n_ab_0=0x1; Address(0x554[8:8],)
SPIWrite 0555,bf,0,7 //ovr_intpo_dac_sync_n_ab_1=0x1; Address(0x554[10:10],)
SPIWrite 0555,ff,0,7 //ovr_intpo_dac_sync_n_cd_1=0x1; Address(0x554[14:14],)
SPIWrite 0015,00,0,7 //PAGE: DIGTOP_MISC=0x0; (Meaning: ); Address(0x15[7:7],)
\\ STEP: serdesConfig/step1
```

\\START: Resetting Serdes

```
SPIWrite 0015,04,0,7 //PAGE: SERDES=0x1; Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,04,0,7
SPIWrite 701b,08,0,7 //DOMAIN_RESET=0x888; Address(0x980d[11:0],)
SPIWrite 701a,88,0,7
SPIWrite 701b,00,0,7 //DOMAIN_RESET=0x0; Address(0x980d[11:0],)
SPIWrite 701a,00,0,7
```

WAIT 0.1

```
SPIWrite 701b,07,0,7 //DOMAIN_RESET=0x777; Address(0x980d[11:0],)
SPIWrite 701a,77,0,7
SPIWrite 701b,00,0,7 //DOMAIN_RESET=0x0; Address(0x980d[11:0],)
SPIWrite 701a,00,0,7
```

WAIT 0.1

\\END: Done resetting Serdes

\\START: Resetting Serdes

```
SPIWrite 0015,00,0,7 //PAGE: SERDES=0x2; Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,40,0,7
SPIWrite 701b,08,0,7 //DOMAIN_RESET=0x888; Address(0x980d[11:0],)
SPIWrite 701a,88,0,7
SPIWrite 701b,00,0,7 //DOMAIN_RESET=0x0; Address(0x980d[11:0],)
SPIWrite 701a,00,0,7
```

WAIT 0.1

```
SPIWrite 701b,07,0,7 //DOMAIN_RESET=0x777; Address(0x980d[11:0],)
SPIWrite 701a,77,0,7
SPIWrite 701b,00,0,7 //DOMAIN_RESET=0x0; Address(0x980d[11:0],)
SPIWrite 701a,00,0,7
```

WAIT 0.1

\\END: Done resetting Serdes

```
SPIWrite 0015,40,0,7 //PAGE: SERDES=0x0; Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,00,0,7
\\ STEP: serdesConfig/step2
```

\\START: Configuring the SERDES

```
SPIWrite 0015,08,0,7 //PAGE: jesd_subchip=0x1; (Meaning: ); Address(0x15[3:3],)
SPIWrite 0021,12,0,7
SPIWrite 0022,12,0,7
SPIWrite 0015,00,0,7 //PAGE: jesd_subchip=0x0; (Meaning: ); Address(0x15[3:3],)
SPIWrite 0015,04,0,7 //PAGE: SERDES=0x3; Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,44,0,7
SPIWrite 702f,c0,0,7
SPIWrite 702e,00,0,7
```

WAIT 0.01

```
SPIWrite 7029,ff,0,7
```

SPIWrite 7028,f0,0,7
SPIWrite 701b,0a,0,7
SPIWrite 701a,aa,0,7
SPIWrite 701b,00,0,7
SPIWrite 701a,00,0,7

WAIT 0.01

SPIWrite 702f,00,0,7
SPIWrite 702e,00,0,7
SPIWrite 7007,00,0,7
SPIWrite 7006,00,0,7
SPIWrite 49f1,90,0,7
SPIWrite 49f0,00,0,7
SPIWrite 49f3,e8,0,7
SPIWrite 49f2,00,0,7
SPIWrite 49e3,c0,0,7
SPIWrite 49e2,00,0,7
SPIWrite 49b5,47,0,7
SPIWrite 49b4,47,0,7
SPIWrite 49ff,fd,0,7
SPIWrite 49fe,b0,0,7
SPIWrite 49ed,1d,0,7
SPIWrite 49ec,c0,0,7
SPIWrite 49e7,52,0,7
SPIWrite 49e6,26,0,7
SPIWrite 49e5,6e,0,7
SPIWrite 49e4,b6,0,7
SPIWrite 49df,a8,0,7
SPIWrite 49de,28,0,7
SPIWrite 49eb,0f,0,7
SPIWrite 49ea,98,0,7
SPIWrite 49e9,32,0,7
SPIWrite 49e8,44,0,7
SPIWrite 49fd,0f,0,7
SPIWrite 49fc,98,0,7
SPIWrite 49fb,32,0,7
SPIWrite 49fa,48,0,7
SPIWrite 49f9,4a,0,7
SPIWrite 49f8,44,0,7
SPIWrite 49f7,79,0,7
SPIWrite 49f6,b6,0,7
SPIWrite 49d9,6c,0,7
SPIWrite 49d8,06,0,7
SPIWrite 4601,10,0,7
SPIWrite 4600,6b,0,7
SPIWrite 4603,64,0,7
SPIWrite 4602,80,0,7
SPIWrite 4605,62,0,7
SPIWrite 4604,00,0,7
SPIWrite 4607,7b,0,7
SPIWrite 4606,33,0,7
SPIWrite 4609,70,0,7
SPIWrite 4608,0a,0,7
SPIWrite 460b,bd,0,7
SPIWrite 460a,68,0,7
SPIWrite 460d,76,0,7
SPIWrite 460c,2d,0,7
SPIWrite 460f,66,0,7
SPIWrite 460e,ab,0,7
SPIWrite 4611,d0,0,7
SPIWrite 4610,08,0,7
SPIWrite 4613,00,0,7
SPIWrite 4612,18,0,7
SPIWrite 4615,66,0,7
SPIWrite 4614,2c,0,7
SPIWrite 4617,3d,0,7
SPIWrite 4616,15,0,7
SPIWrite 4619,00,0,7

SPIWrite 4618,80,0,7
SPIWrite 461b,00,0,7
SPIWrite 461a,02,0,7
SPIWrite 461d,34,0,7
SPIWrite 461c,00,0,7
SPIWrite 461f,00,0,7
SPIWrite 461e,00,0,7
SPIWrite 4621,10,0,7
SPIWrite 4620,1a,0,7
SPIWrite 4639,03,0,7
SPIWrite 4638,40,0,7
SPIWrite 463b,00,0,7
SPIWrite 463a,60,0,7
SPIWrite 463d,00,0,7
SPIWrite 463c,00,0,7
SPIWrite 463f,00,0,7
SPIWrite 463e,00,0,7
SPIWrite 4677,00,0,7
SPIWrite 4676,00,0,7
SPIWrite 4679,00,0,7
SPIWrite 4678,00,0,7
SPIWrite 467b,00,0,7
SPIWrite 467a,00,0,7
SPIWrite 467d,00,0,7
SPIWrite 467c,00,0,7
SPIWrite 4683,9f,0,7
SPIWrite 4682,df,0,7
SPIWrite 4685,b3,0,7
SPIWrite 4684,c0,0,7
SPIWrite 468f,24,0,7
SPIWrite 468e,a2,0,7
SPIWrite 4691,cc,0,7
SPIWrite 4690,34,0,7
SPIWrite 4693,e3,0,7
SPIWrite 4692,d7,0,7
SPIWrite 4695,76,0,7
SPIWrite 4694,60,0,7
SPIWrite 4697,06,0,7
SPIWrite 4696,db,0,7
SPIWrite 4741,03,0,7
SPIWrite 4740,41,0,7
SPIWrite 47e7,00,0,7
SPIWrite 47e6,80,0,7
SPIWrite 47e9,fc,0,7
SPIWrite 47e8,00,0,7
SPIWrite 47eb,1f,0,7
SPIWrite 47ea,fe,0,7
SPIWrite 47ed,00,0,7
SPIWrite 47ec,e0,0,7
SPIWrite 47ef,10,0,7
SPIWrite 47ee,00,0,7
SPIWrite 47f1,68,0,7
SPIWrite 47f0,64,0,7
SPIWrite 47f3,92,0,7
SPIWrite 47f2,30,0,7
SPIWrite 47f5,00,0,7
SPIWrite 47f4,00,0,7
SPIWrite 47f7,6d,0,7
SPIWrite 47f6,83,0,7
SPIWrite 47f9,6d,0,7
SPIWrite 47f8,b6,0,7
SPIWrite 47fb,42,0,7
SPIWrite 47fa,6e,0,7
SPIWrite 47fd,62,0,7
SPIWrite 47fc,78,0,7
SPIWrite 47ff,08,0,7
SPIWrite 47fe,c8,0,7
SPIWrite 4401,10,0,7
SPIWrite 4400,6b,0,7

SPIWrite 4403,64,0,7
SPIWrite 4402,80,0,7
SPIWrite 4405,62,0,7
SPIWrite 4404,00,0,7
SPIWrite 4407,7b,0,7
SPIWrite 4406,33,0,7
SPIWrite 4409,70,0,7
SPIWrite 4408,0a,0,7
SPIWrite 440b,bd,0,7
SPIWrite 440a,68,0,7
SPIWrite 440d,76,0,7
SPIWrite 440c,2d,0,7
SPIWrite 440f,66,0,7
SPIWrite 440e,ab,0,7
SPIWrite 4411,d0,0,7
SPIWrite 4410,08,0,7
SPIWrite 4413,00,0,7
SPIWrite 4412,18,0,7
SPIWrite 4415,66,0,7
SPIWrite 4414,2c,0,7
SPIWrite 4417,3d,0,7
SPIWrite 4416,15,0,7
SPIWrite 4419,00,0,7
SPIWrite 4418,80,0,7
SPIWrite 441b,00,0,7
SPIWrite 441a,02,0,7
SPIWrite 441d,34,0,7
SPIWrite 441c,00,0,7
SPIWrite 441f,00,0,7
SPIWrite 441e,00,0,7
SPIWrite 4421,10,0,7
SPIWrite 4420,1a,0,7
SPIWrite 4439,03,0,7
SPIWrite 4438,40,0,7
SPIWrite 443b,00,0,7
SPIWrite 443a,60,0,7
SPIWrite 443d,00,0,7
SPIWrite 443c,00,0,7
SPIWrite 443f,00,0,7
SPIWrite 443e,00,0,7
SPIWrite 4477,00,0,7
SPIWrite 4476,00,0,7
SPIWrite 4479,00,0,7
SPIWrite 4478,00,0,7
SPIWrite 447b,00,0,7
SPIWrite 447a,00,0,7
SPIWrite 447d,00,0,7
SPIWrite 447c,00,0,7
SPIWrite 4483,9f,0,7
SPIWrite 4482,df,0,7
SPIWrite 4485,b3,0,7
SPIWrite 4484,c0,0,7
SPIWrite 448f,24,0,7
SPIWrite 448e,a2,0,7
SPIWrite 4491,cc,0,7
SPIWrite 4490,34,0,7
SPIWrite 4493,e3,0,7
SPIWrite 4492,d7,0,7
SPIWrite 4495,76,0,7
SPIWrite 4494,60,0,7
SPIWrite 4497,06,0,7
SPIWrite 4496,db,0,7
SPIWrite 4541,03,0,7
SPIWrite 4540,41,0,7
SPIWrite 45e7,00,0,7
SPIWrite 45e6,80,0,7
SPIWrite 45e9,fc,0,7
SPIWrite 45e8,00,0,7
SPIWrite 45eb,1f,0,7

SPIWrite 45ea,fe,0,7
SPIWrite 45ed,00,0,7
SPIWrite 45ec,e0,0,7
SPIWrite 45ef,10,0,7
SPIWrite 45ee,00,0,7
SPIWrite 45f1,68,0,7
SPIWrite 45f0,64,0,7
SPIWrite 45f3,92,0,7
SPIWrite 45f2,30,0,7
SPIWrite 45f5,00,0,7
SPIWrite 45f4,00,0,7
SPIWrite 45f7,6d,0,7
SPIWrite 45f6,83,0,7
SPIWrite 45f9,6d,0,7
SPIWrite 45f8,b6,0,7
SPIWrite 45fb,42,0,7
SPIWrite 45fa,6e,0,7
SPIWrite 45fd,62,0,7
SPIWrite 45fc,78,0,7
SPIWrite 45ff,08,0,7
SPIWrite 45fe,c8,0,7
SPIWrite 4001,10,0,7
SPIWrite 4000,6b,0,7
SPIWrite 4003,64,0,7
SPIWrite 4002,80,0,7
SPIWrite 4005,62,0,7
SPIWrite 4004,00,0,7
SPIWrite 4007,7b,0,7
SPIWrite 4006,33,0,7
SPIWrite 4009,70,0,7
SPIWrite 4008,0a,0,7
SPIWrite 400b,bd,0,7
SPIWrite 400a,68,0,7
SPIWrite 400d,76,0,7
SPIWrite 400c,2d,0,7
SPIWrite 400f,66,0,7
SPIWrite 400e,ab,0,7
SPIWrite 4011,d0,0,7
SPIWrite 4010,08,0,7
SPIWrite 4013,00,0,7
SPIWrite 4012,18,0,7
SPIWrite 4015,66,0,7
SPIWrite 4014,2c,0,7
SPIWrite 4017,3d,0,7
SPIWrite 4016,15,0,7
SPIWrite 4019,00,0,7
SPIWrite 4018,80,0,7
SPIWrite 401b,00,0,7
SPIWrite 401a,02,0,7
SPIWrite 401d,34,0,7
SPIWrite 401c,00,0,7
SPIWrite 401f,00,0,7
SPIWrite 401e,00,0,7
SPIWrite 4021,10,0,7
SPIWrite 4020,1a,0,7
SPIWrite 4039,03,0,7
SPIWrite 4038,40,0,7
SPIWrite 403b,00,0,7
SPIWrite 403a,60,0,7
SPIWrite 403d,00,0,7
SPIWrite 403c,00,0,7
SPIWrite 403f,00,0,7
SPIWrite 403e,00,0,7
SPIWrite 4077,00,0,7
SPIWrite 4076,00,0,7
SPIWrite 4079,00,0,7
SPIWrite 4078,00,0,7
SPIWrite 407b,00,0,7
SPIWrite 407a,00,0,7

SPIWrite 407d,00,0,7
SPIWrite 407c,00,0,7
SPIWrite 4083,9f,0,7
SPIWrite 4082,df,0,7
SPIWrite 4085,b3,0,7
SPIWrite 4084,c0,0,7
SPIWrite 408f,24,0,7
SPIWrite 408e,a2,0,7
SPIWrite 4091,cc,0,7
SPIWrite 4090,34,0,7
SPIWrite 4093,e3,0,7
SPIWrite 4092,d7,0,7
SPIWrite 4095,76,0,7
SPIWrite 4094,60,0,7
SPIWrite 4097,06,0,7
SPIWrite 4096,db,0,7
SPIWrite 4141,03,0,7
SPIWrite 4140,41,0,7
SPIWrite 41e7,00,0,7
SPIWrite 41e6,80,0,7
SPIWrite 41e9,fc,0,7
SPIWrite 41e8,00,0,7
SPIWrite 41eb,9f,0,7
SPIWrite 41ea,fe,0,7
SPIWrite 41ed,00,0,7
SPIWrite 41ec,e0,0,7
SPIWrite 41ef,10,0,7
SPIWrite 41ee,00,0,7
SPIWrite 41f1,68,0,7
SPIWrite 41f0,64,0,7
SPIWrite 41f3,92,0,7
SPIWrite 41f2,30,0,7
SPIWrite 41f5,00,0,7
SPIWrite 41f4,00,0,7
SPIWrite 41f7,6d,0,7
SPIWrite 41f6,87,0,7
SPIWrite 41f9,6d,0,7
SPIWrite 41f8,b6,0,7
SPIWrite 41fb,42,0,7
SPIWrite 41fa,6e,0,7
SPIWrite 41fd,62,0,7
SPIWrite 41fc,7c,0,7
SPIWrite 41ff,88,0,7
SPIWrite 41fe,c8,0,7
SPIWrite 4201,10,0,7
SPIWrite 4200,6b,0,7
SPIWrite 4203,64,0,7
SPIWrite 4202,80,0,7
SPIWrite 4205,62,0,7
SPIWrite 4204,00,0,7
SPIWrite 4207,7b,0,7
SPIWrite 4206,33,0,7
SPIWrite 4209,70,0,7
SPIWrite 4208,0a,0,7
SPIWrite 420b,bd,0,7
SPIWrite 420a,68,0,7
SPIWrite 420d,76,0,7
SPIWrite 420c,2d,0,7
SPIWrite 420f,66,0,7
SPIWrite 420e,ab,0,7
SPIWrite 4211,d0,0,7
SPIWrite 4210,08,0,7
SPIWrite 4213,00,0,7
SPIWrite 4212,18,0,7
SPIWrite 4215,66,0,7
SPIWrite 4214,2c,0,7
SPIWrite 4217,3d,0,7
SPIWrite 4216,15,0,7
SPIWrite 4219,00,0,7

```
SPIWrite 4218,80,0,7
SPIWrite 421b,00,0,7
SPIWrite 421a,02,0,7
SPIWrite 421d,34,0,7
SPIWrite 421c,00,0,7
SPIWrite 421f,00,0,7
SPIWrite 421e,00,0,7
SPIWrite 4221,10,0,7
SPIWrite 4220,1a,0,7
SPIWrite 4239,03,0,7
SPIWrite 4238,40,0,7
SPIWrite 423b,00,0,7
SPIWrite 423a,60,0,7
SPIWrite 423d,00,0,7
SPIWrite 423c,00,0,7
SPIWrite 423f,00,0,7
SPIWrite 423e,00,0,7
SPIWrite 4277,00,0,7
SPIWrite 4276,00,0,7
SPIWrite 4279,00,0,7
SPIWrite 4278,00,0,7
SPIWrite 427b,00,0,7
SPIWrite 427a,00,0,7
SPIWrite 427d,00,0,7
SPIWrite 427c,00,0,7
SPIWrite 4283,9f,0,7
SPIWrite 4282,df,0,7
SPIWrite 4285,b3,0,7
SPIWrite 4284,c0,0,7
SPIWrite 428f,24,0,7
SPIWrite 428e,a2,0,7
SPIWrite 4291,cc,0,7
SPIWrite 4290,34,0,7
SPIWrite 4293,e3,0,7
SPIWrite 4292,d7,0,7
SPIWrite 4295,76,0,7
SPIWrite 4294,60,0,7
SPIWrite 4297,06,0,7
SPIWrite 4296,db,0,7
SPIWrite 4341,03,0,7
SPIWrite 4340,41,0,7
SPIWrite 43e7,00,0,7
SPIWrite 43e6,80,0,7
SPIWrite 43e9,fc,0,7
SPIWrite 43e8,00,0,7
SPIWrite 43eb,9f,0,7
SPIWrite 43ea,fe,0,7
SPIWrite 43ed,00,0,7
SPIWrite 43ec,e0,0,7
SPIWrite 43ef,10,0,7
SPIWrite 43ee,00,0,7
SPIWrite 43f1,68,0,7
SPIWrite 43f0,64,0,7
SPIWrite 43f3,92,0,7
SPIWrite 43f2,30,0,7
SPIWrite 43f5,00,0,7
SPIWrite 43f4,00,0,7
SPIWrite 43f7,6d,0,7
SPIWrite 43f6,87,0,7
SPIWrite 43f9,6d,0,7
SPIWrite 43f8,b6,0,7
SPIWrite 43fb,42,0,7
SPIWrite 43fa,6e,0,7
SPIWrite 43fd,62,0,7
SPIWrite 43fc,7c,0,7
SPIWrite 43ff,88,0,7
SPIWrite 43fe,c8,0,7
SPIWrite 7007,00,0,7
SPIWrite 7006,00,0,7
```

//BUS_WIDTH_LANE0=0x0; Address(0x9803[0:0],)

```

SPIWrite 7007,00,0,7    //BUS_WIDTH_LANE1=0x0;  Address(0x9803[1:1],)
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7    //BUS_WIDTH_LANE2=0x0;  Address(0x9803[2:2],)
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7    //BUS_WIDTH_LANE3=0x0;  Address(0x9803[3:3],)
SPIWrite 7006,00,0,7
SPIWrite 0015,40,0,7    //PAGE: SERDES=0x0;      Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,00,0,7

\\END: Done configuring the SERDES

\\ STEP: serdesConfig/step3

\\START: Loading Serdes Firmware.

SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );      Address(0x13[4:4],)

SIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,01,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0193,82,0,7

SIPoll 00f0,0,7,7

SIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,01,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,82,0,7

SIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );      Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;      Address(0x20[3:3],)

\\Read  MACRO_ERROR=0x0;      Address(0x20[3:3],)

\\Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0x20[4:4],)

\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0x20[5:5],)

\\Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0x20[6:6],)

\\Read  MACRO_ERROR_IN_EXECUTION=0x0;  Address(0x20[7:7],)

SPIWrite 0013,00,0,7    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
SPIWrite 0015,04,0,7    //PAGE: SERDES=0x3;      Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,44,0,7
SPIWrite 702d,00,0,7
SPIWrite 702c,05,0,7
SPIWrite 7025,00,0,7
SPIWrite 7024,08,0,7
SPIWrite 702b,e0,0,7
SPIWrite 702a,20,0,7

```

WAIT 0.01

```
SPIWrite 702d,00,0,7
SPIWrite 702c,02,0,7
SPIWrite 7025,00,0,7
SPIWrite 7024,50,0,7
SPIWrite 702b,e0,0,7
SPIWrite 702a,20,0,7
```

WAIT 0.01

```
SPIWrite 701b,07,0,7    //DOMAIN_RESET=0x777;    Address(0x980d[11:0],)
SPIWrite 701a,77,0,7
SPIWrite 701b,00,0,7    //DOMAIN_RESET=0x0;    Address(0x980d[11:0],)
SPIWrite 701a,00,0,7
```

WAIT 5

```
SPIWrite 0015,40,0,7    //PAGE: SERDES=0x0;    Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,00,0,7
```

\\END: Done loading Serdes Firmware.

\\ STEP: sigChainConfig/step0

\\START: Configuring JESD TX Lane Mux

```
SPIWrite 0015,08,0,7    //PAGE: jesd_subchip=0x1;(Meaning: );    Address(0x15[3:3],)
SPIWrite 004a,14,0,7
SPIWrite 004a,34,0,7
SPIWrite 004b,30,0,7
SPIWrite 004b,20,0,7
SPIWrite 004c,51,0,7
SPIWrite 004c,61,0,7
SPIWrite 004d,75,0,7
SPIWrite 004d,75,0,7
SPIWrite 004e,12,0,7
SPIWrite 004e,42,0,7
SPIWrite 004f,33,0,7
SPIWrite 004f,13,0,7
SPIWrite 0050,50,0,7
SPIWrite 0050,60,0,7
SPIWrite 0051,75,0,7
SPIWrite 0051,75,0,7
```

\\END: Done configuring JESD TX Lane Mux

\\START: Configuring JESD RX Lane Mux

```
SPIWrite 0068,12,0,7
SPIWrite 0068,32,0,7
SPIWrite 0069,34,0,7
SPIWrite 0069,54,0,7
SPIWrite 006a,50,0,7
SPIWrite 006a,10,0,7
SPIWrite 006b,76,0,7
SPIWrite 006b,76,0,7
SPIWrite 006c,12,0,7
SPIWrite 006c,32,0,7
SPIWrite 006d,34,0,7
SPIWrite 006d,54,0,7
SPIWrite 006e,50,0,7
SPIWrite 006e,10,0,7
SPIWrite 006f,76,0,7
SPIWrite 006f,76,0,7
```

\\END: Done configuring JESD RX Lane Mux

\\START: Configuring the Data Muxes

SPIWrite 0044,50,0,7
SPIWrite 0044,50,0,7
SPIWrite 0044,50,0,7
SPIWrite 0044,50,0,7
SPIWrite 0045,fa,0,7
SPIWrite 0045,fa,0,7
SPIWrite 0045,fa,0,7
SPIWrite 0045,fa,0,7
SPIWrite 0046,fa,0,7
SPIWrite 0046,fa,0,7
SPIWrite 0046,fa,0,7
SPIWrite 0046,fa,0,7
SPIWrite 0047,50,0,7
SPIWrite 0047,50,0,7
SPIWrite 0047,50,0,7
SPIWrite 0047,50,0,7
SPIWrite 003a,e4,0,7
SPIWrite 003a,e4,0,7
SPIWrite 003a,e4,0,7
SPIWrite 003a,e4,0,7
SPIWrite 003b,e4,0,7
SPIWrite 003b,e4,0,7
SPIWrite 003b,e4,0,7
SPIWrite 003b,e4,0,7
SPIWrite 003c,00,0,7
SPIWrite 003c,00,0,7
SPIWrite 003d,11,0,7
SPIWrite 003d,11,0,7
SPIWrite 003e,44,0,7
SPIWrite 003e,44,0,7
SPIWrite 003f,55,0,7
SPIWrite 003f,55,0,7
SPIWrite 0036,d8,0,7
SPIWrite 0036,d8,0,7
SPIWrite 0036,d8,0,7
SPIWrite 0036,d8,0,7
SPIWrite 0037,d8,0,7
SPIWrite 0037,d8,0,7
SPIWrite 0037,d8,0,7
SPIWrite 0037,d8,0,7
SPIWrite 0040,44,0,7
SPIWrite 0040,44,0,7
SPIWrite 0041,55,0,7
SPIWrite 0041,55,0,7
SPIWrite 0042,00,0,7
SPIWrite 0042,00,0,7
SPIWrite 0043,11,0,7
SPIWrite 0043,11,0,7
SPIWrite 0038,d8,0,7
SPIWrite 0038,d8,0,7
SPIWrite 0038,d8,0,7
SPIWrite 0038,d8,0,7
SPIWrite 0039,d8,0,7
SPIWrite 0039,d8,0,7
SPIWrite 0039,d8,0,7
SPIWrite 0039,d8,0,7
SPIWrite 0040,44,0,7
SPIWrite 0040,44,0,7
SPIWrite 0041,55,0,7
SPIWrite 0041,55,0,7
SPIWrite 0042,00,0,7
SPIWrite 0042,00,0,7
SPIWrite 0043,11,0,7
SPIWrite 0043,11,0,7
SPIWrite 0066,42,0,7
SPIWrite 0066,22,0,7

SPIWrite 0067,53,0,7
SPIWrite 0067,33,0,7

\\END: Done configuring the Data Muxes

\\START: Configuring JESDTX Sync Mux

SPIWrite 0054,e4,0,7
SPIWrite 0054,d4,0,7
SPIWrite 0054,d8,0,7
SPIWrite 0054,d8,0,7

\\END: Done configuring JESDTX Sync Mux

\\START: Configuring JESDRX Sync Mux

SPIWrite 0061,00,0,7
SPIWrite 0061,00,0,7
SPIWrite 0061,00,0,7
SPIWrite 0061,00,0,7
SPIWrite 0055,e4,0,7
SPIWrite 0055,e0,0,7
SPIWrite 0055,e0,0,7
SPIWrite 0055,a0,0,7

\\END: Done configuring JESDRX Sync Mux

\\START: Setting FIFO and dither in JESD

SPIWrite 0032,10,0,7
SPIWrite 0035,10,0,7
SPIWrite 0030,10,0,7
SPIWrite 0031,10,0,7
SPIWrite 0033,10,0,7
SPIWrite 0034,10,0,7

\\END: Done Setting FIFO and dither in JESD

SPIWrite 0015,00,0,7 //PAGE: jesd_subchip=0x0; (Meaning:); Address(0x15[3:3],)
\\ STEP: sigChainConfig/step1

\\START: Doing RX, TX and FB Digital Chain Config.

SPIWrite 0013,10,4,4 //PAGE: customer_macro=0x1; (Meaning:); Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,01,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,31,0,7

\\Read macro_opcode_operand=0x31000000; Address(0x190[31:0],)

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4 //PAGE: customer_macro=0x0; (Meaning:); Address(0x13[4:4],)
SPIWrite 0013,20,5,5 //PAGE: cm4_macro=0x1; Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read MACRO_ERROR=0x0; Address(0x20[3:3],)

\\Read MACRO_ERROR=0x0; Address(0x20[3:3],)

\\Read MACRO_ERROR_IN_OPCODE=0x0; Address(0x20[4:4],)

\\Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0x20[5:5],)

\\Read MACRO_ERROR_IN_OPERAND=0x0; Address(0x20[6:6],)

\\Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0x20[7:7],)

SPIWrite 0013,00,5,5 //PAGE: cm4_macro=0x0; Address(0x13[5:5],)
SPIWrite 0013,10,4,4 //PAGE: customer_macro=0x1; (Meaning:); Address(0x13[4:4],)
SPIWrite 0193,45,0,7

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4 //PAGE: customer_macro=0x0; (Meaning:); Address(0x13[4:4],)
SPIWrite 0016,40,6,7 //PAGE: fb_top=0x1; Address(0x16[7:6],)
SPIWrite 015b,05,0,2 //FBAsyncFIFORdPtrVal=0x5; Address(0x158[26:24],)
SPIWrite 0016,80,6,7 //PAGE: fb_top=0x2; Address(0x16[7:6],)
SPIWrite 015b,05,0,2 //FBAsyncFIFORdPtrVal=0x5; Address(0x158[26:24],)
SPIWrite 0016,00,6,7 //PAGE: fb_top=0x0; Address(0x16[7:6],)
SPIWrite 0010,04,2,3 //PAGE: rx_top=0x1; Address(0x10[3:2],)
SPIWrite 0120,03,0,2 //RxDecAsyncFIFORdPtrLoad=0x3; Address(0x120[2:0],)
SPIWrite 0010,08,2,3 //PAGE: rx_top=0x2; Address(0x10[3:2],)
SPIWrite 0120,03,0,2 //RxDecAsyncFIFORdPtrLoad=0x3; Address(0x120[2:0],)
SPIWrite 0010,00,2,3 //PAGE: rx_top=0x0; Address(0x10[3:2],)
SPIWrite 0010,01,0,1 //PAGE: tx_top=0x1; Address(0x10[1:0],)
SPIWrite 010d,03,0,2 //RdPtrOffDigOutAsyncFIFO=0x3; Address(0x10c[10:8],)
SPIWrite 0010,02,0,1 //PAGE: tx_top=0x2; Address(0x10[1:0],)
SPIWrite 010d,03,0,2 //RdPtrOffDigOutAsyncFIFO=0x3; Address(0x10c[10:8],)
SPIWrite 0010,01,0,1 //PAGE: tx_top=0x1; Address(0x10[1:0],)
SPIWrite 010b,0d,0,3 //RdPtrOffDigInpAsyncFIFO=0xd; Address(0x108[27:24],)
SPIWrite 0138,01,0,0 //BlockEnable=0x1; (Meaning:); Address(0x138[0:0],)
SPIWrite 0139,01,0,1 //LutUpdateMode=0x1; (Meaning:); Address(0x138[9:8],)
SPIWrite 0148,01,0,0 //BlockEnable=0x1; (Meaning:); Address(0x148[0:0],)
SPIWrite 0149,01,0,1 //LutUpdateMode=0x1; (Meaning:); Address(0x148[9:8],)
SPIWrite 0010,02,0,1 //PAGE: tx_top=0x2; Address(0x10[1:0],)
SPIWrite 010b,0d,0,3 //RdPtrOffDigInpAsyncFIFO=0xd; Address(0x108[27:24],)
SPIWrite 0138,01,0,0 //BlockEnable=0x1; (Meaning:); Address(0x138[0:0],)
SPIWrite 0139,01,0,1 //LutUpdateMode=0x1; (Meaning:); Address(0x138[9:8],)
SPIWrite 0148,01,0,0 //BlockEnable=0x1; (Meaning:); Address(0x148[0:0],)
SPIWrite 0149,01,0,1 //LutUpdateMode=0x1; (Meaning:); Address(0x148[9:8],)
SPIWrite 0010,00,0,1 //PAGE: tx_top=0x0; Address(0x10[1:0],)
SPIWrite 0010,04,2,3 //PAGE: rx_top=0x1; Address(0x10[3:2],)
SPIWrite 0af9,01,0,0 //pdn_in=0x1; (Meaning:); Address(0xaf8[8:8],)
SPIWrite 0afb,01,0,0 //pdn_in=0x1; (Meaning:); Address(0xaf8[24:24],)
SPIWrite 0a50,33,0,7 //gain_component_n=0x33; Address(0xa50[7:0],)
SPIWrite 0a51,33,0,7 //gain_component_n=0x33; Address(0xa50[15:8],)
SPIWrite 0a52,33,0,7 //gain_component_n=0x33; Address(0xa50[23:16],)
SPIWrite 0a53,33,0,7 //gain_component_n=0x33; Address(0xa50[31:24],)
SPIWrite 0a56,0e,0,0 //gain_corrector_bypass=0x0; (Meaning:); Address(0xa54[16:16],)
SPIWrite 0a56,0c,1,1 //gain_corrector_bypass=0x0; (Meaning:); Address(0xa54[17:17],)
SPIWrite 0a56,08,2,2 //gain_corrector_bypass=0x0; (Meaning:); Address(0xa54[18:18],)
SPIWrite 0a56,00,3,3 //gain_corrector_bypass=0x0; (Meaning:); Address(0xa54[19:19],)
SPIWrite 0a54,01,0,0 //rx1_unit_gain_mode=0x1; (Meaning:); Address(0xa54[0:0],)
SPIWrite 0a54,03,1,1 //rx2_unit_gain_mode=0x1; (Meaning:); Address(0xa54[1:1],)
SPIWrite 0c6b,00,0,0 //coef_update_signal=0x0; Address(0xc68[24:24],)
SPIWrite 0c73,00,0,0 //coef_update_signal=0x0; Address(0xc70[24:24],)
SPIWrite 0e6b,00,0,0 //coef_update_signal=0x0; Address(0xe68[24:24],)
SPIWrite 0e73,00,0,0 //coef_update_signal=0x0; Address(0xe70[24:24],)
SPIWrite 0c6b,01,0,0 //coef_update_signal=0x1; Address(0xc68[24:24],)

```

SPIWrite 0c73,01,0,0 //coef_update_signal=0x1; Address(0xc70[24:24],)
SPIWrite 0e6b,01,0,0 //coef_update_signal=0x1; Address(0xe68[24:24],)
SPIWrite 0e73,01,0,0 //coef_update_signal=0x1; Address(0xe70[24:24],)
SPIWrite 0c6b,00,0,0 //coef_update_signal=0x0; Address(0xc68[24:24],)
SPIWrite 0c73,00,0,0 //coef_update_signal=0x0; Address(0xc70[24:24],)
SPIWrite 0e6b,00,0,0 //coef_update_signal=0x0; Address(0xe68[24:24],)
SPIWrite 0e73,00,0,0 //coef_update_signal=0x0; Address(0xe70[24:24],)
SPIWrite 0010,08,2,3 //PAGE: rx_top=0x2; Address(0x10[3:2],)
SPIWrite 0af9,01,0,0 //pdn_in=0x1; (Meaning: ); Address(0xaf8[8:8],)
SPIWrite 0afb,01,0,0 //pdn_in=0x1; (Meaning: ); Address(0xaf8[24:24],)
SPIWrite 0a50,33,0,7 //gain_component_n=0x33; Address(0xa50[7:0],)
SPIWrite 0a51,33,0,7 //gain_component_n=0x33; Address(0xa50[15:8],)
SPIWrite 0a52,33,0,7 //gain_component_n=0x33; Address(0xa50[23:16],)
SPIWrite 0a53,33,0,7 //gain_component_n=0x33; Address(0xa50[31:24],)
SPIWrite 0a56,0e,0,0 //gain_corrector_bypass=0x0; (Meaning: ); Address(0xa54[16:16],)
SPIWrite 0a56,0c,1,1 //gain_corrector_bypass=0x0; (Meaning: ); Address(0xa54[17:17],)
SPIWrite 0a56,08,2,2 //gain_corrector_bypass=0x0; (Meaning: ); Address(0xa54[18:18],)
SPIWrite 0a56,00,3,3 //gain_corrector_bypass=0x0; (Meaning: ); Address(0xa54[19:19],)
SPIWrite 0a54,01,0,0 //rx1_unit_gain_mode=0x1; (Meaning: ); Address(0xa54[0:0],)
SPIWrite 0a54,03,1,1 //rx2_unit_gain_mode=0x1; (Meaning: ); Address(0xa54[1:1],)
SPIWrite 0c6b,00,0,0 //coef_update_signal=0x0; Address(0xc68[24:24],)
SPIWrite 0c73,00,0,0 //coef_update_signal=0x0; Address(0xc70[24:24],)
SPIWrite 0e6b,00,0,0 //coef_update_signal=0x0; Address(0xe68[24:24],)
SPIWrite 0e73,00,0,0 //coef_update_signal=0x0; Address(0xe70[24:24],)
SPIWrite 0c6b,01,0,0 //coef_update_signal=0x1; Address(0xc68[24:24],)
SPIWrite 0c73,01,0,0 //coef_update_signal=0x1; Address(0xc70[24:24],)
SPIWrite 0e6b,01,0,0 //coef_update_signal=0x1; Address(0xe68[24:24],)
SPIWrite 0e73,01,0,0 //coef_update_signal=0x1; Address(0xe70[24:24],)
SPIWrite 0c6b,00,0,0 //coef_update_signal=0x0; Address(0xc68[24:24],)
SPIWrite 0c73,00,0,0 //coef_update_signal=0x0; Address(0xc70[24:24],)
SPIWrite 0e6b,00,0,0 //coef_update_signal=0x0; Address(0xe68[24:24],)
SPIWrite 0e73,00,0,0 //coef_update_signal=0x0; Address(0xe70[24:24],)

```

\\END: Completed RX, TX and FB Digital Chain Config.

```

SPIWrite 0010,00,0,7 //PAGE: rx_top=0x0; Address(0x10[3:2],)
\\ STEP: sigChainConfig/step2

```

\\START: Configuring SR Block

```

SPIWrite 0010,01,0,7 //PAGE: tx_top=0x1; Address(0x10[1:0],)
SPIWrite 0247,0f,0,7 //alarmMask=0xfdc; Address(0x244[28:16],)
SPIWrite 0246,dc,0,7
SPIWrite 022a,01,0,7 //AmplMode=0x1; (Meaning: ); Address(0x228[16:16],)
SPIWrite 023b,00,0,7 //GainStepSize=0x26; Address(0x238[25:16],)
SPIWrite 023a,26,0,7
SPIWrite 0233,00,0,7 //AttnStepSize=0x26; Address(0x230[25:16],)
SPIWrite 0232,26,0,7
SPIWrite 0228,01,0,7 //AmplUpdateCycles=0x1; Address(0x228[6:0],)
SPIWrite 0210,02,0,7 //MultDataMode=0x1; (Meaning: ); Address(0x210[2:1],)
SPIWrite 022f,00,0,7 //fsmWaitCntr=0x13; Address(0x22c[31:16],)
SPIWrite 022e,13,0,7
SPIWrite 0225,00,0,7 //AmplRampAttnDly=0x0; Address(0x224[11:0],)
SPIWrite 0224,00,0,7
SPIWrite 0227,00,0,7 //AmplRampGainDly=0x0; Address(0x224[27:16],)
SPIWrite 0226,00,0,7
SPIWrite 0210,03,0,7 //BlkEnable=0x1; (Meaning: ); Address(0x210[0:0],)
SPIWrite 0447,0f,0,7 //alarmMask=0xfdc; Address(0x444[28:16],)
SPIWrite 0446,dc,0,7
SPIWrite 042a,01,0,7 //AmplMode=0x1; (Meaning: ); Address(0x428[16:16],)
SPIWrite 043b,00,0,7 //GainStepSize=0x26; Address(0x438[25:16],)
SPIWrite 043a,26,0,7
SPIWrite 0433,00,0,7 //AttnStepSize=0x26; Address(0x430[25:16],)
SPIWrite 0432,26,0,7
SPIWrite 0428,01,0,7 //AmplUpdateCycles=0x1; Address(0x428[6:0],)
SPIWrite 0410,02,0,7 //MultDataMode=0x1; (Meaning: ); Address(0x410[2:1],)
SPIWrite 042f,00,0,7 //fsmWaitCntr=0x13; Address(0x42c[31:16],)
SPIWrite 042e,13,0,7
SPIWrite 0425,00,0,7 //AmplRampAttnDly=0x0; Address(0x424[11:0],)

```

```
SPIWrite 0424,00,0,7
SPIWrite 0427,00,0,7 //AmplRampGainDly=0x0; Address(0x424[27:16],)
SPIWrite 0426,00,0,7
SPIWrite 0410,03,0,7 //BlkEnable=0x1;(Meaning: ); Address(0x410[0:0],)
```

\\END: Done Configuring SR Block

\\START: Configuring SR Block

```
SPIWrite 0010,02,0,7 //PAGE: tx_top=0x2; Address(0x10[1:0],)
SPIWrite 0247,0f,0,7 //alarmMask=0xfdc; Address(0x244[28:16],)
SPIWrite 0246,dc,0,7
SPIWrite 022a,01,0,7 //AmplMode=0x1;(Meaning: ); Address(0x228[16:16],)
SPIWrite 023b,00,0,7 //GainStepSize=0x26; Address(0x238[25:16],)
SPIWrite 023a,26,0,7
SPIWrite 0233,00,0,7 //AttnStepSize=0x26; Address(0x230[25:16],)
SPIWrite 0232,26,0,7
SPIWrite 0228,01,0,7 //AmplUpdateCycles=0x1; Address(0x228[6:0],)
SPIWrite 0210,02,0,7 //MultDataMode=0x1;(Meaning: ); Address(0x210[2:1],)
SPIWrite 022f,00,0,7 //fsmWaitCntr=0x13; Address(0x22c[31:16],)
SPIWrite 022e,13,0,7
SPIWrite 0225,00,0,7 //AmplRampAttnDly=0x0; Address(0x224[11:0],)
SPIWrite 0224,00,0,7
SPIWrite 0227,00,0,7 //AmplRampGainDly=0x0; Address(0x224[27:16],)
SPIWrite 0226,00,0,7
SPIWrite 0210,03,0,7 //BlkEnable=0x1;(Meaning: ); Address(0x210[0:0],)
SPIWrite 0447,0f,0,7 //alarmMask=0xfdc; Address(0x444[28:16],)
SPIWrite 0446,dc,0,7
SPIWrite 042a,01,0,7 //AmplMode=0x1;(Meaning: ); Address(0x428[16:16],)
SPIWrite 043b,00,0,7 //GainStepSize=0x26; Address(0x438[25:16],)
SPIWrite 043a,26,0,7
SPIWrite 0433,00,0,7 //AttnStepSize=0x26; Address(0x430[25:16],)
SPIWrite 0432,26,0,7
SPIWrite 0428,01,0,7 //AmplUpdateCycles=0x1; Address(0x428[6:0],)
SPIWrite 0410,02,0,7 //MultDataMode=0x1;(Meaning: ); Address(0x410[2:1],)
SPIWrite 042f,00,0,7 //fsmWaitCntr=0x13; Address(0x42c[31:16],)
SPIWrite 042e,13,0,7
SPIWrite 0425,00,0,7 //AmplRampAttnDly=0x0; Address(0x424[11:0],)
SPIWrite 0424,00,0,7
SPIWrite 0427,00,0,7 //AmplRampGainDly=0x0; Address(0x424[27:16],)
SPIWrite 0426,00,0,7
SPIWrite 0410,03,0,7 //BlkEnable=0x1;(Meaning: ); Address(0x410[0:0],)
```

\\END: Done Configuring SR Block

```
SPIWrite 0010,00,0,7 //PAGE: tx_top=0x0; Address(0x10[1:0],)
\\ STEP: OvTDDpin/step0
```

\\START: Doing Internal TDD settings

```
SPIWrite 0014,04,0,7 //PAGE: TIMING_CON=0x1;(Meaning: ); Address(0x14[2:2],)
SPIWrite 04e7,00,0,7 //enable_multi_sysref=0x0; Address(0x4e4[24:24],)
SPIWrite 04c4,01,0,7 //mode_2t2r=0x1; Address(0x4c4[0:0],)
SPIWrite 04c5,00,0,7 //fdd_mode=0x0; Address(0x4c4[8:8],)
SPIWrite 0206,06,0,7 //force_tg_txAB=0x0; Address(0x204[16:16],)
SPIWrite 0206,04,0,7 //force_tg_rxAB=0x0; Address(0x204[17:17],)
SPIWrite 0206,00,0,7 //force_tg_fbAB=0x0; Address(0x204[18:18],)
SPIWrite 036a,06,0,7 //force_tg_txCD=0x0; Address(0x368[16:16],)
SPIWrite 036a,04,0,7 //force_tg_rxCD=0x0; Address(0x368[17:17],)
SPIWrite 036a,00,0,7 //force_tg_fbCD=0x0; Address(0x368[18:18],)
SPIWrite 04dc,80,0,7 //force_pll_txAB=0x0; Address(0x4dc[6:6],)
SPIWrite 04dd,0d,0,7 //force_pll_txCD=0x0; Address(0x4dc[9:9],)
SPIWrite 04dc,00,0,7 //force_pll_rxAB=0x0; Address(0x4dc[7:7],)
SPIWrite 04dd,09,0,7 //force_pll_rxCD=0x0; Address(0x4dc[10:10],)
SPIWrite 04dd,08,0,7 //force_pll_fbAB=0x0; Address(0x4dc[8:8],)
SPIWrite 04dd,00,0,7 //force_pll_fbCD=0x0; Address(0x4dc[11:11],)
SPIWrite 0110,00,0,7 //fb_vswr_pin_valid_cha=0x0; Address(0x110[0:0],)
SPIWrite 0111,00,0,7 //fb_vswr_pin_valid_chc=0x0; Address(0x110[8:8],)
```

```
SPIWrite 0118,00,0,7 //use_reg_for_tx_gswap_rxtxlo=0x0; Address(0x118[0:0],)
SPIWrite 011c,01,0,7 //use_reg_for_txdsalatch=0x1; Address(0x11c[0:0],)
SPIWrite 0121,00,0,7 //en_reg_for_gswap=0x0; Address(0x120[8:8],)
SPIWrite 0106,0f,0,7 //chsel_gswap=0xf; Address(0x104[19:16],)
SPIWrite 0114,00,0,7 //fb_ncosel_pin_valid_cha=0x0; Address(0x114[0:0],)
SPIWrite 0115,00,0,7 //fb_ncosel_pin_valid_chc=0x0; Address(0x114[8:8],)
SPIWrite 071f,90,0,7 //override_val_fbmuxsel=0x24; Address(0x71c[31:26],)
SPIWrite 071f,93,0,7 //override_fb_muxsel=0x3; Address(0x71c[25:24],)
SPIWrite 04c6,01,0,7 //dc_pll_sync_mode=0x1; Address(0x4c4[16:16],)
SPIWrite 0526,00,0,7 //en_ovr_for_cond_freeze=0x0; Address(0x524[16:16],)
SPIWrite 0621,01,0,7 //config_rise_rxjesdon_chab=0x177; Address(0x620[15:0],)
SPIWrite 0620,77,0,7
SPIWrite 0661,01,0,7 //config_rise_rxjesdon_chcd=0x177; Address(0x660[15:0],)
SPIWrite 0660,77,0,7
SPIWrite 0014,00,0,7 //PAGE: TIMING_CON=0x0; (Meaning: ); Address(0x14[2:2],)
SPIWrite 0014,01,0,7 //PAGE: clktop_2t=0x1; Address(0x14[1:0],)
SPIWrite 005c,10,0,7 //CTL_SEL_CM_BIAS_R_SHRT_RXCML_1P8=0x1; Address(0x5c[4:4],)
SPIWrite 005c,18,0,7 //CTL_FORCE_LDO_FILT_RXCML_1P8=0x1; Address(0x5c[3:3],)
SPIWrite 005c,1c,0,7 //CTL_FORCE_CASCADEFILT_RXCML_1P8=0x1; Address(0x5c[2:2],)
SPIWrite 005c,1e,0,7 //CTL_FORCE_BIASFILT_RXCML_1P8=0x1; Address(0x5c[1:1],)
```

\\END: Completed Internal TDD settings

```
SPIWrite 0014,00,0,7 //PAGE: clktop_2t=0x0; Address(0x14[1:0],)
\\ STEP: OvTDDpin/step1
```

\\START: Overriding TDD Pins internally

```
SPIWrite 0014,04,0,7 //PAGE: TIMING_CON=0x1; (Meaning: ); Address(0x14[2:2],)
SPIWrite 0124,01,0,7 //use_reg_txon_AB=0x1; Address(0x124[0:0],)
SPIWrite 0126,01,0,7 //use_reg_rxon_AB=0x1; Address(0x124[16:16],)
SPIWrite 0128,01,0,7 //use_reg_fbon_AB=0x1; Address(0x128[0:0],)
SPIWrite 012a,01,0,7 //use_reg_txon_CD=0x1; Address(0x128[16:16],)
SPIWrite 012c,01,0,7 //use_reg_rxon_CD=0x1; Address(0x12c[0:0],)
SPIWrite 012e,01,0,7 //use_reg_fbon_CD=0x1; Address(0x12c[16:16],)
SPIWrite 0125,00,0,7 //reg_for_txon_AB=0x0; Address(0x124[8:8],)
SPIWrite 0127,00,0,7 //reg_for_rxon_AB=0x0; Address(0x124[24:24],)
SPIWrite 0129,00,0,7 //reg_for_fbon_AB=0x0; Address(0x128[8:8],)
SPIWrite 012b,00,0,7 //reg_for_txon_CD=0x0; Address(0x128[24:24],)
SPIWrite 012d,00,0,7 //reg_for_rxon_CD=0x0; Address(0x12c[8:8],)
SPIWrite 012f,00,0,7 //reg_for_fbon_CD=0x0; Address(0x12c[24:24],)
```

\\END: Done overriding TDD Pins internally

```
SPIWrite 0014,00,0,7 //PAGE: TIMING_CON=0x0; (Meaning: ); Address(0x14[2:2],)
\\ STEP: OvTDDpin/step2
```

\\START: Overriding TDD Pins internally

```
SPIWrite 0014,04,0,7 //PAGE: TIMING_CON=0x1; (Meaning: ); Address(0x14[2:2],)
SPIWrite 0124,01,0,7 //use_reg_txon_AB=0x1; Address(0x124[0:0],)
SPIWrite 0126,01,0,7 //use_reg_rxon_AB=0x1; Address(0x124[16:16],)
SPIWrite 0128,01,0,7 //use_reg_fbon_AB=0x1; Address(0x128[0:0],)
SPIWrite 012a,01,0,7 //use_reg_txon_CD=0x1; Address(0x128[16:16],)
SPIWrite 012c,01,0,7 //use_reg_rxon_CD=0x1; Address(0x12c[0:0],)
SPIWrite 012e,01,0,7 //use_reg_fbon_CD=0x1; Address(0x12c[16:16],)
SPIWrite 0125,01,0,7 //reg_for_txon_AB=0x1; Address(0x124[8:8],)
SPIWrite 0127,00,0,7 //reg_for_rxon_AB=0x0; Address(0x124[24:24],)
SPIWrite 0129,00,0,7 //reg_for_fbon_AB=0x0; Address(0x128[8:8],)
SPIWrite 012b,01,0,7 //reg_for_txon_CD=0x1; Address(0x128[24:24],)
SPIWrite 012d,00,0,7 //reg_for_rxon_CD=0x0; Address(0x12c[8:8],)
SPIWrite 012f,00,0,7 //reg_for_fbon_CD=0x0; Address(0x12c[24:24],)
```

\\END: Done overriding TDD Pins internally

```
SPIWrite 0014,00,0,7 //PAGE: TIMING_CON=0x0; (Meaning: ); Address(0x14[2:2],)
\\ STEP: analogWrite/step0
```

\\START: Doing DAC Analog Writes

```
SPIWrite 0017,0f,0,3    //PAGE: dac_1t=0xf;    Address(0x17[3:0],)
SPIWrite 00bc,55,0,2
SPIWrite 00bc,55,3,6
SPIWrite 00bd,aa,0,3
SPIWrite 00bd,aa,4,7
SPIWrite 00be,14,0,4
SPIWrite 00bf,19,0,4
SPIWrite 00c0,19,0,4
SPIWrite 0052,b4,2,4
SPIWrite 0052,b4,5,7
SPIWrite 0054,0a,0,3
SPIWrite 0055,14,0,4
SPIWrite 0056,19,0,4
SPIWrite 0057,19,0,4
SPIWrite 0040,18,3,3
SPIWrite 0040,18,4,4
SPIWrite 003f,00,0,7
SPIWrite 003e,00,0,7
SPIWrite 003d,00,0,7
SPIWrite 003c,03,0,7
SPIWrite 007b,03,0,7
SPIWrite 007a,ff,0,7
SPIWrite 007e,03,0,7
SPIWrite 007d,ff,0,7
SPIWrite 0081,03,0,7
SPIWrite 0080,ff,0,7
SPIWrite 0085,03,0,7
SPIWrite 0084,ff,0,7
SPIWrite 0089,00,0,7
SPIWrite 0088,03,0,7
SPIWrite 008d,00,0,7
SPIWrite 008c,03,0,7
SPIWrite 0091,01,0,7
SPIWrite 0090,ff,0,7
SPIWrite 0095,00,0,7
SPIWrite 0094,1f,0,7
SPIWrite 00c1,1e,0,7
SPIWrite 00c2,32,0,7
SPIWrite 006e,aa,0,3
SPIWrite 006e,aa,4,7
SPIWrite 0041,28,2,5
SPIWrite 0042,aa,0,3
SPIWrite 0042,aa,4,7
SPIWrite 0043,aa,0,3
SPIWrite 0043,aa,4,7
SPIWrite 0044,0a,0,3
SPIWrite 006f,aa,0,3
SPIWrite 0045,03,0,7
SPIWrite 0046,03,0,7
SPIWrite 0062,88,0,3
SPIWrite 0062,88,4,7
SPIWrite 0063,88,0,3
SPIWrite 0063,88,4,7
SPIWrite 0065,40,0,7
SPIWrite 0066,40,0,7
SPIWrite 0067,40,0,7
SPIWrite 0068,40,0,7
SPIWrite 0069,40,0,7
SPIWrite 006a,40,0,7
SPIWrite 006b,40,0,7
SPIWrite 006c,40,0,7
SPIWrite 0064,44,0,3
SPIWrite 0064,44,4,7
SPIWrite 00c8,55,0,3
SPIWrite 00c8,55,4,7
SPIWrite 00c9,82,0,3
SPIWrite 00c9,22,4,7
SPIWrite 00d5,e4,0,7
```

```

SPIWrite 00d8,e4,0,7
SPIWrite 00d9,a0,0,7
SPIWrite 00da,a0,0,7
SPIWrite 00af,92,0,7
SPIWrite 00ad,0f,0,3
SPIWrite 00b0,1f,0,7
SPIWrite 00a7,ff,0,7
SPIWrite 00a6,ff,0,7
SPIWrite 00a5,ff,0,7
SPIWrite 00a4,ff,0,7
SPIWrite 00a8,ff,0,7
SPIWrite 00ae,06,0,3
SPIWrite 00cb,ff,0,7
SPIWrite 00cc,ff,0,7
SPIWrite 00d5,b8,0,7
SPIWrite 00d8,b8,0,7
SPIWrite 006f,aa,0,3
SPIWrite 006f,aa,4,7
SPIWrite 006d,06,1,3
SPIWrite 006d,46,4,6
SPIWrite 0047,03,0,7
SPIWrite 009c,02,1,1
SPIWrite 009f,78,0,7
SPIWrite 009e,00,0,7
SPIWrite 0017,00,0,3    //PAGE: dac_1t=0x0;      Address(0x17[3:0],)
SPIWrite 0010,03,0,7    //PAGE: tx_top=0x3;      Address(0x10[1:0],)
SPIWrite 0830,00,0,7    //IndepCorrByp=0x0;(Meaning: );      Address(0x830[0:0],)
SPIWrite 0830,02,0,7    //IndepCorrEn=0x1;(Meaning: );      Address(0x830[1:1],)
SPIWrite 0890,00,0,7    //IndepCorrByp=0x0;(Meaning: );      Address(0x890[0:0],)
SPIWrite 0890,02,0,7    //IndepCorrEn=0x1;(Meaning: );      Address(0x890[1:1],)
SPIWrite 0650,02,0,7    //txIQMCLFSREn=0x1;(Meaning: );      Address(0x650[1:1],)
SPIWrite 06e4,02,0,7    //txIQMCLFSREn=0x1;(Meaning: );      Address(0x6e4[1:1],)
SPIWrite 0831,28,0,7    //dsaMinIndex=0x28;      Address(0x830[13:8],)
SPIWrite 0891,28,0,7    //dsaMinIndex=0x28;      Address(0x890[13:8],)
SPIWrite 0832,01,0,7    //IndepCorrUpdt=0x1;      Address(0x830[16:16],)
SPIWrite 0892,01,0,7    //IndepCorrUpdt=0x1;      Address(0x890[16:16],)
SPIWrite 0833,00,0,7    //CoeffScaling=0x0;(Meaning: );      Address(0x830[24:24],)
SPIWrite 0893,00,0,7    //CoeffScaling=0x0;(Meaning: );      Address(0x890[24:24],)
SPIWrite 0832,00,0,7    //IndepCorrUpdt=0x0;      Address(0x830[16:16],)
SPIWrite 0892,00,0,7    //IndepCorrUpdt=0x0;      Address(0x890[16:16],)
SPIWrite 0010,00,0,7    //PAGE: tx_top=0x0;      Address(0x10[1:0],)

```

\\END: Completed DAC Analog Writes

\\ STEP: analogWrite/step1

\\START: Overriding TDD Pins internally

```

SPIWrite 0014,04,0,7    //PAGE: TIMING_CON=0x1;(Meaning: );      Address(0x14[2:2],)
SPIWrite 0124,01,0,7    //use_reg_txon_AB=0x1;      Address(0x124[0:0],)
SPIWrite 0126,01,0,7    //use_reg_rxon_AB=0x1;      Address(0x124[16:16],)
SPIWrite 0128,01,0,7    //use_reg_fbon_AB=0x1;      Address(0x128[0:0],)
SPIWrite 012a,01,0,7    //use_reg_txon_CD=0x1;      Address(0x128[16:16],)
SPIWrite 012c,01,0,7    //use_reg_rxon_CD=0x1;      Address(0x12c[0:0],)
SPIWrite 012e,01,0,7    //use_reg_fbon_CD=0x1;      Address(0x12c[16:16],)
SPIWrite 0125,00,0,7    //reg_for_txon_AB=0x0;      Address(0x124[8:8],)
SPIWrite 0127,01,0,7    //reg_for_rxon_AB=0x1;      Address(0x124[24:24],)
SPIWrite 0129,00,0,7    //reg_for_fbon_AB=0x0;      Address(0x128[8:8],)
SPIWrite 012b,00,0,7    //reg_for_txon_CD=0x0;      Address(0x128[24:24],)
SPIWrite 012d,01,0,7    //reg_for_rxon_CD=0x1;      Address(0x12c[8:8],)
SPIWrite 012f,00,0,7    //reg_for_fbon_CD=0x0;      Address(0x12c[24:24],)

```

\\END: Done overriding TDD Pins internally

\\START: Doing RX ADC Analog Writes

```

SPIWrite 0014,00,2,2    //PAGE: TIMING_CON=0x0;(Meaning: );      Address(0x14[2:2],)
SPIWrite 0011,01,0,3    //PAGE: rx_ec_i=0x1;      Address(0x11[3:0],)

```

```

SPIWrite 04a0,0c,0,0
SPIWrite 0011,00,0,3 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0011,10,4,7 //PAGE: rx_ec_q=0x1; Address(0x11[7:4],)
SPIWrite 04a0,0c,0,0
SPIWrite 0011,00,4,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0011,02,0,3 //PAGE: rx_ec_i=0x2; Address(0x11[3:0],)
SPIWrite 04a0,0c,0,0
SPIWrite 0011,00,0,3 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0011,20,4,7 //PAGE: rx_ec_q=0x2; Address(0x11[7:4],)
SPIWrite 04a0,0c,0,0
SPIWrite 0011,00,4,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0011,04,0,3 //PAGE: rx_ec_i=0x4; Address(0x11[3:0],)
SPIWrite 04a0,0c,0,0
SPIWrite 0011,00,0,3 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0011,40,4,7 //PAGE: rx_ec_q=0x4; Address(0x11[7:4],)
SPIWrite 04a0,0c,0,0
SPIWrite 0011,00,4,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0011,08,0,3 //PAGE: rx_ec_i=0x8; Address(0x11[3:0],)
SPIWrite 04a0,0c,0,0
SPIWrite 0011,00,0,3 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0011,80,4,7 //PAGE: rx_ec_q=0x8; Address(0x11[7:4],)
SPIWrite 04a0,0c,0,0
SPIWrite 0011,00,0,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0011,0f,0,7 //PAGE: rx_ec_i=0xf; Address(0x11[3:0],)
SPIWrite 0011,ff,0,7
SPIWrite 029d,03,0,7
SPIWrite 029d,1b,0,7
SPIWrite 029e,00,0,7
SPIWrite 029d,db,0,7
SPIWrite 0299,03,0,7
SPIWrite 029e,30,0,7
SPIWrite 029f,0c,0,7
SPIWrite 029f,6c,0,7
SPIWrite 02a0,03,0,7
SPIWrite 029e,30,0,7
SPIWrite 029f,6d,0,7
SPIWrite 02a0,13,0,7
SPIWrite 0284,00,0,7
SPIWrite 0281,00,0,7
SPIWrite 0284,40,0,7
SPIWrite 0338,2b,0,7
SPIWrite 0111,09,0,7
SPIWrite 0011,00,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)

```

\\START: Doing RX IMD vs DSA improvement Analog Writes

```

SPIWrite 0011,0f,0,7 //PAGE: rx_ec_i=0xf; Address(0x11[3:0],)
SPIWrite 0011,0f,0,7
SPIWrite 0b33,00,0,7
SPIWrite 0b32,00,0,7
SPIWrite 0b33,08,0,7
SPIWrite 0c91,20,0,7
SPIWrite 0011,00,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)

```

\\END: Completed RX IMD vs DSA improvement Analog Writes

```

SPIWrite 0011,0f,0,7 //PAGE: rx_ec_i=0xf; Address(0x11[3:0],)
SPIWrite 0500,03,0,7
SPIWrite 0500,03,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0011,f0,0,7 //PAGE: rx_ec_q=0xf; Address(0x11[7:4],)
SPIWrite 0500,03,0,7
SPIWrite 0500,03,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0011,0f,0,7 //PAGE: rx_ec_i=0xf; Address(0x11[3:0],)
SPIWrite 0500,03,0,7
SPIWrite 0500,03,0,7

```

```
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,f0,0,7    //PAGE: rx_ec_q=0xf;    Address(0x11[7:4],)
SPIWrite 0500,03,0,7
SPIWrite 0500,03,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,0f,0,7    //PAGE: rx_ec_i=0xf;    Address(0x11[3:0],)
SPIWrite 0c70,08,0,7
SPIWrite 0c70,18,0,7
SPIWrite 0103,80,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,10,0,7    //PAGE: rx_ec_q=0x1;    Address(0x11[7:4],)
SPIWrite 0c74,02,0,7
SPIWrite 0103,80,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,01,0,7    //PAGE: rx_ec_i=0x1;    Address(0x11[3:0],)
SPIWrite 049f,00,0,7
SPIWrite 049e,00,0,7
SPIWrite 049f,04,0,7
SPIWrite 049e,01,0,7
SPIWrite 049d,00,0,7
SPIWrite 049c,01,0,7
SPIWrite 049c,00,0,7
SPIWrite 049d,00,0,7
SPIWrite 04a2,00,0,7
SPIWrite 04a2,01,0,7
SPIWrite 04a2,00,0,7
SPIWrite 049c,01,0,7
```

WAIT 0.01

```
SPIWrite 049c,00,0,7
```

WAIT 0.05

```
SPIWrite 049d,02,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,10,0,7    //PAGE: rx_ec_q=0x1;    Address(0x11[7:4],)
SPIWrite 049f,00,0,7
SPIWrite 049e,00,0,7
SPIWrite 049f,04,0,7
SPIWrite 049e,01,0,7
SPIWrite 049d,00,0,7
SPIWrite 049c,01,0,7
SPIWrite 049c,00,0,7
SPIWrite 049d,00,0,7
SPIWrite 04a2,00,0,7
SPIWrite 04a2,01,0,7
SPIWrite 04a2,00,0,7
SPIWrite 049c,01,0,7
```

WAIT 0.01

```
SPIWrite 049c,00,0,7
```

WAIT 0.05

```
SPIWrite 049d,02,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,02,0,7    //PAGE: rx_ec_i=0x2;    Address(0x11[3:0],)
SPIWrite 049f,00,0,7
SPIWrite 049e,00,0,7
SPIWrite 049f,04,0,7
SPIWrite 049e,01,0,7
SPIWrite 049d,00,0,7
SPIWrite 049c,01,0,7
SPIWrite 049c,00,0,7
SPIWrite 049d,00,0,7
SPIWrite 04a2,00,0,7
SPIWrite 04a2,01,0,7
```

SPIWrite 04a2,00,0,7
SPIWrite 049c,01,0,7

WAIT 0.01

SPIWrite 049c,00,0,7

WAIT 0.05

SPIWrite 049d,02,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0011,20,0,7 //PAGE: rx_ec_q=0x2; Address(0x11[7:4],)
SPIWrite 049f,00,0,7
SPIWrite 049e,00,0,7
SPIWrite 049f,04,0,7
SPIWrite 049e,01,0,7
SPIWrite 049d,00,0,7
SPIWrite 049c,01,0,7
SPIWrite 049c,00,0,7
SPIWrite 049d,00,0,7
SPIWrite 04a2,00,0,7
SPIWrite 04a2,01,0,7
SPIWrite 04a2,00,0,7
SPIWrite 049c,01,0,7

WAIT 0.01

SPIWrite 049c,00,0,7

WAIT 0.05

SPIWrite 049d,02,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0011,04,0,7 //PAGE: rx_ec_i=0x4; Address(0x11[3:0],)
SPIWrite 049f,00,0,7
SPIWrite 049e,00,0,7
SPIWrite 049f,04,0,7
SPIWrite 049e,01,0,7
SPIWrite 049d,00,0,7
SPIWrite 049c,01,0,7
SPIWrite 049c,00,0,7
SPIWrite 049d,00,0,7
SPIWrite 04a2,00,0,7
SPIWrite 04a2,01,0,7
SPIWrite 04a2,00,0,7
SPIWrite 049c,01,0,7

WAIT 0.01

SPIWrite 049c,00,0,7

WAIT 0.05

SPIWrite 049d,02,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0011,40,0,7 //PAGE: rx_ec_q=0x4; Address(0x11[7:4],)
SPIWrite 049f,00,0,7
SPIWrite 049e,00,0,7
SPIWrite 049f,04,0,7
SPIWrite 049e,01,0,7
SPIWrite 049d,00,0,7
SPIWrite 049c,01,0,7
SPIWrite 049c,00,0,7
SPIWrite 049d,00,0,7
SPIWrite 04a2,00,0,7
SPIWrite 04a2,01,0,7
SPIWrite 04a2,00,0,7
SPIWrite 049c,01,0,7

WAIT 0.01

SPIWrite 049c,00,0,7

WAIT 0.05

SPIWrite 049d,02,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0011,08,0,7 //PAGE: rx_ec_i=0x8; Address(0x11[3:0],)
SPIWrite 049f,00,0,7
SPIWrite 049e,00,0,7
SPIWrite 049f,04,0,7
SPIWrite 049e,01,0,7
SPIWrite 049d,00,0,7
SPIWrite 049c,01,0,7
SPIWrite 049c,00,0,7
SPIWrite 049d,00,0,7
SPIWrite 04a2,00,0,7
SPIWrite 04a2,01,0,7
SPIWrite 04a2,00,0,7
SPIWrite 049c,01,0,7

WAIT 0.01

SPIWrite 049c,00,0,7

WAIT 0.05

SPIWrite 049d,02,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0011,80,0,7 //PAGE: rx_ec_q=0x8; Address(0x11[7:4],)
SPIWrite 049f,00,0,7
SPIWrite 049e,00,0,7
SPIWrite 049f,04,0,7
SPIWrite 049e,01,0,7
SPIWrite 049d,00,0,7
SPIWrite 049c,01,0,7
SPIWrite 049c,00,0,7
SPIWrite 049d,00,0,7
SPIWrite 04a2,00,0,7
SPIWrite 04a2,01,0,7
SPIWrite 04a2,00,0,7
SPIWrite 049c,01,0,7

WAIT 0.01

SPIWrite 049c,00,0,7

WAIT 0.05

SPIWrite 049d,02,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0011,0f,0,7 //PAGE: rx_ec_i=0xf; Address(0x11[3:0],)
SPIWrite 0500,02,0,7
SPIWrite 0500,00,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0011,f0,0,7 //PAGE: rx_ec_q=0xf; Address(0x11[7:4],)
SPIWrite 0500,02,0,7
SPIWrite 0500,00,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0011,0f,0,7 //PAGE: rx_ec_i=0xf; Address(0x11[3:0],)
SPIWrite 0500,00,0,7
SPIWrite 0500,00,0,7
SPIWrite 050a,01,0,7
SPIWrite 0502,01,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0011,f0,0,7 //PAGE: rx_ec_q=0xf; Address(0x11[7:4],)
SPIWrite 0500,00,0,7
SPIWrite 0500,00,0,7

```

SPIWrite 050a,01,0,7
SPIWrite 0502,01,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0011,0f,0,7 //PAGE: rx_ec_i=0xf; Address(0x11[3:0],)
SPIWrite 0c70,10,0,7
SPIWrite 0c70,00,0,7
SPIWrite 0103,00,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0011,10,0,7 //PAGE: rx_ec_q=0x1; Address(0x11[7:4],)
SPIWrite 0c74,00,0,7
SPIWrite 0103,00,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0011,01,0,7 //PAGE: rx_ec_i=0x1; Address(0x11[3:0],)
SPIWrite 0103,70,0,7
SPIWrite 01a1,04,0,7
SPIWrite 0112,05,0,7
SPIWrite 0bf3,03,0,7
SPIWrite 0101,02,0,7
SPIWrite 0100,28,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0011,10,0,7 //PAGE: rx_ec_q=0x1; Address(0x11[7:4],)
SPIWrite 0103,70,0,7
SPIWrite 01a1,04,0,7
SPIWrite 0112,05,0,7
SPIWrite 0101,02,0,7
SPIWrite 0100,28,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0011,02,0,7 //PAGE: rx_ec_i=0x2; Address(0x11[3:0],)
SPIWrite 0103,70,0,7
SPIWrite 01a1,04,0,7
SPIWrite 0112,05,0,7
SPIWrite 0bf3,03,0,7
SPIWrite 0101,02,0,7
SPIWrite 0100,28,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0010,04,0,7 //PAGE: rx_top=0x1; Address(0x10[3:2],)
SPIWrite 0c10,05,0,7 //nl_corr_complete_byp=0x1; (Meaning: ); Address(0xc10[0:0],)
SPIWrite 0c11,01,0,7 //coef_update_pulse_nl=0x1; Address(0xc10[8:8],)

```

WAIT 0.1

```

SPIWrite 0c11,00,0,7 //coef_update_pulse_nl=0x0; Address(0xc10[8:8],)
SPIWrite 0e10,05,0,7 //nl_corr_complete_byp=0x1; (Meaning: ); Address(0xe10[0:0],)
SPIWrite 0e11,01,0,7 //coef_update_pulse_nl=0x1; Address(0xe10[8:8],)

```

WAIT 0.1

```

SPIWrite 0e11,00,0,7 //coef_update_pulse_nl=0x0; Address(0xe10[8:8],)
SPIWrite 0010,00,0,7 //PAGE: rx_top=0x0; Address(0x10[3:2],)
SPIWrite 0011,04,0,7 //PAGE: rx_ec_i=0x4; Address(0x11[3:0],)
SPIWrite 0103,70,0,7
SPIWrite 01a1,04,0,7
SPIWrite 0112,05,0,7
SPIWrite 0bf3,03,0,7
SPIWrite 0101,02,0,7
SPIWrite 0100,28,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0011,40,0,7 //PAGE: rx_ec_q=0x4; Address(0x11[7:4],)
SPIWrite 0103,70,0,7
SPIWrite 01a1,04,0,7
SPIWrite 0112,05,0,7
SPIWrite 0101,02,0,7

```

```

SPIWrite 0100,28,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0011,08,0,7 //PAGE: rx_ec_i=0x8; Address(0x11[3:0],)
SPIWrite 0103,70,0,7
SPIWrite 01a1,04,0,7
SPIWrite 0112,05,0,7
SPIWrite 0bf3,03,0,7
SPIWrite 0101,02,0,7
SPIWrite 0100,28,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0011,80,0,7 //PAGE: rx_ec_q=0x8; Address(0x11[7:4],)
SPIWrite 0103,70,0,7
SPIWrite 01a1,04,0,7
SPIWrite 0112,05,0,7
SPIWrite 0101,02,0,7
SPIWrite 0100,28,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0010,08,0,7 //PAGE: rx_top=0x2; Address(0x10[3:2],)
SPIWrite 0c10,05,0,7 //nl_corr_complete_byp=0x1; (Meaning: ); Address(0xc10[0:0],)
SPIWrite 0c11,01,0,7 //coef_update_pulse_nl=0x1; Address(0xc10[8:8],)

```

WAIT 0.1

```

SPIWrite 0c11,00,0,7 //coef_update_pulse_nl=0x0; Address(0xc10[8:8],)
SPIWrite 0e10,05,0,7 //nl_corr_complete_byp=0x1; (Meaning: ); Address(0xe10[0:0],)
SPIWrite 0e11,01,0,7 //coef_update_pulse_nl=0x1; Address(0xe10[8:8],)

```

WAIT 0.1

```

SPIWrite 0e11,00,0,7 //coef_update_pulse_nl=0x0; Address(0xe10[8:8],)
SPIWrite 0010,00,0,7 //PAGE: rx_top=0x0; Address(0x10[3:2],)
SPIWrite 0012,0f,0,7 //PAGE: rx_ec_common=0xf; Address(0x12[3:0],)
SPIWrite 04c4,20,0,7
SPIWrite 0012,00,0,7 //PAGE: rx_ec_common=0x0; Address(0x12[3:0],)
SPIWrite 0014,01,0,7 //PAGE: clktop_2t=0x1; Address(0x14[1:0],)
SPIWrite 006b,10,0,7 //MASK_PDN_SYNC_RXCML_R=0x1; Address(0x68[28:28],)
SPIWrite 006b,18,0,7 //MASK_PDN_SYNC_RXCML_L=0x1; Address(0x68[27:27],)
SPIWrite 0014,00,0,7 //PAGE: clktop_2t=0x0; Address(0x14[1:0],)
SPIWrite 0011,f0,0,7 //PAGE: rx_ec_q=0xf; Address(0x11[7:4],)
SPIWrite 0293,00,0,7
SPIWrite 0b93,ec,0,7
SPIWrite 0b85,8d,0,7
SPIWrite 0b93,ec,0,7
SPIWrite 0b92,65,0,7
SPIWrite 0b91,cd,0,7
SPIWrite 0b95,1c,0,7
SPIWrite 0b94,e0,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0016,10,0,7 //PAGE: dsa=0x1; Address(0x16[5:4],)
SPIWrite 0180,00,0,7
SPIWrite 0016,20,0,7 //PAGE: dsa=0x2; Address(0x16[5:4],)
SPIWrite 0180,00,0,7

```

\\END: Completed RX ADC Analog Writes

```

SPIWrite 0016,00,0,7 //PAGE: dsa=0x0; Address(0x16[5:4],)
\\ STEP: analogWrite/step2

```

\\START: Overriding TDD Pins internally

```

SPIWrite 0014,04,0,7 //PAGE: TIMING_CON=0x1; (Meaning: ); Address(0x14[2:2],)
SPIWrite 0124,01,0,7 //use_reg_txon_AB=0x1; Address(0x124[0:0],)
SPIWrite 0126,01,0,7 //use_reg_rxon_AB=0x1; Address(0x124[16:16],)
SPIWrite 0128,01,0,7 //use_reg_fbon_AB=0x1; Address(0x128[0:0],)
SPIWrite 012a,01,0,7 //use_reg_txon_CD=0x1; Address(0x128[16:16],)
SPIWrite 012c,01,0,7 //use_reg_rxon_CD=0x1; Address(0x12c[0:0],)
SPIWrite 012e,01,0,7 //use_reg_fbon_CD=0x1; Address(0x12c[16:16],)
SPIWrite 0125,00,0,7 //reg_for_txon_AB=0x0; Address(0x124[8:8],)
SPIWrite 0127,00,0,7 //reg_for_rxon_AB=0x0; Address(0x124[24:24],)

```

```
SPIWrite 0129,01,0,7    //reg_for_fbon_AB=0x1;  Address(0x128[8:8],)
SPIWrite 012b,00,0,7    //reg_for_txon_CD=0x0;  Address(0x128[24:24],)
SPIWrite 012d,00,0,7    //reg_for_rxon_CD=0x0;  Address(0x12c[8:8],)
SPIWrite 012f,01,0,7    //reg_for_fbon_CD=0x1;  Address(0x12c[24:24],)
```

\\END: Done overriding TDD Pins internally

\\START: Doing FB ADC Analog Writes

```
SPIWrite 0014,00,2,2    //PAGE: TIMING_CON=0x0;(Meaning: );      Address(0x14[2:2],)
SPIWrite 0010,10,4,4    //PAGE: fb_ec=0x1;  Address(0x10[4:4],0x10[6:6],)
SPIWrite 0010,10,6,6
SPIWrite 00b0,03,1,1
SPIWrite 0188,09,3,3
SPIWrite 0140,28,3,3
SPIWrite 0138,28,3,3
SPIWrite 0190,09,3,3
SPIWrite 0168,39,3,3
SPIWrite 0160,39,3,3
SPIWrite 0119,32,0,3
SPIWrite 0121,32,0,3
SPIWrite 0129,32,0,3
SPIWrite 0131,32,0,3
SPIWrite 0119,32,0,3
SPIWrite 0121,32,0,3
SPIWrite 0129,32,0,3
SPIWrite 0131,32,0,3
SPIWrite 0010,00,4,4    //PAGE: fb_ec=0x0;  Address(0x10[4:4],0x10[6:6],)
SPIWrite 0010,00,6,6
SPIWrite 0010,20,5,5    //PAGE: fb_ana=0x1;      Address(0x10[5:5],0x10[7:7],)
SPIWrite 0010,20,7,7
SPIWrite 0085,08,2,4
SPIWrite 0102,08,3,3
SPIWrite 0010,00,5,5    //PAGE: fb_ana=0x0;      Address(0x10[5:5],0x10[7:7],)
SPIWrite 0010,00,7,7
SPIWrite 0010,00,4,4    //PAGE: fb_ec=0x2;  Address(0x10[4:4],0x10[6:6],)
SPIWrite 0010,40,6,6
SPIWrite 00b0,03,1,1
SPIWrite 0188,09,3,3
SPIWrite 0140,28,3,3
SPIWrite 0138,28,3,3
SPIWrite 0190,09,3,3
SPIWrite 0168,39,3,3
SPIWrite 0160,39,3,3
SPIWrite 0119,32,0,3
SPIWrite 0121,32,0,3
SPIWrite 0129,32,0,3
SPIWrite 0131,32,0,3
SPIWrite 0119,32,0,3
SPIWrite 0121,32,0,3
SPIWrite 0129,32,0,3
SPIWrite 0131,32,0,3
SPIWrite 0010,40,4,4    //PAGE: fb_ec=0x0;  Address(0x10[4:4],0x10[6:6],)
SPIWrite 0010,00,6,6
SPIWrite 0010,00,5,5    //PAGE: fb_ana=0x2;      Address(0x10[5:5],0x10[7:7],)
SPIWrite 0010,80,7,7
SPIWrite 0085,08,2,4
SPIWrite 0102,08,3,3
SPIWrite 0010,80,5,5    //PAGE: fb_ana=0x0;      Address(0x10[5:5],0x10[7:7],)
SPIWrite 0010,00,7,7
SPIWrite 0017,10,4,5    //PAGE: dac_2t=0x1;      Address(0x17[5:4],)
SPIWrite 002e,04,2,2
SPIWrite 0017,20,4,5    //PAGE: dac_2t=0x2;      Address(0x17[5:4],)
SPIWrite 002e,04,2,2
SPIWrite 0017,00,4,5    //PAGE: dac_2t=0x0;      Address(0x17[5:4],)
SPIWrite 0017,40,6,7    //PAGE: ana_2r=0x1;      Address(0x17[7:6],)
SPIWrite 003f,20,3,5
SPIWrite 003f,26,1,2
```

```

SPIWrite 0017,80,6,7 //PAGE: ana_2r=0x2; Address(0x17[7:6],)
SPIWrite 003f,20,3,5
SPIWrite 003f,26,1,2
SPIWrite 0017,00,6,7 //PAGE: ana_2r=0x0; Address(0x17[7:6],)
SPIWrite 0010,20,5,5 //PAGE: fb_ana=0x1; Address(0x10[5:5],0x10[7:7],)
SPIWrite 0010,20,7,7
SPIWrite 0080,10,4,4
SPIWrite 0080,18,3,3
SPIWrite 009a,01,0,0
SPIWrite 0095,01,0,0
SPIWrite 0094,c0,6,7
SPIWrite 0010,00,5,5 //PAGE: fb_ana=0x0; Address(0x10[5:5],0x10[7:7],)
SPIWrite 0010,00,7,7
SPIWrite 0010,10,4,4 //PAGE: fb_ec=0x1; Address(0x10[4:4],0x10[6:6],)
SPIWrite 0010,10,6,6
SPIWrite 0150,31,0,0
SPIWrite 0150,31,4,4
SPIWrite 0150,31,5,5
SPIWrite 0108,22,0,0
SPIWrite 0108,22,5,5
SPIWrite 0150,b1,7,7
SPIWrite 025e,40,0,7
SPIWrite 025d,00,7,7
SPIWrite 0028,a1,0,0
SPIWrite 0028,a0,0,0
SPIWrite 00a2,00,0,5
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a2,00,0,5
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0010,00,4,4 //PAGE: fb_ec=0x0; Address(0x10[4:4],0x10[6:6],)
SPIWrite 0010,00,6,6
SPIWrite 0010,00,5,5 //PAGE: fb_ana=0x2; Address(0x10[5:5],0x10[7:7],)
SPIWrite 0010,80,7,7
SPIWrite 0080,10,4,4
SPIWrite 0080,18,3,3
SPIWrite 009a,01,0,0
SPIWrite 0095,01,0,0
SPIWrite 0094,c0,6,7
SPIWrite 0010,80,5,5 //PAGE: fb_ana=0x0; Address(0x10[5:5],0x10[7:7],)
SPIWrite 0010,00,7,7
SPIWrite 0010,00,4,4 //PAGE: fb_ec=0x2; Address(0x10[4:4],0x10[6:6],)
SPIWrite 0010,40,6,6
SPIWrite 0150,31,0,0
SPIWrite 0150,31,4,4
SPIWrite 0150,31,5,5
SPIWrite 0108,22,0,0
SPIWrite 0108,22,5,5
SPIWrite 0150,b1,7,7
SPIWrite 025e,40,0,7
SPIWrite 025d,00,7,7
SPIWrite 0028,a1,0,0
SPIWrite 0028,a0,0,0
SPIWrite 00a2,00,0,5
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a2,00,0,5
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0010,40,4,4 //PAGE: fb_ec=0x0; Address(0x10[4:4],0x10[6:6],)
SPIWrite 0010,00,6,6
SPIWrite 0013,10,4,4 //PAGE: customer_macro=0x1; (Meaning: ); Address(0x13[4:4],)
SPIWrite 00a3,00,0,7
SPIWrite 00a2,01,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,14,0,7

```

\\START: Enabling/Disabling Temp Sensor

```
SPIWrite 0013,00,0,7 //PAGE: customer_macro=0x0;(Meaning: ); Address(0x13[4:4],)
SPIWrite 0015,80,0,7 //PAGE: DIGTOP_MISC=0x1;(Meaning: ); Address(0x15[7:7],)
SPIWrite 03a3,08,0,7 //temp_sense1_sel_input=0x1;(Meaning: ); Address(0x3a0[27:27],)
SPIWrite 03a0,02,0,7 //temp_sense1_en=0x1; Address(0x3a0[1:1],)
SPIWrite 03a0,02,0,7 //temp_sense1_soft_reset=0x0; Address(0x3a0[0:0],)
SPIWrite 03a0,0e,0,7 //temp_sense1_div1=0x3;(Meaning: ); Address(0x3a0[3:2],)
SPIWrite 03a0,3e,0,7 //temp_sense1_div2=0x3;(Meaning: ); Address(0x3a0[5:4],)
SPIWrite 03a0,7e,0,7 //temp_sense1_analog_powerup=0x1;(Meaning: ); Address(0x3a0[6:6],)
SPIWrite 0722,02,0,7 //temp_sense_25m_clock_ungate=0x1;(Meaning: ); Address(0x720[17:17],)
```

\\END: Done enabling/Disabling Temp Sensor

\\END: Completed FB ADC Analog Writes

```
SPIWrite 0015,00,0,7 //PAGE: DIGTOP_MISC=0x0;(Meaning: ); Address(0x15[7:7],)
\\ STEP: analogWrite/step3
```

\\START: Doing Writes to support AB and CD independent TDD

```
SPIWrite 0011,10,0,7 //PAGE: rx_ec_q=0x1; Address(0x11[7:4],)
SPIWrite 0f05,01,0,7
SPIWrite 0f05,05,0,7
SPIWrite 0c75,01,0,7
SPIWrite 0c75,03,0,7
SPIWrite 0c75,83,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0017,01,0,7 //PAGE: dac_1t=0x1; Address(0x17[3:0],)
SPIWrite 0057,39,0,7
SPIWrite 006d,47,0,7
SPIWrite 0050,04,0,7
SPIWrite 0017,00,0,7 //PAGE: dac_1t=0x0; Address(0x17[3:0],)
SPIWrite 0011,01,0,7 //PAGE: rx_ec_i=0x1; Address(0x11[3:0],)
SPIWrite 0c73,80,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0011,20,0,7 //PAGE: rx_ec_q=0x2; Address(0x11[7:4],)
SPIWrite 0f05,01,0,7
SPIWrite 0f05,05,0,7
SPIWrite 0c75,01,0,7
SPIWrite 0c75,03,0,7
SPIWrite 0c75,83,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0017,02,0,7 //PAGE: dac_1t=0x2; Address(0x17[3:0],)
SPIWrite 0057,39,0,7
SPIWrite 006d,47,0,7
SPIWrite 0050,04,0,7
SPIWrite 0017,00,0,7 //PAGE: dac_1t=0x0; Address(0x17[3:0],)
SPIWrite 0011,02,0,7 //PAGE: rx_ec_i=0x2; Address(0x11[3:0],)
SPIWrite 0c73,80,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0011,40,0,7 //PAGE: rx_ec_q=0x4; Address(0x11[7:4],)
SPIWrite 0f05,01,0,7
SPIWrite 0f05,05,0,7
SPIWrite 0c75,01,0,7
SPIWrite 0c75,03,0,7
SPIWrite 0c75,83,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0017,04,0,7 //PAGE: dac_1t=0x4; Address(0x17[3:0],)
SPIWrite 0057,39,0,7
SPIWrite 006d,47,0,7
SPIWrite 0050,04,0,7
SPIWrite 0017,00,0,7 //PAGE: dac_1t=0x0; Address(0x17[3:0],)
SPIWrite 0011,04,0,7 //PAGE: rx_ec_i=0x4; Address(0x11[3:0],)
SPIWrite 0c73,80,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0011,80,0,7 //PAGE: rx_ec_q=0x8; Address(0x11[7:4],)
SPIWrite 0f05,01,0,7
```

```

SPIWrite 0f05,05,0,7
SPIWrite 0c75,01,0,7
SPIWrite 0c75,03,0,7
SPIWrite 0c75,83,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0017,08,0,7 //PAGE: dac_1t=0x8; Address(0x17[3:0],)
SPIWrite 0057,39,0,7
SPIWrite 006d,47,0,7
SPIWrite 0050,04,0,7
SPIWrite 0017,00,0,7 //PAGE: dac_1t=0x0; Address(0x17[3:0],)
SPIWrite 0011,08,0,7 //PAGE: rx_ec_i=0x8; Address(0x11[3:0],)
SPIWrite 0c73,80,0,7
SPIWrite 0011,00,0,7 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0014,01,0,7 //PAGE: clktop_2t=0x1; Address(0x14[1:0],)
SPIWrite 006b,38,0,7 //MASK_PDN_SYNC_CROSS31=0x1; Address(0x68[29:29],)
SPIWrite 006b,38,0,7 //MASK_PDN_SYNC_RXCML_R=0x1; Address(0x68[28:28],)
SPIWrite 006b,38,0,7 //MASK_PDN_SYNC_RXCML_L=0x1; Address(0x68[27:27],)
SPIWrite 006b,3c,0,7 //MASK_PDN_FAST_RXCML_R=0x1; Address(0x68[26:26],)
SPIWrite 006b,3e,0,7 //MASK_PDN_FAST_RXCML_L=0x1; Address(0x68[25:25],)
SPIWrite 006b,3f,0,7 //MASK_PDN_FAST_PLL13_CROSS_OUT=0x1; Address(0x68[24:24],)
SPIWrite 006c,3e,0,7 //MASK_PDN_SYNC_CROSS13=0x1; Address(0x6c[5:5],)
SPIWrite 006c,3e,0,7 //MASK_PDN_SYNC_TXCML_R=0x1; Address(0x6c[4:4],)
SPIWrite 006c,3e,0,7 //MASK_PDN_SYNC_TXCML_L=0x1; Address(0x6c[3:3],)
SPIWrite 006c,3e,0,7 //MASK_PDN_FAST_TXCML_R=0x1; Address(0x6c[2:2],)
SPIWrite 006c,3e,0,7 //MASK_PDN_FAST_TXCML_L=0x1; Address(0x6c[1:1],)
SPIWrite 006c,3f,0,7 //MASK_PDN_FAST_PLL31_CROSS_OUT=0x1; Address(0x6c[0:0],)
SPIWrite 006f,10,0,7 //MASK_PDN_FAST_DCCLKROUTE_FBAB=0x1; Address(0x6c[28:28],)
SPIWrite 006f,14,0,7 //MASK_PDN_FAST_DCCLKROUTE_RXAB=0x1; Address(0x6c[26:26],)
SPIWrite 006f,15,0,7 //MASK_PDN_FAST_DCCLKROUTE_TXAB=0x1; Address(0x6c[24:24],)
SPIWrite 006f,35,0,7 //MASK_PDN_FAST_DCCLKROUTE_FBCD=0x1; Address(0x6c[29:29],)
SPIWrite 006f,3d,0,7 //MASK_PDN_FAST_DCCLKROUTE_RXCD=0x1; Address(0x6c[27:27],)
SPIWrite 006f,3f,0,7 //MASK_PDN_FAST_DCCLKROUTE_TXCD=0x1; Address(0x6c[25:25],)
SPIWrite 0014,00,0,7 //PAGE: clktop_2t=0x0; Address(0x14[1:0],)
SPIWrite 0017,20,0,7 //PAGE: dac_2t=0x2; Address(0x17[5:4],)
SPIWrite 002a,08,0,7
SPIWrite 0017,10,0,7 //PAGE: dac_2t=0x1; Address(0x17[5:4],)
SPIWrite 002a,08,0,7
SPIWrite 0017,20,0,7 //PAGE: dac_2t=0x2; Address(0x17[5:4],)
SPIWrite 002a,48,0,7
SPIWrite 0017,10,0,7 //PAGE: dac_2t=0x1; Address(0x17[5:4],)
SPIWrite 002a,48,0,7

```

\\END: Completed writes to support AB and CD independent TDD

```

SPIWrite 0017,00,0,7 //PAGE: dac_2t=0x0; Address(0x17[5:4],)
SPIWrite 0013,10,0,7 //PAGE: customer_macro=0x1; (Meaning: ); Address(0x13[4:4],)

```

SPIPoll 00f0,0,0,1

```

SPIWrite 00a3,00,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,18,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,07,0,7
SPIWrite 00a6,04,0,7
SPIWrite 00a5,02,0,7
SPIWrite 00a4,00,0,7
SPIWrite 00ab,00,0,7
SPIWrite 00aa,00,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00a8,00,0,7
SPIWrite 0193,12,0,7

```

SPIPoll 00f0,0,7,7

```

SPIWrite 0013,00,4,4 //PAGE: customer_macro=0x0; (Meaning: ); Address(0x13[4:4],)
SPIWrite 0011,10,4,7 //PAGE: rx_ec_q=0x1; Address(0x11[7:4],)
SPIWrite 0281,80,7,7
SPIWrite 0284,40,6,6

```

```

SPIWrite 0284,c0,7,7
SPIWrite 0334,30,6,7
SPIWrite 0335,3c,0,2
SPIWrite 0011,00,4,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0011,01,0,3 //PAGE: rx_ec_i=0x1; Address(0x11[3:0],)
SPIWrite 0335,3c,0,2
SPIWrite 0281,80,7,7
SPIWrite 0284,40,6,6
SPIWrite 0284,c0,7,7
SPIWrite 0334,32,6,7
SPIWrite 0011,00,0,3 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0012,01,0,3 //PAGE: rx_ec_common=0x1; Address(0x12[3:0],)
SPIWrite 028a,80,7,7
SPIWrite 0012,00,0,3 //PAGE: rx_ec_common=0x0; Address(0x12[3:0],)
SPIWrite 0011,20,4,7 //PAGE: rx_ec_q=0x2; Address(0x11[7:4],)
SPIWrite 0281,80,7,7
SPIWrite 0284,40,6,6
SPIWrite 0284,c0,7,7
SPIWrite 0334,32,6,7
SPIWrite 0335,3c,0,2
SPIWrite 0011,00,4,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0011,02,0,3 //PAGE: rx_ec_i=0x2; Address(0x11[3:0],)
SPIWrite 0335,3c,0,2
SPIWrite 0281,80,7,7
SPIWrite 0284,40,6,6
SPIWrite 0284,c0,7,7
SPIWrite 0334,31,6,7
SPIWrite 0011,00,0,3 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0012,02,0,3 //PAGE: rx_ec_common=0x2; Address(0x12[3:0],)
SPIWrite 028a,80,7,7
SPIWrite 0012,00,0,3 //PAGE: rx_ec_common=0x0; Address(0x12[3:0],)
SPIWrite 0011,40,4,7 //PAGE: rx_ec_q=0x4; Address(0x11[7:4],)
SPIWrite 0281,80,7,7
SPIWrite 0284,40,6,6
SPIWrite 0284,c0,7,7
SPIWrite 0334,31,6,7
SPIWrite 0335,3c,0,2
SPIWrite 0011,00,4,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0011,04,0,3 //PAGE: rx_ec_i=0x4; Address(0x11[3:0],)
SPIWrite 0335,3c,0,2
SPIWrite 0281,80,7,7
SPIWrite 0284,40,6,6
SPIWrite 0284,c0,7,7
SPIWrite 0334,32,6,7
SPIWrite 0011,00,0,3 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0012,04,0,3 //PAGE: rx_ec_common=0x4; Address(0x12[3:0],)
SPIWrite 028a,80,7,7
SPIWrite 0012,00,0,3 //PAGE: rx_ec_common=0x0; Address(0x12[3:0],)
SPIWrite 0011,80,4,7 //PAGE: rx_ec_q=0x8; Address(0x11[7:4],)
SPIWrite 0281,80,7,7
SPIWrite 0284,40,6,6
SPIWrite 0284,c0,7,7
SPIWrite 0334,31,6,7
SPIWrite 0335,3c,0,2
SPIWrite 0011,00,4,7 //PAGE: rx_ec_q=0x0; Address(0x11[7:4],)
SPIWrite 0011,08,0,3 //PAGE: rx_ec_i=0x8; Address(0x11[3:0],)
SPIWrite 0335,3c,0,2
SPIWrite 0281,80,7,7
SPIWrite 0284,40,6,6
SPIWrite 0284,c0,7,7
SPIWrite 0334,31,6,7
SPIWrite 0011,00,0,3 //PAGE: rx_ec_i=0x0; Address(0x11[3:0],)
SPIWrite 0012,08,0,3 //PAGE: rx_ec_common=0x8; Address(0x12[3:0],)
SPIWrite 028a,80,7,7
SPIWrite 0012,00,0,7 //PAGE: rx_ec_common=0x0; Address(0x12[3:0],)
\\ STEP: jesdConfig/step0

```

\\START: Configuring Device JESD TX

```

SPIWrite 0015,01,0,7    //PAGE: rx_jesd=0x1;    Address(0x15[0:0],0x15[4:4],)
SPIWrite 0015,01,0,7
SPIWrite 00b0,04,0,7    //hd_sts_pll_lock_override=0x1;    Address(0xb0[2:2],)
SPIWrite 00b0,0c,0,7    //hd_sts_pll_lock_reg=0x1;    Address(0xb0[3:3],)
SPIWrite 0052,05,0,7    //ddc_bypass_8lanemode_en=0x0;    Address(0x50[20:20],)
SPIWrite 0045,e0,0,7    //init_state=0x1;(Meaning: );    Address(0x44[15:15],)
SPIWrite 0045,e0,0,7    //fifo_init_state=0x1;    Address(0x44[13:13],)
SPIWrite 0045,e0,0,7    //fb_init_state=0x1;(Meaning: );    Address(0x44[14:14],)
SPIWrite 0026,0f,0,7    //jesd_clear_data=0xf;    Address(0x24[19:16],)
SPIWrite 0020,37,0,7    //sysref_jesd_mode=0x1;    Address(0x20[7:5],)
SPIWrite 0020,3f,0,7    //k_m1=0x1f;    Address(0x20[4:0],)
SPIWrite 0021,1f,0,7    //fb_k_m1=0x1f;    Address(0x20[12:8],)
SPIWrite 0043,06,0,7    //jesd_mode=0x6;    Address(0x40[30:24],)
SPIWrite 0044,12,0,7    //fb_jesd_mode=0x12;    Address(0x44[6:0],)
SPIWrite 0076,01,0,7    //adc_jesd_root_clk_div=0x1;    Address(0x74[23:16],)
SPIWrite 00c0,00,0,7    //ddc_rd_clk_ratio_rx1=0x0;    Address(0xc0[4:0],)
SPIWrite 00c0,20,0,7    //ddc_rd_clk_ratio_rx1_override=0x1;    Address(0xc0[5:5],)
SPIWrite 00c1,00,0,7    //ddc_rd_clk_ratio_rx2=0x0;    Address(0xc0[12:8],)
SPIWrite 00c1,20,0,7    //ddc_rd_clk_ratio_rx2_override=0x1;    Address(0xc0[13:13],)
SPIWrite 00c4,00,0,7    //jesd_tx_clk_ratio_rx1=0x0;    Address(0xc4[4:0],)
SPIWrite 00c4,20,0,7    //jesd_tx_clk_ratio_rx1_override=0x1;    Address(0xc4[5:5],)
SPIWrite 00c5,00,0,7    //jesd_tx_clk_ratio_rx2=0x0;    Address(0xc4[12:8],)
SPIWrite 00c5,20,0,7    //jesd_tx_clk_ratio_rx2_override=0x1;    Address(0xc4[13:13],)
SPIWrite 0060,04,0,7    //jesd_system_mode=0x1;    Address(0x60[3:2],)
SPIWrite 0080,01,0,7    //scr_64b_initval=0x1;
Address(0x80[7:0],0x80[15:8],0x80[23:16],0x80[31:24],0x84[7:0],0x84[15:8],0x84[23:16],0x84[25:24],)
SPIWrite 0081,00,0,7
SPIWrite 0082,00,0,7
SPIWrite 0083,00,0,7
SPIWrite 0084,00,0,7
SPIWrite 0085,00,0,7
SPIWrite 0086,00,0,7
SPIWrite 0087,00,0,7
SPIWrite 0088,00,0,7    //scr_64b_en=0x0;    Address(0x88[0:0],)
SPIWrite 004f,00,0,7    //jesd_std_sel=0x0;(Meaning: );    Address(0x4c[25:24],)
SPIWrite 005f,08,0,7    //dedicated_rx_fb_lane_mode=0x1;    Address(0x5c[27:27],)
SPIWrite 00ca,01,0,7    //sample_drop_mode_rx1=0x1;    Address(0xc8[19:16],)
SPIWrite 00ca,11,0,7    //sample_drop_mode_rx2=0x1;    Address(0xc8[23:20],)
SPIWrite 0022,00,0,7    //scr=0x0;(Meaning: );    Address(0x20[16:16],)
SPIWrite 0023,00,0,7    //fb_scr=0x0;(Meaning: );    Address(0x20[24:24],)
SPIWrite 0025,07,0,7    //lane_ena=0x7;    Address(0x24[11:8],)
SPIWrite 0077,04,0,7    //sysref_to_ddc_jesd_clk_div_override=0x1;    Address(0x74[26:26],)
SPIWrite 008f,00,0,7    //init_o_mf_counter=0x0;    Address(0x8c[25:16],)
SPIWrite 008e,00,0,7
SPIWrite 0045,e0,0,7    //init_state=0x1;(Meaning: );    Address(0x44[15:15],)
SPIWrite 0045,e0,0,7    //fifo_init_state=0x1;    Address(0x44[13:13],)
SPIWrite 0045,e0,0,7    //fb_init_state=0x1;(Meaning: );    Address(0x44[14:14],)

```

\\END: Done configuring Device JESD TX

```

SPIWrite 0015,00,0,7    //PAGE: rx_jesd=0x0;    Address(0x15[0:0],0x15[4:4],)
SPIWrite 0015,00,0,7
\\ STEP: jesdConfig/step1

```

\\START: Configuring Device JESD RX

```

SPIWrite 0015,02,0,7    //PAGE: tx_jesd=0x1;    Address(0x15[1:1],0x15[5:5],)
SPIWrite 0015,02,0,7
SPIWrite 007f,1f,0,7    //k_m1=0x1f;    Address(0x7c[31:24],)
SPIWrite 007e,1f,0,7    //rbd_m1=0x1f;    Address(0x7c[23:16],)
SPIWrite 0020,01,0,7    //init_state_tx0=0x1;(Meaning: );    Address(0x20[0:0],)
SPIWrite 0081,ff,0,7    //jesd_clear_data=0xff;    Address(0x80[15:8],)
SPIWrite 0021,01,0,7    //dac_jesd_root_clk_div=0x1;(Meaning: );    Address(0x20[15:8],)
SPIWrite 013d,00,0,7    //duc_wr_clk_ratio_tx0=0x0;(Meaning: );    Address(0x13c[12:8],)
SPIWrite 013f,00,0,7    //jesd_rx_clk_ratio_tx0=0x0;(Meaning: );    Address(0x13c[28:24],)
SPIWrite 0024,07,0,7    //jesd_mode_tx0=0x7;(Meaning: );    Address(0x24[4:0],)
SPIWrite 013d,20,0,7    //duc_wr_clk_ratio_tx0_override=0x1;    Address(0x13c[13:13],)
SPIWrite 013f,20,0,7    //jesd_rx_clk_ratio_tx0_override=0x1;    Address(0x13c[29:29],)

```

```

SPIWrite 002d,9b,0,7 //spi_txenable=0x1; Address(0x2c[8:8],)
SPIWrite 0093,ff,0,7 //spidac=0x7fff; Address(0x90[31:24],0x94[7:0],)
SPIWrite 0094,7f,0,7
SPIWrite 0093,ff,0,7 //spidac=0x7fff; Address(0x90[31:24],0x94[7:0],)
SPIWrite 0094,7f,0,7
SPIWrite 0092,00,0,7 //spidac_ena=0x0; Address(0x90[23:23],)
SPIWrite 0092,00,0,7 //spidac_ena=0x0; Address(0x90[23:23],)
SPIWrite 008b,df,0,7 //sync_request_ena=0xdf; Address(0x88[31:24],)
SPIWrite 008c,00,0,7 //error_ena=0x0; Address(0x8c[7:0],)
SPIWrite 0123,7f,0,7 //comma_align_valid_thresh_tx0=0x7f; Address(0x120[30:24],)
SPIWrite 0148,00,0,7 //jesd_h_ena=0x0; Address(0x148[1:1],)
SPIWrite 0148,00,0,7 //jesd_c_ena=0x0; Address(0x148[0:0],)
SPIWrite 007d,12,0,7 //scr=0x0; Address(0x7c[15:15],)
SPIWrite 007c,0f,0,7 //lane_ena=0xf; Address(0x7c[7:0],)
SPIWrite 0134,04,0,7 //sysref_to_dac_jesd_clk_div_override=0x1; Address(0x134[2:2],)
SPIWrite 0020,01,0,7 //init_state_tx0=0x1;(Meaning: ); Address(0x20[0:0],)
SPIWrite 0173,cc,0,7 //alarms_mask=0x15151515cccc0fff; Address(0x170[31:0],0x174[31:0],)
SPIWrite 0172,cc,0,7
SPIWrite 0171,0f,0,7
SPIWrite 0170,ff,0,7
SPIWrite 0177,15,0,7
SPIWrite 0176,15,0,7
SPIWrite 0175,15,0,7
SPIWrite 0174,15,0,7
SPIWrite 017b,cc,0,7 //alarms_to_pap_mask=0x15151515cccc0fff;
Address(0x178[31:0],0x17c[31:0],)
SPIWrite 017a,cc,0,7
SPIWrite 0179,0f,0,7
SPIWrite 0178,ff,0,7
SPIWrite 017f,15,0,7
SPIWrite 017e,15,0,7
SPIWrite 017d,15,0,7
SPIWrite 017c,15,0,7

```

\\END: Done configuring Device JESD RX

```

SPIWrite 0015,00,0,7 //PAGE: tx_jesd=0x0; Address(0x15[1:1],0x15[5:5],)
SPIWrite 0015,00,0,7
\\ STEP: jesdConfig/step2

```

\\START: Configuring Device JESD TX

```

SPIWrite 0015,00,0,7 //PAGE: rx_jesd=0x2; Address(0x15[0:0],0x15[4:4],)
SPIWrite 0015,10,0,7
SPIWrite 00b0,04,0,7 //hd_sts_pll_lock_override=0x1; Address(0xb0[2:2],)
SPIWrite 00b0,0c,0,7 //hd_sts_pll_lock_reg=0x1; Address(0xb0[3:3],)
SPIWrite 0052,05,0,7 //ddc_bypass_8lanemode_en=0x0; Address(0x50[20:20],)
SPIWrite 0045,e0,0,7 //init_state=0x1;(Meaning: ); Address(0x44[15:15],)
SPIWrite 0045,e0,0,7 //fifo_init_state=0x1; Address(0x44[13:13],)
SPIWrite 0045,e0,0,7 //fb_init_state=0x1;(Meaning: ); Address(0x44[14:14],)
SPIWrite 0026,0f,0,7 //jesd_clear_data=0xf; Address(0x24[19:16],)
SPIWrite 0020,37,0,7 //sysref_jesd_mode=0x1; Address(0x20[7:5],)
SPIWrite 0020,3f,0,7 //k_m1=0x1f; Address(0x20[4:0],)
SPIWrite 0021,1f,0,7 //fb_k_m1=0x1f; Address(0x20[12:8],)
SPIWrite 0043,06,0,7 //jesd_mode=0x6; Address(0x40[30:24],)
SPIWrite 0044,12,0,7 //fb_jesd_mode=0x12; Address(0x44[6:0],)
SPIWrite 0076,01,0,7 //adc_jesd_root_clk_div=0x1; Address(0x74[23:16],)
SPIWrite 00c0,00,0,7 //ddc_rd_clk_ratio_rx1=0x0; Address(0xc0[4:0],)
SPIWrite 00c0,20,0,7 //ddc_rd_clk_ratio_rx1_override=0x1; Address(0xc0[5:5],)
SPIWrite 00c1,00,0,7 //ddc_rd_clk_ratio_rx2=0x0; Address(0xc0[12:8],)
SPIWrite 00c1,20,0,7 //ddc_rd_clk_ratio_rx2_override=0x1; Address(0xc0[13:13],)
SPIWrite 00c4,00,0,7 //jesd_tx_clk_ratio_rx1=0x0; Address(0xc4[4:0],)
SPIWrite 00c4,20,0,7 //jesd_tx_clk_ratio_rx1_override=0x1; Address(0xc4[5:5],)
SPIWrite 00c5,00,0,7 //jesd_tx_clk_ratio_rx2=0x0; Address(0xc4[12:8],)
SPIWrite 00c5,20,0,7 //jesd_tx_clk_ratio_rx2_override=0x1; Address(0xc4[13:13],)
SPIWrite 0060,04,0,7 //jesd_system_mode=0x1; Address(0x60[3:2],)
SPIWrite 0080,01,0,7 //scr_64b_initval=0x1;
Address(0x80[7:0],0x80[15:8],0x80[23:16],0x80[31:24],0x84[7:0],0x84[15:8],0x84[23:16],0x84[25:24],)

```

```
SPIWrite 0081,00,0,7
SPIWrite 0082,00,0,7
SPIWrite 0083,00,0,7
SPIWrite 0084,00,0,7
SPIWrite 0085,00,0,7
SPIWrite 0086,00,0,7
SPIWrite 0087,00,0,7
SPIWrite 0088,00,0,7 //scr_64b_en=0x0; Address(0x88[0:0],)
SPIWrite 004f,00,0,7 //jesd_std_sel=0x0; (Meaning: ); Address(0x4c[25:24],)
SPIWrite 005f,08,0,7 //dedicated_rx_fb_lane_mode=0x1; Address(0x5c[27:27],)
SPIWrite 00ca,01,0,7 //sample_drop_mode_rx1=0x1; Address(0xc8[19:16],)
SPIWrite 00ca,11,0,7 //sample_drop_mode_rx2=0x1; Address(0xc8[23:20],)
SPIWrite 0022,00,0,7 //scr=0x0; (Meaning: ); Address(0x20[16:16],)
SPIWrite 0023,00,0,7 //fb_scr=0x0; (Meaning: ); Address(0x20[24:24],)
SPIWrite 0025,00,0,7 //lane_ena=0x0; Address(0x24[11:8],)
SPIWrite 0077,04,0,7 //sysref_to_ddc_jesd_clk_div_override=0x1; Address(0x74[26:26],)
SPIWrite 008f,00,0,7 //init_o_mf_counter=0x0; Address(0x8c[25:16],)
SPIWrite 008e,00,0,7
SPIWrite 0045,e0,0,7 //init_state=0x1; (Meaning: ); Address(0x44[15:15],)
SPIWrite 0045,e0,0,7 //fifo_init_state=0x1; Address(0x44[13:13],)
SPIWrite 0045,e0,0,7 //fb_init_state=0x1; (Meaning: ); Address(0x44[14:14],)
```

\\END: Done configuring Device JESD TX

```
SPIWrite 0015,10,0,7 //PAGE: rx_jesd=0x0; Address(0x15[0:0],0x15[4:4],)
SPIWrite 0015,00,0,7
\\ STEP: jesdConfig/step3
```

\\START: Configuring Device JESD RX

```
SPIWrite 0015,00,0,7 //PAGE: tx_jesd=0x2; Address(0x15[1:1],0x15[5:5],)
SPIWrite 0015,20,0,7
SPIWrite 007f,1f,0,7 //k_m1=0x1f; Address(0x7c[31:24],)
SPIWrite 007e,1f,0,7 //rbd_m1=0x1f; Address(0x7c[23:16],)
SPIWrite 0020,01,0,7 //init_state_tx0=0x1; (Meaning: ); Address(0x20[0:0],)
SPIWrite 0081,ff,0,7 //jesd_clear_data=0xff; Address(0x80[15:8],)
SPIWrite 0021,01,0,7 //dac_jesd_root_clk_div=0x1; (Meaning: ); Address(0x20[15:8],)
SPIWrite 013d,00,0,7 //duc_wr_clk_ratio_tx0=0x0; (Meaning: ); Address(0x13c[12:8],)
SPIWrite 013f,00,0,7 //jesd_rx_clk_ratio_tx0=0x0; (Meaning: ); Address(0x13c[28:24],)
SPIWrite 0024,07,0,7 //jesd_mode_tx0=0x7; (Meaning: ); Address(0x24[4:0],)
SPIWrite 013d,20,0,7 //duc_wr_clk_ratio_tx0_override=0x1; Address(0x13c[13:13],)
SPIWrite 013f,20,0,7 //jesd_rx_clk_ratio_tx0_override=0x1; Address(0x13c[29:29],)
SPIWrite 002d,9b,0,7 //spi_txenable=0x1; Address(0x2c[8:8],)
SPIWrite 0093,ff,0,7 //spidac=0x7fff; Address(0x90[31:24],0x94[7:0],)
SPIWrite 0094,7f,0,7
SPIWrite 0093,ff,0,7 //spidac=0x7fff; Address(0x90[31:24],0x94[7:0],)
SPIWrite 0094,7f,0,7
SPIWrite 0092,00,0,7 //spidac_ena=0x0; Address(0x90[23:23],)
SPIWrite 0092,00,0,7 //spidac_ena=0x0; Address(0x90[23:23],)
SPIWrite 008b,df,0,7 //sync_request_ena=0xdf; Address(0x88[31:24],)
SPIWrite 008c,00,0,7 //error_ena=0x0; Address(0x8c[7:0],)
SPIWrite 0123,7f,0,7 //comma_align_valid_thresh_tx0=0x7f; Address(0x120[30:24],)
SPIWrite 0148,00,0,7 //jesd_h_ena=0x0; Address(0x148[1:1],)
SPIWrite 0148,00,0,7 //jesd_c_ena=0x0; Address(0x148[0:0],)
SPIWrite 007d,12,0,7 //scr=0x0; Address(0x7c[15:15],)
SPIWrite 007c,00,0,7 //lane_ena=0x0; Address(0x7c[7:0],)
SPIWrite 0134,04,0,7 //sysref_to_dac_jesd_clk_div_override=0x1; Address(0x134[2:2],)
SPIWrite 0020,01,0,7 //init_state_tx0=0x1; (Meaning: ); Address(0x20[0:0],)
SPIWrite 0173,ff,0,7 //alarms_mask=0xffffffffffffffff; Address(0x170[31:0],0x174[31:0],)
SPIWrite 0172,ff,0,7
SPIWrite 0171,ff,0,7
SPIWrite 0170,ff,0,7
SPIWrite 0177,ff,0,7
SPIWrite 0176,ff,0,7
SPIWrite 0175,ff,0,7
SPIWrite 0174,ff,0,7
SPIWrite 017b,ff,0,7 //alarms_to_pap_mask=0xffffffffffffffff;
Address(0x178[31:0],0x17c[31:0],)
SPIWrite 017a,ff,0,7
```

```
SPIWrite 0179,ff,0,7
SPIWrite 0178,ff,0,7
SPIWrite 017f,ff,0,7
SPIWrite 017e,ff,0,7
SPIWrite 017d,ff,0,7
SPIWrite 017c,ff,0,7
```

\\END: Done configuring Device JESD RX

```
SPIWrite 0015,20,0,7    //PAGE: tx_jesd=0x0;    Address(0x15[1:1],0x15[5:5],)
SPIWrite 0015,00,0,7
```

\\EXTERNAL-ACTION: If you have a RX or TX DSA packet to be applied, apply it here.

\\ STEP: calibration/step0

\\START: Sending Sysref to device from Pin/SPI

\\START: Requesting/releasing SPI Access to PLL Pages

```
SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 01d4,01,0,7    //pll_reg_spi_req_a=0x1;    Address(0x1d4[0:0],)
SPIWrite 0374,00,0,7    //pll_reg_spi_req_b1=0x0;(Meaning: );    Address(0x374[0:0],)
```

SPIPoll 01d5,0,0,1

\\Read pll_reg_spi_a_ack=0x1; Address(0x1d4[8:8],)

\\END: Done requesting/releasing SPI Access to PLL Pages

```
SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0014,01,0,7    //PAGE: clktop_2t=0x1;  Address(0x14[1:0],)
SPIWrite 002c,00,0,7    //TRIM_100N_INT_TXCMLLDVREF1=0x0;  Address(0x2c[7:5],)
```

WAIT 0.001

```
SPIWrite 0014,00,0,7    //PAGE: clktop_2t=0x0;  Address(0x14[1:0],)
SPIWrite 0014,04,0,7    //PAGE: TIMING_CON=0x1;(Meaning: );    Address(0x14[2:2],)
SPIWrite 04d1,00,0,7    //count_len_sysref=0xff;    Address(0x4d0[15:0],)
SPIWrite 04d0,ff,0,7
SPIWrite 0717,00,0,7    //spare_reg_port=0x0;    Address(0x714[31:0],)
SPIWrite 0716,00,0,7
SPIWrite 0715,00,0,7
SPIWrite 0714,00,0,7
SPIWrite 0717,00,0,7    //spare_reg_port=0x101;    Address(0x714[31:0],)
SPIWrite 0716,00,0,7
SPIWrite 0715,01,0,7
SPIWrite 0714,01,0,7
SPIWrite 0717,00,0,7    //spare_reg_port=0x0;    Address(0x714[31:0],)
SPIWrite 0716,00,0,7
SPIWrite 0715,00,0,7
SPIWrite 0714,00,0,7
SPIWrite 0014,00,0,7    //PAGE: TIMING_CON=0x0;(Meaning: );    Address(0x14[2:2],)
SPIWrite 0014,08,0,7    //PAGE: pll=0x1;    Address(0x14[7:3],)
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 0051,8e,0,7    //SYS_REF_FROM_PIN_BYPAS=0x1;  Address(0x50[15:15],)
SPIWrite 0051,8e,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x1;    Address(0x50[11:11],)
SPIWrite 0014,10,0,7    //PAGE: pll=0x2;    Address(0x14[7:3],)
SPIWrite 004e,34,0,7    //lcmgen_usespisysref=0x1;  Address(0x4c[18:18],)
SPIWrite 0014,08,0,7    //PAGE: pll=0x1;    Address(0x14[7:3],)
SPIWrite 004e,30,0,7    //lcmgen_div=0xff;  Address(0x4c[17:2],)
SPIWrite 004d,03,0,7
SPIWrite 004c,fc,0,7
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 004c,fd,0,7    //lcmgen_sync_ena=0x1;  Address(0x4c[0:0],)
SPIWrite 0014,10,0,7    //PAGE: pll=0x2;    Address(0x14[7:3],)
```

```

SPIWrite 004c,fc,0,7 //lcmgen_sync_ena=0x0; Address(0x4c[0:0],)
SPIWrite 0051,8c,0,7 //SYS_REF_FROM_PIN_BYPAS=0x1; Address(0x50[15:15],)
SPIWrite 0051,8c,0,7 //EN_SYNC_TO_PLLDIG_DIV=0x1; Address(0x50[11:11],)
SPIWrite 004e,34,0,7 //lcmgen_usespisysref=0x1; Address(0x4c[18:18],)
SPIWrite 004e,34,0,7 //lcmgen_div=0xff; Address(0x4c[17:2],)
SPIWrite 004d,03,0,7
SPIWrite 004c,fc,0,7
SPIWrite 004c,fc,0,7 //lcmgen_sync_ena=0x0; Address(0x4c[0:0],)
SPIWrite 004c,fd,0,7 //lcmgen_sync_ena=0x1; Address(0x4c[0:0],)
SPIWrite 0014,20,0,7 //PAGE: pll=0x4; Address(0x14[7:3],)
SPIWrite 004c,fc,0,7 //lcmgen_sync_ena=0x0; Address(0x4c[0:0],)
SPIWrite 0051,86,0,7 //SYS_REF_FROM_PIN_BYPAS=0x1; Address(0x50[15:15],)
SPIWrite 0051,8e,0,7 //EN_SYNC_TO_PLLDIG_DIV=0x1; Address(0x50[11:11],)
SPIWrite 0014,10,0,7 //PAGE: pll=0x2; Address(0x14[7:3],)
SPIWrite 004e,34,0,7 //lcmgen_usespisysref=0x1; Address(0x4c[18:18],)
SPIWrite 0014,20,0,7 //PAGE: pll=0x4; Address(0x14[7:3],)
SPIWrite 004e,30,0,7 //lcmgen_div=0xff; Address(0x4c[17:2],)
SPIWrite 004d,03,0,7
SPIWrite 004c,fc,0,7
SPIWrite 004c,fc,0,7 //lcmgen_sync_ena=0x0; Address(0x4c[0:0],)
SPIWrite 004c,fd,0,7 //lcmgen_sync_ena=0x1; Address(0x4c[0:0],)
SPIWrite 0014,40,0,7 //PAGE: pll=0x8; Address(0x14[7:3],)
SPIWrite 004c,fc,0,7 //lcmgen_sync_ena=0x0; Address(0x4c[0:0],)
SPIWrite 0051,86,0,7 //SYS_REF_FROM_PIN_BYPAS=0x1; Address(0x50[15:15],)
SPIWrite 0051,8e,0,7 //EN_SYNC_TO_PLLDIG_DIV=0x1; Address(0x50[11:11],)
SPIWrite 0014,10,0,7 //PAGE: pll=0x2; Address(0x14[7:3],)
SPIWrite 004e,34,0,7 //lcmgen_usespisysref=0x1; Address(0x4c[18:18],)
SPIWrite 0014,40,0,7 //PAGE: pll=0x8; Address(0x14[7:3],)
SPIWrite 004e,30,0,7 //lcmgen_div=0xff; Address(0x4c[17:2],)
SPIWrite 004d,03,0,7
SPIWrite 004c,fc,0,7
SPIWrite 004c,fc,0,7 //lcmgen_sync_ena=0x0; Address(0x4c[0:0],)
SPIWrite 004c,fd,0,7 //lcmgen_sync_ena=0x1; Address(0x4c[0:0],)
SPIWrite 0014,80,0,7 //PAGE: pll=0x10; Address(0x14[7:3],)
SPIWrite 004c,fc,0,7 //lcmgen_sync_ena=0x0; Address(0x4c[0:0],)
SPIWrite 0051,86,0,7 //SYS_REF_FROM_PIN_BYPAS=0x1; Address(0x50[15:15],)
SPIWrite 0051,8e,0,7 //EN_SYNC_TO_PLLDIG_DIV=0x1; Address(0x50[11:11],)
SPIWrite 0014,10,0,7 //PAGE: pll=0x2; Address(0x14[7:3],)
SPIWrite 004e,34,0,7 //lcmgen_usespisysref=0x1; Address(0x4c[18:18],)
SPIWrite 0014,80,0,7 //PAGE: pll=0x10; Address(0x14[7:3],)
SPIWrite 004e,30,0,7 //lcmgen_div=0xff; Address(0x4c[17:2],)
SPIWrite 004d,03,0,7
SPIWrite 004c,fc,0,7
SPIWrite 004c,fc,0,7 //lcmgen_sync_ena=0x0; Address(0x4c[0:0],)
SPIWrite 004c,fd,0,7 //lcmgen_sync_ena=0x1; Address(0x4c[0:0],)

```

WAIT 0.001

```

SPIWrite 0014,10,0,7 //PAGE: pll=0x2; Address(0x14[7:3],)
SPIWrite 004e,34,0,7 //lcmgen_spisysref=0x0; Address(0x4c[19:19],)
SPIWrite 004e,3c,0,7 //lcmgen_spisysref=0x1; Address(0x4c[19:19],)
SPIWrite 004e,34,0,7 //lcmgen_spisysref=0x0; Address(0x4c[19:19],)
SPIWrite 0014,08,0,7 //PAGE: pll=0x1; Address(0x14[7:3],)
SPIWrite 0051,0e,0,7 //SYS_REF_FROM_PIN_BYPAS=0x0; Address(0x50[15:15],)
SPIWrite 0051,06,0,7 //EN_SYNC_TO_PLLDIG_DIV=0x0; Address(0x50[11:11],)
SPIWrite 0014,10,0,7 //PAGE: pll=0x2; Address(0x14[7:3],)
SPIWrite 0051,0c,0,7 //SYS_REF_FROM_PIN_BYPAS=0x0; Address(0x50[15:15],)
SPIWrite 0051,04,0,7 //EN_SYNC_TO_PLLDIG_DIV=0x0; Address(0x50[11:11],)
SPIWrite 0014,20,0,7 //PAGE: pll=0x4; Address(0x14[7:3],)
SPIWrite 0051,0e,0,7 //SYS_REF_FROM_PIN_BYPAS=0x0; Address(0x50[15:15],)
SPIWrite 0051,06,0,7 //EN_SYNC_TO_PLLDIG_DIV=0x0; Address(0x50[11:11],)
SPIWrite 0014,40,0,7 //PAGE: pll=0x8; Address(0x14[7:3],)
SPIWrite 0051,0e,0,7 //SYS_REF_FROM_PIN_BYPAS=0x0; Address(0x50[15:15],)
SPIWrite 0051,06,0,7 //EN_SYNC_TO_PLLDIG_DIV=0x0; Address(0x50[11:11],)
SPIWrite 0014,80,0,7 //PAGE: pll=0x10; Address(0x14[7:3],)
SPIWrite 0051,0e,0,7 //SYS_REF_FROM_PIN_BYPAS=0x0; Address(0x50[15:15],)
SPIWrite 0051,06,0,7 //EN_SYNC_TO_PLLDIG_DIV=0x0; Address(0x50[11:11],)
SPIWrite 0014,00,0,7 //PAGE: pll=0x0; Address(0x14[7:3],)
SPIWrite 0014,01,0,7 //PAGE: clktop_2t=0x1; Address(0x14[1:0],)

```

```
SPIWrite 002c,00,0,7    //TRIM_100N_INT_TXCMLLDVREF1=0x0;   Address(0x2c[7:5],)

\\START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0014,00,0,7    //PAGE: clktop_2t=0x0;   Address(0x14[1:0],)
SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1; (Meaning: );   Address(0x15[7:7],)
SPIWrite 01d4,00,0,7    //pll_reg_spi_req_a=0x0;   Address(0x1d4[0:0],)
SPIWrite 0374,00,0,7    //pll_reg_spi_req_b1=0x0; (Meaning: );   Address(0x374[0:0],)

WAIT 0.01
```

```
\\END: Done requesting/releasing SPI Access to PLL Pages
```

```
\\END: Done sending Sysref to device from Pin/SPI
```

```
\\START: Staggered TDD Toggle
```

```
SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0; (Meaning: );   Address(0x15[7:7],)
SPIWrite 0014,04,0,7    //PAGE: TIMING_CON=0x1; (Meaning: );   Address(0x14[2:2],)
SPIWrite 0124,01,0,7    //use_reg_txon_AB=0x1;   Address(0x124[0:0],)
SPIWrite 0126,01,0,7    //use_reg_rxon_AB=0x1;   Address(0x124[16:16],)
SPIWrite 0128,01,0,7    //use_reg_fbon_AB=0x1;   Address(0x128[0:0],)
SPIWrite 012a,01,0,7    //use_reg_txon_CD=0x1;   Address(0x128[16:16],)
SPIWrite 012c,01,0,7    //use_reg_rxon_CD=0x1;   Address(0x12c[0:0],)
SPIWrite 012e,01,0,7    //use_reg_fbon_CD=0x1;   Address(0x12c[16:16],)
SPIWrite 0127,00,0,7    //reg_for_rxon_AB=0x0;   Address(0x124[24:24],)
SPIWrite 012d,00,0,7    //reg_for_rxon_CD=0x0;   Address(0x12c[8:8],)
SPIWrite 0127,01,0,7    //reg_for_rxon_AB=0x1;   Address(0x124[24:24],)
SPIWrite 012d,01,0,7    //reg_for_rxon_CD=0x1;   Address(0x12c[8:8],)
SPIWrite 0127,00,0,7    //reg_for_rxon_AB=0x0;   Address(0x124[24:24],)
SPIWrite 012d,00,0,7    //reg_for_rxon_CD=0x0;   Address(0x12c[8:8],)
SPIWrite 0125,00,0,7    //reg_for_txon_AB=0x0;   Address(0x124[8:8],)
SPIWrite 012b,00,0,7    //reg_for_txon_CD=0x0;   Address(0x128[24:24],)
SPIWrite 0129,00,0,7    //reg_for_fbon_AB=0x0;   Address(0x128[8:8],)
SPIWrite 012f,00,0,7    //reg_for_fbon_CD=0x0;   Address(0x12c[24:24],)
SPIWrite 0125,01,0,7    //reg_for_txon_AB=0x1;   Address(0x124[8:8],)
SPIWrite 012b,01,0,7    //reg_for_txon_CD=0x1;   Address(0x128[24:24],)
SPIWrite 0129,01,0,7    //reg_for_fbon_AB=0x1;   Address(0x128[8:8],)
SPIWrite 012f,01,0,7    //reg_for_fbon_CD=0x1;   Address(0x12c[24:24],)
```

```
\\END: Done Staggered TDD Toggle
```

```
SPIWrite 0014,00,0,7    //PAGE: TIMING_CON=0x0; (Meaning: );   Address(0x14[2:2],)
\\ STEP: calibration/step1
```

```
\\START: Enabling RX DC correction
```

```
SPIWrite 0010,0c,0,7    //PAGE: rx_top=0x3;   Address(0x10[3:2],)
SPIWrite 0401,01,0,7    //dc_freeze_reg=0x1; (Meaning: );   Address(0x400[8:8],)
SPIWrite 0420,00,0,7    //alpha_update_signal=0x0;   Address(0x420[0:0],)
SPIWrite 0420,01,0,7    //alpha_update_signal=0x1;   Address(0x420[0:0],)
SPIWrite 0420,00,0,7    //alpha_update_signal=0x0;   Address(0x420[0:0],)
SPIWrite 0401,00,0,7    //dc_freeze_reg=0x0; (Meaning: );   Address(0x400[8:8],)
SPIWrite 0400,00,0,7    //bypass=0x0; (Meaning: );   Address(0x400[0:0],)
SPIWrite 0411,01,0,7    //dc_freeze_reg=0x1; (Meaning: );   Address(0x410[8:8],)
SPIWrite 0421,00,0,7    //alpha_update_signal=0x0;   Address(0x420[8:8],)
SPIWrite 0421,01,0,7    //alpha_update_signal=0x1;   Address(0x420[8:8],)
SPIWrite 0421,00,0,7    //alpha_update_signal=0x0;   Address(0x420[8:8],)
SPIWrite 0411,00,0,7    //dc_freeze_reg=0x0; (Meaning: );   Address(0x410[8:8],)
SPIWrite 0410,00,0,7    //bypass=0x0; (Meaning: );   Address(0x410[0:0],)
SPIWrite 0801,01,0,7    //dc_freeze_reg=0x1; (Meaning: );   Address(0x800[8:8],)
SPIWrite 0820,00,0,7    //alpha_update_signal=0x0;   Address(0x820[0:0],)
SPIWrite 0820,01,0,7    //alpha_update_signal=0x1;   Address(0x820[0:0],)
SPIWrite 0820,00,0,7    //alpha_update_signal=0x0;   Address(0x820[0:0],)
SPIWrite 0801,00,0,7    //dc_freeze_reg=0x0; (Meaning: );   Address(0x800[8:8],)
SPIWrite 0800,00,0,7    //bypass=0x0; (Meaning: );   Address(0x800[0:0],)
```

```
SPIWrite 0811,01,0,7 //dc_freeze_reg=0x1;(Meaning: ); Address(0x810[8:8],)
SPIWrite 0821,00,0,7 //alpha_update_signal=0x0; Address(0x820[8:8],)
SPIWrite 0821,01,0,7 //alpha_update_signal=0x1; Address(0x820[8:8],)
SPIWrite 0821,00,0,7 //alpha_update_signal=0x0; Address(0x820[8:8],)
SPIWrite 0811,00,0,7 //dc_freeze_reg=0x0;(Meaning: ); Address(0x810[8:8],)
SPIWrite 0810,00,0,7 //bypass=0x0;(Meaning: ); Address(0x810[0:0],)
```

\\END: Done enabling RX DC correction

```
SPIWrite 0010,00,0,7 //PAGE: rx_top=0x0; Address(0x10[3:2],)
\\ STEP: gpioConfig/step0
```

\\Removing the force on Sync Pin.

```
SPIWrite 0015,80,0,7 //PAGE: DIGTOP_MISC=0x1;(Meaning: ); Address(0x15[7:7],)
SPIWrite 0555,fd,0,7 //ovr_sel_intpo_dac_sync_n_ab_0=0x0; Address(0x554[9:9],)
SPIWrite 0555,f5,0,7 //ovr_sel_intpo_dac_sync_n_ab_1=0x0; Address(0x554[11:11],)
SPIWrite 0555,d5,0,7 //ovr_sel_intpo_dac_sync_n_cd_0=0x0; Address(0x554[13:13],)
SPIWrite 0555,55,0,7 //ovr_sel_intpo_dac_sync_n_cd_1=0x0; Address(0x554[15:15],)
```

\\START: Configuring GPIO

```
SPIWrite 0538,05,0,7 //preferred_input_sel_gpio_78=0x1; Address(0x538[4:2],)
SPIWrite 0538,05,0,7 //buf_dir_ctrl_gpio_78=0x1; Address(0x538[1:0],)
SPIWrite 0550,2a,0,7 //ovr_sel_intpi_tdd_2t_en_cd=0x0; Address(0x550[7:7],)
SPIWrite 04e4,01,0,7 //preferred_input_sel_gpio_57=0x0; Address(0x4e4[4:2],)
SPIWrite 04e5,2c,0,7 //crossbar_sel_input_gpio_57=0x2c; Address(0x4e4[15:8],)
SPIWrite 04e4,01,0,7 //buf_dir_ctrl_gpio_57=0x1; Address(0x4e4[1:0],)
SPIWrite 0554,df,0,7 //ovr_sel_intpi_adc_sync_n_cd_0=0x0; Address(0x554[5:5],)
SPIWrite 04b4,01,0,7 //preferred_input_sel_gpio_45=0x0; Address(0x4b4[4:2],)
SPIWrite 04b5,24,0,7 //crossbar_sel_input_gpio_45=0x24; Address(0x4b4[15:8],)
SPIWrite 04b4,01,0,7 //buf_dir_ctrl_gpio_45=0x1; Address(0x4b4[1:0],)
SPIWrite 05c1,a8,0,7 //ovr_sel_intpi_fspic_data_in=0x0; Address(0x5c0[9:9],)
SPIWrite 0458,21,0,7 //preferred_output_sel_gpio_22=0x1; Address(0x458[7:5],)
SPIWrite 0458,22,0,7 //buf_dir_ctrl_gpio_22=0x2; Address(0x458[1:0],)
SPIWrite 0571,00,0,7 //ovr_sel_intpo_alarm_2=0x0; Address(0x570[13:13],)
SPIWrite 0454,05,0,7 //preferred_input_sel_gpio_21=0x1; Address(0x454[4:2],)
SPIWrite 0454,05,0,7 //buf_dir_ctrl_gpio_21=0x1; Address(0x454[1:0],)
SPIWrite 056d,02,0,7 //ovr_sel_intpi_global_pdn=0x0; Address(0x56c[11:11],)
SPIWrite 0420,05,0,7 //preferred_input_sel_gpio_8=0x1; Address(0x420[4:2],)
SPIWrite 0420,05,0,7 //buf_dir_ctrl_gpio_8=0x1; Address(0x420[1:0],)
SPIWrite 0551,00,0,7 //ovr_sel_intpi_tdd_1f_en_ab=0x0; Address(0x550[9:9],)
SPIWrite 0468,05,0,7 //preferred_input_sel_gpio_26=0x1; Address(0x468[4:2],)
SPIWrite 0468,05,0,7 //buf_dir_ctrl_gpio_26=0x1; Address(0x468[1:0],)
SPIWrite 0550,22,0,7 //ovr_sel_intpi_tdd_2r_en_cd=0x0; Address(0x550[3:3],)
SPIWrite 04c8,05,0,7 //preferred_input_sel_gpio_50=0x1; Address(0x4c8[4:2],)
SPIWrite 04c8,05,0,7 //buf_dir_ctrl_gpio_50=0x1; Address(0x4c8[1:0],)
SPIWrite 05c0,a2,0,7 //ovr_sel_intpi_fspia_clk=0x0; Address(0x5c0[3:3],)
SPIWrite 04f8,01,0,7 //preferred_input_sel_gpio_62=0x0; Address(0x4f8[4:2],)
SPIWrite 04f9,03,0,7 //crossbar_sel_input_gpio_62=0x3; Address(0x4f8[15:8],)
SPIWrite 04f8,01,0,7 //buf_dir_ctrl_gpio_62=0x1; Address(0x4f8[1:0],)
SPIWrite 05c0,22,0,7 //ovr_sel_intpi_fspib_clk=0x0; Address(0x5c0[7:7],)
SPIWrite 046c,21,0,7 //preferred_output_sel_gpio_27=0x1; Address(0x46c[7:5],)
SPIWrite 046c,22,0,7 //buf_dir_ctrl_gpio_27=0x2; Address(0x46c[1:0],)
SPIWrite 0571,00,0,7 //ovr_sel_intpo_alarm_1=0x0; Address(0x570[11:11],)
SPIWrite 040c,05,0,7 //preferred_input_sel_gpio_3=0x1; Address(0x40c[4:2],)
SPIWrite 040c,05,0,7 //buf_dir_ctrl_gpio_3=0x1; Address(0x40c[1:0],)
SPIWrite 0550,02,0,7 //ovr_sel_intpi_tdd_2t_en_ab=0x0; Address(0x550[5:5],)
SPIWrite 0444,05,0,7 //preferred_input_sel_gpio_17=0x1; Address(0x444[4:2],)
SPIWrite 0444,05,0,7 //buf_dir_ctrl_gpio_17=0x1; Address(0x444[1:0],)
SPIWrite 05b0,23,0,7 //ovr_sel_intpi_spib1_clk=0x0; Address(0x5b0[3:3],)
SPIWrite 052c,01,0,7 //preferred_input_sel_gpio_75=0x0; Address(0x52c[4:2],)
SPIWrite 052d,23,0,7 //crossbar_sel_input_gpio_75=0x23; Address(0x52c[15:8],)
SPIWrite 052c,01,0,7 //buf_dir_ctrl_gpio_75=0x1; Address(0x52c[1:0],)
SPIWrite 05c0,02,0,7 //ovr_sel_intpi_fspib_data_in=0x0; Address(0x5c0[5:5],)
SPIWrite 0520,22,0,7 //preferred_output_sel_gpio_72=0x1; Address(0x520[7:5],)
SPIWrite 0520,22,0,7 //buf_dir_ctrl_gpio_72=0x2; Address(0x520[1:0],)
SPIWrite 0555,55,0,7 //ovr_sel_intpo_dac_sync_n_cd_0=0x0; Address(0x554[13:13],)
SPIWrite 04c0,05,0,7 //preferred_input_sel_gpio_48=0x1; Address(0x4c0[4:2],)
```

```

SPIWrite 04c0,05,0,7 //buf_dir_ctrl_gpio_48=0x1; Address(0x4c0[1:0],)
SPIWrite 0554,dd,0,7 //ovr_sel_intpi_adc_sync_n_ab_0=0x0; Address(0x554[1:1],)
SPIWrite 04ac,01,0,7 //preferred_input_sel_gpio_43=0x0; Address(0x4ac[4:2],)
SPIWrite 04ad,04,0,7 //crossbar_sel_input_gpio_43=0x4; Address(0x4ac[15:8],)
SPIWrite 04ac,01,0,7 //buf_dir_ctrl_gpio_43=0x1; Address(0x4ac[1:0],)
SPIWrite 05c1,a0,0,7 //ovr_sel_intpi_fspic_clk=0x0; Address(0x5c0[11:11],)
SPIWrite 04d8,05,0,7 //preferred_input_sel_gpio_54=0x1; Address(0x4d8[4:2],)
SPIWrite 04d8,05,0,7 //buf_dir_ctrl_gpio_54=0x1; Address(0x4d8[1:0],)
SPIWrite 05c0,00,0,7 //ovr_sel_intpi_fspia_data_in=0x0; Address(0x5c0[1:1],)
SPIWrite 050c,05,0,7 //preferred_input_sel_gpio_67=0x1; Address(0x50c[4:2],)
SPIWrite 050c,05,0,7 //buf_dir_ctrl_gpio_67=0x1; Address(0x50c[1:0],)
SPIWrite 05c1,20,0,7 //ovr_sel_intpi_fspid_clk=0x0; Address(0x5c0[15:15],)
SPIWrite 0530,01,0,7 //preferred_input_sel_gpio_76=0x0; Address(0x530[4:2],)
SPIWrite 0531,2b,0,7 //crossbar_sel_input_gpio_76=0x2b; Address(0x530[15:8],)
SPIWrite 0530,01,0,7 //buf_dir_ctrl_gpio_76=0x1; Address(0x530[1:0],)
SPIWrite 0554,d5,0,7 //ovr_sel_intpi_adc_sync_n_ab_1=0x0; Address(0x554[3:3],)
SPIWrite 04cc,05,0,7 //preferred_input_sel_gpio_51=0x1; Address(0x4cc[4:2],)
SPIWrite 04cc,05,0,7 //buf_dir_ctrl_gpio_51=0x1; Address(0x4cc[1:0],)
SPIWrite 0550,00,0,7 //ovr_sel_intpi_tdd_2r_en_ab=0x0; Address(0x550[1:1],)
SPIWrite 0430,05,0,7 //preferred_input_sel_gpio_12=0x1; Address(0x430[4:2],)
SPIWrite 0430,05,0,7 //buf_dir_ctrl_gpio_12=0x1; Address(0x430[1:0],)
SPIWrite 05b0,03,0,7 //ovr_sel_intbipi_spib1_sdi=0x0; Address(0x5b0[5:5],)
SPIWrite 0438,05,0,7 //preferred_input_sel_gpio_14=0x1; Address(0x438[4:2],)
SPIWrite 0438,05,0,7 //buf_dir_ctrl_gpio_14=0x1; Address(0x438[1:0],)
SPIWrite 05b0,01,0,7 //ovr_sel_intpi_spib1_cs_n=0x0; Address(0x5b0[1:1],)
SPIWrite 042c,21,0,7 //preferred_output_sel_gpio_11=0x1; Address(0x42c[7:5],)
SPIWrite 042c,22,0,7 //buf_dir_ctrl_gpio_11=0x2; Address(0x42c[1:0],)
SPIWrite 05b0,01,0,7 //ovr_sel_intpo_spib1_sdo=0x0; Address(0x5b0[7:7],)
SPIWrite 0514,05,0,7 //preferred_input_sel_gpio_69=0x1; Address(0x514[4:2],)
SPIWrite 0514,05,0,7 //buf_dir_ctrl_gpio_69=0x1; Address(0x514[1:0],)
SPIWrite 05c1,00,0,7 //ovr_sel_intpi_fspid_data_in=0x0; Address(0x5c0[13:13],)
SPIWrite 04f4,05,0,7 //preferred_input_sel_gpio_61=0x1; Address(0x4f4[4:2],)
SPIWrite 04f4,05,0,7 //buf_dir_ctrl_gpio_61=0x1; Address(0x4f4[1:0],)
SPIWrite 0554,55,0,7 //ovr_sel_intpi_adc_sync_n_cd_1=0x0; Address(0x554[7:7],)
SPIWrite 04bc,22,0,7 //preferred_output_sel_gpio_47=0x1; Address(0x4bc[7:5],)
SPIWrite 04bc,22,0,7 //buf_dir_ctrl_gpio_47=0x2; Address(0x4bc[1:0],)
SPIWrite 0555,55,0,7 //ovr_sel_intpo_dac_sync_n_ab_0=0x0; Address(0x554[9:9],)

```

\\END: Done Configuring GPIO

\\START: Configuring Interrupt Pins

```

SPIWrite 0119,03,0,7 //alarm_mask_lsb_for_alarm0=0x31f; Address(0x118[15:0],)
SPIWrite 0118,1f,0,7
SPIWrite 011b,00,0,7 //alarm_mask_msb_for_alarm0=0x0; Address(0x118[31:16],)
SPIWrite 011a,00,0,7
SPIWrite 011d,00,0,7 //alarm_mask_lsb_for_alarm1=0x20; Address(0x11c[15:0],)
SPIWrite 011c,20,0,7
SPIWrite 011f,00,0,7 //alarm_mask_msb_for_alarm1=0x0; Address(0x11c[31:16],)
SPIWrite 011e,00,0,7

```

\\END: Done configuring Interrupt Pins

\\START: Configuring Aux ADC

```

SPIWrite 0100,00,0,7 //auxadc_powerup=0x0; Address(0x100[0:0],)
SPIWrite 0100,00,0,7 //auxadc_en_conv=0x0; Address(0x100[1:1],)
SPIWrite 0100,00,0,7 //auxadc_soft_reset=0x0; Address(0x100[3:3],)
SPIWrite 0106,01,0,7 //auxadc_sar_bit_mode=0x1; (Meaning: ); Address(0x104[16:16],)
SPIWrite 0102,20,0,7 //auxadc_INP_MUX=0x1; (Meaning: ); Address(0x100[23:21],)
SPIWrite 0102,20,0,7 //auxadc_INM_MUX=0x0; (Meaning: ); Address(0x100[20:18],)
SPIWrite 0733,04,0,7 //aux_adc_reg_sar_delay=0x4; Address(0x730[26:24],)
SPIWrite 0101,08,0,7 //auxadc_clk_div=0x1; (Meaning: ); Address(0x100[12:11],)
SPIWrite 0101,0a,0,7 //auxadc_duty_cycle_clk=0x2; (Meaning: ); Address(0x100[10:8],)
SPIWrite 0108,00,0,7 //auxadc_offset_estim_phase_en=0x0; Address(0x108[5:5],)
SPIWrite 0105,a0,0,7 //auxadc_sar_averaging=0x5; (Meaning: ); Address(0x104[15:13],)
SPIWrite 0105,a1,0,7 //auxadc_sar_logic_niter=0x1; Address(0x104[9:8],)

```

```

SPIWrite 0106,05,0,7 //auxadc_inp_buf_chop=0x2;(Meaning: ); Address(0x104[18:17],)
SPIWrite 0106,15,0,7 //auxadc_incm_buf_chop=0x2;(Meaning: ); Address(0x104[20:19],)
SPIWrite 0106,95,0,7 //auxadc_inp_buf_mux_ctrl=0x4;(Meaning: ); Address(0x104[23:21],)
SPIWrite 0105,a1,0,7 //auxadc_sar_logic_state_start=0x0; Address(0x104[12:10],)
SPIWrite 0108,00,0,7 //auxadc_offset_data_out=0x0; Address(0x108[6:6],)
SPIWrite 0108,00,0,7 //auxadc_offsetvlaue_force_en=0x0; Address(0x108[4:4],)
SPIWrite 0107,00,0,7
SPIWrite 0108,00,0,7 //auxadc_offset_corr_value_msb=0x0; Address(0x108[3:0],)
SPIWrite 0730,00,0,7 //aux_adc_reg_cap_code_force_en=0x0; Address(0x730[6:6],)
SPIWrite 0730,00,0,7 //aux_adc_reg_cap_code_p_force_val=0x0; Address(0x730[5:0],)
SPIWrite 0731,00,0,7 //aux_adc_reg_res_code1_force_en=0x0; Address(0x730[13:13],)
SPIWrite 0731,00,0,7 //aux_adc_reg_res_code2_force_en=0x0; Address(0x730[14:14],)
SPIWrite 0731,00,0,7 //aux_adc_reg_res_code3_force_en=0x0; Address(0x730[15:15],)
SPIWrite 0731,00,0,7 //aux_adc_reg_res_code1_p_force_val=0x0; Address(0x730[12:8],)
SPIWrite 0732,00,0,7 //aux_adc_reg_res_code2_p_force_val=0x0; Address(0x730[20:16],)
SPIWrite 0732,00,0,7 //aux_adc_reg_res_code3_p_force_val=0x0; Address(0x730[23:21],)
SPIWrite 0103,00,0,7 //auxadc_inp_res_term_imeas=0x0;(Meaning: ); Address(0x100[31:30],)
SPIWrite 0733,04,0,7 //aux_adc_EN_TP=0x0;(Meaning: ); Address(0x730[31:28],)
SPIWrite 0737,00,0,7 //temp_sense2_cfg1=0x0; Address(0x734[31:0],)
SPIWrite 0736,00,0,7
SPIWrite 0735,00,0,7
SPIWrite 0734,00,0,7
SPIWrite 0104,00,0,7 //auxadc_TM_IN_MUX_SEL=0x0;(Meaning: ); Address(0x104[2:0],)
SPIWrite 0104,00,0,7 //auxadc_TP_IN_MUX_SEL=0x0;(Meaning: ); Address(0x104[5:3],)
SPIWrite 0102,20,0,7

```

WAIT 0.1

```

SPIWrite 0100,00,0,7 //auxadc_soft_reset=0x0; Address(0x100[3:3],)

```

WAIT 0.1

```

SPIWrite 0100,02,0,7 //auxadc_en_conv=0x1; Address(0x100[1:1],)

```

\\END: Done configuring Aux ADC

```

SPIWrite 0015,00,0,7 //PAGE: DIGTOP_MISC=0x0;(Meaning: ); Address(0x15[7:7],)
\\ STEP: rxIqMc/step0

```

\\START: Doing RX IQMC Correction

\\START: Doing RX IQMC Correction Configuration

```

SPIWrite 0018,10,0,7 //PAGE: rx_iqmc=0x1; Address(0x18[4:4],)
SPIWrite 0348,04,0,7
SPIWrite 0348,44,0,7
SPIWrite 0018,00,4,4 //PAGE: rx_iqmc=0x0; Address(0x18[4:4],)
SPIWrite 0013,10,4,4 //PAGE: customer_macro=0x1;(Meaning: ); Address(0x13[4:4],)

```

SPIPoll 00f0,0,0,1

```

SPIWrite 00a3,00,0,7
SPIWrite 00a2,01,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,02,0,7
SPIWrite 0193,01,0,7

```

```

\\Read macro_opcode_operand=0x1000000; Address(0x190[31:0],)

```

SPIPoll 00f0,0,7,7

```

SPIWrite 0013,00,4,4 //PAGE: customer_macro=0x0;(Meaning: ); Address(0x13[4:4],)
SPIWrite 0013,20,5,5 //PAGE: cm4_macro=0x1; Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

```

```

\\Read MACRO_ERROR=0x0; Address(0x20[3:3],)

```

```

\\Read  MACRO_ERROR=0x0;      Address(0x20[3:3],)

\\Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0x20[4:4],)

\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0x20[5:5],)

\\Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0x20[6:6],)

\\Read  MACRO_ERROR_IN_EXECUTION=0x0;  Address(0x20[7:7],)

\\Read  MACRO_STATUS_RESULT_0=0x11119e;      Address(0x34[31:0],)

SPIWrite 0013,00,5,5      //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
SPIWrite 0018,10,4,4      //PAGE: rx_iqmc=0x1;    Address(0x18[4:4],)
SPIWrite 036c,08,3,3
SPIWrite 036c,0a,0,2
SPIWrite 0381,00,7,7
SPIWrite 0305,00,0,0
SPIWrite 0305,02,1,1
SPIWrite 0341,00,0,3
SPIWrite 0340,04,0,7
SPIWrite 0343,40,6,6
SPIWrite 0334,03,0,6
SPIWrite 0334,83,7,7
SPIWrite 037e,7f,0,6
SPIWrite 037e,ff,7,7
SPIWrite 0335,1c,0,6
SPIWrite 0335,9c,7,7
SPIWrite 0320,14,0,6
SPIWrite 0320,94,7,7
SPIWrite 0321,14,0,6
SPIWrite 0321,94,7,7
SPIWrite 0324,04,0,2
SPIWrite 0324,0c,3,3
SPIWrite 0324,4c,4,6
SPIWrite 0324,cc,7,7
SPIWrite 0342,00,0,7
SPIWrite 0341,c0,4,7
SPIWrite 0343,c0,7,7
SPIWrite 0327,02,0,6
SPIWrite 0327,82,7,7
SPIWrite 0322,02,0,6
SPIWrite 0322,82,7,7
SPIWrite 0318,08,0,6
SPIWrite 0318,88,7,7
SPIWrite 0348,44,2,2
SPIWrite 0348,44,6,6
SPIWrite 031c,00,0,5
SPIWrite 031c,80,7,7
SPIWrite 030f,03,0,5
SPIWrite 030f,83,7,7
SPIWrite 0350,00,7,7
SPIWrite 034f,00,7,7
SPIWrite 0359,3c,2,6
SPIWrite 035a,01,0,6
SPIWrite 035b,02,0,6
SPIWrite 0359,bc,7,7
SPIWrite 035a,81,7,7
SPIWrite 035b,82,7,7

```

```

\\END: Done configuring RX IQMC Correction

```

\\END: Did RX IQMC Correction

SPIWrite 0018,00,0,7 //PAGE: rx_iqmc=0x0; Address(0x18[4:4],)
\\ STEP: agcConfig/step0

\\START: Doing AGC Config

SPIWrite 0010,0c,0,7 //PAGE: rx_top=0x3; Address(0x10[3:2],)
SPIWrite 04cd,00,0,7 //blank_time_rf_det=0x64; Address(0x4cc[15:0],)
SPIWrite 04cc,64,0,7
SPIWrite 04cf,01,0,7 //blank_time=0x1f4; Address(0x4cc[31:16],)
SPIWrite 04ce,f4,0,7
SPIWrite 0275,03,0,7 //blank_time_for_ext_comp_change=0x3e8; Address(0x274[15:0],)
SPIWrite 0274,e8,0,7
SPIWrite 0cd1,02,0,7 //disable_hysterisis=0x1; (Meaning:); Address(0xcd0[9:9],)
SPIWrite 0cd1,02,0,7 //dig_gain_dis=0x0; Address(0xcd0[8:8],)
SPIWrite 0cd1,02,0,7 //dig_gain_dis=0x0; Address(0xcd0[8:8],)
SPIWrite 0a80,b3,0,7 //gain_comp_stg_2_3_dec_chain=0xb3; Address(0xa80[7:0],)

\\START: Configuring Small Step Attack Detector

SPIWrite 0209,01,0,7 //small_step_attack_step_size=0x1; Address(0x208[13:8],)
SPIWrite 0239,0b,0,7 //small_step_attack_sig_th_high=0xb53; Address(0x238[11:0],)
SPIWrite 0238,53,0,7
SPIWrite 023b,0b,0,7 //small_step_attack_sig_th_low=0xb53; Address(0x238[27:16],)
SPIWrite 023a,53,0,7
SPIWrite 021a,00,0,7 //small_step_attack_win_len=0x100; Address(0x218[23:0],)
SPIWrite 0219,01,0,7
SPIWrite 0218,00,0,7
SPIWrite 024e,00,0,7 //small_step_attack_num_hits=0x20; Address(0x24c[23:0],)
SPIWrite 024d,00,0,7
SPIWrite 024c,20,0,7
SPIWrite 0200,48,0,7 //small_step_attack_en=0x0; (Meaning:); Address(0x200[1:1],)
SPIWrite 0204,0a,0,7 //small_step_attack_det_en=0x1; (Meaning:); Address(0x204[1:1],)

\\END: Done configuring Small Step Attack Detector

\\START: Configuring Small Step Decay Detector

SPIWrite 020b,01,0,7 //small_step_decay_step_size=0x1; Address(0x208[29:24],)
SPIWrite 0241,07,0,7 //small_step_decay_sig_th_high=0x725; Address(0x240[11:0],)
SPIWrite 0240,25,0,7
SPIWrite 0243,07,0,7 //small_step_decay_sig_th_low=0x725; Address(0x240[27:16],)
SPIWrite 0242,25,0,7
SPIWrite 0222,00,0,7 //small_step_decay_win_len=0x200; Address(0x220[23:0],)
SPIWrite 0221,02,0,7
SPIWrite 0220,00,0,7
SPIWrite 0256,00,0,7 //small_step_decay_num_hits=0x20; Address(0x254[23:0],)
SPIWrite 0255,00,0,7
SPIWrite 0254,20,0,7
SPIWrite 0200,40,0,7 //small_step_decay_en=0x0; (Meaning:); Address(0x200[3:3],)
SPIWrite 0204,0a,0,7 //small_step_decay_det_en=0x1; (Meaning:); Address(0x204[3:3],)

\\END: Done configuring Small Step Decay Detector

SPIWrite 08cd,00,0,7 //blank_time_rf_det=0x64; Address(0x8cc[15:0],)
SPIWrite 08cc,64,0,7
SPIWrite 08cf,01,0,7 //blank_time=0x1f4; Address(0x8cc[31:16],)
SPIWrite 08ce,f4,0,7
SPIWrite 0675,03,0,7 //blank_time_for_ext_comp_change=0x3e8; Address(0x674[15:0],)
SPIWrite 0674,e8,0,7
SPIWrite 0ed1,02,0,7 //disable_hysterisis=0x1; (Meaning:); Address(0xed0[9:9],)
SPIWrite 0ed1,02,0,7 //dig_gain_dis=0x0; Address(0xed0[8:8],)
SPIWrite 0ed1,02,0,7 //dig_gain_dis=0x0; Address(0xed0[8:8],)
SPIWrite 0a81,b3,0,7 //gain_comp_stg_2_3_dec_chain=0xb3; Address(0xa80[15:8],)

\\START: Configuring Small Step Attack Detector

```
SPIWrite 0609,01,0,7    //small_step_attack_step_size=0x1;  Address(0x608[13:8],)
SPIWrite 0639,0b,0,7    //small_step_attack_sig_th_high=0xb53;  Address(0x638[11:0],)
SPIWrite 0638,53,0,7
SPIWrite 063b,0b,0,7    //small_step_attack_sig_th_low=0xb53;  Address(0x638[27:16],)
SPIWrite 063a,53,0,7
SPIWrite 061a,00,0,7    //small_step_attack_win_len=0x100;  Address(0x618[23:0],)
SPIWrite 0619,01,0,7
SPIWrite 0618,00,0,7
SPIWrite 064e,00,0,7    //small_step_attack_num_hits=0x20;  Address(0x64c[23:0],)
SPIWrite 064d,00,0,7
SPIWrite 064c,20,0,7
SPIWrite 0600,48,0,7    //small_step_attack_en=0x0;(Meaning: );  Address(0x600[1:1],)
SPIWrite 0604,0a,0,7    //small_step_attack_det_en=0x1;(Meaning: );  Address(0x604[1:1],)
```

\\END: Done configuring Small Step Attack Detector

\\START: Configuring Small Step Decay Detector

```
SPIWrite 060b,01,0,7    //small_step_decay_step_size=0x1;  Address(0x608[29:24],)
SPIWrite 0641,07,0,7    //small_step_decay_sig_th_high=0x725;  Address(0x640[11:0],)
SPIWrite 0640,25,0,7
SPIWrite 0643,07,0,7    //small_step_decay_sig_th_low=0x725;  Address(0x640[27:16],)
SPIWrite 0642,25,0,7
SPIWrite 0622,00,0,7    //small_step_decay_win_len=0x200;  Address(0x620[23:0],)
SPIWrite 0621,02,0,7
SPIWrite 0620,00,0,7
SPIWrite 0656,00,0,7    //small_step_decay_num_hits=0x20;  Address(0x654[23:0],)
SPIWrite 0655,00,0,7
SPIWrite 0654,20,0,7
SPIWrite 0600,40,0,7    //small_step_decay_en=0x0;(Meaning: );  Address(0x600[3:3],)
SPIWrite 0604,0a,0,7    //small_step_decay_det_en=0x1;(Meaning: );  Address(0x604[3:3],)
```

\\END: Done configuring Small Step Decay Detector

```
SPIWrite 0010,00,0,7    //PAGE: rx_top=0x0;  Address(0x10[3:2],)
SPIWrite 0016,30,0,7    //PAGE: dsa=0x3;  Address(0x16[5:4],)
SPIWrite 0040,00,0,7
```

\\END: Completed AGC Config

```
SPIWrite 0016,00,0,7    //PAGE: dsa=0x0;  Address(0x16[5:4],)
\\ STEP: attnSet/step0
```

\\START: Setting TX DSA Attenuation

```
SPIWrite 0016,30,0,7    //PAGE: dsa=0x3;  Address(0x16[5:4],)
SPIWrite 0100,01,0,7
SPIWrite 0102,00,0,7
SPIWrite 0102,01,0,7
SPIWrite 0102,00,0,7
```

\\END: Done setting TX DSA Attenuation

\\START: Setting TX DSA Attenuation

```
SPIWrite 0120,01,0,7
SPIWrite 0122,00,0,7
SPIWrite 0122,01,0,7
SPIWrite 0122,00,0,7
```

\\END: Done setting TX DSA Attenuation

\\START: Setting TX DSA Attenuation

```
SPIWrite 0100,0d,0,7
SPIWrite 0102,00,0,7
```

SPIWrite 0102,01,0,7
SPIWrite 0102,00,0,7

\\END: Done setting TX DSA Attenuation

SPIWrite 0050,00,0,7

\\START: Setting TX DSA Attenuation

SPIWrite 0120,0d,0,7
SPIWrite 0122,00,0,7
SPIWrite 0122,01,0,7
SPIWrite 0122,00,0,7

\\END: Done setting TX DSA Attenuation

SPIWrite 00b0,00,0,7
SPIWrite 0150,0c,0,7

\\START: Setting TX DSA Attenuation

SPIWrite 0100,0d,0,7
SPIWrite 0102,00,0,7
SPIWrite 0102,01,0,7
SPIWrite 0102,00,0,7

\\END: Done setting TX DSA Attenuation

SPIWrite 0050,00,0,7

\\START: Setting TX DSA Attenuation

SPIWrite 0120,0d,0,7
SPIWrite 0122,00,0,7
SPIWrite 0122,01,0,7
SPIWrite 0122,00,0,7

\\END: Done setting TX DSA Attenuation

SPIWrite 00b0,00,0,7
SPIWrite 0150,0c,0,7
SPIWrite 0016,00,0,7 //PAGE: dsa=0x0; Address(0x16[5:4],)
\\ STEP: dacJesdLinkUp/step0

\\START: Clearing All Alarms

SPIWrite 001a,ff,0,7 //alarms_clear=0x1ff; Address(0x1a[7:0],0x1b[0:0],)
SPIWrite 001b,01,0,7
SPIWrite 001a,00,0,7 //alarms_clear=0x0; Address(0x1a[7:0],0x1b[0:0],)
SPIWrite 001b,00,0,7
SPIWrite 0013,20,0,7 //PAGE: cm4_macro=0x1; Address(0x13[5:5],)
SPIWrite 02e5,20,0,7
SPIWrite 02e5,00,0,7

\\START: Clearing JESD RX Data and alarms

SPIWrite 0013,00,0,7 //PAGE: cm4_macro=0x0; Address(0x13[5:5],)
SPIWrite 0015,02,0,7 //PAGE: tx_jesd=0x3; Address(0x15[1:1],0x15[5:5],)
SPIWrite 0015,22,0,7
SPIWrite 0081,ff,0,7 //jesd_clear_data=0xff; Address(0x80[15:8],)
SPIWrite 0081,00,0,7 //jesd_clear_data=0x0; Address(0x80[15:8],)
SPIWrite 002d,db,0,7 //serdes_fifo_err_clear=0x1; Address(0x2c[14:14],)
SPIWrite 002d,9b,0,7 //serdes_fifo_err_clear=0x0; Address(0x2c[14:14],)
SPIWrite 0190,01,0,7 //clear_all_alarms=0x1; Address(0x190[0:0],)
SPIWrite 0190,00,0,7 //clear_all_alarms=0x0; Address(0x190[0:0],)
SPIWrite 0190,04,0,7 //clear_all_alarms_to_pap=0x1; Address(0x190[2:2],)
SPIWrite 0190,00,0,7 //clear_all_alarms_to_pap=0x0; Address(0x190[2:2],)

\\END: Done clearing JESD RX Data and alarms

\\START: Clearing JESD TX Data and alarms

```
SPIWrite 0015,20,0,7    //PAGE: tx_jesd=0x0;    Address(0x15[1:1],0x15[5:5],)
SPIWrite 0015,00,0,7
SPIWrite 0015,01,0,7    //PAGE: rx_jesd=0x3;    Address(0x15[0:0],0x15[4:4],)
SPIWrite 0015,11,0,7
SPIWrite 00b1,0f,0,7    //alarms_serdes_fifo_errors_clear=0xf; Address(0xb0[11:8],)
SPIWrite 00b1,00,0,7    //alarms_serdes_fifo_errors_clear=0x0; Address(0xb0[11:8],)
SPIWrite 0026,0f,0,7    //jesd_clear_data=0xf; Address(0x24[19:16],)
SPIWrite 0026,00,0,7    //jesd_clear_data=0x0; Address(0x24[19:16],)
SPIWrite 0045,c0,0,7    //fifo_init_state=0x0; Address(0x44[13:13],)
```

\\END: Done clearing JESD TX Data and alarms

\\START: Requesting/releasing SPI Access to PLL Pages

```
SPIWrite 0015,10,0,7    //PAGE: rx_jesd=0x0;    Address(0x15[0:0],0x15[4:4],)
SPIWrite 0015,00,0,7
SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 01d4,01,0,7    //pll_reg_spi_req_a=0x1;    Address(0x1d4[0:0],)
SPIWrite 0374,00,0,7    //pll_reg_spi_req_b1=0x0;(Meaning: );    Address(0x374[0:0],)
```

SPIPoll 01d5,0,0,1

\\Read pll_reg_spi_a_ack=0x1; Address(0x1d4[8:8],)

\\END: Done requesting/releasing SPI Access to PLL Pages

```
SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0014,f8,0,7    //PAGE: pll=0x1f;    Address(0x14[7:3],)
SPIWrite 0066,08,0,7    //lock_lost_rst=0x1;    Address(0x64[19:19],)
SPIWrite 0066,00,0,7    //lock_lost_rst=0x0;    Address(0x64[19:19],)
```

\\START: Requesting/releasing SPI Access to PLL Pages

```
SPIWrite 0014,00,0,7    //PAGE: pll=0x0;    Address(0x14[7:3],)
SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 01d4,00,0,7    //pll_reg_spi_req_a=0x0;    Address(0x1d4[0:0],)
SPIWrite 0374,00,0,7    //pll_reg_spi_req_b1=0x0;(Meaning: );    Address(0x374[0:0],)
```

WAIT 0.01

\\END: Done requesting/releasing SPI Access to PLL Pages

```
SPIWrite 064a,0f,0,7    //pap_alarm_clear=0xf; Address(0x648[19:16],)
SPIWrite 064a,00,0,7    //pap_alarm_clear=0x0; Address(0x648[19:16],)
```

\\END: Done clearing All Alarms

```
SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
\\ STEP: dacJesdLinkUp/step1
SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );    Address(0x13[4:4],)
```

SPIPoll 00f0,0,0,1

```
SPIWrite 00a3,00,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,4a,0,7
```

```
SPIWrite 0193,31,0,7

\\Read  macro_opcode_operand=0x31000000;    Address(0x190[31:0],)

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0; (Meaning: );    Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;    Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)

\\Read  MACRO_ERROR_IN_OPCODE=0x0;    Address(0x20[4:4],)

\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;    Address(0x20[5:5],)

\\Read  MACRO_ERROR_IN_OPERAND=0x0;    Address(0x20[6:6],)

\\Read  MACRO_ERROR_IN_EXECUTION=0x0;    Address(0x20[7:7],)

\\Read  MACRO_READY=0x1;    Address(0x20[0:0],)

\\Read  MACRO_ACK=0x1;    Address(0x20[1:1],)

\\Read  MACRO_DONE=0x1;    Address(0x20[2:2],)

SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)

\\START: Enabling RX IQMC Correction

SPIWrite 0013,00,5,5    //PAGE: cm4_macro=0x0;    Address(0x13[5:5],)
SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1; (Meaning: );    Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,02,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,0f,0,7
SPIWrite 0193,38,0,7

\\Read  macro_opcode_operand=0x38000000;    Address(0x190[31:0],)

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0; (Meaning: );    Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;    Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)
```

\\Read MACRO_ERROR=0x0; Address(0x20[3:3],)

\\Read MACRO_ERROR_IN_OPCODE=0x0; Address(0x20[4:4],)

\\Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0x20[5:5],)

\\Read MACRO_ERROR_IN_OPERAND=0x0; Address(0x20[6:6],)

\\Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0x20[7:7],)

\\Read MACRO_READY=0x1; Address(0x20[0:0],)

\\Read MACRO_ACK=0x1; Address(0x20[1:1],)

\\Read MACRO_DONE=0x1; Address(0x20[2:2],)

SPIReadCheck 0020,3,3,00

\\Read MACRO_ERROR=0x0; Address(0x20[3:3],)

WAIT 0.5

SPIWrite 0013,00,5,5 //PAGE: cm4_macro=0x0; Address(0x13[5:5],)
SPIWrite 0010,0c,2,3 //PAGE: rx_top=0x3; Address(0x10[3:2],)
SPIWrite 0501,00,0,0 //bypass_mode=0x0; (Meaning:); Address(0x500[8:8],)
SPIWrite 0901,00,0,0 //bypass_mode=0x0; (Meaning:); Address(0x900[8:8],)
SPIWrite 0500,00,0,0 //bypass_mode=0x0; (Meaning:); Address(0x500[0:0],)
SPIWrite 0900,00,0,0 //bypass_mode=0x0; (Meaning:); Address(0x900[0:0],)

\\END: Done enabling RX IQMC Correction

\\START: Disabling TDD overrides

SPIWrite 0010,00,0,7 //PAGE: rx_top=0x0; Address(0x10[3:2],)
SPIWrite 0014,04,0,7 //PAGE: TIMING_CON=0x1; (Meaning:); Address(0x14[2:2],)
SPIWrite 0124,00,0,7 //use_reg_txon_AB=0x0; Address(0x124[0:0],)
SPIWrite 0126,00,0,7 //use_reg_rxon_AB=0x0; Address(0x124[16:16],)
SPIWrite 0128,00,0,7 //use_reg_fbon_AB=0x0; Address(0x128[0:0],)
SPIWrite 012a,00,0,7 //use_reg_txon_CD=0x0; Address(0x128[16:16],)
SPIWrite 012c,00,0,7 //use_reg_rxon_CD=0x0; Address(0x12c[0:0],)
SPIWrite 012e,00,0,7 //use_reg_fbon_CD=0x0; Address(0x12c[16:16],)

\\END: Done disabling TDD overrides

\\START: Putting the System to Sleep/Waking it up

SPIWrite 0014,00,0,7 //PAGE: TIMING_CON=0x0; (Meaning:); Address(0x14[2:2],)
SPIWrite 0015,80,0,7 //PAGE: DIGTOP_MISC=0x1; (Meaning:); Address(0x15[7:7],)
SPIWrite 0914,00,0,7 //mask_pdn_high_intr=0x0; Address(0x914[0:0],)
SPIWrite 0918,00,0,7 //mask_pdn_fall_intr=0x0; Address(0x918[0:0],)
SPIWrite 0015,00,7,7 //PAGE: DIGTOP_MISC=0x0; (Meaning:); Address(0x15[7:7],)
SPIWrite 0013,10,4,4 //PAGE: customer_macro=0x1; (Meaning:); Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,08,0,7

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SPIWrite 00a1,03,0,7
SPIWrite 00a0,ff,0,7
SPIWrite 0193,39,0,7

SPIPoll 00f0,0,7,7

SPIPoll 00f0,0,0,1

SPIWrite 0193,3a,0,7

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0; (Meaning: );    Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;    Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)

\\Read  MACRO_ERROR_IN_OPCODE=0x0;    Address(0x20[4:4],)

\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;    Address(0x20[5:5],)

\\Read  MACRO_ERROR_IN_OPERAND=0x0;    Address(0x20[6:6],)

\\Read  MACRO_ERROR_IN_EXECUTION=0x0;    Address(0x20[7:7],)

\\END: Done putting the System to Sleep/Waking it up

SPIWrite 0013,00,0,7    //PAGE: cm4_macro=0x0;    Address(0x13[5:5],)

\\END: Device Config Complete

SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1; (Meaning: );    Address(0x15[7:7],)
SPIWrite 0550,02,0,7    //ovr_sel_intpi_tdd_2r_en_ab=0x1;    Address(0x550[1:1],)
SPIWrite 0550,03,0,7    //ovr_intpi_tdd_2r_en_ab=0x1;    Address(0x550[0:0],)
SPIWrite 0550,23,0,7    //ovr_sel_intpi_tdd_2t_en_ab=0x1;    Address(0x550[5:5],)
SPIWrite 0550,33,0,7    //ovr_intpi_tdd_2t_en_ab=0x1;    Address(0x550[4:4],)
SPIWrite 0550,3b,0,7    //ovr_sel_intpi_tdd_2r_en_cd=0x1;    Address(0x550[3:3],)
SPIWrite 0550,3f,0,7    //ovr_intpi_tdd_2r_en_cd=0x1;    Address(0x550[2:2],)
SPIWrite 0550,bf,0,7    //ovr_sel_intpi_tdd_2t_en_cd=0x1;    Address(0x550[7:7],)
SPIWrite 0550,ff,0,7    //ovr_intpi_tdd_2t_en_cd=0x1;    Address(0x550[6:6],)
SPIWrite 0278,03,0,7    //pull_ctrl_gpio_30=0x3;    Address(0x278[2:0],)
SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0; (Meaning: );    Address(0x15[7:7],)

\\Device Bringup is Completed

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