```
\\AFE77xx
\\START: Doing AFE Config


\\AFE77xx
\\Library Version: 2.21

\\ STEP: rstDevice/step0

\\AFE77xx
\\EXTERNAL-ACTION: Toggle Hardware Reset


\\AFE77xx
\\START: Resetting the Device


//AFE77xx
SPIWrite 0000,30,0,7    //global_soft_reset=0x0;    Address(0x0[7:7],)
SPIWrite 0000,b0,0,7    //global_soft_reset=0x1;    Address(0x0[7:7],)
SPIWrite 0000,30,0,7    //global_soft_reset=0x0;    Address(0x0[7:7],)
SPIWrite 0000,30,0,7    //global_4pin=0x1;  Address(0x0[4:4],)
SPIWrite 0000,30,0,7    //global_ascend=0x1;    Address(0x0[5:5],)
SPIReadCheck 0003,0,7,0a

\\Read  chip_type=0xa;  Address(0x3[7:0],)

SPIReadCheck 0004,0,7,77
SPIReadCheck 0005,0,7,00

\\Read  chip_id=0x77;   Address(0x4[7:0],0x5[7:0],)

SPIReadCheck 0006,0,7,11

\\Read  chip_ver=0x11;  Address(0x6[7:0],)


\\Read  vendor_id=0x451;    Address(0x7[7:0],0x8[7:0],)


\\END: Done resetting the Device


\\The list of parameters. In the arrays of 2 elements, each value corresponds to one 2T2R1F.
// jesdKFb: [32, 32];  agcRegConfigParams: [{'coarseIndexBits': 4, 'dgcMode': 3, 'windowLenSa':
128, 'thresholdSd': -10.0, 'stepSizeSa': 1, 'thresholdBa': -1.0, 'thresholdLowSd': -10,
'numHitsSa': 8, 'stepSizePa': 1, 'numHitsSd': 8, 'thresholdLowSa': -3.0, 'thresholdPd': -18.0,
'coarseStep': 3, 'enablePd': False, 'enablePa': False, 'windowLenBa': 32, 'enableEl': False,
'stepSizePd': 1, 'windowLenBd': 32768, 'thresholdSa': -3.0, 'fdsaOffset': 0, 'regFreeze': 0,
'thresholdPa': -9.0, 'ovrEn': 1, 'windowLenPd': 32768, 'floatingPointMode': 0, 'windowLenPa':
6, 'enableBd': False, 'dgcEnable': 1, 'stepSizeBa': 3, 'enableSd': True, 'numHitsBd': 8,
'enableBa': False, 'gainControl': 2, 'pinFreezeEn': 0, 'freeze': 0, 'floatingPointFormat': 0,
'ovrDetEn': [16768, 16704, 16672, 16656], 'enableIa': 1, 'stepSizeSd': 1, 'thresholdLowBd':
-12.0, 'modePd': 0, 'thresholdLowBa': -1.0, 'gainMargin': 2, 'modePa': 0, 'enableSa': True,
'ovrOnLsbEn': [0, 0], 'numHitsBa': 8, 'thresholdBd': -12.0, 'lnabypassGain': 16, 'windowLenSd':
131072, 'phmOvrEn': 0, 'stepSizeBd': 3}, {'coarseIndexBits': 4, 'dgcMode': 3, 'windowLenSa':
128, 'thresholdSd': -10.0, 'stepSizeSa': 1, 'thresholdBa': -1.0, 'thresholdLowSd': -10,
'numHitsSa': 8, 'stepSizePa': 1, 'numHitsSd': 8, 'thresholdLowSa': -3.0, 'thresholdPd': -18.0,
'coarseStep': 3, 'enablePd': False, 'enablePa': False, 'windowLenBa': 32, 'enableEl': False,
'stepSizePd': 1, 'windowLenBd': 32768, 'thresholdSa': -3.0, 'fdsaOffset': 0, 'regFreeze': 0,
'thresholdPa': -9.0, 'ovrEn': 1, 'windowLenPd': 32768, 'floatingPointMode': 0, 'windowLenPa':
6, 'enableBd': False, 'dgcEnable': 1, 'stepSizeBa': 3, 'enableSd': True, 'numHitsBd': 8,
'enableBa': False, 'gainControl': 2, 'pinFreezeEn': 0, 'freeze': 0, 'floatingPointFormat': 0,
'ovrDetEn': [16768, 16704, 16672, 16656], 'enableIa': 1, 'stepSizeSd': 1, 'thresholdLowBd':
-12.0, 'modePd': 0, 'thresholdLowBa': -1.0, 'gainMargin': 2, 'modePa': 0, 'enableSa': True,
'ovrOnLsbEn': [0, 0], 'numHitsBa': 8, 'thresholdBd': -12.0, 'lnabypassGain': 16, 'windowLenSd':
131072, 'phmOvrEn': 0, 'stepSizeBd': 3}, {'coarseIndexBits': 4, 'dgcMode': 3, 'windowLenSa':
128, 'thresholdSd': -10.0, 'stepSizeSa': 1, 'thresholdBa': -1.0, 'thresholdLowSd': -10,
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'numHitsSa': 8, 'stepSizePa': 1, 'numHitsSd': 8, 'thresholdLowSa': -3.0, 'thresholdPd': -18.0,
'coarseStep': 3, 'enablePd': False, 'enablePa': False, 'windowLenBa': 32, 'enableEl': False,
'stepSizePd': 1, 'windowLenBd': 32768, 'thresholdSa': -3.0, 'fdsaOffset': 0, 'regFreeze': 0,
'thresholdPa': -9.0, 'ovrEn': 1, 'windowLenPd': 32768, 'floatingPointMode': 0, 'windowLenPa':
6, 'enableBd': False, 'dgcEnable': 1, 'stepSizeBa': 3, 'enableSd': True, 'numHitsBd': 8,
'enableBa': False, 'gainControl': 2, 'pinFreezeEn': 0, 'freeze': 0, 'floatingPointFormat': 0,
'ovrDetEn': [16768, 16704, 16672, 16656], 'enableIa': 1, 'stepSizeSd': 1, 'thresholdLowBd':
-12.0, 'modePd': 0, 'thresholdLowBa': -1.0, 'gainMargin': 2, 'modePa': 0, 'enableSa': True,
'ovrOnLsbEn': [0, 0], 'numHitsBa': 8, 'thresholdBd': -12.0, 'lnabypassGain': 16, 'windowLenSd':
131072, 'phmOvrEn': 0, 'stepSizeBd': 3}, {'coarseIndexBits': 4, 'dgcMode': 3, 'windowLenSa':
128, 'thresholdSd': -10.0, 'stepSizeSa': 1, 'thresholdBa': -1.0, 'thresholdLowSd': -10,
'numHitsSa': 8, 'stepSizePa': 1, 'numHitsSd': 8, 'thresholdLowSa': -3.0, 'thresholdPd': -18.0,
'coarseStep': 3, 'enablePd': False, 'enablePa': False, 'windowLenBa': 32, 'enableEl': False,
'stepSizePd': 1, 'windowLenBd': 32768, 'thresholdSa': -3.0, 'fdsaOffset': 0, 'regFreeze': 0,
'thresholdPa': -9.0, 'ovrEn': 1, 'windowLenPd': 32768, 'floatingPointMode': 0, 'windowLenPa':
6, 'enableBd': False, 'dgcEnable': 1, 'stepSizeBa': 3, 'enableSd': True, 'numHitsBd': 8,
'enableBa': False, 'gainControl': 2, 'pinFreezeEn': 0, 'freeze': 0, 'floatingPointFormat': 0,
'ovrDetEn': [16768, 16704, 16672, 16656], 'enableIa': 1, 'stepSizeSd': 1, 'thresholdLowBd':
-12.0, 'modePd': 0, 'thresholdLowBa': -1.0, 'gainMargin': 2, 'modePa': 0, 'enableSa': True,
'ovrOnLsbEn': [0, 0], 'numHitsBa': 8, 'thresholdBd': -12.0, 'lnabypassGain': 16, 'windowLenSd':
131072, 'phmOvrEn': 0, 'stepSizeBd': 3}]; enableLowIfNcoFb: [0, 0]; useDifferentKforRxFbTx:
False; jesdProtocol: 0;
// fbNco: [2344.95, 3450.24]; usePllExternalLoClock: [False, False]; jesdTxFBABSyncMux: 2;
txDsaCalibMode: 0; enableReliabilityDetector: True;
// jesdRxLaneMux: [0, 1, 2, 3, 4, 5, 6, 7]; fbDsaPerTx: [0, 0, 0, 0]; useAdcStfWrites: 0;
LMFSHdTx: ['44210', '44210']; useDifferentScrforRxFbTx: False;
// X: 61.44; serdesManualCTLEEn: False; halfRateModeRx: 0; lowIfNcoTx: [0.0, 0.0];
serdesTxLanePolarity: [False, False, False, False, False, False, False, False];
// useGlobalSleep: 1; txIqmcExternalDelayValue: [0, 0, 0, 0]; txDsaGainStepDelay: 5;
pdnUnusedLanes: 1; enableDacDither: 0;
// dedicatedLaneMode: [1, 1]; chipType: 16; txIqMcCalibMode: 2; initTxLowIfNco: 0;
pllLoopBw: 1;
// enableLowIfNcoTx: [0, 0]; chipVersion: 17; intPinsParams: [{'JESD': True, 'SPI': 0,
'SRTXA': 0, 'SRTXB': 0, 'SRTXC': 0, 'SRTXD': 0, 'PLL4': True, 'PLL0': True, 'PLL1': True,
'PLL2': True, 'PLL3': True}, {'JESD': 0, 'SPI': True, 'SRTXA': 0, 'SRTXB': 0, 'SRTXC': 0,
'SRTXD': 0, 'PLL4': 0, 'PLL0': 0, 'PLL1': 0, 'PLL2': 0, 'PLL3': 0}]; pdnSysrefBuffer: 0;
LMFSHdFb: ['22210', '22210'];
// jesdScrFb: [False, False]; enableTxIqmcLolPowerUpCorr: False; defaultRxDsa: [0, 0, 0, 0];
enableRxIqmcLolPowerUpCorr: False; defaultTxDsa: [39, 39, 39, 39];
// jesdLoopbackEn: 0; ddcFactorRx: [12, 12]; syncLoopBack: True; jesdTxFBCDSyncMux: 3;
useTxLowIfNcoForCalib: 0;
// enableRxIqmcLolTrackingCorr: True; enableTxJesdLinks: [1, 1]; pllMuxModes: 4;
enableTxIqmcDelayChar: False; halfRateModeTx: 0;
// lowIfNcoRx: [0.0, 0.0]; fbDsaPerTxEn: False; jesdRxRbd: [31, 31]; FRef: 491.52;
lowIfNcoFb: [0.0, 0.0];
// simulationMode: False; lmfcOffset: 0; rxDsaPacketFilePath: ; setLoForCoherence: True;
gpioMapping: {'D14': u'tdd_2t_en_cd', 'D10': u'rxd_ext_lnabypass', 'D11': u'rxc_ext_lnabypass',
'D12': u'rxc_digpkdet_hth', 'U5': u'adc_sync_n_ab_1', 'U7': u'rxb_digpkdet_lth', 'E17':
u'alarm_2', 'E16': u'global_pdn', 'T13': u'tdd_1f_en_ab', 'C13': u'tdd_2r_en_cd', 'C12':
u'rxc_digpkdet_lth', 'U12': u'rxa_digpkdet_lth', 'C17': u'alarm_1', 'U14': u'tdd_2t_en_ab',
'U16': u'spib1_clk', 'A5': u'dac_sync_n_cd_0', 'V5': u'adc_sync_n_ab_0', 'V7':
u'rxb_digpkdet_hth', 'C7': u'rxd_digpkdet_lth', 'E13': u'tdd_1f_en_cd', 'C5':
u'adc_sync_n_cd_0', 'V12': u'rxa_digpkdet_hth', 'V13': u'tdd_2r_en_ab', 'V10':
u'rxb_ext_lnabypass', 'V11': u'rxa_ext_lnabypass', 'V16': u'intbipi_spib1_sdi', 'V14':
u'spib1_cs_n', 'V15': u'spib1_sdo', 'D7': u'rxd_digpkdet_hth', 'D5': u'adc_sync_n_cd_1', 'Y5':
u'dac_sync_n_ab_0'};
// Fs: 2949.12; pllLo: [2344.95, 2949.12, 3450.24, 2344.95, 3439.26];
txIqmcFullBandEstimation: False; txDsaPacketFilePath: ; srConfigParams: [{'enable': False,
'amplMode': 1, 'GainStepSize': 38, 'AttnStepSize': 38, 'alarmMask': 4060, 'AmplRampGainDly': 0,
'mode': 0, 'threshold': 30, 'AmplRampAttnDly': 0, 'AmplUpdateCycles': 6}, {'enable': False,
'amplMode': 1, 'GainStepSize': 38, 'AttnStepSize': 38, 'alarmMask': 4060, 'AmplRampGainDly': 0,
'mode': 0, 'threshold': 30, 'AmplRampAttnDly': 0, 'AmplUpdateCycles': 6}, {'enable': False,
'amplMode': 1, 'GainStepSize': 38, 'AttnStepSize': 38, 'alarmMask': 4060, 'AmplRampGainDly': 0,
'mode': 0, 'threshold': 30, 'AmplRampAttnDly': 0, 'AmplUpdateCycles': 6}, {'enable': False,
'amplMode': 1, 'GainStepSize': 38, 'AttnStepSize': 38, 'alarmMask': 4060, 'AmplRampGainDly': 0,
'mode': 0, 'threshold': 30, 'AmplRampAttnDly': 0, 'AmplUpdateCycles': 6}];
// jesdAlarmPinMask: [1519143632681832447L, 1519143632681832447L]; serdesFirmware: True;
fbNcoBand1: [2344.95, 2344.95]; jesdABLvdsSync: 0; serdesRxLanePolarity: [False, False,
False, False, False, False, False, False];

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// jesdScrTx: [False, False];  rxDsaCalibMode: 0;  useOnlyAbSide: 0;  jesdK: [32, 32];
sampDropByFb: [1, 1];
// enableLowIfNcoRx: [0, 0];  enableTxDsaFactoryCal: False;  halfRateModeFb: 0;  jesdScr:
[False, False];  releaseTxMuxControlToPins: False;
// jesdKTx: [32, 32];  jesdAlarmPapMask: [1519143632681832447L, 1519143632681832447L];
latteLibVersion: 2.21;  enableTxIqmcLolHostUpdateMode: False;  ducFactorTx: [6, 6];
// jesdRxABSyncMux: 0;  customerConfig: True;  jesdTxRxABSyncMux: 0;  serdesTxPostCursor: [0,
0, 0, 0, 0, 0, 0, 0];  enableRxFbJesdLinks: [1, 1];
// chipId: 119;  defaultFbDsa: [3, 3];  useMacros: True;  serdesTxMainCursor: [7, 7, 7, 7, 7,
7, 7, 7];  executeLinkUpSequenceSeparately: True;
// sampDropByRx: [1, 1];  enableRxDsaFactoryCal: False;  enableAuxAdc: True;  ddcFactorFb: [6,
6];  serdesManualCTLE: [6, 6, 6, 6, 6, 6, 6, 6];
// enableTxIqmcLolTrackingCorr: False;  jesdRxCDSyncMux: 2;  useSpiSysref: False;
sysrefFreqDiv: 192;  jesdTxRxCDSyncMux: 1;
// useNewSerdesAgcSetting: 1;  jesdScrRx: [False, False];  systemMode: [2, 2];  enableFbCd:
True;  setTxLoFbNcoFreqForTxCalib: True;
// enableTxSigGen: False;  mode2t2r: 1;  jesdKRx: [32, 32];  rxAdcBw: 100;  jesdTxLaneMux: [0,
1, 4, 5, 2, 3, 6, 7];
// txDsaUpdateMode: 1;  LMFSHdRx: ['24410', '24410'];  txDigDelay: [0, 0, 0, 0];
serdesTxPreCursor: [0, 0, 0, 0, 0, 0, 0, 0];  gpioConfigMode: 3;
// jesdCDLvdsSync: 0;


\\Doing LMK config


\\Doing LMK config

\\ STEP: wakeUp/step0

\\START: Waking up device

SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0600,03,0,7    //misc_spi_global_pdn_ctrl=0x1;     Address(0x600[0:0],)
SPIWrite 0600,01,0,7    //misc_spi_global_pdn_sig=0x0;  Address(0x600[1:1],)

\\END: Done waking up device


\\START: Loading Efuse Chain

SPIWrite 07f0,00,0,7    //spi_ovr_sys_autoload_chain=0x0;   Address(0x7f0[5:2],)
SPIWrite 0804,00,0,7    //spi_ovr_sys_autoload_chain=0x0;   Address(0x804[5:2],)
SPIWrite 07f0,3c,0,7    //spi_ovr_sys_autoload_chain=0xf;   Address(0x7f0[5:2],)
SPIWrite 0804,3c,0,7    //spi_ovr_sys_autoload_chain=0xf;   Address(0x804[5:2],)
SPIWrite 07f0,3c,0,7    //spi_sys_rstn_ctrl=0x0;    Address(0x7f0[1:0],)
SPIWrite 07f0,3d,0,7    //spi_sys_rstn_ctrl=0x1;    Address(0x7f0[1:0],)
SPIWrite 07f0,3f,0,7    //spi_sys_rstn_ctrl=0x3;    Address(0x7f0[1:0],)
SPIWrite 07f0,3c,0,7    //spi_sys_rstn_ctrl=0x0;    Address(0x7f0[1:0],)
SPIWrite 0804,3c,0,7    //spi_sys_rstn_ctrl=0x0;    Address(0x804[1:0],)
SPIWrite 0804,3d,0,7    //spi_sys_rstn_ctrl=0x1;    Address(0x804[1:0],)
SPIWrite 0804,3f,0,7    //spi_sys_rstn_ctrl=0x3;    Address(0x804[1:0],)
SPIWrite 0804,3c,0,7    //spi_sys_rstn_ctrl=0x0;    Address(0x804[1:0],)
SPIWrite 07f0,00,0,7    //spi_ovr_sys_autoload_chain=0x0;   Address(0x7f0[5:2],)
SPIWrite 0804,00,0,7    //spi_ovr_sys_autoload_chain=0x0;   Address(0x804[5:2],)

WAIT 0.01


\\END: Done loading Efuse Chain


\\START: Checking Efuse Chain


\\Read  obs_func_spi_chain_autoload_done=0xf;   Address(0x138[3:0],)


\\Read  obs_func_spi_chain_autoload_error=0x0;  Address(0x138[7:4],)
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\\Read  obs_func_spi_chain_autoload_done=0xf;   Address(0x13c[3:0],)


\\Read  obs_func_spi_chain_autoload_error=0x0;  Address(0x13c[7:4],)


\\END: Done checking Efuse Chain


\\START: Enabling/Disabling Efuse Clock

SPIWrite 0135,01,0,7    //spi_ovr_sys_clk_gate=0x1;     Address(0x134[8:8],)
SPIWrite 0131,01,0,7    //spi_ovr_sys_clk_gate=0x1;     Address(0x130[8:8],)

\\END: Done enabling/Disabling Efuse Clock

SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
\\ STEP: rstMCU/step0

\\START: Resetting Top MC

SPIWrite 0013,10,0,7    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0140,01,0,7

\\END: Done resetting Top MC


\\START: Resetting Top MC

SPIWrite 0140,00,0,7

\\END: Done resetting Top MC


WAIT 0.1

SPIWrite 0013,00,0,7    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
\\ STEP: rstMCU/step1
SPIWrite 0012,10,4,4    //PAGE: sys_calib_macro_memory=0x1;(Meaning: );     Address(0x12[4:4],)
SPIWrite 0040,00,0,7
SPIWrite 0020,00,0,7
SPIWrite 0021,00,0,7
SPIWrite 0022,00,0,7
SPIWrite 0023,00,0,7
SPIWrite 0024,11,0,7
SPIWrite 0025,8a,0,7
SPIWrite 0026,02,0,7
SPIWrite 0027,00,0,7
SPIWrite 0028,b5,0,7
SPIWrite 0029,a4,0,7
SPIWrite 002a,6d,0,7
SPIWrite 002b,ea,0,7
SPIWrite 002c,7d,0,7
SPIWrite 002d,19,0,7
SPIWrite 002e,ce,0,7
SPIWrite 002f,ca,0,7
SPIWrite 0030,10,0,7
SPIWrite 0031,00,0,7
SPIWrite 0032,99,0,7
SPIWrite 0033,10,0,7
SPIWrite 0034,0a,0,7
SPIWrite 0035,01,0,7
SPIWrite 0036,12,0,7
SPIWrite 0037,00,0,7
SPIWrite 0038,11,0,7
SPIWrite 0039,00,0,7
SPIWrite 003a,9e,0,7
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SPIWrite 003b,11,0,7
SPIWrite 003c,05,0,7
SPIWrite 003d,06,0,7
SPIWrite 003e,12,0,7
SPIWrite 003f,00,0,7
SPIWrite 0040,00,0,7
SPIWrite 0041,00,0,7
SPIWrite 0042,00,0,7
SPIWrite 0043,05,0,7
SPIWrite 0044,09,0,7
SPIWrite 0045,08,0,7
SPIWrite 0046,17,0,7
SPIWrite 0047,00,0,7
SPIWrite 0048,00,0,7
SPIWrite 0049,00,0,7
SPIWrite 004a,00,0,7
SPIWrite 004b,00,0,7
SPIWrite 004c,00,0,7
SPIWrite 004d,00,0,7
SPIWrite 004e,00,0,7
SPIWrite 004f,00,0,7
SPIWrite 0050,ad,0,7
SPIWrite 0051,f1,0,7
SPIWrite 0052,08,0,7
SPIWrite 0053,0d,0,7
SPIWrite 0054,00,0,7
SPIWrite 0055,21,0,7
SPIWrite 0056,7f,0,7
SPIWrite 0057,4a,0,7
SPIWrite 0058,00,0,7
SPIWrite 0059,91,0,7
SPIWrite 005a,50,0,7
SPIWrite 005b,7d,0,7
SPIWrite 005c,00,0,7
SPIWrite 005d,90,0,7
SPIWrite 005e,00,0,7
SPIWrite 005f,98,0,7
SPIWrite 0060,c0,0,7
SPIWrite 0061,b1,0,7
SPIWrite 0062,10,0,7
SPIWrite 0063,46,0,7
SPIWrite 0064,81,0,7
SPIWrite 0065,75,0,7
SPIWrite 0066,00,0,7
SPIWrite 0067,bf,0,7
SPIWrite 0068,0a,0,7
SPIWrite 0069,46,0,7
SPIWrite 006a,01,0,7
SPIWrite 006b,92,0,7
SPIWrite 006c,82,0,7
SPIWrite 006d,7d,0,7
SPIWrite 006e,01,0,7
SPIWrite 006f,92,0,7
SPIWrite 0070,01,0,7
SPIWrite 0071,9a,0,7
SPIWrite 0072,01,0,7
SPIWrite 0073,2a,0,7
SPIWrite 0074,0d,0,7
SPIWrite 0075,d0,0,7
SPIWrite 0076,01,0,7
SPIWrite 0077,23,0,7
SPIWrite 0078,20,0,7
SPIWrite 0079,22,0,7
SPIWrite 007a,c0,0,7
SPIWrite 007b,f2,0,7
SPIWrite 007c,00,0,7
SPIWrite 007d,02,0,7
SPIWrite 007e,52,0,7
SPIWrite 007f,1e,0,7
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SPIWrite 0080,fd,0,7
SPIWrite 0081,d1,0,7
SPIWrite 0082,00,0,7
SPIWrite 0083,bf,0,7
SPIWrite 0084,00,0,7
SPIWrite 0085,bf,0,7
SPIWrite 0086,c3,0,7
SPIWrite 0087,75,0,7
SPIWrite 0088,82,0,7
SPIWrite 0089,7d,0,7
SPIWrite 008a,01,0,7
SPIWrite 008b,92,0,7
SPIWrite 008c,01,0,7
SPIWrite 008d,9a,0,7
SPIWrite 008e,01,0,7
SPIWrite 008f,2a,0,7
SPIWrite 0090,f2,0,7
SPIWrite 0091,d1,0,7
SPIWrite 0092,c1,0,7
SPIWrite 0093,75,0,7
SPIWrite 0094,02,0,7
SPIWrite 0095,b0,0,7
SPIWrite 0096,70,0,7
SPIWrite 0097,47,0,7
SPIWrite 0098,2d,0,7
SPIWrite 0099,e9,0,7
SPIWrite 009a,f0,0,7
SPIWrite 009b,47,0,7
SPIWrite 009c,6d,0,7
SPIWrite 009d,4c,0,7
SPIWrite 009e,21,0,7
SPIWrite 009f,79,0,7
SPIWrite 00a0,60,0,7
SPIWrite 00a1,79,0,7
SPIWrite 00a2,08,0,7
SPIWrite 00a3,43,0,7
SPIWrite 00a4,65,0,7
SPIWrite 00a5,d0,0,7
SPIWrite 00a6,dc,0,7
SPIWrite 00a7,48,0,7
SPIWrite 00a8,df,0,7
SPIWrite 00a9,f8,0,7
SPIWrite 00aa,68,0,7
SPIWrite 00ab,a3,0,7
SPIWrite 00ac,22,0,7
SPIWrite 00ad,88,0,7
SPIWrite 00ae,00,0,7
SPIWrite 00af,88,0,7
SPIWrite 00b0,da,0,7
SPIWrite 00b1,f8,0,7
SPIWrite 00b2,08,0,7
SPIWrite 00b3,14,0,7
SPIWrite 00b4,50,0,7
SPIWrite 00b5,43,0,7
SPIWrite 00b6,c0,0,7
SPIWrite 00b7,10,0,7
SPIWrite 00b8,88,0,7
SPIWrite 00b9,47,0,7
SPIWrite 00ba,20,0,7
SPIWrite 00bb,79,0,7
SPIWrite 00bc,58,0,7
SPIWrite 00bd,b3,0,7
SPIWrite 00be,4f,0,7
SPIWrite 00bf,f0,0,7
SPIWrite 00c0,78,0,7
SPIWrite 00c1,47,0,7
SPIWrite 00c2,01,0,7
SPIWrite 00c3,20,0,7
SPIWrite 00c4,4f,0,7
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SPIWrite 00c5,f0,0,7
SPIWrite 00c6,2f,0,7
SPIWrite 00c7,46,0,7
SPIWrite 00c8,97,0,7
SPIWrite 00c9,f8,0,7
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SPIWrite 00cb,91,0,7
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SPIWrite 00d6,00,0,7
SPIWrite 00d7,11,0,7
SPIWrite 00d8,41,0,7
SPIWrite 00d9,f0,0,7
SPIWrite 00da,80,0,7
SPIWrite 00db,71,0,7
SPIWrite 00dc,c6,0,7
SPIWrite 00dd,f8,0,7
SPIWrite 00de,00,0,7
SPIWrite 00df,11,0,7
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SPIWrite 00fd,f8,0,7
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SPIWrite 00ff,51,0,7
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SPIWrite 0101,f3,0,7
SPIWrite 0102,00,0,7
SPIWrite 0103,61,0,7
SPIWrite 0104,87,0,7
SPIWrite 0105,f8,0,7
SPIWrite 0106,39,0,7
SPIWrite 0107,91,0,7
SPIWrite 0108,d6,0,7
SPIWrite 0109,f8,0,7
```

```
SPIWrite 010a,00,0,7
SPIWrite 010b,01,0,7
SPIWrite 010c,25,0,7
SPIWrite 010d,71,0,7
SPIWrite 010e,61,0,7
SPIWrite 010f,f3,0,7
SPIWrite 0110,18,0,7
SPIWrite 0111,60,0,7
SPIWrite 0112,c6,0,7
SPIWrite 0113,f8,0,7
SPIWrite 0114,00,0,7
SPIWrite 0115,01,0,7
SPIWrite 0116,60,0,7
SPIWrite 0117,79,0,7
SPIWrite 0118,58,0,7
SPIWrite 0119,b3,0,7
SPIWrite 011a,4f,0,7
SPIWrite 011b,f0,0,7
SPIWrite 011c,78,0,7
SPIWrite 011d,47,0,7
SPIWrite 011e,01,0,7
SPIWrite 011f,20,0,7
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SPIWrite 013d,25,0,7
SPIWrite 013e,86,0,7
SPIWrite 013f,f8,0,7
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SPIWrite 0142,63,0,7
SPIWrite 0143,7b,0,7
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SPIWrite 0145,f8,0,7
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SPIWrite 0147,31,0,7
SPIWrite 0148,22,0,7
SPIWrite 0149,7b,0,7
SPIWrite 014a,86,0,7
SPIWrite 014b,f8,0,7
SPIWrite 014c,20,0,7
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SPIWrite 0153,f8,0,7
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SPIWrite 0155,14,0,7
SPIWrite 0156,65,0,7
SPIWrite 0157,71,0,7
SPIWrite 0158,88,0,7
SPIWrite 0159,47,0,7
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SPIWrite 0174,f0,0,7
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SPIWrite 0176,2d,0,7
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SPIWrite 0178,f0,0,7
SPIWrite 0179,47,0,7
SPIWrite 017a,36,0,7
SPIWrite 017b,4c,0,7
SPIWrite 017c,a1,0,7
SPIWrite 017d,78,0,7
SPIWrite 017e,e0,0,7
SPIWrite 017f,78,0,7
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SPIWrite 0182,65,0,7
SPIWrite 0183,d0,0,7
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SPIWrite 0185,48,0,7
SPIWrite 0186,df,0,7
SPIWrite 0187,f8,0,7
SPIWrite 0188,8c,0,7
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SPIWrite 018b,88,0,7
SPIWrite 018c,00,0,7
SPIWrite 018d,88,0,7
SPIWrite 018e,da,0,7
SPIWrite 018f,f8,0,7
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SPIWrite 0191,14,0,7
SPIWrite 0192,50,0,7
SPIWrite 0193,43,0,7
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SPIWrite 0198,a0,0,7
SPIWrite 0199,78,0,7
SPIWrite 019a,58,0,7
SPIWrite 019b,b3,0,7
SPIWrite 019c,4f,0,7
SPIWrite 019d,f0,0,7
SPIWrite 019e,f0,0,7
SPIWrite 019f,47,0,7
SPIWrite 01a0,01,0,7
SPIWrite 01a1,20,0,7
SPIWrite 01a2,4f,0,7
SPIWrite 01a3,f0,0,7
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SPIWrite 01b4,00,0,7
SPIWrite 01b5,11,0,7
SPIWrite 01b6,41,0,7
SPIWrite 01b7,f0,0,7
SPIWrite 01b8,80,0,7
SPIWrite 01b9,71,0,7
SPIWrite 01ba,c6,0,7
SPIWrite 01bb,f8,0,7
SPIWrite 01bc,00,0,7
SPIWrite 01bd,11,0,7
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SPIWrite 01c0,86,0,7
SPIWrite 01c1,f8,0,7
SPIWrite 01c2,02,0,7
SPIWrite 01c3,51,0,7
SPIWrite 01c4,e3,0,7
SPIWrite 01c5,79,0,7
SPIWrite 01c6,86,0,7
SPIWrite 01c7,f8,0,7
SPIWrite 01c8,01,0,7
SPIWrite 01c9,31,0,7
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SPIWrite 01ce,00,0,7
SPIWrite 01cf,21,0,7
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SPIWrite 01d1,f8,0,7
SPIWrite 01d2,02,0,7
SPIWrite 01d3,01,0,7
SPIWrite 01d4,da,0,7
SPIWrite 01d5,f8,0,7
SPIWrite 01d6,08,0,7
SPIWrite 01d7,14,0,7
SPIWrite 01d8,88,0,7
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SPIWrite 01db,f8,0,7
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SPIWrite 01dd,51,0,7
SPIWrite 01de,c8,0,7
SPIWrite 01df,f3,0,7
SPIWrite 01e0,00,0,7
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SPIWrite 01f8,4f,0,7
SPIWrite 01f9,f0,0,7
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SPIWrite 021d,f8,0,7
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SPIWrite 0222,86,0,7
SPIWrite 0223,f8,0,7
SPIWrite 0224,21,0,7
SPIWrite 0225,31,0,7
SPIWrite 0226,22,0,7
SPIWrite 0227,7a,0,7
SPIWrite 0228,86,0,7
SPIWrite 0229,f8,0,7
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SPIWrite 0231,f8,0,7
SPIWrite 0232,08,0,7
SPIWrite 0233,14,0,7
SPIWrite 0234,88,0,7
SPIWrite 0235,47,0,7
SPIWrite 0236,86,0,7
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SPIWrite 023e,87,0,7
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SPIWrite 0249,f3,0,7
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SPIWrite 024c,c6,0,7
SPIWrite 024d,f8,0,7
SPIWrite 024e,20,0,7
SPIWrite 024f,01,0,7
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SPIWrite 0252,f0,0,7
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SPIWrite 0255,00,0,7
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SPIWrite 025d,4b,0,7
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SPIWrite 025f,4c,0,7
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SPIWrite 026b,88,0,7
SPIWrite 026c,05,0,7
SPIWrite 026d,91,0,7
SPIWrite 026e,24,0,7
SPIWrite 026f,78,0,7
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SPIWrite 0271,92,0,7
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SPIWrite 0274,03,0,7
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SPIWrite 028f,78,0,7
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SPIWrite 02a7,20,0,7
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SPIWrite 02ac,21,0,7
SPIWrite 02ad,68,0,7
SPIWrite 02ae,41,0,7
SPIWrite 02af,f0,0,7
SPIWrite 02b0,80,0,7
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SPIWrite 02be,06,0,7
SPIWrite 02bf,9b,0,7
SPIWrite 02c0,84,0,7
SPIWrite 02c1,f8,0,7
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SPIWrite 02c6,84,0,7
SPIWrite 02c7,f8,0,7
SPIWrite 02c8,a3,0,7
SPIWrite 02c9,98,0,7
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SPIWrite 02ec,00,0,7
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SPIWrite 02f3,46,0,7
SPIWrite 02f4,bb,0,7
SPIWrite 02f5,f1,0,7
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SPIWrite 02f9,bf,0,7
SPIWrite 02fa,ba,0,7
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SPIWrite 02fc,01,0,7
SPIWrite 02fd,0f,0,7
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SPIWrite 0302,02,0,7
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SPIWrite 0305,e1,0,7
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SPIWrite 0309,00,0,7
SPIWrite 030a,c5,0,7
SPIWrite 030b,b2,0,7
SPIWrite 030c,65,0,7
SPIWrite 030d,70,0,7
SPIWrite 030e,84,0,7
SPIWrite 030f,f8,0,7
SPIWrite 0310,02,0,7
SPIWrite 0311,90,0,7
SPIWrite 0312,d8,0,7
SPIWrite 0313,f8,0,7
SPIWrite 0314,08,0,7
SPIWrite 0315,14,0,7
SPIWrite 0316,48,0,7
SPIWrite 0317,46,0,7
SPIWrite 0318,88,0,7
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SPIWrite 031c,07,0,7
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SPIWrite 031e,d8,0,7
SPIWrite 031f,f8,0,7
SPIWrite 0320,08,0,7
SPIWrite 0321,14,0,7
SPIWrite 0322,88,0,7
SPIWrite 0323,47,0,7
SPIWrite 0324,ff,0,7
SPIWrite 0325,f7,0,7
SPIWrite 0326,94,0,7
SPIWrite 0327,fe,0,7
SPIWrite 0328,28,0,7
SPIWrite 0329,e2,0,7
SPIWrite 032a,0b,0,7
SPIWrite 032b,eb,0,7
SPIWrite 032c,05,0,7
SPIWrite 032d,00,0,7
SPIWrite 032e,c5,0,7
SPIWrite 032f,b2,0,7
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SPIWrite 05e3,0f,0,7
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SPIWrite 0a96,18,0,7
SPIWrite 0a97,75,0,7
SPIWrite 0a98,98,0,7
SPIWrite 0a99,76,0,7
SPIWrite 0a9a,24,0,7
SPIWrite 0a9b,4c,0,7
SPIWrite 0a9c,58,0,7
SPIWrite 0a9d,75,0,7
SPIWrite 0a9e,1e,0,7
SPIWrite 0a9f,4d,0,7
SPIWrite 0aa0,c2,0,7
SPIWrite 0aa1,f8,0,7
SPIWrite 0aa2,00,0,7
SPIWrite 0aa3,42,0,7
SPIWrite 0aa4,27,0,7
SPIWrite 0aa5,24,0,7
SPIWrite 0aa6,5c,0,7
SPIWrite 0aa7,76,0,7
SPIWrite 0aa8,1c,0,7
SPIWrite 0aa9,4c,0,7
SPIWrite 0aaa,c5,0,7
SPIWrite 0aab,f8,0,7
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SPIWrite 0aae,1c,0,7
SPIWrite 0aaf,4b,0,7
SPIWrite 0ab0,c5,0,7
SPIWrite 0ab1,f8,0,7
SPIWrite 0ab2,b8,0,7
SPIWrite 0ab3,30,0,7
SPIWrite 0ab4,1b,0,7
SPIWrite 0ab5,4c,0,7
SPIWrite 0ab6,c5,0,7
SPIWrite 0ab7,f8,0,7
SPIWrite 0ab8,bc,0,7
SPIWrite 0ab9,40,0,7
SPIWrite 0aba,1b,0,7
SPIWrite 0abb,4b,0,7
SPIWrite 0abc,c5,0,7
SPIWrite 0abd,f8,0,7
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SPIWrite 0abe,c0,0,7
SPIWrite 0abf,30,0,7
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SPIWrite 0ac1,22,0,7
SPIWrite 0ac2,0a,0,7
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SPIWrite 0ac4,1b,0,7
SPIWrite 0ac5,4c,0,7
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SPIWrite 0ac9,41,0,7
SPIWrite 0aca,19,0,7
SPIWrite 0acb,4b,0,7
SPIWrite 0acc,58,0,7
SPIWrite 0acd,60,0,7
SPIWrite 0ace,98,0,7
SPIWrite 0acf,60,0,7
SPIWrite 0ad0,4a,0,7
SPIWrite 0ad1,70,0,7
SPIWrite 0ad2,8a,0,7
SPIWrite 0ad3,70,0,7
SPIWrite 0ad4,c8,0,7
SPIWrite 0ad5,70,0,7
SPIWrite 0ad6,08,0,7
SPIWrite 0ad7,71,0,7
SPIWrite 0ad8,48,0,7
SPIWrite 0ad9,71,0,7
SPIWrite 0ada,88,0,7
SPIWrite 0adb,71,0,7
SPIWrite 0adc,0a,0,7
SPIWrite 0add,72,0,7
SPIWrite 0ade,0a,0,7
SPIWrite 0adf,74,0,7
SPIWrite 0ae0,ca,0,7
SPIWrite 0ae1,74,0,7
SPIWrite 0ae2,38,0,7
SPIWrite 0ae3,bd,0,7
SPIWrite 0ae4,00,0,7
SPIWrite 0ae5,e4,0,7
SPIWrite 0ae6,00,0,7
SPIWrite 0ae7,e0,0,7
SPIWrite 0ae8,00,0,7
SPIWrite 0ae9,00,0,7
SPIWrite 0aea,01,0,7
SPIWrite 0aeb,20,0,7
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SPIWrite 0aed,52,0,7
SPIWrite 0aee,00,0,7
SPIWrite 0aef,20,0,7
SPIWrite 0af0,03,0,7
SPIWrite 0af1,8c,0,7
SPIWrite 0af2,02,0,7
SPIWrite 0af3,00,0,7
SPIWrite 0af4,19,0,7
SPIWrite 0af5,8b,0,7
SPIWrite 0af6,02,0,7
SPIWrite 0af7,00,0,7
SPIWrite 0af8,8d,0,7
SPIWrite 0af9,8b,0,7
SPIWrite 0afa,02,0,7
SPIWrite 0afb,00,0,7
SPIWrite 0afc,c1,0,7
SPIWrite 0afd,8c,0,7
SPIWrite 0afe,02,0,7
SPIWrite 0aff,00,0,7
SPIWrite 0b00,99,0,7
SPIWrite 0b01,8e,0,7
SPIWrite 0b02,02,0,7
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SPIWrite 0b03,00,0,7
SPIWrite 0b04,5d,0,7
SPIWrite 0b05,8e,0,7
SPIWrite 0b06,02,0,7
SPIWrite 0b07,00,0,7
SPIWrite 0b08,cd,0,7
SPIWrite 0b09,8d,0,7
SPIWrite 0b0a,02,0,7
SPIWrite 0b0b,00,0,7
SPIWrite 0b0c,09,0,7
SPIWrite 0b0d,8e,0,7
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SPIWrite 0b11,8f,0,7
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SPIWrite 0b15,8f,0,7
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SPIWrite 0b1e,02,0,7
SPIWrite 0b1f,00,0,7
SPIWrite 0b20,63,0,7
SPIWrite 0b21,89,0,7
SPIWrite 0b22,02,0,7
SPIWrite 0b23,00,0,7
SPIWrite 0b24,37,0,7
SPIWrite 0b25,88,0,7
SPIWrite 0b26,02,0,7
SPIWrite 0b27,00,0,7
SPIWrite 0b28,d1,0,7
SPIWrite 0b29,88,0,7
SPIWrite 0b2a,02,0,7
SPIWrite 0b2b,00,0,7
SPIWrite 0b2c,a5,0,7
SPIWrite 0b2d,8f,0,7
SPIWrite 0b2e,02,0,7
SPIWrite 0b2f,00,0,7
SPIWrite 0b30,40,0,7
SPIWrite 0b31,00,0,7
SPIWrite 0b32,01,0,7
SPIWrite 0b33,20,0,7
SPIWrite 0b34,ad,0,7
SPIWrite 0b35,87,0,7
SPIWrite 0b36,02,0,7
SPIWrite 0b37,00,0,7
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SPIWrite 0b3b,4d,0,7
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SPIWrite 0b3d,f8,0,7
SPIWrite 0b3e,e4,0,7
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SPIWrite 0b40,4f,0,7
SPIWrite 0b41,f0,0,7
SPIWrite 0b42,00,0,7
SPIWrite 0b43,0c,0,7
SPIWrite 0b44,60,0,7
SPIWrite 0b45,46,0,7
SPIWrite 0b46,2b,0,7
SPIWrite 0b47,78,0,7
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SPIWrite 0b49,f8,0,7
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SPIWrite 0b4d,1e,0,7
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SPIWrite 0b4f,e0,0,7
SPIWrite 0b50,02,0,7
SPIWrite 0b51,22,0,7
SPIWrite 0b52,c0,0,7
SPIWrite 0b53,f2,0,7
SPIWrite 0b54,00,0,7
SPIWrite 0b55,02,0,7
SPIWrite 0b56,52,0,7
SPIWrite 0b57,1e,0,7
SPIWrite 0b58,fd,0,7
SPIWrite 0b59,d1,0,7
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SPIWrite 0b5b,bf,0,7
SPIWrite 0b5c,00,0,7
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SPIWrite 0b5f,1c,0,7
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SPIWrite 0b61,b2,0,7
SPIWrite 0b62,11,0,7
SPIWrite 0b63,e0,0,7
SPIWrite 0b64,81,0,7
SPIWrite 0b65,00,0,7
SPIWrite 0b66,01,0,7
SPIWrite 0b67,eb,0,7
SPIWrite 0b68,c0,0,7
SPIWrite 0b69,01,0,7
SPIWrite 0b6a,6a,0,7
SPIWrite 0b6b,18,0,7
SPIWrite 0b6c,54,0,7
SPIWrite 0b6d,68,0,7
SPIWrite 0b6e,91,0,7
SPIWrite 0b6f,68,0,7
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SPIWrite 0b71,68,0,7
SPIWrite 0b72,d2,0,7
SPIWrite 0b73,68,0,7
SPIWrite 0b74,40,0,7
SPIWrite 0b75,1c,0,7
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SPIWrite 0b7c,22,0,7
SPIWrite 0b7d,60,0,7
SPIWrite 0b7e,86,0,7
SPIWrite 0b7f,42,0,7
SPIWrite 0b80,f0,0,7
SPIWrite 0b81,dc,0,7
SPIWrite 0b82,2a,0,7
SPIWrite 0b83,48,0,7
SPIWrite 0b84,01,0,7
SPIWrite 0b85,78,0,7
SPIWrite 0b86,60,0,7
SPIWrite 0b87,46,0,7
SPIWrite 0b88,81,0,7
SPIWrite 0b89,42,0,7
SPIWrite 0b8a,e1,0,7
SPIWrite 0b8b,dc,0,7
SPIWrite 0b8c,98,0,7
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SPIWrite 0b93,19,0,7
SPIWrite 0b94,51,0,7
SPIWrite 0b95,f8,0,7
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SPIWrite 0b97,2c,0,7
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SPIWrite 0b99,58,0,7
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SPIWrite 0b9b,f8,0,7
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SPIWrite 0b9d,1c,0,7
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SPIWrite 0ba7,f8,0,7
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SPIWrite 0bb2,4f,0,7
SPIWrite 0bb3,f0,0,7
SPIWrite 0bb4,00,0,7
SPIWrite 0bb5,0c,0,7
SPIWrite 0bb6,60,0,7
SPIWrite 0bb7,46,0,7
SPIWrite 0bb8,5c,0,7
SPIWrite 0bb9,78,0,7
SPIWrite 0bba,81,0,7
SPIWrite 0bbb,f8,0,7
SPIWrite 0bbc,00,0,7
SPIWrite 0bbd,c0,0,7
SPIWrite 0bbe,66,0,7
SPIWrite 0bbf,1e,0,7
SPIWrite 0bc0,19,0,7
SPIWrite 0bc1,e0,0,7
SPIWrite 0bc2,02,0,7
SPIWrite 0bc3,22,0,7
SPIWrite 0bc4,c0,0,7
SPIWrite 0bc5,f2,0,7
SPIWrite 0bc6,00,0,7
SPIWrite 0bc7,02,0,7
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SPIWrite 0bc9,1e,0,7
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SPIWrite 0bcc,00,0,7
SPIWrite 0bcd,bf,0,7
SPIWrite 0bce,00,0,7
SPIWrite 0bcf,bf,0,7
SPIWrite 0bd0,40,0,7
SPIWrite 0bd1,1c,0,7
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SPIWrite 0bd5,e0,0,7
SPIWrite 0bd6,81,0,7
SPIWrite 0bd7,00,0,7
SPIWrite 0bd8,01,0,7
SPIWrite 0bd9,eb,0,7
SPIWrite 0bda,c0,0,7
SPIWrite 0bdb,01,0,7
SPIWrite 0bdc,5a,0,7
SPIWrite 0bdd,18,0,7
SPIWrite 0bde,d2,0,7
SPIWrite 0bdf,f8,0,7
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SPIWrite 0be1,50,0,7
SPIWrite 0be2,d2,0,7
SPIWrite 0be3,f8,0,7
SPIWrite 0be4,98,0,7
SPIWrite 0be5,10,0,7
SPIWrite 0be6,2f,0,7
SPIWrite 0be7,68,0,7
SPIWrite 0be8,d2,0,7
SPIWrite 0be9,f8,0,7
SPIWrite 0bea,9c,0,7
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SPIWrite 0bf1,40,0,7
SPIWrite 0bf2,0a,0,7
SPIWrite 0bf3,43,0,7
SPIWrite 0bf4,2a,0,7
SPIWrite 0bf5,60,0,7
SPIWrite 0bf6,86,0,7
SPIWrite 0bf7,42,0,7
SPIWrite 0bf8,ed,0,7
SPIWrite 0bf9,dc,0,7
SPIWrite 0bfa,0c,0,7
SPIWrite 0bfb,48,0,7
SPIWrite 0bfc,01,0,7
SPIWrite 0bfd,78,0,7
SPIWrite 0bfe,60,0,7
SPIWrite 0bff,46,0,7
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SPIWrite 0c01,42,0,7
SPIWrite 0c02,de,0,7
SPIWrite 0c03,dc,0,7
SPIWrite 0c04,a0,0,7
SPIWrite 0c05,00,0,7
SPIWrite 0c06,00,0,7
SPIWrite 0c07,eb,0,7
SPIWrite 0c08,c4,0,7
SPIWrite 0c09,00,0,7
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SPIWrite 0c1b,40,0,7
SPIWrite 0c1c,01,0,7
SPIWrite 0c1d,43,0,7
SPIWrite 0c1e,11,0,7
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SPIWrite 0c21,bd,0,7
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SPIWrite 0c23,47,0,7
SPIWrite 0c24,97,0,7
SPIWrite 0c25,01,0,7
SPIWrite 0c26,00,0,7
SPIWrite 0c27,a2,0,7
SPIWrite 0c28,74,0,7
SPIWrite 0c29,4f,0,7
SPIWrite 0c2a,00,0,7
SPIWrite 0c2b,20,0,7
SPIWrite 0c2c,0f,0,7
SPIWrite 0c2d,00,0,7
SPIWrite 0c2e,01,0,7
SPIWrite 0c2f,20,0,7
SPIWrite 0c30,84,0,7
SPIWrite 0c31,46,0,7
SPIWrite 0c32,35,0,7
SPIWrite 0c33,48,0,7
SPIWrite 0c34,b0,0,7
SPIWrite 0c35,b5,0,7
SPIWrite 0c36,00,0,7
SPIWrite 0c37,f1,0,7
SPIWrite 0c38,0e,0,7
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SPIWrite 0c3f,d1,0,7
SPIWrite 0c40,2f,0,7
SPIWrite 0c41,4a,0,7
SPIWrite 0c42,30,0,7
SPIWrite 0c43,49,0,7
SPIWrite 0c44,d2,0,7
SPIWrite 0c45,f8,0,7
SPIWrite 0c46,e8,0,7
SPIWrite 0c47,3c,0,7
SPIWrite 0c48,dc,0,7
SPIWrite 0c49,0a,0,7
SPIWrite 0c4a,05,0,7
SPIWrite 0c4b,d3,0,7
SPIWrite 0c4c,92,0,7
SPIWrite 0c4d,f8,0,7
SPIWrite 0c4e,de,0,7
SPIWrite 0c4f,5c,0,7
SPIWrite 0c50,0c,0,7
SPIWrite 0c51,68,0,7
SPIWrite 0c52,65,0,7
SPIWrite 0c53,f3,0,7
SPIWrite 0c54,c3,0,7
SPIWrite 0c55,04,0,7
SPIWrite 0c56,0c,0,7
SPIWrite 0c57,60,0,7
SPIWrite 0c58,1c,0,7
SPIWrite 0c59,0b,0,7
SPIWrite 0c5a,05,0,7
SPIWrite 0c5b,d3,0,7
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SPIWrite 0c5c,92,0,7
SPIWrite 0c5d,f8,0,7
SPIWrite 0c5e,e2,0,7
SPIWrite 0c5f,5c,0,7
SPIWrite 0c60,0c,0,7
SPIWrite 0c61,68,0,7
SPIWrite 0c62,65,0,7
SPIWrite 0c63,f3,0,7
SPIWrite 0c64,04,0,7
SPIWrite 0c65,14,0,7
SPIWrite 0c66,0c,0,7
SPIWrite 0c67,60,0,7
SPIWrite 0c68,5c,0,7
SPIWrite 0c69,0b,0,7
SPIWrite 0c6a,05,0,7
SPIWrite 0c6b,d3,0,7
SPIWrite 0c6c,92,0,7
SPIWrite 0c6d,f8,0,7
SPIWrite 0c6e,df,0,7
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SPIWrite 0c79,0b,0,7
SPIWrite 0c7a,05,0,7
SPIWrite 0c7b,d3,0,7
SPIWrite 0c7c,92,0,7
SPIWrite 0c7d,f8,0,7
SPIWrite 0c7e,e0,0,7
SPIWrite 0c7f,5c,0,7
SPIWrite 0c80,8c,0,7
SPIWrite 0c81,68,0,7
SPIWrite 0c82,65,0,7
SPIWrite 0c83,f3,0,7
SPIWrite 0c84,41,0,7
SPIWrite 0c85,04,0,7
SPIWrite 0c86,8c,0,7
SPIWrite 0c87,60,0,7
SPIWrite 0c88,db,0,7
SPIWrite 0c89,0b,0,7
SPIWrite 0c8a,05,0,7
SPIWrite 0c8b,d3,0,7
SPIWrite 0c8c,92,0,7
SPIWrite 0c8d,f8,0,7
SPIWrite 0c8e,e1,0,7
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SPIWrite 0c93,f3,0,7
SPIWrite 0c94,41,0,7
SPIWrite 0c95,03,0,7
SPIWrite 0c96,cb,0,7
SPIWrite 0c97,60,0,7
SPIWrite 0c98,01,0,7
SPIWrite 0c99,25,0,7
SPIWrite 0c9a,92,0,7
SPIWrite 0c9b,f8,0,7
SPIWrite 0c9c,e2,0,7
SPIWrite 0c9d,3c,0,7
SPIWrite 0c9e,92,0,7
SPIWrite 0c9f,f8,0,7
SPIWrite 0ca0,de,0,7
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SPIWrite 0ca1,4c,0,7
SPIWrite 0ca2,92,0,7
SPIWrite 0ca3,f8,0,7
SPIWrite 0ca4,df,0,7
SPIWrite 0ca5,1c,0,7
SPIWrite 0ca6,92,0,7
SPIWrite 0ca7,f8,0,7
SPIWrite 0ca8,e0,0,7
SPIWrite 0ca9,7c,0,7
SPIWrite 0caa,85,0,7
SPIWrite 0cab,73,0,7
SPIWrite 0cac,83,0,7
SPIWrite 0cad,f0,0,7
SPIWrite 0cae,ff,0,7
SPIWrite 0caf,03,0,7
SPIWrite 0cb0,84,0,7
SPIWrite 0cb1,f0,0,7
SPIWrite 0cb2,ff,0,7
SPIWrite 0cb3,04,0,7
SPIWrite 0cb4,82,0,7
SPIWrite 0cb5,f8,0,7
SPIWrite 0cb6,e2,0,7
SPIWrite 0cb7,3c,0,7
SPIWrite 0cb8,81,0,7
SPIWrite 0cb9,f0,0,7
SPIWrite 0cba,ff,0,7
SPIWrite 0cbb,01,0,7
SPIWrite 0cbc,82,0,7
SPIWrite 0cbd,f8,0,7
SPIWrite 0cbe,de,0,7
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SPIWrite 0cc2,e1,0,7
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SPIWrite 0cc5,f8,0,7
SPIWrite 0cc6,df,0,7
SPIWrite 0cc7,1c,0,7
SPIWrite 0cc8,87,0,7
SPIWrite 0cc9,f0,0,7
SPIWrite 0cca,ff,0,7
SPIWrite 0ccb,00,0,7
SPIWrite 0ccc,82,0,7
SPIWrite 0ccd,f8,0,7
SPIWrite 0cce,e0,0,7
SPIWrite 0ccf,0c,0,7
SPIWrite 0cd0,85,0,7
SPIWrite 0cd1,f0,0,7
SPIWrite 0cd2,ff,0,7
SPIWrite 0cd3,03,0,7
SPIWrite 0cd4,82,0,7
SPIWrite 0cd5,f8,0,7
SPIWrite 0cd6,e1,0,7
SPIWrite 0cd7,3c,0,7
SPIWrite 0cd8,60,0,7
SPIWrite 0cd9,46,0,7
SPIWrite 0cda,f5,0,7
SPIWrite 0cdb,f7,0,7
SPIWrite 0cdc,38,0,7
SPIWrite 0cdd,fe,0,7
SPIWrite 0cde,b0,0,7
SPIWrite 0cdf,bd,0,7
SPIWrite 0ce0,10,0,7
SPIWrite 0ce1,b5,0,7
SPIWrite 0ce2,0b,0,7
SPIWrite 0ce3,4a,0,7
SPIWrite 0ce4,09,0,7
SPIWrite 0ce5,4c,0,7
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SPIWrite 0ce6,08,0,7
SPIWrite 0ce7,48,0,7
SPIWrite 0ce8,00,0,7
SPIWrite 0ce9,21,0,7
SPIWrite 0cea,c4,0,7
SPIWrite 0ceb,f8,0,7
SPIWrite 0cec,08,0,7
SPIWrite 0ced,24,0,7
SPIWrite 0cee,0e,0,7
SPIWrite 0cef,30,0,7
SPIWrite 0cf0,01,0,7
SPIWrite 0cf1,70,0,7
SPIWrite 0cf2,e7,0,7
SPIWrite 0cf3,f7,0,7
SPIWrite 0cf4,99,0,7
SPIWrite 0cf5,fa,0,7
SPIWrite 0cf6,07,0,7
SPIWrite 0cf7,49,0,7
SPIWrite 0cf8,c4,0,7
SPIWrite 0cf9,f8,0,7
SPIWrite 0cfa,08,0,7
SPIWrite 0cfb,14,0,7
SPIWrite 0cfc,10,0,7
SPIWrite 0cfd,bd,0,7
SPIWrite 0cfe,c0,0,7
SPIWrite 0cff,46,0,7
SPIWrite 0d00,d8,0,7
SPIWrite 0d01,33,0,7
SPIWrite 0d02,00,0,7
SPIWrite 0d03,20,0,7
SPIWrite 0d04,48,0,7
SPIWrite 0d05,00,0,7
SPIWrite 0d06,03,0,7
SPIWrite 0d07,a8,0,7
SPIWrite 0d08,00,0,7
SPIWrite 0d09,00,0,7
SPIWrite 0d0a,01,0,7
SPIWrite 0d0b,20,0,7
SPIWrite 0d0c,40,0,7
SPIWrite 0d0d,52,0,7
SPIWrite 0d0e,00,0,7
SPIWrite 0d0f,20,0,7
SPIWrite 0d10,11,0,7
SPIWrite 0d11,8c,0,7
SPIWrite 0d12,02,0,7
SPIWrite 0d13,00,0,7
SPIWrite 0d14,2f,0,7
SPIWrite 0d15,e9,0,7
SPIWrite 0d16,01,0,7
SPIWrite 0d17,00,0,7
SPIWrite 0d18,4a,0,7
SPIWrite 0d19,08,0,7
SPIWrite 0d1a,07,0,7
SPIWrite 0d1b,d3,0,7
SPIWrite 0d1c,4f,0,7
SPIWrite 0d1d,f0,0,7
SPIWrite 0d1e,f0,0,7
SPIWrite 0d1f,43,0,7
SPIWrite 0d20,d3,0,7
SPIWrite 0d21,f8,0,7
SPIWrite 0d22,04,0,7
SPIWrite 0d23,21,0,7
SPIWrite 0d24,60,0,7
SPIWrite 0d25,f3,0,7
SPIWrite 0d26,08,0,7
SPIWrite 0d27,22,0,7
SPIWrite 0d28,c3,0,7
SPIWrite 0d29,f8,0,7
SPIWrite 0d2a,04,0,7
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SPIWrite 0d2b,21,0,7
SPIWrite 0d2c,8a,0,7
SPIWrite 0d2d,08,0,7
SPIWrite 0d2e,07,0,7
SPIWrite 0d2f,d3,0,7
SPIWrite 0d30,4f,0,7
SPIWrite 0d31,f0,0,7
SPIWrite 0d32,f0,0,7
SPIWrite 0d33,43,0,7
SPIWrite 0d34,d3,0,7
SPIWrite 0d35,f8,0,7
SPIWrite 0d36,04,0,7
SPIWrite 0d37,21,0,7
SPIWrite 0d38,60,0,7
SPIWrite 0d39,f3,0,7
SPIWrite 0d3a,49,0,7
SPIWrite 0d3b,22,0,7
SPIWrite 0d3c,c3,0,7
SPIWrite 0d3d,f8,0,7
SPIWrite 0d3e,04,0,7
SPIWrite 0d3f,21,0,7
SPIWrite 0d40,27,0,7
SPIWrite 0d41,4a,0,7
SPIWrite 0d42,cb,0,7
SPIWrite 0d43,08,0,7
SPIWrite 0d44,03,0,7
SPIWrite 0d45,d3,0,7
SPIWrite 0d46,13,0,7
SPIWrite 0d47,68,0,7
SPIWrite 0d48,60,0,7
SPIWrite 0d49,f3,0,7
SPIWrite 0d4a,08,0,7
SPIWrite 0d4b,23,0,7
SPIWrite 0d4c,13,0,7
SPIWrite 0d4d,60,0,7
SPIWrite 0d4e,09,0,7
SPIWrite 0d4f,09,0,7
SPIWrite 0d50,03,0,7
SPIWrite 0d51,d3,0,7
SPIWrite 0d52,11,0,7
SPIWrite 0d53,68,0,7
SPIWrite 0d54,60,0,7
SPIWrite 0d55,f3,0,7
SPIWrite 0d56,49,0,7
SPIWrite 0d57,21,0,7
SPIWrite 0d58,11,0,7
SPIWrite 0d59,60,0,7
SPIWrite 0d5a,70,0,7
SPIWrite 0d5b,47,0,7
SPIWrite 0d5c,b0,0,7
SPIWrite 0d5d,b5,0,7
SPIWrite 0d5e,21,0,7
SPIWrite 0d5f,4c,0,7
SPIWrite 0d60,04,0,7
SPIWrite 0d61,f1,0,7
SPIWrite 0d62,08,0,7
SPIWrite 0d63,05,0,7
SPIWrite 0d64,22,0,7
SPIWrite 0d65,7b,0,7
SPIWrite 0d66,63,0,7
SPIWrite 0d67,78,0,7
SPIWrite 0d68,29,0,7
SPIWrite 0d69,68,0,7
SPIWrite 0d6a,00,0,7
SPIWrite 0d6b,20,0,7
SPIWrite 0d6c,9a,0,7
SPIWrite 0d6d,42,0,7
SPIWrite 0d6e,01,0,7
SPIWrite 0d6f,f1,0,7
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SPIWrite 0d70,01,0,7
SPIWrite 0d71,01,0,7
SPIWrite 0d72,29,0,7
SPIWrite 0d73,60,0,7
SPIWrite 0d74,08,0,7
SPIWrite 0d75,bf,0,7
SPIWrite 0d76,01,0,7
SPIWrite 0d77,20,0,7
SPIWrite 0d78,e1,0,7
SPIWrite 0d79,78,0,7
SPIWrite 0d7a,ff,0,7
SPIWrite 0d7b,f7,0,7
SPIWrite 0d7c,cd,0,7
SPIWrite 0d7d,ff,0,7
SPIWrite 0d7e,60,0,7
SPIWrite 0d7f,78,0,7
SPIWrite 0d80,00,0,7
SPIWrite 0d81,27,0,7
SPIWrite 0d82,00,0,7
SPIWrite 0d83,b9,0,7
SPIWrite 0d84,01,0,7
SPIWrite 0d85,27,0,7
SPIWrite 0d86,18,0,7
SPIWrite 0d87,49,0,7
SPIWrite 0d88,00,0,7
SPIWrite 0d89,22,0,7
SPIWrite 0d8a,67,0,7
SPIWrite 0d8b,70,0,7
SPIWrite 0d8c,07,0,7
SPIWrite 0d8d,b9,0,7
SPIWrite 0d8e,01,0,7
SPIWrite 0d8f,22,0,7
SPIWrite 0d90,08,0,7
SPIWrite 0d91,68,0,7
SPIWrite 0d92,20,0,7
SPIWrite 0d93,f0,0,7
SPIWrite 0d94,04,0,7
SPIWrite 0d95,00,0,7
SPIWrite 0d96,40,0,7
SPIWrite 0d97,ea,0,7
SPIWrite 0d98,82,0,7
SPIWrite 0d99,00,0,7
SPIWrite 0d9a,08,0,7
SPIWrite 0d9b,60,0,7
SPIWrite 0d9c,b0,0,7
SPIWrite 0d9d,bd,0,7
SPIWrite 0d9e,b0,0,7
SPIWrite 0d9f,b5,0,7
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SPIWrite 0da1,4c,0,7
SPIWrite 0da2,25,0,7
SPIWrite 0da3,1d,0,7
SPIWrite 0da4,22,0,7
SPIWrite 0da5,7b,0,7
SPIWrite 0da6,23,0,7
SPIWrite 0da7,78,0,7
SPIWrite 0da8,29,0,7
SPIWrite 0da9,68,0,7
SPIWrite 0daa,00,0,7
SPIWrite 0dab,20,0,7
SPIWrite 0dac,9a,0,7
SPIWrite 0dad,42,0,7
SPIWrite 0dae,01,0,7
SPIWrite 0daf,f1,0,7
SPIWrite 0db0,01,0,7
SPIWrite 0db1,01,0,7
SPIWrite 0db2,29,0,7
SPIWrite 0db3,60,0,7
SPIWrite 0db4,08,0,7
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SPIWrite 0db5,bf,0,7
SPIWrite 0db6,01,0,7
SPIWrite 0db7,20,0,7
SPIWrite 0db8,a1,0,7
SPIWrite 0db9,78,0,7
SPIWrite 0dba,ff,0,7
SPIWrite 0dbb,f7,0,7
SPIWrite 0dbc,ad,0,7
SPIWrite 0dbd,ff,0,7
SPIWrite 0dbe,20,0,7
SPIWrite 0dbf,78,0,7
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SPIWrite 0dc1,27,0,7
SPIWrite 0dc2,00,0,7
SPIWrite 0dc3,b9,0,7
SPIWrite 0dc4,01,0,7
SPIWrite 0dc5,27,0,7
SPIWrite 0dc6,08,0,7
SPIWrite 0dc7,49,0,7
SPIWrite 0dc8,00,0,7
SPIWrite 0dc9,22,0,7
SPIWrite 0dca,27,0,7
SPIWrite 0dcb,70,0,7
SPIWrite 0dcc,07,0,7
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SPIWrite 0dcf,22,0,7
SPIWrite 0dd0,08,0,7
SPIWrite 0dd1,68,0,7
SPIWrite 0dd2,20,0,7
SPIWrite 0dd3,f0,0,7
SPIWrite 0dd4,02,0,7
SPIWrite 0dd5,00,0,7
SPIWrite 0dd6,40,0,7
SPIWrite 0dd7,ea,0,7
SPIWrite 0dd8,42,0,7
SPIWrite 0dd9,00,0,7
SPIWrite 0dda,08,0,7
SPIWrite 0ddb,60,0,7
SPIWrite 0ddc,b0,0,7
SPIWrite 0ddd,bd,0,7
SPIWrite 0dde,c0,0,7
SPIWrite 0ddf,46,0,7
SPIWrite 0de0,04,0,7
SPIWrite 0de1,01,0,7
SPIWrite 0de2,00,0,7
SPIWrite 0de3,f8,0,7
SPIWrite 0de4,40,0,7
SPIWrite 0de5,00,0,7
SPIWrite 0de6,01,0,7
SPIWrite 0de7,20,0,7
SPIWrite 0de8,70,0,7
SPIWrite 0de9,01,0,7
SPIWrite 0dea,02,0,7
SPIWrite 0deb,a8,0,7
SPIWrite 0dec,21,0,7
SPIWrite 0ded,48,0,7
SPIWrite 0dee,10,0,7
SPIWrite 0def,b5,0,7
SPIWrite 0df0,df,0,7
SPIWrite 0df1,f7,0,7
SPIWrite 0df2,14,0,7
SPIWrite 0df3,fc,0,7
SPIWrite 0df4,4f,0,7
SPIWrite 0df5,f0,0,7
SPIWrite 0df6,2e,0,7
SPIWrite 0df7,40,0,7
SPIWrite 0df8,d0,0,7
SPIWrite 0df9,f8,0,7
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SPIWrite 0dfa,f8,0,7
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SPIWrite 0dfc,1e,0,7
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SPIWrite 0dff,f8,0,7
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SPIWrite 0e02,4f,0,7
SPIWrite 0e03,f0,0,7
SPIWrite 0e04,2f,0,7
SPIWrite 0e05,44,0,7
SPIWrite 0e06,6f,0,7
SPIWrite 0e07,f3,0,7
SPIWrite 0e08,9f,0,7
SPIWrite 0e09,42,0,7
SPIWrite 0e0a,6f,0,7
SPIWrite 0e0b,f3,0,7
SPIWrite 0e0c,9f,0,7
SPIWrite 0e0d,41,0,7
SPIWrite 0e0e,1a,0,7
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SPIWrite 0e11,f8,0,7
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SPIWrite 0e16,6f,0,7
SPIWrite 0e17,f3,0,7
SPIWrite 0e18,9f,0,7
SPIWrite 0e19,40,0,7
SPIWrite 0e1a,d4,0,7
SPIWrite 0e1b,f8,0,7
SPIWrite 0e1c,58,0,7
SPIWrite 0e1d,16,0,7
SPIWrite 0e1e,98,0,7
SPIWrite 0e1f,62,0,7
SPIWrite 0e20,6f,0,7
SPIWrite 0e21,f3,0,7
SPIWrite 0e22,9f,0,7
SPIWrite 0e23,41,0,7
SPIWrite 0e24,d9,0,7
SPIWrite 0e25,62,0,7
SPIWrite 0e26,10,0,7
SPIWrite 0e27,bd,0,7
SPIWrite 0e28,12,0,7
SPIWrite 0e29,48,0,7
SPIWrite 0e2a,10,0,7
SPIWrite 0e2b,b5,0,7
SPIWrite 0e2c,df,0,7
SPIWrite 0e2d,f7,0,7
SPIWrite 0e2e,ac,0,7
SPIWrite 0e2f,ff,0,7
SPIWrite 0e30,4f,0,7
SPIWrite 0e31,f0,0,7
SPIWrite 0e32,2e,0,7
SPIWrite 0e33,42,0,7
SPIWrite 0e34,10,0,7
SPIWrite 0e35,48,0,7
SPIWrite 0e36,d2,0,7
SPIWrite 0e37,f8,0,7
SPIWrite 0e38,f8,0,7
SPIWrite 0e39,32,0,7
SPIWrite 0e3a,01,0,7
SPIWrite 0e3b,6a,0,7
SPIWrite 0e3c,61,0,7
SPIWrite 0e3d,f3,0,7
SPIWrite 0e3e,11,0,7
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SPIWrite 0e3f,03,0,7
SPIWrite 0e40,c2,0,7
SPIWrite 0e41,f8,0,7
SPIWrite 0e42,f8,0,7
SPIWrite 0e43,32,0,7
SPIWrite 0e44,41,0,7
SPIWrite 0e45,6a,0,7
SPIWrite 0e46,d2,0,7
SPIWrite 0e47,f8,0,7
SPIWrite 0e48,58,0,7
SPIWrite 0e49,46,0,7
SPIWrite 0e4a,4f,0,7
SPIWrite 0e4b,f0,0,7
SPIWrite 0e4c,2f,0,7
SPIWrite 0e4d,43,0,7
SPIWrite 0e4e,61,0,7
SPIWrite 0e4f,f3,0,7
SPIWrite 0e50,11,0,7
SPIWrite 0e51,04,0,7
SPIWrite 0e52,81,0,7
SPIWrite 0e53,6a,0,7
SPIWrite 0e54,c2,0,7
SPIWrite 0e55,f8,0,7
SPIWrite 0e56,58,0,7
SPIWrite 0e57,46,0,7
SPIWrite 0e58,c0,0,7
SPIWrite 0e59,6a,0,7
SPIWrite 0e5a,d3,0,7
SPIWrite 0e5b,f8,0,7
SPIWrite 0e5c,f8,0,7
SPIWrite 0e5d,22,0,7
SPIWrite 0e5e,61,0,7
SPIWrite 0e5f,f3,0,7
SPIWrite 0e60,11,0,7
SPIWrite 0e61,02,0,7
SPIWrite 0e62,c3,0,7
SPIWrite 0e63,f8,0,7
SPIWrite 0e64,f8,0,7
SPIWrite 0e65,22,0,7
SPIWrite 0e66,d3,0,7
SPIWrite 0e67,f8,0,7
SPIWrite 0e68,58,0,7
SPIWrite 0e69,16,0,7
SPIWrite 0e6a,60,0,7
SPIWrite 0e6b,f3,0,7
SPIWrite 0e6c,11,0,7
SPIWrite 0e6d,01,0,7
SPIWrite 0e6e,c3,0,7
SPIWrite 0e6f,f8,0,7
SPIWrite 0e70,58,0,7
SPIWrite 0e71,16,0,7
SPIWrite 0e72,10,0,7
SPIWrite 0e73,bd,0,7
SPIWrite 0e74,b2,0,7
SPIWrite 0e75,43,0,7
SPIWrite 0e76,00,0,7
SPIWrite 0e77,20,0,7
SPIWrite 0e78,00,0,7
SPIWrite 0e79,00,0,7
SPIWrite 0e7a,01,0,7
SPIWrite 0e7b,20,0,7
SPIWrite 0e7c,38,0,7
SPIWrite 0e7d,b5,0,7
SPIWrite 0e7e,1d,0,7
SPIWrite 0e7f,4c,0,7
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SPIWrite 0e81,f1,0,7
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SPIWrite 0e83,00,0,7
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SPIWrite 0e84,00,0,7
SPIWrite 0e85,78,0,7
SPIWrite 0e86,03,0,7
SPIWrite 0e87,28,0,7
SPIWrite 0e88,02,0,7
SPIWrite 0e89,d0,0,7
SPIWrite 0e8a,f0,0,7
SPIWrite 0e8b,f7,0,7
SPIWrite 0e8c,e7,0,7
SPIWrite 0e8d,fe,0,7
SPIWrite 0e8e,38,0,7
SPIWrite 0e8f,bd,0,7
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SPIWrite 0e91,25,0,7
SPIWrite 0e92,84,0,7
SPIWrite 0e93,f8,0,7
SPIWrite 0e94,70,0,7
SPIWrite 0e95,50,0,7
SPIWrite 0e96,f0,0,7
SPIWrite 0e97,f7,0,7
SPIWrite 0e98,e1,0,7
SPIWrite 0e99,fe,0,7
SPIWrite 0e9a,02,0,7
SPIWrite 0e9b,20,0,7
SPIWrite 0e9c,84,0,7
SPIWrite 0e9d,f8,0,7
SPIWrite 0e9e,70,0,7
SPIWrite 0e9f,00,0,7
SPIWrite 0ea0,f0,0,7
SPIWrite 0ea1,f7,0,7
SPIWrite 0ea2,dc,0,7
SPIWrite 0ea3,fe,0,7
SPIWrite 0ea4,03,0,7
SPIWrite 0ea5,20,0,7
SPIWrite 0ea6,84,0,7
SPIWrite 0ea7,f8,0,7
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SPIWrite 0ea9,00,0,7
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SPIWrite 0eab,f0,0,7
SPIWrite 0eac,b0,0,7
SPIWrite 0ead,41,0,7
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SPIWrite 0eba,0e,0,7
SPIWrite 0ebb,4c,0,7
SPIWrite 0ebc,04,0,7
SPIWrite 0ebd,f1,0,7
SPIWrite 0ebe,70,0,7
SPIWrite 0ebf,00,0,7
SPIWrite 0ec0,00,0,7
SPIWrite 0ec1,78,0,7
SPIWrite 0ec2,03,0,7
SPIWrite 0ec3,28,0,7
SPIWrite 0ec4,02,0,7
SPIWrite 0ec5,d0,0,7
SPIWrite 0ec6,f0,0,7
SPIWrite 0ec7,f7,0,7
SPIWrite 0ec8,7d,0,7
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SPIWrite 0ec9,ff,0,7
SPIWrite 0eca,70,0,7
SPIWrite 0ecb,bd,0,7
SPIWrite 0ecc,01,0,7
SPIWrite 0ecd,20,0,7
SPIWrite 0ece,84,0,7
SPIWrite 0ecf,f8,0,7
SPIWrite 0ed0,70,0,7
SPIWrite 0ed1,00,0,7
SPIWrite 0ed2,f0,0,7
SPIWrite 0ed3,f7,0,7
SPIWrite 0ed4,77,0,7
SPIWrite 0ed5,ff,0,7
SPIWrite 0ed6,4f,0,7
SPIWrite 0ed7,f0,0,7
SPIWrite 0ed8,b0,0,7
SPIWrite 0ed9,46,0,7
SPIWrite 0eda,02,0,7
SPIWrite 0edb,20,0,7
SPIWrite 0edc,96,0,7
SPIWrite 0edd,f8,0,7
SPIWrite 0ede,45,0,7
SPIWrite 0edf,51,0,7
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SPIWrite 0ee1,f8,0,7
SPIWrite 0ee2,70,0,7
SPIWrite 0ee3,00,0,7
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SPIWrite 0ee5,f7,0,7
SPIWrite 0ee6,6e,0,7
SPIWrite 0ee7,ff,0,7
SPIWrite 0ee8,03,0,7
SPIWrite 0ee9,20,0,7
SPIWrite 0eea,84,0,7
SPIWrite 0eeb,f8,0,7
SPIWrite 0eec,70,0,7
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SPIWrite 0eee,86,0,7
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SPIWrite 0ef1,51,0,7
SPIWrite 0ef2,70,0,7
SPIWrite 0ef3,bd,0,7
SPIWrite 0ef4,d8,0,7
SPIWrite 0ef5,33,0,7
SPIWrite 0ef6,00,0,7
SPIWrite 0ef7,20,0,7
SPIWrite 0ef8,80,0,7
SPIWrite 0ef9,b5,0,7
SPIWrite 0efa,17,0,7
SPIWrite 0efb,49,0,7
SPIWrite 0efc,15,0,7
SPIWrite 0efd,48,0,7
SPIWrite 0efe,8a,0,7
SPIWrite 0eff,7e,0,7
SPIWrite 0f00,00,0,7
SPIWrite 0f01,68,0,7
SPIWrite 0f02,01,0,7
SPIWrite 0f03,2a,0,7
SPIWrite 0f04,00,0,7
SPIWrite 0f05,f0,0,7
SPIWrite 0f06,3f,0,7
SPIWrite 0f07,00,0,7
SPIWrite 0f08,c0,0,7
SPIWrite 0f09,f3,0,7
SPIWrite 0f0a,c2,0,7
SPIWrite 0f0b,07,0,7
SPIWrite 0f0c,21,0,7
SPIWrite 0f0d,d1,0,7
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SPIWrite 0f0f,f0,0,7
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SPIWrite 0f11,00,0,7
SPIWrite 0f12,0b,0,7
SPIWrite 0f13,d0,0,7
SPIWrite 0f14,40,0,7
SPIWrite 0f15,1e,0,7
SPIWrite 0f16,07,0,7
SPIWrite 0f17,d0,0,7
SPIWrite 0f18,40,0,7
SPIWrite 0f19,1e,0,7
SPIWrite 0f1a,03,0,7
SPIWrite 0f1b,d0,0,7
SPIWrite 0f1c,40,0,7
SPIWrite 0f1d,1e,0,7
SPIWrite 0f1e,08,0,7
SPIWrite 0f1f,d1,0,7
SPIWrite 0f20,88,0,7
SPIWrite 0f21,7f,0,7
SPIWrite 0f22,04,0,7
SPIWrite 0f23,e0,0,7
SPIWrite 0f24,48,0,7
SPIWrite 0f25,7f,0,7
SPIWrite 0f26,02,0,7
SPIWrite 0f27,e0,0,7
SPIWrite 0f28,08,0,7
SPIWrite 0f29,7f,0,7
SPIWrite 0f2a,00,0,7
SPIWrite 0f2b,e0,0,7
SPIWrite 0f2c,c8,0,7
SPIWrite 0f2d,7e,0,7
SPIWrite 0f2e,0b,0,7
SPIWrite 0f2f,4a,0,7
SPIWrite 0f30,10,0,7
SPIWrite 0f31,70,0,7
SPIWrite 0f32,5f,0,7
SPIWrite 0f33,b1,0,7
SPIWrite 0f34,7f,0,7
SPIWrite 0f35,1e,0,7
SPIWrite 0f36,07,0,7
SPIWrite 0f37,d0,0,7
SPIWrite 0f38,7f,0,7
SPIWrite 0f39,1e,0,7
SPIWrite 0f3a,03,0,7
SPIWrite 0f3b,d0,0,7
SPIWrite 0f3c,7f,0,7
SPIWrite 0f3d,1e,0,7
SPIWrite 0f3e,08,0,7
SPIWrite 0f3f,d1,0,7
SPIWrite 0f40,88,0,7
SPIWrite 0f41,7f,0,7
SPIWrite 0f42,04,0,7
SPIWrite 0f43,e0,0,7
SPIWrite 0f44,48,0,7
SPIWrite 0f45,7f,0,7
SPIWrite 0f46,02,0,7
SPIWrite 0f47,e0,0,7
SPIWrite 0f48,08,0,7
SPIWrite 0f49,7f,0,7
SPIWrite 0f4a,00,0,7
SPIWrite 0f4b,e0,0,7
SPIWrite 0f4c,c8,0,7
SPIWrite 0f4d,7e,0,7
SPIWrite 0f4e,04,0,7
SPIWrite 0f4f,49,0,7
SPIWrite 0f50,08,0,7
SPIWrite 0f51,70,0,7
SPIWrite 0f52,80,0,7
```

```
SPIWrite 0f53,bd,0,7
SPIWrite 0f54,d4,0,7
SPIWrite 0f55,06,0,7
SPIWrite 0f56,06,0,7
SPIWrite 0f57,a8,0,7
SPIWrite 0f58,00,0,7
SPIWrite 0f59,00,0,7
SPIWrite 0f5a,01,0,7
SPIWrite 0f5b,20,0,7
SPIWrite 0f5c,50,0,7
SPIWrite 0f5d,01,0,7
SPIWrite 0f5e,00,0,7
SPIWrite 0f5f,ae,0,7
SPIWrite 0f60,50,0,7
SPIWrite 0f61,01,0,7
SPIWrite 0f62,00,0,7
SPIWrite 0f63,af,0,7
SPIWrite 0f64,15,0,7
SPIWrite 0f65,48,0,7
SPIWrite 0f66,08,0,7
SPIWrite 0f67,b5,0,7
SPIWrite 0f68,ea,0,7
SPIWrite 0f69,f7,0,7
SPIWrite 0f6a,6c,0,7
SPIWrite 0f6b,f9,0,7
SPIWrite 0f6c,4f,0,7
SPIWrite 0f6d,f0,0,7
SPIWrite 0f6e,2e,0,7
SPIWrite 0f6f,41,0,7
SPIWrite 0f70,13,0,7
SPIWrite 0f71,48,0,7
SPIWrite 0f72,d1,0,7
SPIWrite 0f73,f8,0,7
SPIWrite 0f74,98,0,7
SPIWrite 0f75,29,0,7
SPIWrite 0f76,d1,0,7
SPIWrite 0f77,f8,0,7
SPIWrite 0f78,b8,0,7
SPIWrite 0f79,1b,0,7
SPIWrite 0f7a,02,0,7
SPIWrite 0f7b,63,0,7
SPIWrite 0f7c,4f,0,7
SPIWrite 0f7d,f0,0,7
SPIWrite 0f7e,2f,0,7
SPIWrite 0f7f,42,0,7
SPIWrite 0f80,41,0,7
SPIWrite 0f81,63,0,7
SPIWrite 0f82,d2,0,7
SPIWrite 0f83,f8,0,7
SPIWrite 0f84,98,0,7
SPIWrite 0f85,19,0,7
SPIWrite 0f86,81,0,7
SPIWrite 0f87,63,0,7
SPIWrite 0f88,d2,0,7
SPIWrite 0f89,f8,0,7
SPIWrite 0f8a,b8,0,7
SPIWrite 0f8b,1b,0,7
SPIWrite 0f8c,c1,0,7
SPIWrite 0f8d,63,0,7
SPIWrite 0f8e,08,0,7
SPIWrite 0f8f,bd,0,7
SPIWrite 0f90,0a,0,7
SPIWrite 0f91,48,0,7
SPIWrite 0f92,08,0,7
SPIWrite 0f93,b5,0,7
SPIWrite 0f94,ea,0,7
SPIWrite 0f95,f7,0,7
SPIWrite 0f96,b8,0,7
SPIWrite 0f97,fa,0,7
```

```
SPIWrite 0f98,09,0,7
SPIWrite 0f99,48,0,7
SPIWrite 0f9a,4f,0,7
SPIWrite 0f9b,f0,0,7
SPIWrite 0f9c,2e,0,7
SPIWrite 0f9d,43,0,7
SPIWrite 0f9e,01,0,7
SPIWrite 0f9f,6b,0,7
SPIWrite 0fa0,42,0,7
SPIWrite 0fa1,6b,0,7
SPIWrite 0fa2,c3,0,7
SPIWrite 0fa3,f8,0,7
SPIWrite 0fa4,98,0,7
SPIWrite 0fa5,19,0,7
SPIWrite 0fa6,81,0,7
SPIWrite 0fa7,6b,0,7
SPIWrite 0fa8,c3,0,7
SPIWrite 0fa9,f8,0,7
SPIWrite 0faa,b8,0,7
SPIWrite 0fab,2b,0,7
SPIWrite 0fac,4f,0,7
SPIWrite 0fad,f0,0,7
SPIWrite 0fae,2f,0,7
SPIWrite 0faf,42,0,7
SPIWrite 0fb0,c2,0,7
SPIWrite 0fb1,f8,0,7
SPIWrite 0fb2,98,0,7
SPIWrite 0fb3,19,0,7
SPIWrite 0fb4,c0,0,7
SPIWrite 0fb5,6b,0,7
SPIWrite 0fb6,c2,0,7
SPIWrite 0fb7,f8,0,7
SPIWrite 0fb8,b8,0,7
SPIWrite 0fb9,0b,0,7
SPIWrite 0fba,08,0,7
SPIWrite 0fbb,bd,0,7
SPIWrite 0fbc,b2,0,7
SPIWrite 0fbd,43,0,7
SPIWrite 0fbe,00,0,7
SPIWrite 0fbf,20,0,7
SPIWrite 0fc0,00,0,7
SPIWrite 0fc1,00,0,7
SPIWrite 0fc2,01,0,7
SPIWrite 0fc3,20,0,7
SPIWrite 0fc4,2d,0,7
SPIWrite 0fc5,e9,0,7
SPIWrite 0fc6,8e,0,7
SPIWrite 0fc7,41,0,7
SPIWrite 0fc8,80,0,7
SPIWrite 0fc9,46,0,7
SPIWrite 0fca,1f,0,7
SPIWrite 0fcb,46,0,7
SPIWrite 0fcc,68,0,7
SPIWrite 0fcd,46,0,7
SPIWrite 0fce,f0,0,7
SPIWrite 0fcf,f7,0,7
SPIWrite 0fd0,70,0,7
SPIWrite 0fd1,fa,0,7
SPIWrite 0fd2,00,0,7
SPIWrite 0fd3,2f,0,7
SPIWrite 0fd4,14,0,7
SPIWrite 0fd5,bf,0,7
SPIWrite 0fd6,04,0,7
SPIWrite 0fd7,20,0,7
SPIWrite 0fd8,08,0,7
SPIWrite 0fd9,20,0,7
SPIWrite 0fda,bd,0,7
SPIWrite 0fdb,f8,0,7
SPIWrite 0fdc,06,0,7
```

```
SPIWrite 0fdd,10,0,7
SPIWrite 0fde,02,0,7
SPIWrite 0fdf,29,0,7
SPIWrite 0fe0,0e,0,7
SPIWrite 0fe1,d1,0,7
SPIWrite 0fe2,bd,0,7
SPIWrite 0fe3,f9,0,7
SPIWrite 0fe4,04,0,7
SPIWrite 0fe5,10,0,7
SPIWrite 0fe6,11,0,7
SPIWrite 0fe7,fb,0,7
SPIWrite 0fe8,00,0,7
SPIWrite 0fe9,f1,0,7
SPIWrite 0fea,ad,0,7
SPIWrite 0feb,f8,0,7
SPIWrite 0fec,04,0,7
SPIWrite 0fed,10,0,7
SPIWrite 0fee,9d,0,7
SPIWrite 0fef,f8,0,7
SPIWrite 0ff0,08,0,7
SPIWrite 0ff1,10,0,7
SPIWrite 0ff2,47,0,7
SPIWrite 0ff3,00,0,7
SPIWrite 0ff4,c9,0,7
SPIWrite 0ff5,19,0,7
SPIWrite 0ff6,ad,0,7
SPIWrite 0ff7,f8,0,7
SPIWrite 0ff8,06,0,7
SPIWrite 0ff9,10,0,7
SPIWrite 0ffa,00,0,7
SPIWrite 0ffb,23,0,7
SPIWrite 0ffc,8d,0,7
SPIWrite 0ffd,f8,0,7
SPIWrite 0ffe,08,0,7
SPIWrite 0fff,30,0,7
SPIWrite 1000,9d,0,7
SPIWrite 1001,e8,0,7
SPIWrite 1002,07,0,7
SPIWrite 1003,00,0,7
SPIWrite 1004,88,0,7
SPIWrite 1005,e8,0,7
SPIWrite 1006,07,0,7
SPIWrite 1007,00,0,7
SPIWrite 1008,bd,0,7
SPIWrite 1009,e8,0,7
SPIWrite 100a,8e,0,7
SPIWrite 100b,81,0,7
SPIWrite 100c,00,0,7
SPIWrite 100d,00,0,7
SPIWrite 100e,00,0,7
SPIWrite 100f,00,0,7
SPIWrite 1010,00,0,7
SPIWrite 1011,00,0,7
SPIWrite 1012,00,0,7
SPIWrite 1013,00,0,7
SPIWrite 1014,00,0,7
SPIWrite 1015,00,0,7
SPIWrite 1016,00,0,7
SPIWrite 1017,00,0,7
SPIWrite 1018,00,0,7
SPIWrite 1019,00,0,7
SPIWrite 101a,00,0,7
SPIWrite 101b,00,0,7
SPIWrite 101c,00,0,7
SPIWrite 101d,00,0,7
SPIWrite 101e,00,0,7
SPIWrite 101f,00,0,7

WAIT 0.5
```

```
SPIWrite 0012,00,4,4    //PAGE: sys_calib_macro_memory=0x0;(Meaning: );     Address(0x12[4:4],)
SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,10,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,81,0,7

SPIPoll 00f0,1,1,1


SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)

\\Read  MACRO_READY=0x1;    Address(0x20[0:0],)


\\Read  MACRO_ACK=0x1;  Address(0x20[1:1],)


\\Read  MACRO_DONE=0x1;     Address(0x20[2:2],)

SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)

SPIWrite 0013,00,5,5    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
SPIWrite 0012,10,4,4    //PAGE: sys_calib_macro_memory=0x1;(Meaning: );     Address(0x12[4:4],)
SPIWrite 0040,00,0,7
SPIWrite 0020,00,0,7
SPIWrite 0021,7c,0,7
SPIWrite 0022,01,0,7
SPIWrite 0023,20,0,7
SPIWrite 0024,91,0,7
SPIWrite 0025,00,0,7
SPIWrite 0026,00,0,7
SPIWrite 0027,00,0,7
SPIWrite 0028,cd,0,7
SPIWrite 0029,d3,0,7
SPIWrite 002a,01,0,7
SPIWrite 002b,00,0,7
SPIWrite 002c,e9,0,7
SPIWrite 002d,d3,0,7
SPIWrite 002e,01,0,7
SPIWrite 002f,00,0,7
SPIWrite 0030,db,0,7
SPIWrite 0031,d3,0,7
SPIWrite 0032,01,0,7
SPIWrite 0033,00,0,7
SPIWrite 0034,05,0,7
SPIWrite 0035,d4,0,7
SPIWrite 0036,01,0,7
SPIWrite 0037,00,0,7
SPIWrite 0038,a3,0,7
SPIWrite 0039,d3,0,7
SPIWrite 003a,01,0,7
SPIWrite 003b,00,0,7
SPIWrite 003c,00,0,7
SPIWrite 003d,00,0,7
```

```
SPIWrite 003e,00,0,7
SPIWrite 003f,00,0,7
SPIWrite 0040,00,0,7
SPIWrite 0041,00,0,7
SPIWrite 0042,00,0,7
SPIWrite 0043,00,0,7
SPIWrite 0044,00,0,7
SPIWrite 0045,00,0,7
SPIWrite 0046,00,0,7
SPIWrite 0047,00,0,7
SPIWrite 0048,00,0,7
SPIWrite 0049,00,0,7
SPIWrite 004a,00,0,7
SPIWrite 004b,00,0,7
SPIWrite 004c,b1,0,7
SPIWrite 004d,d3,0,7
SPIWrite 004e,01,0,7
SPIWrite 004f,00,0,7
SPIWrite 0050,f7,0,7
SPIWrite 0051,d3,0,7
SPIWrite 0052,01,0,7
SPIWrite 0053,00,0,7
SPIWrite 0054,00,0,7
SPIWrite 0055,00,0,7
SPIWrite 0056,00,0,7
SPIWrite 0057,00,0,7
SPIWrite 0058,bf,0,7
SPIWrite 0059,d3,0,7
SPIWrite 005a,01,0,7
SPIWrite 005b,00,0,7
SPIWrite 005c,af,0,7
SPIWrite 005d,d3,0,7
SPIWrite 005e,01,0,7
SPIWrite 005f,00,0,7
SPIWrite 0060,9f,0,7
SPIWrite 0061,d5,0,7
SPIWrite 0062,01,0,7
SPIWrite 0063,00,0,7
SPIWrite 0064,57,0,7
SPIWrite 0065,d4,0,7
SPIWrite 0066,01,0,7
SPIWrite 0067,00,0,7
SPIWrite 0068,61,0,7
SPIWrite 0069,d4,0,7
SPIWrite 006a,01,0,7
SPIWrite 006b,00,0,7
SPIWrite 006c,31,0,7
SPIWrite 006d,d4,0,7
SPIWrite 006e,01,0,7
SPIWrite 006f,00,0,7
SPIWrite 0070,43,0,7
SPIWrite 0071,d4,0,7
SPIWrite 0072,01,0,7
SPIWrite 0073,00,0,7
SPIWrite 0074,55,0,7
SPIWrite 0075,d4,0,7
SPIWrite 0076,01,0,7
SPIWrite 0077,00,0,7
SPIWrite 0078,21,0,7
SPIWrite 0079,d4,0,7
SPIWrite 007a,01,0,7
SPIWrite 007b,00,0,7
SPIWrite 007c,55,0,7
SPIWrite 007d,d4,0,7
SPIWrite 007e,01,0,7
SPIWrite 007f,00,0,7
SPIWrite 0080,15,0,7
SPIWrite 0081,ff,0,7
SPIWrite 0082,00,0,7
```

```
SPIWrite 0083,00,0,7
SPIWrite 0084,55,0,7
SPIWrite 0085,d4,0,7
SPIWrite 0086,01,0,7
SPIWrite 0087,00,0,7
SPIWrite 0088,79,0,7
SPIWrite 0089,80,0,7
SPIWrite 008a,02,0,7
SPIWrite 008b,00,0,7
SPIWrite 008c,55,0,7
SPIWrite 008d,d4,0,7
SPIWrite 008e,01,0,7
SPIWrite 008f,00,0,7
SPIWrite 0090,55,0,7
SPIWrite 0091,d4,0,7
SPIWrite 0092,01,0,7
SPIWrite 0093,00,0,7
SPIWrite 0094,57,0,7
SPIWrite 0095,81,0,7
SPIWrite 0096,02,0,7
SPIWrite 0097,00,0,7
SPIWrite 0098,55,0,7
SPIWrite 0099,d4,0,7
SPIWrite 009a,01,0,7
SPIWrite 009b,00,0,7
SPIWrite 009c,55,0,7
SPIWrite 009d,d4,0,7
SPIWrite 009e,01,0,7
SPIWrite 009f,00,0,7
SPIWrite 00a0,6d,0,7
SPIWrite 00a1,d4,0,7
SPIWrite 00a2,01,0,7
SPIWrite 00a3,00,0,7
SPIWrite 00a4,55,0,7
SPIWrite 00a5,d4,0,7
SPIWrite 00a6,01,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a8,55,0,7
SPIWrite 00a9,d4,0,7
SPIWrite 00aa,01,0,7
SPIWrite 00ab,00,0,7
SPIWrite 00ac,79,0,7
SPIWrite 00ad,fd,0,7
SPIWrite 00ae,00,0,7
SPIWrite 00af,00,0,7
SPIWrite 00b0,55,0,7
SPIWrite 00b1,d4,0,7
SPIWrite 00b2,01,0,7
SPIWrite 00b3,00,0,7
SPIWrite 00b4,55,0,7
SPIWrite 00b5,d4,0,7
SPIWrite 00b6,01,0,7
SPIWrite 00b7,00,0,7
SPIWrite 00b8,d9,0,7
SPIWrite 00b9,8e,0,7
SPIWrite 00ba,02,0,7
SPIWrite 00bb,00,0,7
SPIWrite 00bc,7f,0,7
SPIWrite 00bd,8d,0,7
SPIWrite 00be,02,0,7
SPIWrite 00bf,00,0,7
SPIWrite 00c0,3d,0,7
SPIWrite 00c1,8d,0,7
SPIWrite 00c2,02,0,7
SPIWrite 00c3,00,0,7
SPIWrite 0012,00,4,4    //PAGE: sys_calib_macro_memory=0x0;(Meaning: );     Address(0x12[4:4],)
SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1
```

```
SPIWrite 00a3,10,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,10,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,81,0,7

SPIPoll 00f0,1,1,1


SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)

\\Read  MACRO_READY=0x1;    Address(0x20[0:0],)


\\Read  MACRO_ACK=0x1;  Address(0x20[1:1],)


\\Read  MACRO_DONE=0x1;     Address(0x20[2:2],)

SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)

SPIWrite 0013,00,5,5    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,10,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,81,0,7

SPIPoll 00f0,1,1,1


SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)

\\Read  MACRO_READY=0x1;    Address(0x20[0:0],)


\\Read  MACRO_ACK=0x1;  Address(0x20[1:1],)


\\Read  MACRO_DONE=0x1;     Address(0x20[2:2],)

SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)

SPIWrite 0013,00,0,7    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
\\ STEP: rstMCU/step2
```

```
\\START: Loading PLL EFuse trims

SPIWrite 0013,10,0,7    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0144,00,0,7
SPIWrite 0144,00,0,7
SPIWrite 0013,00,0,7    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0013,02,0,7    //PAGE: cm4top_dram=0x1;(Meaning: );    Address(0x13[1:1],)
SPIWrite 3f10,20,0,7
SPIWrite 3f12,ce,0,7
SPIWrite 3f13,ff,0,7
SPIWrite 3f14,7f,0,7
SPIWrite 3f15,00,0,7
SPIWrite 3ee6,01,0,7
SPIWrite 3f64,01,0,7
SPIWrite 3f65,01,0,7
SPIWrite 3f66,02,0,7
SPIWrite 3f67,01,0,7
SPIWrite 0013,00,0,7    //PAGE: cm4top_dram=0x0;(Meaning: );    Address(0x13[1:1],)
SPIWrite 0013,10,0,7    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,25,0,7

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,0,7    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0013,20,0,7    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)

SPIWrite 0013,00,0,7    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
SPIWrite 0013,10,0,7    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,12,0,7

SPIPoll 00f0,0,7,7


\\END: Done Loading PLL EFuse trims


\\START: Configuring TOP parameters for MCU


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,03,0,7
SPIWrite 00a1,1f,0,7
SPIWrite 00a0,1f,0,7
SPIWrite 0193,21,0,7

\\Read  macro_opcode_operand=0x21000000;    Address(0x190[31:0],)
```

```
SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0x20[4:4],)


\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0x20[5:5],)


\\Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0x20[6:6],)


\\Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0x20[7:7],)

SPIWrite 0013,00,5,5    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0193,25,0,7

\\Read  macro_opcode_operand=0x25000000;    Address(0x190[31:0],)


SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0x20[4:4],)


\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0x20[5:5],)


\\Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0x20[6:6],)


\\Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0x20[7:7],)

SPIWrite 0013,00,5,5    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,05,0,7
SPIWrite 00a2,04,0,7
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SPIWrite 00a1,05,0,7
SPIWrite 00a0,04,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,04,0,7
SPIWrite 00a4,04,0,7
SPIWrite 0193,26,0,7

\\Read  macro_opcode_operand=0x26000000;    Address(0x190[31:0],)


SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0x20[4:4],)


\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0x20[5:5],)


\\Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0x20[6:6],)


\\Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0x20[7:7],)

SPIWrite 0013,00,5,5    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 00ab,00,0,7
SPIWrite 00aa,00,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00a8,00,0,7
SPIWrite 00af,00,0,7
SPIWrite 00ae,00,0,7
SPIWrite 00ad,00,0,7
SPIWrite 00ac,00,0,7
SPIWrite 00b3,00,0,7
SPIWrite 00b2,23,0,7
SPIWrite 00b1,c7,0,7
SPIWrite 00b0,f6,0,7
SPIWrite 00b7,00,0,7
SPIWrite 00b6,23,0,7
SPIWrite 00b5,c7,0,7
SPIWrite 00b4,f6,0,7
SPIWrite 00bb,00,0,7
SPIWrite 00ba,34,0,7
SPIWrite 00b9,a5,0,7
SPIWrite 00b8,80,0,7
SPIWrite 00bf,00,0,7
SPIWrite 00be,23,0,7
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SPIWrite 00bd,c7,0,7
SPIWrite 00bc,f6,0,7
SPIWrite 0193,24,0,7

\\Read  macro_opcode_operand=0x24000000;    Address(0x190[31:0],)


SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0x20[4:4],)


\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0x20[5:5],)


\\Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0x20[6:6],)


\\Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0x20[7:7],)


\\END: Done configuring TOP parameters for MCU

SPIWrite 0013,00,0,7    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
\\ STEP: efusebyMCU/step0

\\START: Loading PLL EFuse trims

SPIWrite 0013,10,0,7    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,1f,0,7
SPIWrite 00a1,7c,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,09,0,7
SPIWrite 00a6,08,0,7
SPIWrite 00a5,02,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,12,0,7

SPIPoll 00f0,0,7,7


\\END: Done Loading PLL EFuse trims

SPIWrite 0013,00,0,7    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0014,04,0,7    //PAGE: TIMING_CON=0x1;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0717,00,0,7    //spare_reg_port=0x101;     Address(0x714[31:0],)
SPIWrite 0716,00,0,7
SPIWrite 0715,01,0,7
SPIWrite 0714,01,0,7
SPIWrite 0014,00,0,7    //PAGE: TIMING_CON=0x0;(Meaning: );     Address(0x14[2:2],)
\\ STEP: pll0Config/step0

\\START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
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```
SPIWrite 01d4,01,0,7    //pll_reg_spi_req_a=0x1;    Address(0x1d4[0:0],)
SPIWrite 0374,00,0,7    //pll_reg_spi_req_b1=0x0;(Meaning: );   Address(0x374[0:0],)

SPIPoll 01d5,0,0,1


\\Read  pll_reg_spi_a_ack=0x1;  Address(0x1d4[8:8],)


\\END: Done requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
\\ STEP: pll0Config/step1

\\START: Configure PLL

SPIWrite 0014,08,0,7    //PAGE: pll=0x1;    Address(0x14[7:3],)
SPIWrite 004b,33,0,7    //PLL_SPARE0=0xcc000;   Address(0x48[31:10],)
SPIWrite 004a,00,0,7
SPIWrite 0049,00,0,7
SPIWrite 005e,97,0,7    //EN_VCO=0x1;   Address(0x5c[23:23],)
SPIWrite 0028,13,0,7    //N=0x13;   Address(0x28[7:0],)
SPIWrite 0036,13,0,7    //N_to_CAL=0x13;    Address(0x34[23:16],)
SPIWrite 0035,08,0,7    //CAL_CONTROL=0x8;  Address(0x34[12:8],)
SPIWrite 0051,06,0,7    //CTL_REF_DIV=0x1;(Meaning: );  Address(0x50[8:6],)
SPIWrite 0050,40,0,7
SPIWrite 0051,06,0,7    //EN_DIV8_CLK_TO_PLLDIG=0x1;    Address(0x50[9:9],)
SPIWrite 0051,06,0,7    //EN_CLK_TO_PLLDIG=0x1;     Address(0x50[10:10],)
SPIWrite 0051,0e,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x1;    Address(0x50[11:11],)
SPIWrite 003c,40,0,7    //CTL_DIV_23_45=0x0;    Address(0x3c[0:0],)
SPIWrite 005e,97,0,7    //EN_FRAC_N_MODE=0x1;   Address(0x5c[16:16],)
SPIWrite 0033,03,0,7    //EN_FRAC_MODE=0x1;     Address(0x30[24:24],)
SPIWrite 003f,0c,0,7    //CTL_TEST_MUX=0x0;     Address(0x3c[31:30],)
SPIWrite 0049,01,0,7    //EN_VCO_PKDET=0x1;     Address(0x48[8:8],)
SPIWrite 0048,2f,0,7    //VCO_PKDT_BIAS=0x7;    Address(0x48[2:0],)
SPIWrite 0044,27,0,7    //CTL_VCO_IB_GM=0x7;    Address(0x44[2:0],)
SPIWrite 0043,4c,0,7    //CTL_VCO_IB_TAIL=0xc;  Address(0x40[27:24],)
SPIWrite 0043,0c,0,7    //CTL_VCO_IB_GM_SLOPE=0x0;  Address(0x40[30:28],)
SPIWrite 0042,04,0,7    //CTL_VCO_IB_TAIL_SLOPE=0x0;    Address(0x40[22:19],)
SPIWrite 0046,00,0,7    //CTL_VCO_IB_GM1=0x0;   Address(0x44[22:21],)
SPIWrite 0040,28,0,7    //CTL_VB_VAR_SLOPE=0x0;     Address(0x40[2:0],)
SPIWrite 002e,00,0,7    //F=0x4fec;     Address(0x2c[19:0],)
SPIWrite 002d,4f,0,7
SPIWrite 002c,ec,0,7
SPIWrite 0032,03,0,7    //D=0x3c000;    Address(0x30[19:0],)
SPIWrite 0031,c0,0,7
SPIWrite 0030,00,0,7
SPIWrite 0033,03,0,7    //F_order=0x1;  Address(0x30[27:25],)
SPIWrite 0039,40,0,7    //EN_LOCK_DETECT=0x1;   Address(0x38[14:14],)
SPIWrite 003f,14,0,7    //CTL_PFD_DEL=0x2;  Address(0x3c[29:27],)
SPIWrite 003f,12,0,7    //CTL_OUT_DIV=0x2;  Address(0x3c[26:24],)
SPIWrite 003c,40,0,7    //CTL_LDO_ANA=0x4;  Address(0x3c[6:4],)
SPIWrite 003d,24,0,7    //CTL_LDO_RF=0x4;   Address(0x3c[10:8],)
SPIWrite 0052,10,0,7    //CTL_FBDIV_LDO_PROG=0x8;   Address(0x50[20:17],)
SPIWrite 003a,08,0,7    //CTL_CP_IREF=0x2;  Address(0x38[20:18],)
SPIWrite 003b,30,0,7    //CTL_CP_IOUT=0x3;  Address(0x38[29:28],)
SPIWrite 0034,03,0,7    //lock_acc=0x3;     Address(0x34[1:0],)
SPIWrite 0034,0f,0,7    //lock_cnt=0x3;     Address(0x34[3:2],)
SPIWrite 0034,1f,0,7    //lock_err=0x1;     Address(0x34[5:4],)
SPIWrite 0066,04,0,7    //lock_rst=0x1;     Address(0x64[18:18],)
SPIWrite 0066,00,0,7    //lock_rst=0x0;     Address(0x64[18:18],)
SPIWrite 0066,08,0,7    //lock_lost_rst=0x1;    Address(0x64[19:19],)
SPIWrite 0066,00,0,7    //lock_lost_rst=0x0;    Address(0x64[19:19],)
SPIWrite 0034,1f,0,7    //EN_CAL=0x0;   Address(0x34[6:6],)
SPIWrite 0034,5f,0,7    //EN_CAL=0x1;   Address(0x34[6:6],)

WAIT 0.01

SPIWrite 005e,9f,0,7    //EN_I_OFFSET=0x1;  Address(0x5c[19:19],)
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SPIWrite 003c,40,0,7    //CTL_I_OFST_UP_DN=0x0;     Address(0x3c[1:1],)
SPIWrite 0065,10,0,7    //CTL_I_OFST_REF=0x1;   Address(0x64[14:12],)
SPIWrite 003c,48,0,7    //CTL_I_OFFSET=0x2;     Address(0x3c[3:2],)

SPIPoll 0062,7,7,1

SPIReadCheck 0062,7,7,80

\\Read  lock=0x1;   Address(0x60[23:23],)

SPIWrite 0066,03,0,7    //vctrl=0x3;    Address(0x64[17:16],)
SPIWrite 0048,af,0,7    //EN_VCTRL_CMP=0x1;     Address(0x48[7:7],)

\\END: Done configuring PLL

SPIWrite 0014,00,0,7    //PAGE: pll=0x0;    Address(0x14[7:3],)
\\ STEP: pll1Config/step0

\\START: Configure PLL

SPIWrite 0014,10,0,7    //PAGE: pll=0x2;    Address(0x14[7:3],)
SPIWrite 005e,97,0,7    //EN_VCO=0x1;   Address(0x5c[23:23],)
SPIWrite 0028,12,0,7    //N=0x12;   Address(0x28[7:0],)
SPIWrite 0036,12,0,7    //N_to_CAL=0x12;    Address(0x34[23:16],)
SPIWrite 0035,08,0,7    //CAL_CONTROL=0x8;  Address(0x34[12:8],)
SPIWrite 0051,06,0,7    //CTL_REF_DIV=0x1;(Meaning: );  Address(0x50[8:6],)
SPIWrite 0050,40,0,7
SPIWrite 0051,06,0,7    //EN_DIV8_CLK_TO_PLLDIG=0x1;    Address(0x50[9:9],)
SPIWrite 0051,06,0,7    //EN_CLK_TO_PLLDIG=0x1;     Address(0x50[10:10],)
SPIWrite 0051,0e,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x1;    Address(0x50[11:11],)
SPIWrite 003c,40,0,7    //CTL_DIV_23_45=0x0;    Address(0x3c[0:0],)
SPIWrite 005e,96,0,7    //EN_FRAC_N_MODE=0x0;   Address(0x5c[16:16],)
SPIWrite 0033,02,0,7    //EN_FRAC_MODE=0x0;     Address(0x30[24:24],)
SPIWrite 003f,0c,0,7    //CTL_TEST_MUX=0x0;     Address(0x3c[31:30],)
SPIWrite 0049,01,0,7    //EN_VCO_PKDET=0x1;     Address(0x48[8:8],)
SPIWrite 0048,2f,0,7    //VCO_PKDT_BIAS=0x7;    Address(0x48[2:0],)
SPIWrite 0044,27,0,7    //CTL_VCO_IB_GM=0x7;    Address(0x44[2:0],)
SPIWrite 0043,4c,0,7    //CTL_VCO_IB_TAIL=0xc;  Address(0x40[27:24],)
SPIWrite 0043,0c,0,7    //CTL_VCO_IB_GM_SLOPE=0x0;  Address(0x40[30:28],)
SPIWrite 0042,04,0,7    //CTL_VCO_IB_TAIL_SLOPE=0x0;    Address(0x40[22:19],)
SPIWrite 0046,00,0,7    //CTL_VCO_IB_GM1=0x0;   Address(0x44[22:21],)
SPIWrite 0040,28,0,7    //CTL_VB_VAR_SLOPE=0x0;     Address(0x40[2:0],)
SPIWrite 002e,00,0,7    //F=0x0;    Address(0x2c[19:0],)
SPIWrite 002d,00,0,7
SPIWrite 002c,00,0,7
SPIWrite 0032,02,0,7    //D=0x20000;    Address(0x30[19:0],)
SPIWrite 0031,00,0,7
SPIWrite 0030,00,0,7
SPIWrite 0033,02,0,7    //F_order=0x1;  Address(0x30[27:25],)
SPIWrite 0039,40,0,7    //EN_LOCK_DETECT=0x1;   Address(0x38[14:14],)
SPIWrite 003f,14,0,7    //CTL_PFD_DEL=0x2;  Address(0x3c[29:27],)
SPIWrite 003f,13,0,7    //CTL_OUT_DIV=0x3;  Address(0x3c[26:24],)
SPIWrite 003c,40,0,7    //CTL_LDO_ANA=0x4;  Address(0x3c[6:4],)
SPIWrite 003d,24,0,7    //CTL_LDO_RF=0x4;   Address(0x3c[10:8],)
SPIWrite 0052,10,0,7    //CTL_FBDIV_LDO_PROG=0x8;   Address(0x50[20:17],)
SPIWrite 003a,08,0,7    //CTL_CP_IREF=0x2;  Address(0x38[20:18],)
SPIWrite 003b,30,0,7    //CTL_CP_IOUT=0x3;  Address(0x38[29:28],)
SPIWrite 0034,03,0,7    //lock_acc=0x3;     Address(0x34[1:0],)
SPIWrite 0034,0f,0,7    //lock_cnt=0x3;     Address(0x34[3:2],)
SPIWrite 0034,1f,0,7    //lock_err=0x1;     Address(0x34[5:4],)
SPIWrite 0066,04,0,7    //lock_rst=0x1;     Address(0x64[18:18],)
SPIWrite 0066,00,0,7    //lock_rst=0x0;     Address(0x64[18:18],)
SPIWrite 0066,08,0,7    //lock_lost_rst=0x1;    Address(0x64[19:19],)
SPIWrite 0066,00,0,7    //lock_lost_rst=0x0;    Address(0x64[19:19],)
SPIWrite 0034,1f,0,7    //EN_CAL=0x0;   Address(0x34[6:6],)
SPIWrite 0034,5f,0,7    //EN_CAL=0x1;   Address(0x34[6:6],)

WAIT 0.01
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SPIWrite 005e,96,0,7    //EN_I_OFFSET=0x0;  Address(0x5c[19:19],)

SPIPoll 0062,7,7,1

SPIReadCheck 0062,7,7,80

\\Read  lock=0x1;   Address(0x60[23:23],)

SPIWrite 0051,0c,0,7    //EN_DIV8_CLK_TO_PLLDIG=0x0;    Address(0x50[9:9],)
SPIWrite 0066,03,0,7    //vctrl=0x3;    Address(0x64[17:16],)
SPIWrite 0048,af,0,7    //EN_VCTRL_CMP=0x1;     Address(0x48[7:7],)

\\END: Done configuring PLL

SPIWrite 0014,00,0,7    //PAGE: pll=0x0;    Address(0x14[7:3],)
\\ STEP: pll2Config/step0

\\START: Configure PLL

SPIWrite 0014,20,0,7    //PAGE: pll=0x4;    Address(0x14[7:3],)
SPIWrite 004b,33,0,7    //PLL_SPARE0=0xcc000;   Address(0x48[31:10],)
SPIWrite 004a,00,0,7
SPIWrite 0049,00,0,7
SPIWrite 005e,97,0,7    //EN_VCO=0x1;   Address(0x5c[23:23],)
SPIWrite 0028,0e,0,7    //N=0xe;    Address(0x28[7:0],)
SPIWrite 0036,0e,0,7    //N_to_CAL=0xe;     Address(0x34[23:16],)
SPIWrite 0035,08,0,7    //CAL_CONTROL=0x8;  Address(0x34[12:8],)
SPIWrite 0051,06,0,7    //CTL_REF_DIV=0x1;(Meaning: );  Address(0x50[8:6],)
SPIWrite 0050,40,0,7
SPIWrite 0051,06,0,7    //EN_DIV8_CLK_TO_PLLDIG=0x1;    Address(0x50[9:9],)
SPIWrite 0051,06,0,7    //EN_CLK_TO_PLLDIG=0x1;     Address(0x50[10:10],)
SPIWrite 0051,0e,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x1;    Address(0x50[11:11],)
SPIWrite 003c,41,0,7    //CTL_DIV_23_45=0x1;    Address(0x3c[0:0],)
SPIWrite 005e,97,0,7    //EN_FRAC_N_MODE=0x1;   Address(0x5c[16:16],)
SPIWrite 0033,03,0,7    //EN_FRAC_MODE=0x1;     Address(0x30[24:24],)
SPIWrite 003f,0c,0,7    //CTL_TEST_MUX=0x0;     Address(0x3c[31:30],)
SPIWrite 0049,01,0,7    //EN_VCO_PKDET=0x1;     Address(0x48[8:8],)
SPIWrite 0048,2f,0,7    //VCO_PKDT_BIAS=0x7;    Address(0x48[2:0],)
SPIWrite 0044,27,0,7    //CTL_VCO_IB_GM=0x7;    Address(0x44[2:0],)
SPIWrite 0043,4c,0,7    //CTL_VCO_IB_TAIL=0xc;  Address(0x40[27:24],)
SPIWrite 0043,0c,0,7    //CTL_VCO_IB_GM_SLOPE=0x0;  Address(0x40[30:28],)
SPIWrite 0042,04,0,7    //CTL_VCO_IB_TAIL_SLOPE=0x0;    Address(0x40[22:19],)
SPIWrite 0046,00,0,7    //CTL_VCO_IB_GM1=0x0;   Address(0x44[22:21],)
SPIWrite 0040,28,0,7    //CTL_VB_VAR_SLOPE=0x0;     Address(0x40[2:0],)
SPIWrite 002e,00,0,7    //F=0x2580;     Address(0x2c[19:0],)
SPIWrite 002d,25,0,7
SPIWrite 002c,80,0,7
SPIWrite 0032,03,0,7    //D=0x3c000;    Address(0x30[19:0],)
SPIWrite 0031,c0,0,7
SPIWrite 0030,00,0,7
SPIWrite 0033,03,0,7    //F_order=0x1;  Address(0x30[27:25],)
SPIWrite 0039,40,0,7    //EN_LOCK_DETECT=0x1;   Address(0x38[14:14],)
SPIWrite 003f,14,0,7    //CTL_PFD_DEL=0x2;  Address(0x3c[29:27],)
SPIWrite 003f,11,0,7    //CTL_OUT_DIV=0x1;  Address(0x3c[26:24],)
SPIWrite 003c,41,0,7    //CTL_LDO_ANA=0x4;  Address(0x3c[6:4],)
SPIWrite 003d,24,0,7    //CTL_LDO_RF=0x4;   Address(0x3c[10:8],)
SPIWrite 0052,10,0,7    //CTL_FBDIV_LDO_PROG=0x8;   Address(0x50[20:17],)
SPIWrite 003a,08,0,7    //CTL_CP_IREF=0x2;  Address(0x38[20:18],)
SPIWrite 003b,30,0,7    //CTL_CP_IOUT=0x3;  Address(0x38[29:28],)
SPIWrite 0034,03,0,7    //lock_acc=0x3;     Address(0x34[1:0],)
SPIWrite 0034,0f,0,7    //lock_cnt=0x3;     Address(0x34[3:2],)
SPIWrite 0034,1f,0,7    //lock_err=0x1;     Address(0x34[5:4],)
SPIWrite 0066,04,0,7    //lock_rst=0x1;     Address(0x64[18:18],)
SPIWrite 0066,00,0,7    //lock_rst=0x0;     Address(0x64[18:18],)
SPIWrite 0066,08,0,7    //lock_lost_rst=0x1;    Address(0x64[19:19],)
SPIWrite 0066,00,0,7    //lock_lost_rst=0x0;    Address(0x64[19:19],)
SPIWrite 0034,1f,0,7    //EN_CAL=0x0;   Address(0x34[6:6],)
SPIWrite 0034,5f,0,7    //EN_CAL=0x1;   Address(0x34[6:6],)
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WAIT 0.01

SPIWrite 005e,9f,0,7    //EN_I_OFFSET=0x1;  Address(0x5c[19:19],)
SPIWrite 003c,41,0,7    //CTL_I_OFST_UP_DN=0x0;     Address(0x3c[1:1],)
SPIWrite 0065,10,0,7    //CTL_I_OFST_REF=0x1;   Address(0x64[14:12],)
SPIWrite 003c,49,0,7    //CTL_I_OFFSET=0x2;     Address(0x3c[3:2],)

SPIPoll 0062,7,7,1

SPIReadCheck 0062,7,7,80

\\Read  lock=0x1;   Address(0x60[23:23],)

SPIWrite 0066,03,0,7    //vctrl=0x3;    Address(0x64[17:16],)
SPIWrite 0048,af,0,7    //EN_VCTRL_CMP=0x1;     Address(0x48[7:7],)

\\END: Done configuring PLL

SPIWrite 0014,00,0,7    //PAGE: pll=0x0;    Address(0x14[7:3],)
\\ STEP: pll3Config/step0

\\START: Configure PLL

SPIWrite 0014,40,0,7    //PAGE: pll=0x8;    Address(0x14[7:3],)
SPIWrite 004b,33,0,7    //PLL_SPARE0=0xcc000;   Address(0x48[31:10],)
SPIWrite 004a,00,0,7
SPIWrite 0049,00,0,7
SPIWrite 005e,97,0,7    //EN_VCO=0x1;   Address(0x5c[23:23],)
SPIWrite 0028,13,0,7    //N=0x13;   Address(0x28[7:0],)
SPIWrite 0036,13,0,7    //N_to_CAL=0x13;    Address(0x34[23:16],)
SPIWrite 0035,08,0,7    //CAL_CONTROL=0x8;  Address(0x34[12:8],)
SPIWrite 0051,06,0,7    //CTL_REF_DIV=0x1;(Meaning: );  Address(0x50[8:6],)
SPIWrite 0050,40,0,7
SPIWrite 0051,06,0,7    //EN_DIV8_CLK_TO_PLLDIG=0x1;    Address(0x50[9:9],)
SPIWrite 0051,06,0,7    //EN_CLK_TO_PLLDIG=0x1;     Address(0x50[10:10],)
SPIWrite 0051,0e,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x1;    Address(0x50[11:11],)
SPIWrite 003c,40,0,7    //CTL_DIV_23_45=0x0;    Address(0x3c[0:0],)
SPIWrite 005e,97,0,7    //EN_FRAC_N_MODE=0x1;   Address(0x5c[16:16],)
SPIWrite 0033,03,0,7    //EN_FRAC_MODE=0x1;     Address(0x30[24:24],)
SPIWrite 003f,0c,0,7    //CTL_TEST_MUX=0x0;     Address(0x3c[31:30],)
SPIWrite 0049,01,0,7    //EN_VCO_PKDET=0x1;     Address(0x48[8:8],)
SPIWrite 0048,2f,0,7    //VCO_PKDT_BIAS=0x7;    Address(0x48[2:0],)
SPIWrite 0044,27,0,7    //CTL_VCO_IB_GM=0x7;    Address(0x44[2:0],)
SPIWrite 0043,4c,0,7    //CTL_VCO_IB_TAIL=0xc;  Address(0x40[27:24],)
SPIWrite 0043,0c,0,7    //CTL_VCO_IB_GM_SLOPE=0x0;  Address(0x40[30:28],)
SPIWrite 0042,04,0,7    //CTL_VCO_IB_TAIL_SLOPE=0x0;    Address(0x40[22:19],)
SPIWrite 0046,00,0,7    //CTL_VCO_IB_GM1=0x0;   Address(0x44[22:21],)
SPIWrite 0040,28,0,7    //CTL_VB_VAR_SLOPE=0x0;     Address(0x40[2:0],)
SPIWrite 002e,00,0,7    //F=0x4fec;     Address(0x2c[19:0],)
SPIWrite 002d,4f,0,7
SPIWrite 002c,ec,0,7
SPIWrite 0032,03,0,7    //D=0x3c000;    Address(0x30[19:0],)
SPIWrite 0031,c0,0,7
SPIWrite 0030,00,0,7
SPIWrite 0033,03,0,7    //F_order=0x1;  Address(0x30[27:25],)
SPIWrite 0039,40,0,7    //EN_LOCK_DETECT=0x1;   Address(0x38[14:14],)
SPIWrite 003f,14,0,7    //CTL_PFD_DEL=0x2;  Address(0x3c[29:27],)
SPIWrite 003f,12,0,7    //CTL_OUT_DIV=0x2;  Address(0x3c[26:24],)
SPIWrite 003c,40,0,7    //CTL_LDO_ANA=0x4;  Address(0x3c[6:4],)
SPIWrite 003d,24,0,7    //CTL_LDO_RF=0x4;   Address(0x3c[10:8],)
SPIWrite 0052,10,0,7    //CTL_FBDIV_LDO_PROG=0x8;   Address(0x50[20:17],)
SPIWrite 003a,08,0,7    //CTL_CP_IREF=0x2;  Address(0x38[20:18],)
SPIWrite 003b,30,0,7    //CTL_CP_IOUT=0x3;  Address(0x38[29:28],)
SPIWrite 0034,03,0,7    //lock_acc=0x3;     Address(0x34[1:0],)
SPIWrite 0034,0f,0,7    //lock_cnt=0x3;     Address(0x34[3:2],)
SPIWrite 0034,1f,0,7    //lock_err=0x1;     Address(0x34[5:4],)
SPIWrite 0066,04,0,7    //lock_rst=0x1;     Address(0x64[18:18],)
SPIWrite 0066,00,0,7    //lock_rst=0x0;     Address(0x64[18:18],)
SPIWrite 0066,08,0,7    //lock_lost_rst=0x1;    Address(0x64[19:19],)
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SPIWrite 0066,00,0,7    //lock_lost_rst=0x0;    Address(0x64[19:19],)
SPIWrite 0034,1f,0,7    //EN_CAL=0x0;   Address(0x34[6:6],)
SPIWrite 0034,5f,0,7    //EN_CAL=0x1;   Address(0x34[6:6],)

WAIT 0.01

SPIWrite 005e,9f,0,7    //EN_I_OFFSET=0x1;  Address(0x5c[19:19],)
SPIWrite 003c,40,0,7    //CTL_I_OFST_UP_DN=0x0;     Address(0x3c[1:1],)
SPIWrite 0065,10,0,7    //CTL_I_OFST_REF=0x1;   Address(0x64[14:12],)
SPIWrite 003c,48,0,7    //CTL_I_OFFSET=0x2;     Address(0x3c[3:2],)

SPIPoll 0062,7,7,1

SPIReadCheck 0062,7,7,80

\\Read  lock=0x1;   Address(0x60[23:23],)

SPIWrite 0066,03,0,7    //vctrl=0x3;    Address(0x64[17:16],)
SPIWrite 0048,af,0,7    //EN_VCTRL_CMP=0x1;     Address(0x48[7:7],)

\\END: Done configuring PLL

SPIWrite 0014,00,0,7    //PAGE: pll=0x0;    Address(0x14[7:3],)
\\ STEP: pll4PowerDown/step0

\\START: Powers up/down the PLL

SPIWrite 0014,80,0,7    //PAGE: pll=0x10;   Address(0x14[7:3],)
SPIWrite 005e,17,0,7    //EN_VCO=0x0;   Address(0x5c[23:23],)
SPIWrite 0014,00,0,7    //PAGE: pll=0x0;    Address(0x14[7:3],)
\\ STEP: pll4PowerDown/step1

\\START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 01d4,00,0,7    //pll_reg_spi_req_a=0x0;    Address(0x1d4[0:0],)
SPIWrite 0374,00,0,7    //pll_reg_spi_req_b1=0x0;(Meaning: );   Address(0x374[0:0],)

WAIT 0.01


\\END: Done requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
\\ STEP: efuseToAnalog/step0
SPIWrite 0013,20,0,7    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIWrite 0084,21,0,7
SPIWrite 0084,61,0,7
SPIWrite 0084,21,0,7
SPIWrite 0084,21,0,7
SPIWrite 0084,01,0,7
SPIWrite 0088,01,0,7
SPIWrite 0013,00,0,7    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
\\ STEP: efuseToAnalog/step1

\\START: Loading EFuse Packets

SPIWrite 0013,10,0,7    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,04,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,07,0,7
SPIWrite 00a4,00,0,7
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SPIWrite 00ab,11,0,7
SPIWrite 00aa,0b,0,7
SPIWrite 00a9,0a,0,7
SPIWrite 00a8,07,0,7
SPIWrite 00af,00,0,7
SPIWrite 00ae,00,0,7
SPIWrite 00ad,00,0,7
SPIWrite 00ac,14,0,7
SPIWrite 0193,12,0,7

SPIPoll 00f0,0,7,7


\\END: Done Loading Efuse packets

SPIWrite 0013,00,0,7    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
\\ STEP: topConfig/step0

\\START: Doing Top & DSA initialization

SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0649,80,0,7    //dsa_abcd_addr_range=0x1;  Address(0x648[15:15],)
SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0014,01,0,7    //PAGE: clktop_2t=0x1;  Address(0x14[1:0],)
SPIWrite 006c,08,0,7    //MASK_PDN_SYNC_TXCML_L=0x1;    Address(0x6c[3:3],)
SPIWrite 006c,18,0,7    //MASK_PDN_SYNC_TXCML_R=0x1;    Address(0x6c[4:4],)
SPIWrite 006c,1c,0,7    //MASK_PDN_FAST_TXCML_R=0x1;    Address(0x6c[2:2],)
SPIWrite 006c,1e,0,7    //MASK_PDN_FAST_TXCML_L=0x1;    Address(0x6c[1:1],)
SPIWrite 0014,00,0,7    //PAGE: clktop_2t=0x0;  Address(0x14[1:0],)
SPIWrite 0018,01,0,7    //PAGE: ana_4t4r=0x1;(Meaning: );   Address(0x18[0:0],)
SPIWrite 0050,00,0,7
SPIWrite 0054,00,0,7
SPIWrite 0050,00,0,7
SPIWrite 0054,00,0,7
SPIWrite 0018,00,0,7    //PAGE: ana_4t4r=0x0;(Meaning: );   Address(0x18[0:0],)
SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 039c,00,0,7    //sync_lvds_mode_ab=0x0;(Meaning: );    Address(0x39c[0:0],)
SPIWrite 039c,00,0,7    //sync_lvds_mode_cd=0x0;(Meaning: );    Address(0x39c[1:1],)
SPIWrite 0330,00,0,7    //pull_ctrl_gpio_76=0x0;    Address(0x330[2:0],)
SPIWrite 02e4,00,0,7    //pull_ctrl_gpio_57=0x0;    Address(0x2e4[2:0],)
SPIWrite 02f4,00,0,7    //pull_ctrl_gpio_61=0x0;    Address(0x2f4[2:0],)
SPIWrite 02c0,00,0,7    //pull_ctrl_gpio_48=0x0;    Address(0x2c0[2:0],)
SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0016,30,0,7    //PAGE: dsa=0x3;    Address(0x16[5:4],)
SPIWrite 0180,01,0,7
SPIWrite 02fb,00,0,7
SPIWrite 065b,00,0,7
SPIWrite 02fd,00,0,7
SPIWrite 065d,00,0,7
SPIWrite 02fe,00,0,7
SPIWrite 0305,00,0,7
SPIWrite 030e,00,0,7
SPIWrite 065e,00,0,7
SPIWrite 0665,00,0,7
SPIWrite 066e,00,0,7
SPIWrite 0040,03,0,7
SPIWrite 0311,00,0,7
SPIWrite 0671,00,0,7
SPIWrite 02c8,01,0,7
SPIWrite 02d0,01,0,7
SPIWrite 0630,01,0,7
SPIWrite 0051,00,0,7
SPIWrite 00b1,00,0,7
SPIWrite 0677,01,0,7
SPIWrite 0676,f0,0,7
SPIWrite 0675,03,0,7
SPIWrite 0674,e0,0,7
SPIWrite 067b,01,0,7
SPIWrite 067a,f0,0,7
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SPIWrite 0679,03,0,7
SPIWrite 0678,21,0,7
SPIWrite 067f,01,0,7
SPIWrite 067e,f0,0,7
SPIWrite 067d,02,0,7
SPIWrite 067c,82,0,7
SPIWrite 0683,01,0,7
SPIWrite 0682,f0,0,7
SPIWrite 0681,02,0,7
SPIWrite 0680,23,0,7
SPIWrite 0687,01,0,7
SPIWrite 0686,f0,0,7
SPIWrite 0685,01,0,7
SPIWrite 0684,c4,0,7
SPIWrite 068b,01,0,7
SPIWrite 068a,f0,0,7
SPIWrite 0689,01,0,7
SPIWrite 0688,85,0,7
SPIWrite 068f,01,0,7
SPIWrite 068e,f0,0,7
SPIWrite 068d,01,0,7
SPIWrite 068c,46,0,7
SPIWrite 0693,01,0,7
SPIWrite 0692,f0,0,7
SPIWrite 0691,01,0,7
SPIWrite 0690,27,0,7
SPIWrite 0697,01,0,7
SPIWrite 0696,e0,0,7
SPIWrite 0695,01,0,7
SPIWrite 0694,08,0,7
SPIWrite 069b,01,0,7
SPIWrite 069a,e0,0,7
SPIWrite 0699,00,0,7
SPIWrite 0698,e9,0,7
SPIWrite 069f,01,0,7
SPIWrite 069e,f0,0,7
SPIWrite 069d,00,0,7
SPIWrite 069c,ca,0,7
SPIWrite 06a3,01,0,7
SPIWrite 06a2,f0,0,7
SPIWrite 06a1,00,0,7
SPIWrite 06a0,ab,0,7
SPIWrite 06a7,01,0,7
SPIWrite 06a6,f0,0,7
SPIWrite 06a5,00,0,7
SPIWrite 06a4,8c,0,7
SPIWrite 06ab,01,0,7
SPIWrite 06aa,f0,0,7
SPIWrite 06a9,00,0,7
SPIWrite 06a8,8d,0,7
SPIWrite 06af,01,0,7
SPIWrite 06ae,f0,0,7
SPIWrite 06ad,00,0,7
SPIWrite 06ac,6e,0,7
SPIWrite 06b3,01,0,7
SPIWrite 06b2,f0,0,7
SPIWrite 06b1,00,0,7
SPIWrite 06b0,6f,0,7
SPIWrite 06b7,01,0,7
SPIWrite 06b6,d0,0,7
SPIWrite 06b5,00,0,7
SPIWrite 06b4,70,0,7
SPIWrite 06bb,01,0,7
SPIWrite 06ba,b0,0,7
SPIWrite 06b9,00,0,7
SPIWrite 06b8,71,0,7
SPIWrite 06bf,01,0,7
SPIWrite 06be,80,0,7
SPIWrite 06bd,00,0,7
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SPIWrite 06bc,72,0,7
SPIWrite 06c3,01,0,7
SPIWrite 06c2,50,0,7
SPIWrite 06c1,00,0,7
SPIWrite 06c0,73,0,7
SPIWrite 06c7,01,0,7
SPIWrite 06c6,20,0,7
SPIWrite 06c5,00,0,7
SPIWrite 06c4,74,0,7
SPIWrite 06cb,00,0,7
SPIWrite 06ca,60,0,7
SPIWrite 06c9,00,0,7
SPIWrite 06c8,75,0,7
SPIWrite 06cf,00,0,7
SPIWrite 06ce,20,0,7
SPIWrite 06cd,00,0,7
SPIWrite 06cc,76,0,7
SPIWrite 06d3,00,0,7
SPIWrite 06d2,00,0,7
SPIWrite 06d1,00,0,7
SPIWrite 06d0,77,0,7
SPIWrite 06d7,00,0,7
SPIWrite 06d6,00,0,7
SPIWrite 06d5,00,0,7
SPIWrite 06d4,78,0,7
SPIWrite 06db,00,0,7
SPIWrite 06da,40,0,7
SPIWrite 06d9,00,0,7
SPIWrite 06d8,59,0,7
SPIWrite 06df,00,0,7
SPIWrite 06de,00,0,7
SPIWrite 06dd,00,0,7
SPIWrite 06dc,5a,0,7
SPIWrite 06e3,00,0,7
SPIWrite 06e2,00,0,7
SPIWrite 06e1,00,0,7
SPIWrite 06e0,5b,0,7
SPIWrite 06e7,00,0,7
SPIWrite 06e6,00,0,7
SPIWrite 06e5,00,0,7
SPIWrite 06e4,5c,0,7
SPIWrite 06eb,01,0,7
SPIWrite 06ea,30,0,7
SPIWrite 06e9,00,0,7
SPIWrite 06e8,3d,0,7
SPIWrite 06ef,00,0,7
SPIWrite 06ee,f0,0,7
SPIWrite 06ed,00,0,7
SPIWrite 06ec,3e,0,7
SPIWrite 06f3,00,0,7
SPIWrite 06f2,f0,0,7
SPIWrite 06f1,00,0,7
SPIWrite 06f0,3e,0,7
SPIWrite 06f7,00,0,7
SPIWrite 06f6,f0,0,7
SPIWrite 06f5,00,0,7
SPIWrite 06f4,3e,0,7
SPIWrite 06fb,00,0,7
SPIWrite 06fa,f0,0,7
SPIWrite 06f9,00,0,7
SPIWrite 06f8,3e,0,7
SPIWrite 06ff,00,0,7
SPIWrite 06fe,f0,0,7
SPIWrite 06fd,00,0,7
SPIWrite 06fc,3e,0,7
SPIWrite 0703,00,0,7
SPIWrite 0702,f0,0,7
SPIWrite 0701,00,0,7
SPIWrite 0700,3e,0,7
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SPIWrite 0707,00,0,7
SPIWrite 0706,f0,0,7
SPIWrite 0705,00,0,7
SPIWrite 0704,3e,0,7
SPIWrite 0317,01,0,7
SPIWrite 0316,f0,0,7
SPIWrite 0315,03,0,7
SPIWrite 0314,e0,0,7
SPIWrite 031b,01,0,7
SPIWrite 031a,f0,0,7
SPIWrite 0319,03,0,7
SPIWrite 0318,21,0,7
SPIWrite 031f,01,0,7
SPIWrite 031e,f0,0,7
SPIWrite 031d,02,0,7
SPIWrite 031c,82,0,7
SPIWrite 0323,01,0,7
SPIWrite 0322,f0,0,7
SPIWrite 0321,02,0,7
SPIWrite 0320,23,0,7
SPIWrite 0327,01,0,7
SPIWrite 0326,f0,0,7
SPIWrite 0325,01,0,7
SPIWrite 0324,c4,0,7
SPIWrite 032b,01,0,7
SPIWrite 032a,f0,0,7
SPIWrite 0329,01,0,7
SPIWrite 0328,85,0,7
SPIWrite 032f,01,0,7
SPIWrite 032e,f0,0,7
SPIWrite 032d,01,0,7
SPIWrite 032c,46,0,7
SPIWrite 0333,01,0,7
SPIWrite 0332,f0,0,7
SPIWrite 0331,01,0,7
SPIWrite 0330,27,0,7
SPIWrite 0337,01,0,7
SPIWrite 0336,e0,0,7
SPIWrite 0335,01,0,7
SPIWrite 0334,08,0,7
SPIWrite 033b,01,0,7
SPIWrite 033a,e0,0,7
SPIWrite 0339,00,0,7
SPIWrite 0338,e9,0,7
SPIWrite 033f,01,0,7
SPIWrite 033e,f0,0,7
SPIWrite 033d,00,0,7
SPIWrite 033c,ca,0,7
SPIWrite 0343,01,0,7
SPIWrite 0342,f0,0,7
SPIWrite 0341,00,0,7
SPIWrite 0340,ab,0,7
SPIWrite 0347,01,0,7
SPIWrite 0346,f0,0,7
SPIWrite 0345,00,0,7
SPIWrite 0344,8c,0,7
SPIWrite 034b,01,0,7
SPIWrite 034a,f0,0,7
SPIWrite 0349,00,0,7
SPIWrite 0348,8d,0,7
SPIWrite 034f,01,0,7
SPIWrite 034e,f0,0,7
SPIWrite 034d,00,0,7
SPIWrite 034c,6e,0,7
SPIWrite 0353,01,0,7
SPIWrite 0352,f0,0,7
SPIWrite 0351,00,0,7
SPIWrite 0350,6f,0,7
SPIWrite 0357,01,0,7
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SPIWrite 0356,d0,0,7
SPIWrite 0355,00,0,7
SPIWrite 0354,70,0,7
SPIWrite 035b,01,0,7
SPIWrite 035a,b0,0,7
SPIWrite 0359,00,0,7
SPIWrite 0358,71,0,7
SPIWrite 035f,01,0,7
SPIWrite 035e,80,0,7
SPIWrite 035d,00,0,7
SPIWrite 035c,72,0,7
SPIWrite 0363,01,0,7
SPIWrite 0362,50,0,7
SPIWrite 0361,00,0,7
SPIWrite 0360,73,0,7
SPIWrite 0367,01,0,7
SPIWrite 0366,20,0,7
SPIWrite 0365,00,0,7
SPIWrite 0364,74,0,7
SPIWrite 036b,00,0,7
SPIWrite 036a,60,0,7
SPIWrite 0369,00,0,7
SPIWrite 0368,75,0,7
SPIWrite 036f,00,0,7
SPIWrite 036e,20,0,7
SPIWrite 036d,00,0,7
SPIWrite 036c,76,0,7
SPIWrite 0373,00,0,7
SPIWrite 0372,00,0,7
SPIWrite 0371,00,0,7
SPIWrite 0370,77,0,7
SPIWrite 0377,00,0,7
SPIWrite 0376,00,0,7
SPIWrite 0375,00,0,7
SPIWrite 0374,78,0,7
SPIWrite 037b,00,0,7
SPIWrite 037a,40,0,7
SPIWrite 0379,00,0,7
SPIWrite 0378,59,0,7
SPIWrite 037f,00,0,7
SPIWrite 037e,00,0,7
SPIWrite 037d,00,0,7
SPIWrite 037c,5a,0,7
SPIWrite 0383,00,0,7
SPIWrite 0382,00,0,7
SPIWrite 0381,00,0,7
SPIWrite 0380,5b,0,7
SPIWrite 0387,00,0,7
SPIWrite 0386,00,0,7
SPIWrite 0385,00,0,7
SPIWrite 0384,5c,0,7
SPIWrite 038b,01,0,7
SPIWrite 038a,30,0,7
SPIWrite 0389,00,0,7
SPIWrite 0388,3d,0,7
SPIWrite 038f,00,0,7
SPIWrite 038e,f0,0,7
SPIWrite 038d,00,0,7
SPIWrite 038c,3e,0,7
SPIWrite 0393,00,0,7
SPIWrite 0392,f0,0,7
SPIWrite 0391,00,0,7
SPIWrite 0390,3e,0,7
SPIWrite 0397,00,0,7
SPIWrite 0396,f0,0,7
SPIWrite 0395,00,0,7
SPIWrite 0394,3e,0,7
SPIWrite 039b,00,0,7
SPIWrite 039a,f0,0,7
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SPIWrite 0399,00,0,7
SPIWrite 0398,3e,0,7
SPIWrite 039f,00,0,7
SPIWrite 039e,f0,0,7
SPIWrite 039d,00,0,7
SPIWrite 039c,3e,0,7
SPIWrite 03a3,00,0,7
SPIWrite 03a2,f0,0,7
SPIWrite 03a1,00,0,7
SPIWrite 03a0,3e,0,7
SPIWrite 03a7,00,0,7
SPIWrite 03a6,f0,0,7
SPIWrite 03a5,00,0,7
SPIWrite 03a4,3e,0,7
SPIWrite 09a8,ff,0,7
SPIWrite 09b0,ff,0,7
SPIWrite 09b8,ff,0,7
SPIWrite 09c0,ff,0,7
SPIWrite 09c8,ff,0,7
SPIWrite 09d0,ff,0,7
SPIWrite 09d8,ff,0,7
SPIWrite 09e0,ff,0,7
SPIWrite 09e8,ff,0,7
SPIWrite 09f0,ff,0,7
SPIWrite 09f8,ff,0,7
SPIWrite 0a00,ff,0,7
SPIWrite 0a08,ff,0,7
SPIWrite 0a10,ff,0,7
SPIWrite 0a18,ff,0,7
SPIWrite 0a20,ff,0,7
SPIWrite 0a28,ff,0,7
SPIWrite 0a30,ff,0,7
SPIWrite 0a38,ff,0,7
SPIWrite 0a40,ff,0,7
SPIWrite 0a48,ff,0,7
SPIWrite 0a50,ff,0,7
SPIWrite 0a58,ff,0,7
SPIWrite 0a60,ff,0,7
SPIWrite 0a68,ff,0,7
SPIWrite 0a70,ff,0,7
SPIWrite 0a78,ff,0,7
SPIWrite 0a80,ff,0,7
SPIWrite 0a88,ff,0,7
SPIWrite 0a90,ff,0,7
SPIWrite 0a98,ff,0,7
SPIWrite 0aa0,ff,0,7
SPIWrite 0aa8,ff,0,7
SPIWrite 0ab0,fe,0,7
SPIWrite 0ab8,fc,0,7
SPIWrite 0ac0,f8,0,7
SPIWrite 0ac8,f0,0,7
SPIWrite 0ad0,e0,0,7
SPIWrite 0ad8,c0,0,7
SPIWrite 0ae0,80,0,7
SPIWrite 09af,ff,0,7
SPIWrite 09ae,ff,0,7
SPIWrite 09ad,ff,0,7
SPIWrite 09ac,ff,0,7
SPIWrite 09b7,ff,0,7
SPIWrite 09b6,ff,0,7
SPIWrite 09b5,ff,0,7
SPIWrite 09b4,fe,0,7
SPIWrite 09bf,ff,0,7
SPIWrite 09be,ff,0,7
SPIWrite 09bd,ff,0,7
SPIWrite 09bc,fc,0,7
SPIWrite 09c7,ff,0,7
SPIWrite 09c6,ff,0,7
SPIWrite 09c5,ff,0,7
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SPIWrite 09c4,f8,0,7
SPIWrite 09cf,ff,0,7
SPIWrite 09ce,ff,0,7
SPIWrite 09cd,ff,0,7
SPIWrite 09cc,f0,0,7
SPIWrite 09d7,ff,0,7
SPIWrite 09d6,ff,0,7
SPIWrite 09d5,ff,0,7
SPIWrite 09d4,e0,0,7
SPIWrite 09df,ff,0,7
SPIWrite 09de,ff,0,7
SPIWrite 09dd,ff,0,7
SPIWrite 09dc,c0,0,7
SPIWrite 09e7,ff,0,7
SPIWrite 09e6,ff,0,7
SPIWrite 09e5,ff,0,7
SPIWrite 09e4,80,0,7
SPIWrite 09ef,ff,0,7
SPIWrite 09ee,ff,0,7
SPIWrite 09ed,ff,0,7
SPIWrite 09ec,00,0,7
SPIWrite 09f7,ff,0,7
SPIWrite 09f6,ff,0,7
SPIWrite 09f5,fe,0,7
SPIWrite 09f4,00,0,7
SPIWrite 09ff,ff,0,7
SPIWrite 09fe,ff,0,7
SPIWrite 09fd,fc,0,7
SPIWrite 09fc,00,0,7
SPIWrite 0a07,ff,0,7
SPIWrite 0a06,ff,0,7
SPIWrite 0a05,f8,0,7
SPIWrite 0a04,00,0,7
SPIWrite 0a0f,ff,0,7
SPIWrite 0a0e,ff,0,7
SPIWrite 0a0d,f0,0,7
SPIWrite 0a0c,00,0,7
SPIWrite 0a17,ff,0,7
SPIWrite 0a16,ff,0,7
SPIWrite 0a15,e0,0,7
SPIWrite 0a14,00,0,7
SPIWrite 0a1f,ff,0,7
SPIWrite 0a1e,ff,0,7
SPIWrite 0a1d,c0,0,7
SPIWrite 0a1c,00,0,7
SPIWrite 0a27,ff,0,7
SPIWrite 0a26,ff,0,7
SPIWrite 0a25,80,0,7
SPIWrite 0a24,00,0,7
SPIWrite 0a2f,ff,0,7
SPIWrite 0a2e,ff,0,7
SPIWrite 0a2d,00,0,7
SPIWrite 0a2c,00,0,7
SPIWrite 0a37,ff,0,7
SPIWrite 0a36,fe,0,7
SPIWrite 0a35,00,0,7
SPIWrite 0a34,00,0,7
SPIWrite 0a3f,ff,0,7
SPIWrite 0a3e,fc,0,7
SPIWrite 0a3d,00,0,7
SPIWrite 0a3c,00,0,7
SPIWrite 0a47,ff,0,7
SPIWrite 0a46,f8,0,7
SPIWrite 0a45,00,0,7
SPIWrite 0a44,00,0,7
SPIWrite 0a4f,ff,0,7
SPIWrite 0a4e,f0,0,7
SPIWrite 0a4d,00,0,7
SPIWrite 0a4c,00,0,7
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SPIWrite 0a57,ff,0,7
SPIWrite 0a56,e0,0,7
SPIWrite 0a55,00,0,7
SPIWrite 0a54,00,0,7
SPIWrite 0a5f,ff,0,7
SPIWrite 0a5e,c0,0,7
SPIWrite 0a5d,00,0,7
SPIWrite 0a5c,00,0,7
SPIWrite 0a67,ff,0,7
SPIWrite 0a66,80,0,7
SPIWrite 0a65,00,0,7
SPIWrite 0a64,00,0,7
SPIWrite 0a6f,ff,0,7
SPIWrite 0a6e,00,0,7
SPIWrite 0a6d,00,0,7
SPIWrite 0a6c,00,0,7
SPIWrite 0a77,fe,0,7
SPIWrite 0a76,00,0,7
SPIWrite 0a75,00,0,7
SPIWrite 0a74,00,0,7
SPIWrite 0a7f,fc,0,7
SPIWrite 0a7e,00,0,7
SPIWrite 0a7d,00,0,7
SPIWrite 0a7c,00,0,7
SPIWrite 0a87,f8,0,7
SPIWrite 0a86,00,0,7
SPIWrite 0a85,00,0,7
SPIWrite 0a84,00,0,7
SPIWrite 0a8f,f0,0,7
SPIWrite 0a8e,00,0,7
SPIWrite 0a8d,00,0,7
SPIWrite 0a8c,00,0,7
SPIWrite 0a97,e0,0,7
SPIWrite 0a96,00,0,7
SPIWrite 0a95,00,0,7
SPIWrite 0a94,00,0,7
SPIWrite 0a9f,c0,0,7
SPIWrite 0a9e,00,0,7
SPIWrite 0a9d,00,0,7
SPIWrite 0a9c,00,0,7
SPIWrite 0aa7,80,0,7
SPIWrite 0aa6,00,0,7
SPIWrite 0aa5,00,0,7
SPIWrite 0aa4,00,0,7
SPIWrite 0aaf,00,0,7
SPIWrite 0aae,00,0,7
SPIWrite 0aad,00,0,7
SPIWrite 0aac,00,0,7
SPIWrite 0ab7,00,0,7
SPIWrite 0ab6,00,0,7
SPIWrite 0ab5,00,0,7
SPIWrite 0ab4,00,0,7
SPIWrite 0abf,00,0,7
SPIWrite 0abe,00,0,7
SPIWrite 0abd,00,0,7
SPIWrite 0abc,00,0,7
SPIWrite 0ac7,00,0,7
SPIWrite 0ac6,00,0,7
SPIWrite 0ac5,00,0,7
SPIWrite 0ac4,00,0,7
SPIWrite 0acf,00,0,7
SPIWrite 0ace,00,0,7
SPIWrite 0acd,00,0,7
SPIWrite 0acc,00,0,7
SPIWrite 0ad7,00,0,7
SPIWrite 0ad6,00,0,7
SPIWrite 0ad5,00,0,7
SPIWrite 0ad4,00,0,7
SPIWrite 0adf,00,0,7
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SPIWrite 0ade,00,0,7
SPIWrite 0add,00,0,7
SPIWrite 0adc,00,0,7
SPIWrite 0ae7,00,0,7
SPIWrite 0ae6,00,0,7
SPIWrite 0ae5,00,0,7
SPIWrite 0ae4,00,0,7
SPIWrite 0bc8,ff,0,7
SPIWrite 0bd0,ff,0,7
SPIWrite 0bd8,ff,0,7
SPIWrite 0be0,ff,0,7
SPIWrite 0be8,ff,0,7
SPIWrite 0bf0,ff,0,7
SPIWrite 0bf8,ff,0,7
SPIWrite 0c00,ff,0,7
SPIWrite 0c08,ff,0,7
SPIWrite 0c10,ff,0,7
SPIWrite 0c18,ff,0,7
SPIWrite 0c20,ff,0,7
SPIWrite 0c28,ff,0,7
SPIWrite 0c30,ff,0,7
SPIWrite 0c38,ff,0,7
SPIWrite 0c40,ff,0,7
SPIWrite 0c48,ff,0,7
SPIWrite 0c50,ff,0,7
SPIWrite 0c58,ff,0,7
SPIWrite 0c60,ff,0,7
SPIWrite 0c68,ff,0,7
SPIWrite 0c70,ff,0,7
SPIWrite 0c78,ff,0,7
SPIWrite 0c80,ff,0,7
SPIWrite 0c88,ff,0,7
SPIWrite 0c90,ff,0,7
SPIWrite 0c98,ff,0,7
SPIWrite 0ca0,ff,0,7
SPIWrite 0ca8,ff,0,7
SPIWrite 0cb0,ff,0,7
SPIWrite 0cb8,ff,0,7
SPIWrite 0cc0,ff,0,7
SPIWrite 0cc8,ff,0,7
SPIWrite 0cd0,fe,0,7
SPIWrite 0cd8,fc,0,7
SPIWrite 0ce0,f8,0,7
SPIWrite 0ce8,f0,0,7
SPIWrite 0cf0,e0,0,7
SPIWrite 0cf8,c0,0,7
SPIWrite 0d00,80,0,7
SPIWrite 0bcf,ff,0,7
SPIWrite 0bce,ff,0,7
SPIWrite 0bcd,ff,0,7
SPIWrite 0bcc,ff,0,7
SPIWrite 0bd7,ff,0,7
SPIWrite 0bd6,ff,0,7
SPIWrite 0bd5,ff,0,7
SPIWrite 0bd4,fe,0,7
SPIWrite 0bdf,ff,0,7
SPIWrite 0bde,ff,0,7
SPIWrite 0bdd,ff,0,7
SPIWrite 0bdc,fc,0,7
SPIWrite 0be7,ff,0,7
SPIWrite 0be6,ff,0,7
SPIWrite 0be5,ff,0,7
SPIWrite 0be4,f8,0,7
SPIWrite 0bef,ff,0,7
SPIWrite 0bee,ff,0,7
SPIWrite 0bed,ff,0,7
SPIWrite 0bec,f0,0,7
SPIWrite 0bf7,ff,0,7
SPIWrite 0bf6,ff,0,7
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SPIWrite 0bf5,ff,0,7
SPIWrite 0bf4,e0,0,7
SPIWrite 0bff,ff,0,7
SPIWrite 0bfe,ff,0,7
SPIWrite 0bfd,ff,0,7
SPIWrite 0bfc,c0,0,7
SPIWrite 0c07,ff,0,7
SPIWrite 0c06,ff,0,7
SPIWrite 0c05,ff,0,7
SPIWrite 0c04,80,0,7
SPIWrite 0c0f,ff,0,7
SPIWrite 0c0e,ff,0,7
SPIWrite 0c0d,ff,0,7
SPIWrite 0c0c,00,0,7
SPIWrite 0c17,ff,0,7
SPIWrite 0c16,ff,0,7
SPIWrite 0c15,fe,0,7
SPIWrite 0c14,00,0,7
SPIWrite 0c1f,ff,0,7
SPIWrite 0c1e,ff,0,7
SPIWrite 0c1d,fc,0,7
SPIWrite 0c1c,00,0,7
SPIWrite 0c27,ff,0,7
SPIWrite 0c26,ff,0,7
SPIWrite 0c25,f8,0,7
SPIWrite 0c24,00,0,7
SPIWrite 0c2f,ff,0,7
SPIWrite 0c2e,ff,0,7
SPIWrite 0c2d,f0,0,7
SPIWrite 0c2c,00,0,7
SPIWrite 0c37,ff,0,7
SPIWrite 0c36,ff,0,7
SPIWrite 0c35,e0,0,7
SPIWrite 0c34,00,0,7
SPIWrite 0c3f,ff,0,7
SPIWrite 0c3e,ff,0,7
SPIWrite 0c3d,c0,0,7
SPIWrite 0c3c,00,0,7
SPIWrite 0c47,ff,0,7
SPIWrite 0c46,ff,0,7
SPIWrite 0c45,80,0,7
SPIWrite 0c44,00,0,7
SPIWrite 0c4f,ff,0,7
SPIWrite 0c4e,ff,0,7
SPIWrite 0c4d,00,0,7
SPIWrite 0c4c,00,0,7
SPIWrite 0c57,ff,0,7
SPIWrite 0c56,fe,0,7
SPIWrite 0c55,00,0,7
SPIWrite 0c54,00,0,7
SPIWrite 0c5f,ff,0,7
SPIWrite 0c5e,fc,0,7
SPIWrite 0c5d,00,0,7
SPIWrite 0c5c,00,0,7
SPIWrite 0c67,ff,0,7
SPIWrite 0c66,f8,0,7
SPIWrite 0c65,00,0,7
SPIWrite 0c64,00,0,7
SPIWrite 0c6f,ff,0,7
SPIWrite 0c6e,f0,0,7
SPIWrite 0c6d,00,0,7
SPIWrite 0c6c,00,0,7
SPIWrite 0c77,ff,0,7
SPIWrite 0c76,e0,0,7
SPIWrite 0c75,00,0,7
SPIWrite 0c74,00,0,7
SPIWrite 0c7f,ff,0,7
SPIWrite 0c7e,c0,0,7
SPIWrite 0c7d,00,0,7
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SPIWrite 0c7c,00,0,7
SPIWrite 0c87,ff,0,7
SPIWrite 0c86,80,0,7
SPIWrite 0c85,00,0,7
SPIWrite 0c84,00,0,7
SPIWrite 0c8f,ff,0,7
SPIWrite 0c8e,00,0,7
SPIWrite 0c8d,00,0,7
SPIWrite 0c8c,00,0,7
SPIWrite 0c97,fe,0,7
SPIWrite 0c96,00,0,7
SPIWrite 0c95,00,0,7
SPIWrite 0c94,00,0,7
SPIWrite 0c9f,fc,0,7
SPIWrite 0c9e,00,0,7
SPIWrite 0c9d,00,0,7
SPIWrite 0c9c,00,0,7
SPIWrite 0ca7,f8,0,7
SPIWrite 0ca6,00,0,7
SPIWrite 0ca5,00,0,7
SPIWrite 0ca4,00,0,7
SPIWrite 0caf,f0,0,7
SPIWrite 0cae,00,0,7
SPIWrite 0cad,00,0,7
SPIWrite 0cac,00,0,7
SPIWrite 0cb7,e0,0,7
SPIWrite 0cb6,00,0,7
SPIWrite 0cb5,00,0,7
SPIWrite 0cb4,00,0,7
SPIWrite 0cbf,c0,0,7
SPIWrite 0cbe,00,0,7
SPIWrite 0cbd,00,0,7
SPIWrite 0cbc,00,0,7
SPIWrite 0cc7,80,0,7
SPIWrite 0cc6,00,0,7
SPIWrite 0cc5,00,0,7
SPIWrite 0cc4,00,0,7
SPIWrite 0ccf,00,0,7
SPIWrite 0cce,00,0,7
SPIWrite 0ccd,00,0,7
SPIWrite 0ccc,00,0,7
SPIWrite 0cd7,00,0,7
SPIWrite 0cd6,00,0,7
SPIWrite 0cd5,00,0,7
SPIWrite 0cd4,00,0,7
SPIWrite 0cdf,00,0,7
SPIWrite 0cde,00,0,7
SPIWrite 0cdd,00,0,7
SPIWrite 0cdc,00,0,7
SPIWrite 0ce7,00,0,7
SPIWrite 0ce6,00,0,7
SPIWrite 0ce5,00,0,7
SPIWrite 0ce4,00,0,7
SPIWrite 0cef,00,0,7
SPIWrite 0cee,00,0,7
SPIWrite 0ced,00,0,7
SPIWrite 0cec,00,0,7
SPIWrite 0cf7,00,0,7
SPIWrite 0cf6,00,0,7
SPIWrite 0cf5,00,0,7
SPIWrite 0cf4,00,0,7
SPIWrite 0cff,00,0,7
SPIWrite 0cfe,00,0,7
SPIWrite 0cfd,00,0,7
SPIWrite 0cfc,00,0,7
SPIWrite 0d07,00,0,7
SPIWrite 0d06,00,0,7
SPIWrite 0d05,00,0,7
SPIWrite 0d04,00,0,7
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SPIWrite 09a2,00,0,7
SPIWrite 09a2,01,0,7
SPIWrite 09a2,00,0,7
SPIWrite 0bc2,00,0,7
SPIWrite 0bc2,01,0,7
SPIWrite 0bc2,00,0,7
SPIWrite 0101,18,0,7
SPIWrite 0121,18,0,7
SPIWrite 0103,01,0,7
SPIWrite 0123,01,0,7
SPIWrite 0100,01,0,7
SPIWrite 0102,00,0,7
SPIWrite 0102,01,0,7
SPIWrite 0102,00,0,7
SPIWrite 0100,00,0,7
SPIWrite 0102,00,0,7
SPIWrite 0102,01,0,7
SPIWrite 0102,00,0,7
SPIWrite 0120,01,0,7
SPIWrite 0122,00,0,7
SPIWrite 0122,01,0,7
SPIWrite 0122,00,0,7
SPIWrite 0120,00,0,7
SPIWrite 0122,00,0,7
SPIWrite 0122,01,0,7
SPIWrite 0122,00,0,7
SPIWrite 0103,00,0,7
SPIWrite 0123,00,0,7
SPIWrite 0155,0f,0,7
SPIWrite 0994,01,0,7
SPIWrite 0bb4,01,0,7
SPIWrite 0016,00,0,7    //PAGE: dsa=0x0;    Address(0x16[5:4],)
SPIWrite 0016,10,0,7    //PAGE: dsa=0x1;    Address(0x16[5:4],)
SPIWrite 0df2,00,0,7
SPIWrite 0df1,00,0,7
SPIWrite 0df0,00,0,7
SPIWrite 0df6,01,0,7
SPIWrite 0df5,08,0,7
SPIWrite 0df4,20,0,7
SPIWrite 0dfa,03,0,7
SPIWrite 0df9,0c,0,7
SPIWrite 0df8,4c,0,7
SPIWrite 0dfe,04,0,7
SPIWrite 0dfd,90,0,7
SPIWrite 0dfc,74,0,7
SPIWrite 0e02,06,0,7
SPIWrite 0e01,94,0,7
SPIWrite 0e00,a4,0,7
SPIWrite 0e06,08,0,7
SPIWrite 0e05,9c,0,7
SPIWrite 0e04,d8,0,7
SPIWrite 0e0a,0a,0,7
SPIWrite 0e09,a1,0,7
SPIWrite 0e08,0c,0,7
SPIWrite 0e0e,0c,0,7
SPIWrite 0e0d,a9,0,7
SPIWrite 0e0c,40,0,7
SPIWrite 0e12,0e,0,7
SPIWrite 0e11,ad,0,7
SPIWrite 0e10,74,0,7
SPIWrite 0e16,10,0,7
SPIWrite 0e15,b1,0,7
SPIWrite 0e14,a8,0,7
SPIWrite 0e1a,12,0,7
SPIWrite 0e19,b9,0,7
SPIWrite 0e18,dc,0,7
SPIWrite 0e1e,14,0,7
SPIWrite 0e1d,be,0,7
SPIWrite 0e1c,10,0,7
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SPIWrite 0e22,16,0,7
SPIWrite 0e21,c2,0,7
SPIWrite 0e20,44,0,7
SPIWrite 0e26,18,0,7
SPIWrite 0e25,46,0,7
SPIWrite 0e24,70,0,7
SPIWrite 0e2a,19,0,7
SPIWrite 0e29,ca,0,7
SPIWrite 0e28,94,0,7
SPIWrite 0e2e,1b,0,7
SPIWrite 0e2d,4e,0,7
SPIWrite 0e2c,b8,0,7
SPIWrite 0e32,1c,0,7
SPIWrite 0e31,d2,0,7
SPIWrite 0e30,d8,0,7
SPIWrite 0e36,1d,0,7
SPIWrite 0e35,d6,0,7
SPIWrite 0e34,f4,0,7
SPIWrite 0e3a,1e,0,7
SPIWrite 0e39,db,0,7
SPIWrite 0e38,10,0,7
SPIWrite 0e3e,1f,0,7
SPIWrite 0e3d,df,0,7
SPIWrite 0e3c,24,0,7
SPIWrite 0e42,1f,0,7
SPIWrite 0e41,e3,0,7
SPIWrite 0e40,40,0,7
SPIWrite 0e46,1f,0,7
SPIWrite 0e45,e7,0,7
SPIWrite 0e44,54,0,7
SPIWrite 0e4a,1f,0,7
SPIWrite 0e49,e7,0,7
SPIWrite 0e48,68,0,7
SPIWrite 0e4e,1f,0,7
SPIWrite 0e4d,e7,0,7
SPIWrite 0e4c,7c,0,7
SPIWrite 0e52,1f,0,7
SPIWrite 0e51,e7,0,7
SPIWrite 0e50,88,0,7
SPIWrite 0e56,1f,0,7
SPIWrite 0e55,e7,0,7
SPIWrite 0e54,98,0,7
SPIWrite 0e5a,1f,0,7
SPIWrite 0e59,e7,0,7
SPIWrite 0e58,a4,0,7
SPIWrite 0e5e,1f,0,7
SPIWrite 0e5d,e7,0,7
SPIWrite 0e5c,b0,0,7
SPIWrite 0e62,1f,0,7
SPIWrite 0e61,e7,0,7
SPIWrite 0e60,b8,0,7
SPIWrite 0e66,1f,0,7
SPIWrite 0e65,e7,0,7
SPIWrite 0e64,c0,0,7
SPIWrite 0e6a,1f,0,7
SPIWrite 0e69,e7,0,7
SPIWrite 0e68,c8,0,7
SPIWrite 0e6e,1f,0,7
SPIWrite 0e6d,e7,0,7
SPIWrite 0e6c,d0,0,7
SPIWrite 0dd1,01,0,7
SPIWrite 0016,20,0,7    //PAGE: dsa=0x2;    Address(0x16[5:4],)
SPIWrite 0df2,00,0,7
SPIWrite 0df1,00,0,7
SPIWrite 0df0,00,0,7
SPIWrite 0df6,00,0,7
SPIWrite 0df5,84,0,7
SPIWrite 0df4,88,0,7
SPIWrite 0dfa,01,0,7
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SPIWrite 0df9,10,0,7
SPIWrite 0df8,a0,0,7
SPIWrite 0dfe,02,0,7
SPIWrite 0dfd,98,0,7
SPIWrite 0dfc,b9,0,7
SPIWrite 0e02,04,0,7
SPIWrite 0e01,20,0,7
SPIWrite 0e00,df,0,7
SPIWrite 0e06,06,0,7
SPIWrite 0e05,25,0,7
SPIWrite 0e04,12,0,7
SPIWrite 0e0a,08,0,7
SPIWrite 0e09,a9,0,7
SPIWrite 0e08,41,0,7
SPIWrite 0e0e,0b,0,7
SPIWrite 0e0d,31,0,7
SPIWrite 0e0c,5e,0,7
SPIWrite 0e12,0f,0,7
SPIWrite 0e11,31,0,7
SPIWrite 0e10,92,0,7
SPIWrite 0e16,15,0,7
SPIWrite 0e15,b5,0,7
SPIWrite 0e14,98,0,7
SPIWrite 0e1a,20,0,7
SPIWrite 0e19,ba,0,7
SPIWrite 0e18,de,0,7
SPIWrite 0e1e,25,0,7
SPIWrite 0e1d,42,0,7
SPIWrite 0e1c,c0,0,7
SPIWrite 0e22,25,0,7
SPIWrite 0e21,4a,0,7
SPIWrite 0e20,d8,0,7
SPIWrite 0e26,25,0,7
SPIWrite 0e25,4b,0,7
SPIWrite 0e24,00,0,7
SPIWrite 0e2a,25,0,7
SPIWrite 0e29,53,0,7
SPIWrite 0e28,15,0,7
SPIWrite 0e2e,25,0,7
SPIWrite 0e2d,57,0,7
SPIWrite 0e2c,2b,0,7
SPIWrite 0e32,25,0,7
SPIWrite 0e31,5b,0,7
SPIWrite 0e30,40,0,7
SPIWrite 0e36,25,0,7
SPIWrite 0e35,5f,0,7
SPIWrite 0e34,53,0,7
SPIWrite 0e3a,25,0,7
SPIWrite 0e39,63,0,7
SPIWrite 0e38,64,0,7
SPIWrite 0e3e,25,0,7
SPIWrite 0e3d,67,0,7
SPIWrite 0e3c,74,0,7
SPIWrite 0e42,25,0,7
SPIWrite 0e41,6b,0,7
SPIWrite 0e40,81,0,7
SPIWrite 0e46,25,0,7
SPIWrite 0e45,6b,0,7
SPIWrite 0e44,81,0,7
SPIWrite 0e4a,25,0,7
SPIWrite 0e49,6b,0,7
SPIWrite 0e48,81,0,7
SPIWrite 0e4e,25,0,7
SPIWrite 0e4d,6b,0,7
SPIWrite 0e4c,81,0,7
SPIWrite 0e52,25,0,7
SPIWrite 0e51,6b,0,7
SPIWrite 0e50,81,0,7
SPIWrite 0e56,25,0,7
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SPIWrite 0e55,6b,0,7
SPIWrite 0e54,81,0,7
SPIWrite 0e5a,25,0,7
SPIWrite 0e59,6b,0,7
SPIWrite 0e58,81,0,7
SPIWrite 0e5e,25,0,7
SPIWrite 0e5d,6b,0,7
SPIWrite 0e5c,81,0,7
SPIWrite 0e62,25,0,7
SPIWrite 0e61,6b,0,7
SPIWrite 0e60,81,0,7
SPIWrite 0e66,25,0,7
SPIWrite 0e65,6b,0,7
SPIWrite 0e64,81,0,7
SPIWrite 0e6a,25,0,7
SPIWrite 0e69,6b,0,7
SPIWrite 0e68,81,0,7
SPIWrite 0e6e,25,0,7
SPIWrite 0e6d,6b,0,7
SPIWrite 0e6c,81,0,7
SPIWrite 0dd1,01,0,7

\\END: Done Top & DSA initialization

SPIWrite 0016,00,0,7    //PAGE: dsa=0x0;    Address(0x16[5:4],)
\\ STEP: clkMuxConfig/step0

\\START: Configuring PLL Mux

SPIWrite 0014,01,0,7    //PAGE: clktop_2t=0x1;  Address(0x14[1:0],)
SPIWrite 0064,00,0,7    //CTL_SEL_CLK_MUX_CROSS_PLL_TOP_1P8_L=0x0;(Meaning: );
Address(0x64[0:0],)
SPIWrite 0064,02,0,7    //CTL_SEL_CLK_MUX_CROSS_PLL_TOP_1P8_R=0x1;(Meaning: );
Address(0x64[1:1],)
SPIWrite 0062,01,0,7    //CTL_SEL_CLK_MUX_CROSS_PLL_BOT_L=0x1;(Meaning: );  Address(0x60[16:16],)
SPIWrite 0062,01,0,7    //CTL_SEL_CLK_MUX_CROSS_PLL_BOT_R=0x0;(Meaning: );  Address(0x60[17:17],)
SPIWrite 0070,04,0,7    //FORCE_PDN_GBL_RXCML_L=0x1;    Address(0x70[2:2],)
SPIWrite 0070,04,0,7    //FORCE_PDN_GBL_RXCML_R=0x0;    Address(0x70[3:3],)
SPIWrite 0071,00,0,7    //SEL_CLK_MUX_RX_1P8_L=0x0;(Meaning: );     Address(0x70[8:8],)
SPIWrite 0071,02,0,7    //SEL_CLK_MUX_RX_1P8_R=0x1;(Meaning: );     Address(0x70[9:9],)
SPIWrite 0071,02,0,7    //SEL_CLK_MUX_TX_1P8_L=0x0;(Meaning: );     Address(0x70[10:10],)
SPIWrite 0071,0a,0,7    //SEL_CLK_MUX_TX_1P8_R=0x1;(Meaning: );     Address(0x70[11:11],)
SPIWrite 0071,2a,0,7    //SEL_PDN_FAST_MUX_31_CROSS_1P8=0x1;    Address(0x70[13:13],)
SPIWrite 0060,01,0,7    //CTL_EN_CROSS_PLL_BLOCK_1P8=0x1;(Meaning: );   Address(0x60[0:0],)
SPIWrite 0060,03,0,7    //CTL_SEL_CROSS_PLL_DIR_1P8=0x1;(Meaning: );    Address(0x60[1:1],)
SPIWrite 0014,00,0,7    //PAGE: clktop_2t=0x0;  Address(0x14[1:0],)
SPIWrite 0011,10,0,7    //PAGE: rx_ec_q=0x1;    Address(0x11[7:4],)
SPIWrite 0f0d,20,0,7
SPIWrite 0011,20,0,7    //PAGE: rx_ec_q=0x2;    Address(0x11[7:4],)
SPIWrite 0f0d,20,0,7
SPIWrite 0011,40,0,7    //PAGE: rx_ec_q=0x4;    Address(0x11[7:4],)
SPIWrite 0f0d,00,0,7
SPIWrite 0011,80,0,7    //PAGE: rx_ec_q=0x8;    Address(0x11[7:4],)
SPIWrite 0f0d,00,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0a00,01,0,7    //use_register_values_for_refclk_trim=0x1;  Address(0xa00[0:0],)
SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0014,01,0,7    //PAGE: clktop_2t=0x1;  Address(0x14[1:0],)
SPIWrite 0065,08,0,7    //CTL_LOWPOWER_MODE_REFINBUF_1P8=0x1;   Address(0x64[11:11],)
SPIWrite 0065,18,0,7    //CTL_LOWPOWER_MODE_SYSREFBUF_1P8=0x1;  Address(0x64[12:12],)

\\END: Done configuring PLL Mux

SPIWrite 0014,00,0,7    //PAGE: clktop_2t=0x0;  Address(0x14[1:0],)
\\ STEP: serdesConfig/step0

\\START: Enabling access to SERDES
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```
SPIWrite 0015,08,0,7    //PAGE: jesd_subchip=0x1;(Meaning: );   Address(0x15[3:3],)
SPIWrite 0020,07,0,7
SPIWrite 0020,07,0,7
SPIWrite 0021,12,0,7
SPIWrite 0022,12,0,7
SPIWrite 0021,12,0,7
SPIWrite 0022,12,0,7
SPIWrite 0021,12,0,7
SPIWrite 0022,12,0,7
SPIWrite 0015,00,0,7    //PAGE: jesd_subchip=0x0;(Meaning: );   Address(0x15[3:3],)
SPIWrite 0015,04,0,7    //PAGE: SERDES=0x1;     Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,04,0,7
SPIWrite 7007,00,0,7    //BUS_WIDTH_LANE3=0x0;  Address(0x9803[3:3],)
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7    //BUS_WIDTH_LANE2=0x0;  Address(0x9803[2:2],)
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7    //BUS_WIDTH_LANE1=0x0;  Address(0x9803[1:1],)
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7    //BUS_WIDTH_LANE0=0x0;  Address(0x9803[0:0],)
SPIWrite 7006,00,0,7
SPIWrite 0015,00,0,7    //PAGE: SERDES=0x2;     Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,40,0,7
SPIWrite 7007,00,0,7    //BUS_WIDTH_LANE3=0x0;  Address(0x9803[3:3],)
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7    //BUS_WIDTH_LANE2=0x0;  Address(0x9803[2:2],)
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7    //BUS_WIDTH_LANE1=0x0;  Address(0x9803[1:1],)
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7    //BUS_WIDTH_LANE0=0x0;  Address(0x9803[0:0],)
SPIWrite 7006,00,0,7

\\END: Done enabling access to SERDES


\\Forcing the sync pins to high to ensure random data for SERDES adaptation.

SPIWrite 0015,40,0,7    //PAGE: SERDES=0x0;     Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,00,0,7
SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0520,02,0,7    //buf_dir_ctrl_gpio_72=0x2;     Address(0x520[1:0],)
SPIWrite 0520,02,0,7    //preferred_input_sel_gpio_72=0x0;  Address(0x520[4:2],)
SPIWrite 0520,22,0,7    //preferred_output_sel_gpio_72=0x1;     Address(0x520[7:5],)
SPIWrite 0521,00,0,7    //crossbar_sel_input_gpio_72=0x0;   Address(0x520[15:8],)
SPIWrite 0522,00,0,7    //crossbar_sel_output_gpio_72=0x0;  Address(0x520[23:16],)
SPIWrite 0523,00,0,7    //activ_bir_dir_ctrl_gpio_72=0x0;   Address(0x520[27:25],)
SPIWrite 0528,02,0,7    //buf_dir_ctrl_gpio_74=0x2;     Address(0x528[1:0],)
SPIWrite 0528,02,0,7    //preferred_input_sel_gpio_74=0x0;  Address(0x528[4:2],)
SPIWrite 0528,22,0,7    //preferred_output_sel_gpio_74=0x1;     Address(0x528[7:5],)
SPIWrite 0529,00,0,7    //crossbar_sel_input_gpio_74=0x0;   Address(0x528[15:8],)
SPIWrite 052a,00,0,7    //crossbar_sel_output_gpio_74=0x0;  Address(0x528[23:16],)
SPIWrite 052b,00,0,7    //activ_bir_dir_ctrl_gpio_74=0x0;   Address(0x528[27:25],)
SPIWrite 04bc,02,0,7    //buf_dir_ctrl_gpio_47=0x2;     Address(0x4bc[1:0],)
SPIWrite 04bc,02,0,7    //preferred_input_sel_gpio_47=0x0;  Address(0x4bc[4:2],)
SPIWrite 04bc,22,0,7    //preferred_output_sel_gpio_47=0x1;     Address(0x4bc[7:5],)
SPIWrite 04bd,00,0,7    //crossbar_sel_input_gpio_47=0x0;   Address(0x4bc[15:8],)
SPIWrite 04be,00,0,7    //crossbar_sel_output_gpio_47=0x0;  Address(0x4bc[23:16],)
SPIWrite 04bf,00,0,7    //activ_bir_dir_ctrl_gpio_47=0x0;   Address(0x4bc[27:25],)
SPIWrite 04c4,02,0,7    //buf_dir_ctrl_gpio_49=0x2;     Address(0x4c4[1:0],)
SPIWrite 04c4,02,0,7    //preferred_input_sel_gpio_49=0x0;  Address(0x4c4[4:2],)
SPIWrite 04c4,22,0,7    //preferred_output_sel_gpio_49=0x1;     Address(0x4c4[7:5],)
SPIWrite 04c5,00,0,7    //crossbar_sel_input_gpio_49=0x0;   Address(0x4c4[15:8],)
SPIWrite 04c6,00,0,7    //crossbar_sel_output_gpio_49=0x0;  Address(0x4c4[23:16],)
SPIWrite 04c7,00,0,7    //activ_bir_dir_ctrl_gpio_49=0x0;   Address(0x4c4[27:25],)
SPIWrite 039c,00,0,7    //sync_lvds_mode_ab=0x0;(Meaning: );    Address(0x39c[0:0],)
SPIWrite 039c,00,0,7    //sync_lvds_mode_cd=0x0;(Meaning: );    Address(0x39c[1:1],)
SPIWrite 0555,02,0,7    //ovr_sel_intpo_dac_sync_n_ab_0=0x1;    Address(0x554[9:9],)
SPIWrite 0555,0a,0,7    //ovr_sel_intpo_dac_sync_n_ab_1=0x1;    Address(0x554[11:11],)
SPIWrite 0555,2a,0,7    //ovr_sel_intpo_dac_sync_n_cd_0=0x1;    Address(0x554[13:13],)
SPIWrite 0555,aa,0,7    //ovr_sel_intpo_dac_sync_n_cd_1=0x1;    Address(0x554[15:15],)
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SPIWrite 0555,ba,0,7    //ovr_intpo_dac_sync_n_cd_0=0x1;    Address(0x554[12:12],)
SPIWrite 0555,bb,0,7    //ovr_intpo_dac_sync_n_ab_0=0x1;    Address(0x554[8:8],)
SPIWrite 0555,bf,0,7    //ovr_intpo_dac_sync_n_ab_1=0x1;    Address(0x554[10:10],)
SPIWrite 0555,ff,0,7    //ovr_intpo_dac_sync_n_cd_1=0x1;    Address(0x554[14:14],)
SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
\\ STEP: serdesConfig/step1

\\START: Resetting Serdes

SPIWrite 0015,04,0,7    //PAGE: SERDES=0x1;     Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,04,0,7
SPIWrite 701b,08,0,7    //DOMAIN_RESET=0x888;   Address(0x980d[11:0],)
SPIWrite 701a,88,0,7
SPIWrite 701b,00,0,7    //DOMAIN_RESET=0x0;     Address(0x980d[11:0],)
SPIWrite 701a,00,0,7

WAIT 0.1

SPIWrite 701b,07,0,7    //DOMAIN_RESET=0x777;   Address(0x980d[11:0],)
SPIWrite 701a,77,0,7
SPIWrite 701b,00,0,7    //DOMAIN_RESET=0x0;     Address(0x980d[11:0],)
SPIWrite 701a,00,0,7

WAIT 0.1


\\END: Done resetting Serdes


\\START: Resetting Serdes

SPIWrite 0015,00,0,7    //PAGE: SERDES=0x2;     Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,40,0,7
SPIWrite 701b,08,0,7    //DOMAIN_RESET=0x888;   Address(0x980d[11:0],)
SPIWrite 701a,88,0,7
SPIWrite 701b,00,0,7    //DOMAIN_RESET=0x0;     Address(0x980d[11:0],)
SPIWrite 701a,00,0,7

WAIT 0.1

SPIWrite 701b,07,0,7    //DOMAIN_RESET=0x777;   Address(0x980d[11:0],)
SPIWrite 701a,77,0,7
SPIWrite 701b,00,0,7    //DOMAIN_RESET=0x0;     Address(0x980d[11:0],)
SPIWrite 701a,00,0,7

WAIT 0.1


\\END: Done resetting Serdes

SPIWrite 0015,40,0,7    //PAGE: SERDES=0x0;     Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,00,0,7
\\ STEP: serdesConfig/step2

\\START: Configuring the SERDES

SPIWrite 0015,08,0,7    //PAGE: jesd_subchip=0x1;(Meaning: );   Address(0x15[3:3],)
SPIWrite 0021,12,0,7
SPIWrite 0022,12,0,7
SPIWrite 0015,00,0,7    //PAGE: jesd_subchip=0x0;(Meaning: );   Address(0x15[3:3],)
SPIWrite 0015,04,0,7    //PAGE: SERDES=0x3;     Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,44,0,7
SPIWrite 702f,c0,0,7
SPIWrite 702e,00,0,7

WAIT 0.01

SPIWrite 7029,ff,0,7
SPIWrite 7028,f0,0,7
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SPIWrite 701b,0a,0,7
SPIWrite 701a,aa,0,7
SPIWrite 701b,00,0,7
SPIWrite 701a,00,0,7

WAIT 0.01

SPIWrite 702f,00,0,7
SPIWrite 702e,00,0,7
SPIWrite 7007,00,0,7
SPIWrite 7006,00,0,7
SPIWrite 49f1,92,0,7
SPIWrite 49f0,40,0,7
SPIWrite 49f3,ea,0,7
SPIWrite 49f2,80,0,7
SPIWrite 49e3,f0,0,7
SPIWrite 49e2,00,0,7
SPIWrite 49b5,47,0,7
SPIWrite 49b4,47,0,7
SPIWrite 49ff,fd,0,7
SPIWrite 49fe,b0,0,7
SPIWrite 49ed,1d,0,7
SPIWrite 49ec,c0,0,7
SPIWrite 49e7,52,0,7
SPIWrite 49e6,36,0,7
SPIWrite 49e5,6e,0,7
SPIWrite 49e4,b6,0,7
SPIWrite 49df,a8,0,7
SPIWrite 49de,28,0,7
SPIWrite 49eb,0a,0,7
SPIWrite 49ea,9e,0,7
SPIWrite 49e9,72,0,7
SPIWrite 49e8,44,0,7
SPIWrite 49fd,0a,0,7
SPIWrite 49fc,9e,0,7
SPIWrite 49fb,72,0,7
SPIWrite 49fa,48,0,7
SPIWrite 49f9,4a,0,7
SPIWrite 49f8,66,0,7
SPIWrite 49f7,79,0,7
SPIWrite 49f6,b6,0,7
SPIWrite 49d9,6c,0,7
SPIWrite 49d8,06,0,7
SPIWrite 4601,10,0,7
SPIWrite 4600,6b,0,7
SPIWrite 4603,64,0,7
SPIWrite 4602,80,0,7
SPIWrite 4605,62,0,7
SPIWrite 4604,00,0,7
SPIWrite 4607,7b,0,7
SPIWrite 4606,33,0,7
SPIWrite 4609,70,0,7
SPIWrite 4608,0a,0,7
SPIWrite 460b,bd,0,7
SPIWrite 460a,68,0,7
SPIWrite 460d,76,0,7
SPIWrite 460c,2d,0,7
SPIWrite 460f,66,0,7
SPIWrite 460e,ab,0,7
SPIWrite 4611,d0,0,7
SPIWrite 4610,08,0,7
SPIWrite 4613,00,0,7
SPIWrite 4612,18,0,7
SPIWrite 4615,66,0,7
SPIWrite 4614,2c,0,7
SPIWrite 4617,3d,0,7
SPIWrite 4616,15,0,7
SPIWrite 4619,00,0,7
SPIWrite 4618,80,0,7
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SPIWrite 461b,00,0,7
SPIWrite 461a,02,0,7
SPIWrite 461d,34,0,7
SPIWrite 461c,00,0,7
SPIWrite 461f,00,0,7
SPIWrite 461e,00,0,7
SPIWrite 4621,10,0,7
SPIWrite 4620,1a,0,7
SPIWrite 4639,03,0,7
SPIWrite 4638,40,0,7
SPIWrite 463b,00,0,7
SPIWrite 463a,60,0,7
SPIWrite 463d,00,0,7
SPIWrite 463c,00,0,7
SPIWrite 463f,00,0,7
SPIWrite 463e,00,0,7
SPIWrite 4677,00,0,7
SPIWrite 4676,00,0,7
SPIWrite 4679,00,0,7
SPIWrite 4678,00,0,7
SPIWrite 467b,00,0,7
SPIWrite 467a,00,0,7
SPIWrite 467d,00,0,7
SPIWrite 467c,00,0,7
SPIWrite 4683,9f,0,7
SPIWrite 4682,df,0,7
SPIWrite 4685,b3,0,7
SPIWrite 4684,c0,0,7
SPIWrite 468f,3b,0,7
SPIWrite 468e,9a,0,7
SPIWrite 4691,fa,0,7
SPIWrite 4690,cf,0,7
SPIWrite 4693,bd,0,7
SPIWrite 4692,3c,0,7
SPIWrite 4695,76,0,7
SPIWrite 4694,60,0,7
SPIWrite 4697,06,0,7
SPIWrite 4696,db,0,7
SPIWrite 4741,03,0,7
SPIWrite 4740,41,0,7
SPIWrite 47e7,00,0,7
SPIWrite 47e6,80,0,7
SPIWrite 47e9,fc,0,7
SPIWrite 47e8,00,0,7
SPIWrite 47eb,9f,0,7
SPIWrite 47ea,fe,0,7
SPIWrite 47ed,00,0,7
SPIWrite 47ec,e0,0,7
SPIWrite 47ef,10,0,7
SPIWrite 47ee,00,0,7
SPIWrite 47f1,68,0,7
SPIWrite 47f0,64,0,7
SPIWrite 47f3,92,0,7
SPIWrite 47f2,30,0,7
SPIWrite 47f5,00,0,7
SPIWrite 47f4,00,0,7
SPIWrite 47f7,6d,0,7
SPIWrite 47f6,87,0,7
SPIWrite 47f9,db,0,7
SPIWrite 47f8,6c,0,7
SPIWrite 47fb,42,0,7
SPIWrite 47fa,46,0,7
SPIWrite 47fd,62,0,7
SPIWrite 47fc,7c,0,7
SPIWrite 47ff,88,0,7
SPIWrite 47fe,c8,0,7
SPIWrite 4401,10,0,7
SPIWrite 4400,6b,0,7
SPIWrite 4403,64,0,7
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SPIWrite 4402,80,0,7
SPIWrite 4405,62,0,7
SPIWrite 4404,00,0,7
SPIWrite 4407,7b,0,7
SPIWrite 4406,33,0,7
SPIWrite 4409,70,0,7
SPIWrite 4408,0a,0,7
SPIWrite 440b,bd,0,7
SPIWrite 440a,68,0,7
SPIWrite 440d,76,0,7
SPIWrite 440c,2d,0,7
SPIWrite 440f,66,0,7
SPIWrite 440e,ab,0,7
SPIWrite 4411,d0,0,7
SPIWrite 4410,08,0,7
SPIWrite 4413,00,0,7
SPIWrite 4412,18,0,7
SPIWrite 4415,66,0,7
SPIWrite 4414,2c,0,7
SPIWrite 4417,3d,0,7
SPIWrite 4416,15,0,7
SPIWrite 4419,00,0,7
SPIWrite 4418,80,0,7
SPIWrite 441b,00,0,7
SPIWrite 441a,02,0,7
SPIWrite 441d,34,0,7
SPIWrite 441c,00,0,7
SPIWrite 441f,00,0,7
SPIWrite 441e,00,0,7
SPIWrite 4421,10,0,7
SPIWrite 4420,1a,0,7
SPIWrite 4439,03,0,7
SPIWrite 4438,40,0,7
SPIWrite 443b,00,0,7
SPIWrite 443a,60,0,7
SPIWrite 443d,00,0,7
SPIWrite 443c,00,0,7
SPIWrite 443f,00,0,7
SPIWrite 443e,00,0,7
SPIWrite 4477,00,0,7
SPIWrite 4476,00,0,7
SPIWrite 4479,00,0,7
SPIWrite 4478,00,0,7
SPIWrite 447b,00,0,7
SPIWrite 447a,00,0,7
SPIWrite 447d,00,0,7
SPIWrite 447c,00,0,7
SPIWrite 4483,9f,0,7
SPIWrite 4482,df,0,7
SPIWrite 4485,b3,0,7
SPIWrite 4484,c0,0,7
SPIWrite 448f,3b,0,7
SPIWrite 448e,9a,0,7
SPIWrite 4491,fa,0,7
SPIWrite 4490,cf,0,7
SPIWrite 4493,bd,0,7
SPIWrite 4492,3c,0,7
SPIWrite 4495,76,0,7
SPIWrite 4494,60,0,7
SPIWrite 4497,06,0,7
SPIWrite 4496,db,0,7
SPIWrite 4541,03,0,7
SPIWrite 4540,41,0,7
SPIWrite 45e7,00,0,7
SPIWrite 45e6,80,0,7
SPIWrite 45e9,fc,0,7
SPIWrite 45e8,00,0,7
SPIWrite 45eb,9f,0,7
SPIWrite 45ea,fe,0,7
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SPIWrite 45ed,00,0,7
SPIWrite 45ec,e0,0,7
SPIWrite 45ef,10,0,7
SPIWrite 45ee,00,0,7
SPIWrite 45f1,68,0,7
SPIWrite 45f0,64,0,7
SPIWrite 45f3,92,0,7
SPIWrite 45f2,30,0,7
SPIWrite 45f5,00,0,7
SPIWrite 45f4,00,0,7
SPIWrite 45f7,6d,0,7
SPIWrite 45f6,87,0,7
SPIWrite 45f9,db,0,7
SPIWrite 45f8,6c,0,7
SPIWrite 45fb,42,0,7
SPIWrite 45fa,46,0,7
SPIWrite 45fd,62,0,7
SPIWrite 45fc,7c,0,7
SPIWrite 45ff,88,0,7
SPIWrite 45fe,c8,0,7
SPIWrite 4001,10,0,7
SPIWrite 4000,6b,0,7
SPIWrite 4003,64,0,7
SPIWrite 4002,80,0,7
SPIWrite 4005,62,0,7
SPIWrite 4004,00,0,7
SPIWrite 4007,7b,0,7
SPIWrite 4006,33,0,7
SPIWrite 4009,70,0,7
SPIWrite 4008,0a,0,7
SPIWrite 400b,bd,0,7
SPIWrite 400a,68,0,7
SPIWrite 400d,76,0,7
SPIWrite 400c,2d,0,7
SPIWrite 400f,66,0,7
SPIWrite 400e,ab,0,7
SPIWrite 4011,d0,0,7
SPIWrite 4010,08,0,7
SPIWrite 4013,00,0,7
SPIWrite 4012,18,0,7
SPIWrite 4015,66,0,7
SPIWrite 4014,2c,0,7
SPIWrite 4017,3d,0,7
SPIWrite 4016,15,0,7
SPIWrite 4019,00,0,7
SPIWrite 4018,80,0,7
SPIWrite 401b,00,0,7
SPIWrite 401a,02,0,7
SPIWrite 401d,34,0,7
SPIWrite 401c,00,0,7
SPIWrite 401f,00,0,7
SPIWrite 401e,00,0,7
SPIWrite 4021,10,0,7
SPIWrite 4020,1a,0,7
SPIWrite 4039,03,0,7
SPIWrite 4038,40,0,7
SPIWrite 403b,00,0,7
SPIWrite 403a,60,0,7
SPIWrite 403d,00,0,7
SPIWrite 403c,00,0,7
SPIWrite 403f,00,0,7
SPIWrite 403e,00,0,7
SPIWrite 4077,00,0,7
SPIWrite 4076,00,0,7
SPIWrite 4079,00,0,7
SPIWrite 4078,00,0,7
SPIWrite 407b,00,0,7
SPIWrite 407a,00,0,7
SPIWrite 407d,00,0,7
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SPIWrite 407c,00,0,7
SPIWrite 4083,9f,0,7
SPIWrite 4082,df,0,7
SPIWrite 4085,b3,0,7
SPIWrite 4084,c0,0,7
SPIWrite 408f,3b,0,7
SPIWrite 408e,9a,0,7
SPIWrite 4091,fa,0,7
SPIWrite 4090,cf,0,7
SPIWrite 4093,bd,0,7
SPIWrite 4092,3c,0,7
SPIWrite 4095,76,0,7
SPIWrite 4094,60,0,7
SPIWrite 4097,06,0,7
SPIWrite 4096,db,0,7
SPIWrite 4141,03,0,7
SPIWrite 4140,41,0,7
SPIWrite 41e7,00,0,7
SPIWrite 41e6,80,0,7
SPIWrite 41e9,fc,0,7
SPIWrite 41e8,00,0,7
SPIWrite 41eb,9f,0,7
SPIWrite 41ea,fe,0,7
SPIWrite 41ed,00,0,7
SPIWrite 41ec,e0,0,7
SPIWrite 41ef,10,0,7
SPIWrite 41ee,00,0,7
SPIWrite 41f1,68,0,7
SPIWrite 41f0,64,0,7
SPIWrite 41f3,92,0,7
SPIWrite 41f2,30,0,7
SPIWrite 41f5,00,0,7
SPIWrite 41f4,00,0,7
SPIWrite 41f7,6d,0,7
SPIWrite 41f6,87,0,7
SPIWrite 41f9,db,0,7
SPIWrite 41f8,6c,0,7
SPIWrite 41fb,42,0,7
SPIWrite 41fa,46,0,7
SPIWrite 41fd,62,0,7
SPIWrite 41fc,7c,0,7
SPIWrite 41ff,88,0,7
SPIWrite 41fe,c8,0,7
SPIWrite 4201,10,0,7
SPIWrite 4200,6b,0,7
SPIWrite 4203,64,0,7
SPIWrite 4202,80,0,7
SPIWrite 4205,62,0,7
SPIWrite 4204,00,0,7
SPIWrite 4207,7b,0,7
SPIWrite 4206,33,0,7
SPIWrite 4209,70,0,7
SPIWrite 4208,0a,0,7
SPIWrite 420b,bd,0,7
SPIWrite 420a,68,0,7
SPIWrite 420d,76,0,7
SPIWrite 420c,2d,0,7
SPIWrite 420f,66,0,7
SPIWrite 420e,ab,0,7
SPIWrite 4211,d0,0,7
SPIWrite 4210,08,0,7
SPIWrite 4213,00,0,7
SPIWrite 4212,18,0,7
SPIWrite 4215,66,0,7
SPIWrite 4214,2c,0,7
SPIWrite 4217,3d,0,7
SPIWrite 4216,15,0,7
SPIWrite 4219,00,0,7
SPIWrite 4218,80,0,7
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SPIWrite 421b,00,0,7
SPIWrite 421a,02,0,7
SPIWrite 421d,34,0,7
SPIWrite 421c,00,0,7
SPIWrite 421f,00,0,7
SPIWrite 421e,00,0,7
SPIWrite 4221,10,0,7
SPIWrite 4220,1a,0,7
SPIWrite 4239,03,0,7
SPIWrite 4238,40,0,7
SPIWrite 423b,00,0,7
SPIWrite 423a,60,0,7
SPIWrite 423d,00,0,7
SPIWrite 423c,00,0,7
SPIWrite 423f,00,0,7
SPIWrite 423e,00,0,7
SPIWrite 4277,00,0,7
SPIWrite 4276,00,0,7
SPIWrite 4279,00,0,7
SPIWrite 4278,00,0,7
SPIWrite 427b,00,0,7
SPIWrite 427a,00,0,7
SPIWrite 427d,00,0,7
SPIWrite 427c,00,0,7
SPIWrite 4283,9f,0,7
SPIWrite 4282,df,0,7
SPIWrite 4285,b3,0,7
SPIWrite 4284,c0,0,7
SPIWrite 428f,3b,0,7
SPIWrite 428e,9a,0,7
SPIWrite 4291,fa,0,7
SPIWrite 4290,cf,0,7
SPIWrite 4293,bd,0,7
SPIWrite 4292,3c,0,7
SPIWrite 4295,76,0,7
SPIWrite 4294,60,0,7
SPIWrite 4297,06,0,7
SPIWrite 4296,db,0,7
SPIWrite 4341,03,0,7
SPIWrite 4340,41,0,7
SPIWrite 43e7,00,0,7
SPIWrite 43e6,80,0,7
SPIWrite 43e9,fc,0,7
SPIWrite 43e8,00,0,7
SPIWrite 43eb,9f,0,7
SPIWrite 43ea,fe,0,7
SPIWrite 43ed,00,0,7
SPIWrite 43ec,e0,0,7
SPIWrite 43ef,10,0,7
SPIWrite 43ee,00,0,7
SPIWrite 43f1,68,0,7
SPIWrite 43f0,64,0,7
SPIWrite 43f3,92,0,7
SPIWrite 43f2,30,0,7
SPIWrite 43f5,00,0,7
SPIWrite 43f4,00,0,7
SPIWrite 43f7,6d,0,7
SPIWrite 43f6,87,0,7
SPIWrite 43f9,db,0,7
SPIWrite 43f8,6c,0,7
SPIWrite 43fb,42,0,7
SPIWrite 43fa,46,0,7
SPIWrite 43fd,62,0,7
SPIWrite 43fc,7c,0,7
SPIWrite 43ff,88,0,7
SPIWrite 43fe,c8,0,7
SPIWrite 7007,00,0,7    //BUS_WIDTH_LANE0=0x0;  Address(0x9803[0:0],)
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7    //BUS_WIDTH_LANE1=0x0;  Address(0x9803[1:1],)
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```
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7    //BUS_WIDTH_LANE2=0x0;  Address(0x9803[2:2],)
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7    //BUS_WIDTH_LANE3=0x0;  Address(0x9803[3:3],)
SPIWrite 7006,00,0,7
SPIWrite 0015,40,0,7    //PAGE: SERDES=0x0;     Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,00,0,7

\\END: Done configuring the SERDES

\\ STEP: serdesConfig/step3

\\START: Loading Serdes Firmware.

SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,01,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0193,82,0,7

SPIPoll 00f0,0,7,7


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,01,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,82,0,7

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0x20[4:4],)


\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0x20[5:5],)


\\Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0x20[6:6],)


\\Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0x20[7:7],)

SPIWrite 0013,00,0,7    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
SPIWrite 0015,04,0,7    //PAGE: SERDES=0x3;     Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,44,0,7
SPIWrite 702d,00,0,7
SPIWrite 702c,05,0,7
SPIWrite 7025,00,0,7
SPIWrite 7024,08,0,7
SPIWrite 702b,e0,0,7
SPIWrite 702a,20,0,7

WAIT 0.01
```

```
SPIWrite 702d,00,0,7
SPIWrite 702c,02,0,7
SPIWrite 7025,00,0,7
SPIWrite 7024,50,0,7
SPIWrite 702b,e0,0,7
SPIWrite 702a,20,0,7

WAIT 0.01

SPIWrite 701b,07,0,7    //DOMAIN_RESET=0x777;   Address(0x980d[11:0],)
SPIWrite 701a,77,0,7
SPIWrite 701b,00,0,7    //DOMAIN_RESET=0x0;     Address(0x980d[11:0],)
SPIWrite 701a,00,0,7

WAIT 5

SPIWrite 0015,40,0,7    //PAGE: SERDES=0x0;     Address(0x15[2:2],0x15[6:6],)
SPIWrite 0015,00,0,7

\\END: Done loading Serdes Firmware.

\\ STEP: sigChainConfig/step0

\\START: Configuring JESD TX Lane Mux

SPIWrite 0015,08,0,7    //PAGE: jesd_subchip=0x1;(Meaning: );   Address(0x15[3:3],)
SPIWrite 004a,10,0,7
SPIWrite 004a,10,0,7
SPIWrite 004b,34,0,7
SPIWrite 004b,54,0,7
SPIWrite 004c,52,0,7
SPIWrite 004c,32,0,7
SPIWrite 004d,76,0,7
SPIWrite 004d,76,0,7
SPIWrite 004e,10,0,7
SPIWrite 004e,10,0,7
SPIWrite 004f,34,0,7
SPIWrite 004f,54,0,7
SPIWrite 0050,52,0,7
SPIWrite 0050,32,0,7
SPIWrite 0051,76,0,7
SPIWrite 0051,76,0,7

\\END: Done configuring JESD TX Lane Mux


\\START: Configuring JESD RX Lane Mux

SPIWrite 0068,10,0,7
SPIWrite 0068,10,0,7
SPIWrite 0069,32,0,7
SPIWrite 0069,32,0,7
SPIWrite 006a,54,0,7
SPIWrite 006a,54,0,7
SPIWrite 006b,76,0,7
SPIWrite 006b,76,0,7
SPIWrite 006c,10,0,7
SPIWrite 006c,10,0,7
SPIWrite 006d,32,0,7
SPIWrite 006d,32,0,7
SPIWrite 006e,54,0,7
SPIWrite 006e,54,0,7
SPIWrite 006f,76,0,7
SPIWrite 006f,76,0,7

\\END: Done configuring JESD RX Lane Mux
```

\\START: Configuring the Data Muxes

```
SPIWrite 0044,50,0,7
SPIWrite 0044,50,0,7
SPIWrite 0044,50,0,7
SPIWrite 0044,50,0,7
SPIWrite 0045,fa,0,7
SPIWrite 0045,fa,0,7
SPIWrite 0045,fa,0,7
SPIWrite 0045,fa,0,7
SPIWrite 0046,fa,0,7
SPIWrite 0046,fa,0,7
SPIWrite 0046,fa,0,7
SPIWrite 0046,fa,0,7
SPIWrite 0047,50,0,7
SPIWrite 0047,50,0,7
SPIWrite 0047,50,0,7
SPIWrite 0047,50,0,7
SPIWrite 003a,e4,0,7
SPIWrite 003a,e4,0,7
SPIWrite 003a,e4,0,7
SPIWrite 003a,e4,0,7
SPIWrite 003b,e4,0,7
SPIWrite 003b,e4,0,7
SPIWrite 003b,e4,0,7
SPIWrite 003b,e4,0,7
SPIWrite 003c,00,0,7
SPIWrite 003c,00,0,7
SPIWrite 003d,11,0,7
SPIWrite 003d,11,0,7
SPIWrite 003e,44,0,7
SPIWrite 003e,44,0,7
SPIWrite 003f,55,0,7
SPIWrite 003f,55,0,7
SPIWrite 0036,d8,0,7
SPIWrite 0036,d8,0,7
SPIWrite 0036,d8,0,7
SPIWrite 0036,d8,0,7
SPIWrite 0037,d8,0,7
SPIWrite 0037,d8,0,7
SPIWrite 0037,d8,0,7
SPIWrite 0037,d8,0,7
SPIWrite 0040,44,0,7
SPIWrite 0040,44,0,7
SPIWrite 0041,55,0,7
SPIWrite 0041,55,0,7
SPIWrite 0042,00,0,7
SPIWrite 0042,00,0,7
SPIWrite 0043,11,0,7
SPIWrite 0043,11,0,7
SPIWrite 0038,d8,0,7
SPIWrite 0038,d8,0,7
SPIWrite 0038,d8,0,7
SPIWrite 0038,d8,0,7
SPIWrite 0039,d8,0,7
SPIWrite 0039,d8,0,7
SPIWrite 0039,d8,0,7
SPIWrite 0039,d8,0,7
SPIWrite 0040,44,0,7
SPIWrite 0040,44,0,7
SPIWrite 0041,55,0,7
SPIWrite 0041,55,0,7
SPIWrite 0042,00,0,7
SPIWrite 0042,00,0,7
SPIWrite 0043,11,0,7
SPIWrite 0043,11,0,7
```

\\END: Done configuring the Data Muxes

```
\\START: Configuring JESDTX Sync Mux

SPIWrite 0054,e4,0,7
SPIWrite 0054,d4,0,7
SPIWrite 0054,d8,0,7
SPIWrite 0054,d8,0,7

\\END: Done configuring JESDTX Sync Mux


\\START: Configuring JESDRX Sync Mux

SPIWrite 0061,00,0,7
SPIWrite 0061,00,0,7
SPIWrite 0061,00,0,7
SPIWrite 0061,00,0,7
SPIWrite 0055,e4,0,7
SPIWrite 0055,e0,0,7
SPIWrite 0055,e0,0,7
SPIWrite 0055,a0,0,7

\\END: Done configuring JESDRX Sync Mux


\\START: Setting FIFO and dither in JESD

SPIWrite 0032,10,0,7
SPIWrite 0035,10,0,7
SPIWrite 0030,10,0,7
SPIWrite 0031,10,0,7
SPIWrite 0033,10,0,7
SPIWrite 0034,10,0,7

\\END: Done Setting FIFO and dither in JESD

SPIWrite 0015,00,0,7    //PAGE: jesd_subchip=0x0;(Meaning: );   Address(0x15[3:3],)
\\ STEP: sigChainConfig/step1

\\START: Doing RX, TX and FB Digital Chain Config.

SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,01,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,31,0,7

\\Read  macro_opcode_operand=0x31000000;    Address(0x190[31:0],)


SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)
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```
\\Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0x20[4:4],)


\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0x20[5:5],)


\\Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0x20[6:6],)


\\Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0x20[7:7],)

SPIWrite 0013,00,5,5    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0193,45,0,7

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0016,40,6,7    //PAGE: fb_top=0x1;     Address(0x16[7:6],)
SPIWrite 015b,05,0,2    //FBAsyncFIFORdPtrVal=0x5;  Address(0x158[26:24],)
SPIWrite 0016,80,6,7    //PAGE: fb_top=0x2;     Address(0x16[7:6],)
SPIWrite 015b,05,0,2    //FBAsyncFIFORdPtrVal=0x5;  Address(0x158[26:24],)
SPIWrite 0016,00,6,7    //PAGE: fb_top=0x0;     Address(0x16[7:6],)
SPIWrite 0010,04,2,3    //PAGE: rx_top=0x1;     Address(0x10[3:2],)
SPIWrite 0120,03,0,2    //RxDecAsyncFIFORdPtrLoad=0x3;  Address(0x120[2:0],)
SPIWrite 0010,08,2,3    //PAGE: rx_top=0x2;     Address(0x10[3:2],)
SPIWrite 0120,03,0,2    //RxDecAsyncFIFORdPtrLoad=0x3;  Address(0x120[2:0],)
SPIWrite 0010,00,2,3    //PAGE: rx_top=0x0;     Address(0x10[3:2],)
SPIWrite 0010,01,0,1    //PAGE: tx_top=0x1;     Address(0x10[1:0],)
SPIWrite 010d,03,0,2    //RdPtrOffDigOutAsyncFIFO=0x3;  Address(0x10c[10:8],)
SPIWrite 0010,02,0,1    //PAGE: tx_top=0x2;     Address(0x10[1:0],)
SPIWrite 010d,03,0,2    //RdPtrOffDigOutAsyncFIFO=0x3;  Address(0x10c[10:8],)
SPIWrite 0010,01,0,1    //PAGE: tx_top=0x1;     Address(0x10[1:0],)
SPIWrite 010b,0d,0,3    //RdPtrOffDigInpAsyncFIFO=0xd;  Address(0x108[27:24],)
SPIWrite 0138,01,0,0    //BlockEnable=0x1;(Meaning: );  Address(0x138[0:0],)
SPIWrite 0139,01,0,1    //LutUpdateMode=0x1;(Meaning: );    Address(0x138[9:8],)
SPIWrite 0148,01,0,0    //BlockEnable=0x1;(Meaning: );  Address(0x148[0:0],)
SPIWrite 0149,01,0,1    //LutUpdateMode=0x1;(Meaning: );    Address(0x148[9:8],)
SPIWrite 0010,02,0,1    //PAGE: tx_top=0x2;     Address(0x10[1:0],)
SPIWrite 010b,0d,0,3    //RdPtrOffDigInpAsyncFIFO=0xd;  Address(0x108[27:24],)
SPIWrite 0138,01,0,0    //BlockEnable=0x1;(Meaning: );  Address(0x138[0:0],)
SPIWrite 0139,01,0,1    //LutUpdateMode=0x1;(Meaning: );    Address(0x138[9:8],)
SPIWrite 0148,01,0,0    //BlockEnable=0x1;(Meaning: );  Address(0x148[0:0],)
SPIWrite 0149,01,0,1    //LutUpdateMode=0x1;(Meaning: );    Address(0x148[9:8],)
SPIWrite 0010,00,0,1    //PAGE: tx_top=0x0;     Address(0x10[1:0],)
SPIWrite 0010,04,2,3    //PAGE: rx_top=0x1;     Address(0x10[3:2],)
SPIWrite 0af9,01,0,0    //pdn_in=0x1;(Meaning: );   Address(0xaf8[8:8],)
SPIWrite 0afb,01,0,0    //pdn_in=0x1;(Meaning: );   Address(0xaf8[24:24],)
SPIWrite 0a50,33,0,7    //gain_component_n=0x33;    Address(0xa50[7:0],)
SPIWrite 0a51,33,0,7    //gain_component_n=0x33;    Address(0xa50[15:8],)
SPIWrite 0a52,33,0,7    //gain_component_n=0x33;    Address(0xa50[23:16],)
SPIWrite 0a53,33,0,7    //gain_component_n=0x33;    Address(0xa50[31:24],)
SPIWrite 0a56,0e,0,0    //gain_corrector_bypass=0x0;(Meaning: );    Address(0xa54[16:16],)
SPIWrite 0a56,0c,1,1    //gain_corrector_bypass=0x0;(Meaning: );    Address(0xa54[17:17],)
SPIWrite 0a56,08,2,2    //gain_corrector_bypass=0x0;(Meaning: );    Address(0xa54[18:18],)
SPIWrite 0a56,00,3,3    //gain_corrector_bypass=0x0;(Meaning: );    Address(0xa54[19:19],)
SPIWrite 0a54,01,0,0    //rx1_unit_gain_mode=0x1;(Meaning: );   Address(0xa54[0:0],)
SPIWrite 0a54,03,1,1    //rx2_unit_gain_mode=0x1;(Meaning: );   Address(0xa54[1:1],)
SPIWrite 0c6b,00,0,0    //coef_update_signal=0x0;   Address(0xc68[24:24],)
SPIWrite 0c73,00,0,0    //coef_update_signal=0x0;   Address(0xc70[24:24],)
SPIWrite 0e6b,00,0,0    //coef_update_signal=0x0;   Address(0xe68[24:24],)
SPIWrite 0e73,00,0,0    //coef_update_signal=0x0;   Address(0xe70[24:24],)
SPIWrite 0c6b,01,0,0    //coef_update_signal=0x1;   Address(0xc68[24:24],)
SPIWrite 0c73,01,0,0    //coef_update_signal=0x1;   Address(0xc70[24:24],)
SPIWrite 0e6b,01,0,0    //coef_update_signal=0x1;   Address(0xe68[24:24],)
SPIWrite 0e73,01,0,0    //coef_update_signal=0x1;   Address(0xe70[24:24],)
SPIWrite 0c6b,00,0,0    //coef_update_signal=0x0;   Address(0xc68[24:24],)
SPIWrite 0c73,00,0,0    //coef_update_signal=0x0;   Address(0xc70[24:24],)
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SPIWrite 0e6b,00,0,0    //coef_update_signal=0x0;   Address(0xe68[24:24],)
SPIWrite 0e73,00,0,0    //coef_update_signal=0x0;   Address(0xe70[24:24],)
SPIWrite 0010,08,2,3    //PAGE: rx_top=0x2;     Address(0x10[3:2],)
SPIWrite 0af9,01,0,0    //pdn_in=0x1;(Meaning: );   Address(0xaf8[8:8],)
SPIWrite 0afb,01,0,0    //pdn_in=0x1;(Meaning: );   Address(0xaf8[24:24],)
SPIWrite 0a50,33,0,7    //gain_component_n=0x33;    Address(0xa50[7:0],)
SPIWrite 0a51,33,0,7    //gain_component_n=0x33;    Address(0xa50[15:8],)
SPIWrite 0a52,33,0,7    //gain_component_n=0x33;    Address(0xa50[23:16],)
SPIWrite 0a53,33,0,7    //gain_component_n=0x33;    Address(0xa50[31:24],)
SPIWrite 0a56,0e,0,0    //gain_corrector_bypass=0x0;(Meaning: );    Address(0xa54[16:16],)
SPIWrite 0a56,0c,1,1    //gain_corrector_bypass=0x0;(Meaning: );    Address(0xa54[17:17],)
SPIWrite 0a56,08,2,2    //gain_corrector_bypass=0x0;(Meaning: );    Address(0xa54[18:18],)
SPIWrite 0a56,00,3,3    //gain_corrector_bypass=0x0;(Meaning: );    Address(0xa54[19:19],)
SPIWrite 0a54,01,0,0    //rx1_unit_gain_mode=0x1;(Meaning: );   Address(0xa54[0:0],)
SPIWrite 0a54,03,1,1    //rx2_unit_gain_mode=0x1;(Meaning: );   Address(0xa54[1:1],)
SPIWrite 0c6b,00,0,0    //coef_update_signal=0x0;   Address(0xc68[24:24],)
SPIWrite 0c73,00,0,0    //coef_update_signal=0x0;   Address(0xc70[24:24],)
SPIWrite 0e6b,00,0,0    //coef_update_signal=0x0;   Address(0xe68[24:24],)
SPIWrite 0e73,00,0,0    //coef_update_signal=0x0;   Address(0xe70[24:24],)
SPIWrite 0c6b,01,0,0    //coef_update_signal=0x1;   Address(0xc68[24:24],)
SPIWrite 0c73,01,0,0    //coef_update_signal=0x1;   Address(0xc70[24:24],)
SPIWrite 0e6b,01,0,0    //coef_update_signal=0x1;   Address(0xe68[24:24],)
SPIWrite 0e73,01,0,0    //coef_update_signal=0x1;   Address(0xe70[24:24],)
SPIWrite 0c6b,00,0,0    //coef_update_signal=0x0;   Address(0xc68[24:24],)
SPIWrite 0c73,00,0,0    //coef_update_signal=0x0;   Address(0xc70[24:24],)
SPIWrite 0e6b,00,0,0    //coef_update_signal=0x0;   Address(0xe68[24:24],)
SPIWrite 0e73,00,0,0    //coef_update_signal=0x0;   Address(0xe70[24:24],)

\\END: Completed RX, TX and FB Digital Chain Config.

SPIWrite 0010,00,0,7    //PAGE: rx_top=0x0;     Address(0x10[3:2],)
\\ STEP: sigChainConfig/step2
SPIWrite 0013,10,0,7    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,1e,0,7
SPIWrite 00a1,05,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,2d,0,7

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,0,7    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0013,20,0,7    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)

SPIWrite 0013,00,0,7    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
\\ STEP: OvTDDpin/step0

\\START: Doing Internal TDD settings

SPIWrite 0014,04,0,7    //PAGE: TIMING_CON=0x1;(Meaning: );     Address(0x14[2:2],)
SPIWrite 04e7,00,0,7    //enable_multi_sysref=0x0;  Address(0x4e4[24:24],)
SPIWrite 04c4,01,0,7    //mode_2t2r=0x1;    Address(0x4c4[0:0],)
SPIWrite 04c5,00,0,7    //fdd_mode=0x0;     Address(0x4c4[8:8],)
SPIWrite 0206,06,0,7    //force_tg_txAB=0x0;    Address(0x204[16:16],)
SPIWrite 0206,04,0,7    //force_tg_rxAB=0x0;    Address(0x204[17:17],)
SPIWrite 0206,00,0,7    //force_tg_fbAB=0x0;    Address(0x204[18:18],)
SPIWrite 036a,06,0,7    //force_tg_txCD=0x0;    Address(0x368[16:16],)
SPIWrite 036a,04,0,7    //force_tg_rxCD=0x0;    Address(0x368[17:17],)
SPIWrite 036a,00,0,7    //force_tg_fbCD=0x0;    Address(0x368[18:18],)
SPIWrite 04dc,80,0,7    //force_pll_txAB=0x0;   Address(0x4dc[6:6],)
SPIWrite 04dd,0d,0,7    //force_pll_txCD=0x0;   Address(0x4dc[9:9],)
SPIWrite 04dc,00,0,7    //force_pll_rxAB=0x0;   Address(0x4dc[7:7],)
SPIWrite 04dd,09,0,7    //force_pll_rxCD=0x0;   Address(0x4dc[10:10],)
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SPIWrite 04dd,08,0,7    //force_pll_fbAB=0x0;   Address(0x4dc[8:8],)
SPIWrite 04dd,00,0,7    //force_pll_fbCD=0x0;   Address(0x4dc[11:11],)
SPIWrite 0110,00,0,7    //fb_vswr_pin_valid_cha=0x0;    Address(0x110[0:0],)
SPIWrite 0111,00,0,7    //fb_vswr_pin_valid_chc=0x0;    Address(0x110[8:8],)
SPIWrite 0118,00,0,7    //use_reg_for_tx_gswap_rxtxlo=0x0;  Address(0x118[0:0],)
SPIWrite 011c,01,0,7    //use_reg_for_txdsalatch=0x1;   Address(0x11c[0:0],)
SPIWrite 0121,00,0,7    //en_reg_for_gswap=0x0;     Address(0x120[8:8],)
SPIWrite 0106,0f,0,7    //chsel_gswap=0xf;  Address(0x104[19:16],)
SPIWrite 0114,00,0,7    //fb_ncosel_pin_valid_cha=0x0;  Address(0x114[0:0],)
SPIWrite 0115,00,0,7    //fb_ncosel_pin_valid_chc=0x0;  Address(0x114[8:8],)
SPIWrite 071f,90,0,7    //override_val_fbmuxsel=0x24;   Address(0x71c[31:26],)
SPIWrite 071f,93,0,7    //override_fb_muxsel=0x3;   Address(0x71c[25:24],)
SPIWrite 04c6,01,0,7    //dc_pll_sync_mode=0x1;     Address(0x4c4[16:16],)
SPIWrite 0526,00,0,7    //en_ovr_for_cond_freeze=0x0;   Address(0x524[16:16],)
SPIWrite 0621,01,0,7    //config_rise_rxjesdon_chab=0x177;  Address(0x620[15:0],)
SPIWrite 0620,77,0,7
SPIWrite 0661,01,0,7    //config_rise_rxjesdon_chcd=0x177;  Address(0x660[15:0],)
SPIWrite 0660,77,0,7
SPIWrite 0014,00,0,7    //PAGE: TIMING_CON=0x0;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0014,01,0,7    //PAGE: clktop_2t=0x1;  Address(0x14[1:0],)
SPIWrite 005c,10,0,7    //CTL_SEL_CM_BIAS_R_SHRT_RXCML_1P8=0x1;     Address(0x5c[4:4],)
SPIWrite 005c,18,0,7    //CTL_FORCE_LDO_FILT_RXCML_1P8=0x1;     Address(0x5c[3:3],)
SPIWrite 005c,1c,0,7    //CTL_FORCE_CASCODEFILT_RXCML_1P8=0x1;  Address(0x5c[2:2],)
SPIWrite 005c,1e,0,7    //CTL_FORCE_BIASFILT_RXCML_1P8=0x1;     Address(0x5c[1:1],)

\\END: Completed Internal TDD settings

SPIWrite 0014,00,0,7    //PAGE: clktop_2t=0x0;  Address(0x14[1:0],)
\\ STEP: OvTDDpin/step1

\\START: Overriding TDD Pins internally

SPIWrite 0014,04,0,7    //PAGE: TIMING_CON=0x1;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0124,01,0,7    //use_reg_txon_AB=0x1;  Address(0x124[0:0],)
SPIWrite 0126,01,0,7    //use_reg_rxon_AB=0x1;  Address(0x124[16:16],)
SPIWrite 0128,01,0,7    //use_reg_fbon_AB=0x1;  Address(0x128[0:0],)
SPIWrite 012a,01,0,7    //use_reg_txon_CD=0x1;  Address(0x128[16:16],)
SPIWrite 012c,01,0,7    //use_reg_rxon_CD=0x1;  Address(0x12c[0:0],)
SPIWrite 012e,01,0,7    //use_reg_fbon_CD=0x1;  Address(0x12c[16:16],)
SPIWrite 0125,00,0,7    //reg_for_txon_AB=0x0;  Address(0x124[8:8],)
SPIWrite 0127,00,0,7    //reg_for_rxon_AB=0x0;  Address(0x124[24:24],)
SPIWrite 0129,00,0,7    //reg_for_fbon_AB=0x0;  Address(0x128[8:8],)
SPIWrite 012b,00,0,7    //reg_for_txon_CD=0x0;  Address(0x128[24:24],)
SPIWrite 012d,00,0,7    //reg_for_rxon_CD=0x0;  Address(0x12c[8:8],)
SPIWrite 012f,00,0,7    //reg_for_fbon_CD=0x0;  Address(0x12c[24:24],)

\\END: Done overriding TDD Pins internally

SPIWrite 0014,00,0,7    //PAGE: TIMING_CON=0x0;(Meaning: );     Address(0x14[2:2],)
\\ STEP: OvTDDpin/step2

\\START: Overriding TDD Pins internally

SPIWrite 0014,04,0,7    //PAGE: TIMING_CON=0x1;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0124,01,0,7    //use_reg_txon_AB=0x1;  Address(0x124[0:0],)
SPIWrite 0126,01,0,7    //use_reg_rxon_AB=0x1;  Address(0x124[16:16],)
SPIWrite 0128,01,0,7    //use_reg_fbon_AB=0x1;  Address(0x128[0:0],)
SPIWrite 012a,01,0,7    //use_reg_txon_CD=0x1;  Address(0x128[16:16],)
SPIWrite 012c,01,0,7    //use_reg_rxon_CD=0x1;  Address(0x12c[0:0],)
SPIWrite 012e,01,0,7    //use_reg_fbon_CD=0x1;  Address(0x12c[16:16],)
SPIWrite 0125,01,0,7    //reg_for_txon_AB=0x1;  Address(0x124[8:8],)
SPIWrite 0127,00,0,7    //reg_for_rxon_AB=0x0;  Address(0x124[24:24],)
SPIWrite 0129,00,0,7    //reg_for_fbon_AB=0x0;  Address(0x128[8:8],)
SPIWrite 012b,01,0,7    //reg_for_txon_CD=0x1;  Address(0x128[24:24],)
SPIWrite 012d,00,0,7    //reg_for_rxon_CD=0x0;  Address(0x12c[8:8],)
SPIWrite 012f,00,0,7    //reg_for_fbon_CD=0x0;  Address(0x12c[24:24],)

\\END: Done overriding TDD Pins internally
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SPIWrite 0014,00,0,7    //PAGE: TIMING_CON=0x0;(Meaning: );     Address(0x14[2:2],)
\\ STEP: analogWrite/step0

\\START: Doing DAC Analog Writes

SPIWrite 0017,0f,0,3    //PAGE: dac_1t=0xf;     Address(0x17[3:0],)
SPIWrite 00bc,55,0,2
SPIWrite 00bc,55,3,6
SPIWrite 00bd,aa,0,3
SPIWrite 00bd,aa,4,7
SPIWrite 00be,14,0,4
SPIWrite 00bf,19,0,4
SPIWrite 00c0,19,0,4
SPIWrite 0052,b4,2,4
SPIWrite 0052,b4,5,7
SPIWrite 0054,0a,0,3
SPIWrite 0055,14,0,4
SPIWrite 0056,19,0,4
SPIWrite 0057,19,0,4
SPIWrite 0040,18,3,3
SPIWrite 0040,18,4,4
SPIWrite 003f,00,0,7
SPIWrite 003e,00,0,7
SPIWrite 003d,00,0,7
SPIWrite 003c,03,0,7
SPIWrite 007b,03,0,7
SPIWrite 007a,ff,0,7
SPIWrite 007e,03,0,7
SPIWrite 007d,ff,0,7
SPIWrite 0081,03,0,7
SPIWrite 0080,ff,0,7
SPIWrite 0085,03,0,7
SPIWrite 0084,ff,0,7
SPIWrite 0089,00,0,7
SPIWrite 0088,03,0,7
SPIWrite 008d,00,0,7
SPIWrite 008c,03,0,7
SPIWrite 0091,01,0,7
SPIWrite 0090,ff,0,7
SPIWrite 0095,00,0,7
SPIWrite 0094,1f,0,7
SPIWrite 00c1,1e,0,7
SPIWrite 00c2,32,0,7
SPIWrite 006e,aa,0,3
SPIWrite 006e,aa,4,7
SPIWrite 0041,28,2,5
SPIWrite 0042,aa,0,3
SPIWrite 0042,aa,4,7
SPIWrite 0043,aa,0,3
SPIWrite 0043,aa,4,7
SPIWrite 0044,0a,0,3
SPIWrite 006f,aa,0,3
SPIWrite 0045,03,0,7
SPIWrite 0046,03,0,7
SPIWrite 0062,88,0,3
SPIWrite 0062,88,4,7
SPIWrite 0063,88,0,3
SPIWrite 0063,88,4,7
SPIWrite 0065,40,0,7
SPIWrite 0066,40,0,7
SPIWrite 0067,40,0,7
SPIWrite 0068,40,0,7
SPIWrite 0069,40,0,7
SPIWrite 006a,40,0,7
SPIWrite 006b,40,0,7
SPIWrite 006c,40,0,7
SPIWrite 0064,44,0,3
SPIWrite 0064,44,4,7
SPIWrite 00c8,55,0,3
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SPIWrite 00c8,55,4,7
SPIWrite 00c9,82,0,3
SPIWrite 00c9,22,4,7
SPIWrite 00d5,e4,0,7
SPIWrite 00d8,e4,0,7
SPIWrite 00d9,a0,0,7
SPIWrite 00da,a0,0,7
SPIWrite 00af,92,0,7
SPIWrite 00ad,0f,0,3
SPIWrite 00b0,1f,0,7
SPIWrite 00a7,ff,0,7
SPIWrite 00a6,ff,0,7
SPIWrite 00a5,ff,0,7
SPIWrite 00a4,ff,0,7
SPIWrite 00a8,ff,0,7
SPIWrite 00ae,06,0,3
SPIWrite 00cb,ff,0,7
SPIWrite 00cc,ff,0,7
SPIWrite 00d5,b8,0,7
SPIWrite 00d8,b8,0,7
SPIWrite 006f,aa,0,3
SPIWrite 006f,aa,4,7
SPIWrite 006d,06,1,3
SPIWrite 006d,46,4,6
SPIWrite 0047,03,0,7
SPIWrite 009c,02,1,1
SPIWrite 009f,78,0,7
SPIWrite 009e,00,0,7
SPIWrite 0017,00,0,3    //PAGE: dac_1t=0x0;     Address(0x17[3:0],)
SPIWrite 0010,03,0,7    //PAGE: tx_top=0x3;     Address(0x10[1:0],)
SPIWrite 0830,00,0,7    //IndepCorrByp=0x0;(Meaning: );     Address(0x830[0:0],)
SPIWrite 0830,02,0,7    //IndepCorrEn=0x1;(Meaning: );  Address(0x830[1:1],)
SPIWrite 0890,00,0,7    //IndepCorrByp=0x0;(Meaning: );     Address(0x890[0:0],)
SPIWrite 0890,02,0,7    //IndepCorrEn=0x1;(Meaning: );  Address(0x890[1:1],)
SPIWrite 0650,02,0,7    //txIQMCLFSREn=0x1;(Meaning: );     Address(0x650[1:1],)
SPIWrite 06e4,02,0,7    //txIQMCLFSREn=0x1;(Meaning: );     Address(0x6e4[1:1],)
SPIWrite 0831,28,0,7    //dsaMinIndex=0x28;     Address(0x830[13:8],)
SPIWrite 0891,28,0,7    //dsaMinIndex=0x28;     Address(0x890[13:8],)
SPIWrite 0832,01,0,7    //IndepCorrUpdt=0x1;    Address(0x830[16:16],)
SPIWrite 0892,01,0,7    //IndepCorrUpdt=0x1;    Address(0x890[16:16],)
SPIWrite 0833,00,0,7    //CoeffScaling=0x0;(Meaning: );     Address(0x830[24:24],)
SPIWrite 0893,00,0,7    //CoeffScaling=0x0;(Meaning: );     Address(0x890[24:24],)
SPIWrite 0832,00,0,7    //IndepCorrUpdt=0x0;    Address(0x830[16:16],)
SPIWrite 0892,00,0,7    //IndepCorrUpdt=0x0;    Address(0x890[16:16],)
SPIWrite 0010,00,0,7    //PAGE: tx_top=0x0;     Address(0x10[1:0],)

\\END: Completed DAC Analog Writes

\\ STEP: analogWrite/step1

\\START: Overriding TDD Pins internally

SPIWrite 0014,04,0,7    //PAGE: TIMING_CON=0x1;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0124,01,0,7    //use_reg_txon_AB=0x1;  Address(0x124[0:0],)
SPIWrite 0126,01,0,7    //use_reg_rxon_AB=0x1;  Address(0x124[16:16],)
SPIWrite 0128,01,0,7    //use_reg_fbon_AB=0x1;  Address(0x128[0:0],)
SPIWrite 012a,01,0,7    //use_reg_txon_CD=0x1;  Address(0x128[16:16],)
SPIWrite 012c,01,0,7    //use_reg_rxon_CD=0x1;  Address(0x12c[0:0],)
SPIWrite 012e,01,0,7    //use_reg_fbon_CD=0x1;  Address(0x12c[16:16],)
SPIWrite 0125,00,0,7    //reg_for_txon_AB=0x0;  Address(0x124[8:8],)
SPIWrite 0127,01,0,7    //reg_for_rxon_AB=0x1;  Address(0x124[24:24],)
SPIWrite 0129,00,0,7    //reg_for_fbon_AB=0x0;  Address(0x128[8:8],)
SPIWrite 012b,00,0,7    //reg_for_txon_CD=0x0;  Address(0x128[24:24],)
SPIWrite 012d,01,0,7    //reg_for_rxon_CD=0x1;  Address(0x12c[8:8],)
SPIWrite 012f,00,0,7    //reg_for_fbon_CD=0x0;  Address(0x12c[24:24],)

\\END: Done overriding TDD Pins internally
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\\START: Doing RX ADC Analog Writes

SPIWrite 0014,00,2,2    //PAGE: TIMING_CON=0x0;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0011,01,0,3    //PAGE: rx_ec_i=0x1;    Address(0x11[3:0],)
SPIWrite 04a0,0c,0,0
SPIWrite 0011,00,0,3    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,10,4,7    //PAGE: rx_ec_q=0x1;    Address(0x11[7:4],)
SPIWrite 04a0,0c,0,0
SPIWrite 0011,00,4,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,02,0,3    //PAGE: rx_ec_i=0x2;    Address(0x11[3:0],)
SPIWrite 04a0,0c,0,0
SPIWrite 0011,00,0,3    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,20,4,7    //PAGE: rx_ec_q=0x2;    Address(0x11[7:4],)
SPIWrite 04a0,0c,0,0
SPIWrite 0011,00,4,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,04,0,3    //PAGE: rx_ec_i=0x4;    Address(0x11[3:0],)
SPIWrite 04a0,0c,0,0
SPIWrite 0011,00,0,3    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,40,4,7    //PAGE: rx_ec_q=0x4;    Address(0x11[7:4],)
SPIWrite 04a0,0c,0,0
SPIWrite 0011,00,4,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,08,0,3    //PAGE: rx_ec_i=0x8;    Address(0x11[3:0],)
SPIWrite 04a0,0c,0,0
SPIWrite 0011,00,0,3    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,80,4,7    //PAGE: rx_ec_q=0x8;    Address(0x11[7:4],)
SPIWrite 04a0,0c,0,0
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,0f,0,7    //PAGE: rx_ec_i=0xf;    Address(0x11[3:0],)
SPIWrite 0011,ff,0,7
SPIWrite 029d,03,0,7
SPIWrite 029d,1b,0,7
SPIWrite 029e,00,0,7
SPIWrite 029d,db,0,7
SPIWrite 0299,03,0,7
SPIWrite 029e,30,0,7
SPIWrite 029f,0c,0,7
SPIWrite 029f,6c,0,7
SPIWrite 02a0,03,0,7
SPIWrite 029e,30,0,7
SPIWrite 029f,6d,0,7
SPIWrite 02a0,13,0,7
SPIWrite 0284,00,0,7
SPIWrite 0281,00,0,7
SPIWrite 0284,40,0,7
SPIWrite 0338,2b,0,7
SPIWrite 0111,09,0,7
SPIWrite 0011,00,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)

\\START: Doing RX IMD vs DSA improvement Analog Writes

SPIWrite 0011,0f,0,7    //PAGE: rx_ec_i=0xf;    Address(0x11[3:0],)
SPIWrite 0011,0f,0,7
SPIWrite 0b33,00,0,7
SPIWrite 0b32,00,0,7
SPIWrite 0b33,08,0,7
SPIWrite 0c91,20,0,7
SPIWrite 0011,00,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)

\\END: Completed RX IMD vs DSA improvement Analog Writes

SPIWrite 0011,0f,0,7    //PAGE: rx_ec_i=0xf;    Address(0x11[3:0],)
SPIWrite 0500,03,0,7
SPIWrite 0500,03,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,f0,0,7    //PAGE: rx_ec_q=0xf;    Address(0x11[7:4],)
SPIWrite 0500,03,0,7
SPIWrite 0500,03,0,7
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SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,0f,0,7    //PAGE: rx_ec_i=0xf;    Address(0x11[3:0],)
SPIWrite 0500,03,0,7
SPIWrite 0500,03,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,f0,0,7    //PAGE: rx_ec_q=0xf;    Address(0x11[7:4],)
SPIWrite 0500,03,0,7
SPIWrite 0500,03,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,0f,0,7    //PAGE: rx_ec_i=0xf;    Address(0x11[3:0],)
SPIWrite 0c70,08,0,7
SPIWrite 0c70,18,0,7
SPIWrite 0103,80,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,10,0,7    //PAGE: rx_ec_q=0x1;    Address(0x11[7:4],)
SPIWrite 0c74,02,0,7
SPIWrite 0103,80,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,01,0,7    //PAGE: rx_ec_i=0x1;    Address(0x11[3:0],)
SPIWrite 049f,00,0,7
SPIWrite 049e,00,0,7
SPIWrite 049f,04,0,7
SPIWrite 049e,01,0,7
SPIWrite 049d,00,0,7
SPIWrite 049c,01,0,7
SPIWrite 049c,00,0,7
SPIWrite 049d,00,0,7
SPIWrite 04a2,00,0,7
SPIWrite 04a2,01,0,7
SPIWrite 04a2,00,0,7
SPIWrite 049c,01,0,7

WAIT 0.01

SPIWrite 049c,00,0,7

WAIT 0.05

SPIWrite 049d,02,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,10,0,7    //PAGE: rx_ec_q=0x1;    Address(0x11[7:4],)
SPIWrite 049f,00,0,7
SPIWrite 049e,00,0,7
SPIWrite 049f,04,0,7
SPIWrite 049e,01,0,7
SPIWrite 049d,00,0,7
SPIWrite 049c,01,0,7
SPIWrite 049c,00,0,7
SPIWrite 049d,00,0,7
SPIWrite 04a2,00,0,7
SPIWrite 04a2,01,0,7
SPIWrite 04a2,00,0,7
SPIWrite 049c,01,0,7

WAIT 0.01

SPIWrite 049c,00,0,7

WAIT 0.05

SPIWrite 049d,02,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,02,0,7    //PAGE: rx_ec_i=0x2;    Address(0x11[3:0],)
SPIWrite 049f,00,0,7
SPIWrite 049e,00,0,7
SPIWrite 049f,04,0,7
SPIWrite 049e,01,0,7
SPIWrite 049d,00,0,7
SPIWrite 049c,01,0,7
```

```
SPIWrite 049c,00,0,7
SPIWrite 049d,00,0,7
SPIWrite 04a2,00,0,7
SPIWrite 04a2,01,0,7
SPIWrite 04a2,00,0,7
SPIWrite 049c,01,0,7

WAIT 0.01

SPIWrite 049c,00,0,7

WAIT 0.05

SPIWrite 049d,02,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,20,0,7    //PAGE: rx_ec_q=0x2;    Address(0x11[7:4],)
SPIWrite 049f,00,0,7
SPIWrite 049e,00,0,7
SPIWrite 049f,04,0,7
SPIWrite 049e,01,0,7
SPIWrite 049d,00,0,7
SPIWrite 049c,01,0,7
SPIWrite 049c,00,0,7
SPIWrite 049d,00,0,7
SPIWrite 04a2,00,0,7
SPIWrite 04a2,01,0,7
SPIWrite 04a2,00,0,7
SPIWrite 049c,01,0,7

WAIT 0.01

SPIWrite 049c,00,0,7

WAIT 0.05

SPIWrite 049d,02,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,04,0,7    //PAGE: rx_ec_i=0x4;    Address(0x11[3:0],)
SPIWrite 049f,00,0,7
SPIWrite 049e,00,0,7
SPIWrite 049f,04,0,7
SPIWrite 049e,01,0,7
SPIWrite 049d,00,0,7
SPIWrite 049c,01,0,7
SPIWrite 049c,00,0,7
SPIWrite 049d,00,0,7
SPIWrite 04a2,00,0,7
SPIWrite 04a2,01,0,7
SPIWrite 04a2,00,0,7
SPIWrite 049c,01,0,7

WAIT 0.01

SPIWrite 049c,00,0,7

WAIT 0.05

SPIWrite 049d,02,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,40,0,7    //PAGE: rx_ec_q=0x4;    Address(0x11[7:4],)
SPIWrite 049f,00,0,7
SPIWrite 049e,00,0,7
SPIWrite 049f,04,0,7
SPIWrite 049e,01,0,7
SPIWrite 049d,00,0,7
SPIWrite 049c,01,0,7
SPIWrite 049c,00,0,7
SPIWrite 049d,00,0,7
SPIWrite 04a2,00,0,7
```

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SPIWrite 04a2,01,0,7
SPIWrite 04a2,00,0,7
SPIWrite 049c,01,0,7

WAIT 0.01

SPIWrite 049c,00,0,7

WAIT 0.05

SPIWrite 049d,02,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,08,0,7    //PAGE: rx_ec_i=0x8;    Address(0x11[3:0],)
SPIWrite 049f,00,0,7
SPIWrite 049e,00,0,7
SPIWrite 049f,04,0,7
SPIWrite 049e,01,0,7
SPIWrite 049d,00,0,7
SPIWrite 049c,01,0,7
SPIWrite 049c,00,0,7
SPIWrite 049d,00,0,7
SPIWrite 04a2,00,0,7
SPIWrite 04a2,01,0,7
SPIWrite 04a2,00,0,7
SPIWrite 049c,01,0,7

WAIT 0.01

SPIWrite 049c,00,0,7

WAIT 0.05

SPIWrite 049d,02,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,80,0,7    //PAGE: rx_ec_q=0x8;    Address(0x11[7:4],)
SPIWrite 049f,00,0,7
SPIWrite 049e,00,0,7
SPIWrite 049f,04,0,7
SPIWrite 049e,01,0,7
SPIWrite 049d,00,0,7
SPIWrite 049c,01,0,7
SPIWrite 049c,00,0,7
SPIWrite 049d,00,0,7
SPIWrite 04a2,00,0,7
SPIWrite 04a2,01,0,7
SPIWrite 04a2,00,0,7
SPIWrite 049c,01,0,7

WAIT 0.01

SPIWrite 049c,00,0,7

WAIT 0.05

SPIWrite 049d,02,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,0f,0,7    //PAGE: rx_ec_i=0xf;    Address(0x11[3:0],)
SPIWrite 0500,02,0,7
SPIWrite 0500,00,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,f0,0,7    //PAGE: rx_ec_q=0xf;    Address(0x11[7:4],)
SPIWrite 0500,02,0,7
SPIWrite 0500,00,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,0f,0,7    //PAGE: rx_ec_i=0xf;    Address(0x11[3:0],)
SPIWrite 0500,00,0,7
SPIWrite 0500,00,0,7
SPIWrite 050a,01,0,7
SPIWrite 0502,01,0,7
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```
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,f0,0,7    //PAGE: rx_ec_q=0xf;    Address(0x11[7:4],)
SPIWrite 0500,00,0,7
SPIWrite 0500,00,0,7
SPIWrite 050a,01,0,7
SPIWrite 0502,01,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,0f,0,7    //PAGE: rx_ec_i=0xf;    Address(0x11[3:0],)
SPIWrite 0c70,10,0,7
SPIWrite 0c70,00,0,7
SPIWrite 0103,00,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,10,0,7    //PAGE: rx_ec_q=0x1;    Address(0x11[7:4],)
SPIWrite 0c74,00,0,7
SPIWrite 0103,00,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,01,0,7    //PAGE: rx_ec_i=0x1;    Address(0x11[3:0],)
SPIWrite 0103,00,0,7
SPIWrite 01a1,00,0,7
SPIWrite 0112,00,0,7
SPIWrite 0bf3,00,0,7
SPIWrite 0101,00,0,7
SPIWrite 0100,00,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,10,0,7    //PAGE: rx_ec_q=0x1;    Address(0x11[7:4],)
SPIWrite 0103,00,0,7
SPIWrite 01a1,00,0,7
SPIWrite 0112,00,0,7
SPIWrite 0101,00,0,7
SPIWrite 0100,00,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,02,0,7    //PAGE: rx_ec_i=0x2;    Address(0x11[3:0],)
SPIWrite 0103,00,0,7
SPIWrite 01a1,00,0,7
SPIWrite 0112,00,0,7
SPIWrite 0bf3,00,0,7
SPIWrite 0101,00,0,7
SPIWrite 0100,00,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,20,0,7    //PAGE: rx_ec_q=0x2;    Address(0x11[7:4],)
SPIWrite 0103,00,0,7
SPIWrite 01a1,00,0,7
SPIWrite 0112,00,0,7
SPIWrite 0101,00,0,7
SPIWrite 0100,00,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0010,04,0,7    //PAGE: rx_top=0x1;     Address(0x10[3:2],)
SPIWrite 0c10,05,0,7    //nl_corr_complete_byp=0x1;(Meaning: );     Address(0xc10[0:0],)
SPIWrite 0c11,01,0,7    //coef_update_pulse_nl=0x1;     Address(0xc10[8:8],)

WAIT 0.1

SPIWrite 0c11,00,0,7    //coef_update_pulse_nl=0x0;     Address(0xc10[8:8],)
SPIWrite 0e10,05,0,7    //nl_corr_complete_byp=0x1;(Meaning: );     Address(0xe10[0:0],)
SPIWrite 0e11,01,0,7    //coef_update_pulse_nl=0x1;     Address(0xe10[8:8],)

WAIT 0.1

SPIWrite 0e11,00,0,7    //coef_update_pulse_nl=0x0;     Address(0xe10[8:8],)
SPIWrite 0010,00,0,7    //PAGE: rx_top=0x0;     Address(0x10[3:2],)
SPIWrite 0011,04,0,7    //PAGE: rx_ec_i=0x4;    Address(0x11[3:0],)
SPIWrite 0103,00,0,7
SPIWrite 01a1,00,0,7
SPIWrite 0112,00,0,7
SPIWrite 0bf3,00,0,7
SPIWrite 0101,00,0,7
SPIWrite 0100,00,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,40,0,7    //PAGE: rx_ec_q=0x4;    Address(0x11[7:4],)
```

```
SPIWrite 0103,00,0,7
SPIWrite 01a1,00,0,7
SPIWrite 0112,00,0,7
SPIWrite 0101,00,0,7
SPIWrite 0100,00,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,08,0,7    //PAGE: rx_ec_i=0x8;    Address(0x11[3:0],)
SPIWrite 0103,00,0,7
SPIWrite 01a1,00,0,7
SPIWrite 0112,00,0,7
SPIWrite 0bf3,00,0,7
SPIWrite 0101,00,0,7
SPIWrite 0100,00,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,80,0,7    //PAGE: rx_ec_q=0x8;    Address(0x11[7:4],)
SPIWrite 0103,00,0,7
SPIWrite 01a1,00,0,7
SPIWrite 0112,00,0,7
SPIWrite 0101,00,0,7
SPIWrite 0100,00,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0010,08,0,7    //PAGE: rx_top=0x2;     Address(0x10[3:2],)
SPIWrite 0c10,05,0,7    //nl_corr_complete_byp=0x1;(Meaning: );     Address(0xc10[0:0],)
SPIWrite 0c11,01,0,7    //coef_update_pulse_nl=0x1;     Address(0xc10[8:8],)

WAIT 0.1

SPIWrite 0c11,00,0,7    //coef_update_pulse_nl=0x0;     Address(0xc10[8:8],)
SPIWrite 0e10,05,0,7    //nl_corr_complete_byp=0x1;(Meaning: );     Address(0xe10[0:0],)
SPIWrite 0e11,01,0,7    //coef_update_pulse_nl=0x1;     Address(0xe10[8:8],)

WAIT 0.1

SPIWrite 0e11,00,0,7    //coef_update_pulse_nl=0x0;     Address(0xe10[8:8],)
SPIWrite 0010,00,0,7    //PAGE: rx_top=0x0;     Address(0x10[3:2],)
SPIWrite 0012,0f,0,7    //PAGE: rx_ec_common=0xf;   Address(0x12[3:0],)
SPIWrite 04c4,20,0,7
SPIWrite 0012,00,0,7    //PAGE: rx_ec_common=0x0;   Address(0x12[3:0],)
SPIWrite 0014,01,0,7    //PAGE: clktop_2t=0x1;  Address(0x14[1:0],)
SPIWrite 006b,10,0,7    //MASK_PDN_SYNC_RXCML_R=0x1;    Address(0x68[28:28],)
SPIWrite 006b,18,0,7    //MASK_PDN_SYNC_RXCML_L=0x1;    Address(0x68[27:27],)
SPIWrite 0014,00,0,7    //PAGE: clktop_2t=0x0;  Address(0x14[1:0],)
SPIWrite 0011,f0,0,7    //PAGE: rx_ec_q=0xf;    Address(0x11[7:4],)
SPIWrite 0293,00,0,7
SPIWrite 0b93,ec,0,7
SPIWrite 0b85,8d,0,7
SPIWrite 0b93,ec,0,7
SPIWrite 0b92,65,0,7
SPIWrite 0b91,cd,0,7
SPIWrite 0b95,1c,0,7
SPIWrite 0b94,e0,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0016,10,0,7    //PAGE: dsa=0x1;    Address(0x16[5:4],)
SPIWrite 0180,00,0,7
SPIWrite 0016,20,0,7    //PAGE: dsa=0x2;    Address(0x16[5:4],)
SPIWrite 0180,00,0,7

\\END: Completed RX ADC Analog Writes

SPIWrite 0016,00,0,7    //PAGE: dsa=0x0;    Address(0x16[5:4],)
\\ STEP: analogWrite/step2

\\START: Overriding TDD Pins internally

SPIWrite 0014,04,0,7    //PAGE: TIMING_CON=0x1;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0124,01,0,7    //use_reg_txon_AB=0x1;  Address(0x124[0:0],)
SPIWrite 0126,01,0,7    //use_reg_rxon_AB=0x1;  Address(0x124[16:16],)
SPIWrite 0128,01,0,7    //use_reg_fbon_AB=0x1;  Address(0x128[0:0],)
SPIWrite 012a,01,0,7    //use_reg_txon_CD=0x1;  Address(0x128[16:16],)
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SPIWrite 012c,01,0,7    //use_reg_rxon_CD=0x1;  Address(0x12c[0:0],)
SPIWrite 012e,01,0,7    //use_reg_fbon_CD=0x1;  Address(0x12c[16:16],)
SPIWrite 0125,00,0,7    //reg_for_txon_AB=0x0;  Address(0x124[8:8],)
SPIWrite 0127,00,0,7    //reg_for_rxon_AB=0x0;  Address(0x124[24:24],)
SPIWrite 0129,01,0,7    //reg_for_fbon_AB=0x1;  Address(0x128[8:8],)
SPIWrite 012b,00,0,7    //reg_for_txon_CD=0x0;  Address(0x128[24:24],)
SPIWrite 012d,00,0,7    //reg_for_rxon_CD=0x0;  Address(0x12c[8:8],)
SPIWrite 012f,01,0,7    //reg_for_fbon_CD=0x1;  Address(0x12c[24:24],)

\\END: Done overriding TDD Pins internally


\\START: Doing FB ADC Analog Writes

SPIWrite 0014,00,2,2    //PAGE: TIMING_CON=0x0;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0010,10,4,4    //PAGE: fb_ec=0x1;  Address(0x10[4:4],0x10[6:6],)
SPIWrite 0010,10,6,6
SPIWrite 00b0,03,1,1
SPIWrite 0188,09,3,3
SPIWrite 0140,28,3,3
SPIWrite 0138,28,3,3
SPIWrite 0190,09,3,3
SPIWrite 0168,39,3,3
SPIWrite 0160,39,3,3
SPIWrite 0119,32,0,3
SPIWrite 0121,32,0,3
SPIWrite 0129,32,0,3
SPIWrite 0131,32,0,3
SPIWrite 0119,32,0,3
SPIWrite 0121,32,0,3
SPIWrite 0129,32,0,3
SPIWrite 0131,32,0,3
SPIWrite 0010,00,4,4    //PAGE: fb_ec=0x0;  Address(0x10[4:4],0x10[6:6],)
SPIWrite 0010,00,6,6
SPIWrite 0010,20,5,5    //PAGE: fb_ana=0x1;     Address(0x10[5:5],0x10[7:7],)
SPIWrite 0010,20,7,7
SPIWrite 0085,08,2,4
SPIWrite 0102,08,3,3
SPIWrite 0010,00,5,5    //PAGE: fb_ana=0x0;     Address(0x10[5:5],0x10[7:7],)
SPIWrite 0010,00,7,7
SPIWrite 0010,00,4,4    //PAGE: fb_ec=0x2;  Address(0x10[4:4],0x10[6:6],)
SPIWrite 0010,40,6,6
SPIWrite 00b0,03,1,1
SPIWrite 0188,09,3,3
SPIWrite 0140,28,3,3
SPIWrite 0138,28,3,3
SPIWrite 0190,09,3,3
SPIWrite 0168,39,3,3
SPIWrite 0160,39,3,3
SPIWrite 0119,32,0,3
SPIWrite 0121,32,0,3
SPIWrite 0129,32,0,3
SPIWrite 0131,32,0,3
SPIWrite 0119,32,0,3
SPIWrite 0121,32,0,3
SPIWrite 0129,32,0,3
SPIWrite 0131,32,0,3
SPIWrite 0010,40,4,4    //PAGE: fb_ec=0x0;  Address(0x10[4:4],0x10[6:6],)
SPIWrite 0010,00,6,6
SPIWrite 0010,00,5,5    //PAGE: fb_ana=0x2;     Address(0x10[5:5],0x10[7:7],)
SPIWrite 0010,80,7,7
SPIWrite 0085,08,2,4
SPIWrite 0102,08,3,3
SPIWrite 0010,80,5,5    //PAGE: fb_ana=0x0;     Address(0x10[5:5],0x10[7:7],)
SPIWrite 0010,00,7,7
SPIWrite 0017,10,4,5    //PAGE: dac_2t=0x1;     Address(0x17[5:4],)
SPIWrite 002e,04,2,2
SPIWrite 0017,20,4,5    //PAGE: dac_2t=0x2;     Address(0x17[5:4],)
SPIWrite 002e,04,2,2
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SPIWrite 0017,00,4,5    //PAGE: dac_2t=0x0;     Address(0x17[5:4],)
SPIWrite 0017,40,6,7    //PAGE: ana_2r=0x1;     Address(0x17[7:6],)
SPIWrite 003f,20,3,5
SPIWrite 003f,26,1,2
SPIWrite 0017,80,6,7    //PAGE: ana_2r=0x2;     Address(0x17[7:6],)
SPIWrite 003f,20,3,5
SPIWrite 003f,26,1,2
SPIWrite 0017,00,6,7    //PAGE: ana_2r=0x0;     Address(0x17[7:6],)
SPIWrite 0010,20,5,5    //PAGE: fb_ana=0x1;     Address(0x10[5:5],0x10[7:7],)
SPIWrite 0010,20,7,7
SPIWrite 0080,10,4,4
SPIWrite 0080,18,3,3
SPIWrite 009a,01,0,0
SPIWrite 0095,01,0,0
SPIWrite 0094,c0,6,7
SPIWrite 0010,00,5,5    //PAGE: fb_ana=0x0;     Address(0x10[5:5],0x10[7:7],)
SPIWrite 0010,00,7,7
SPIWrite 0010,10,4,4    //PAGE: fb_ec=0x1;  Address(0x10[4:4],0x10[6:6],)
SPIWrite 0010,10,6,6
SPIWrite 0150,31,0,0
SPIWrite 0150,31,4,4
SPIWrite 0150,31,5,5
SPIWrite 0108,22,0,0
SPIWrite 0108,22,5,5
SPIWrite 0150,b1,7,7
SPIWrite 025e,40,0,7
SPIWrite 025d,00,7,7
SPIWrite 0028,a1,0,0
SPIWrite 0028,a0,0,0
SPIWrite 00a2,00,0,5
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a2,00,0,5
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0010,00,4,4    //PAGE: fb_ec=0x0;  Address(0x10[4:4],0x10[6:6],)
SPIWrite 0010,00,6,6
SPIWrite 0010,00,5,5    //PAGE: fb_ana=0x2;     Address(0x10[5:5],0x10[7:7],)
SPIWrite 0010,80,7,7
SPIWrite 0080,10,4,4
SPIWrite 0080,18,3,3
SPIWrite 009a,01,0,0
SPIWrite 0095,01,0,0
SPIWrite 0094,c0,6,7
SPIWrite 0010,80,5,5    //PAGE: fb_ana=0x0;     Address(0x10[5:5],0x10[7:7],)
SPIWrite 0010,00,7,7
SPIWrite 0010,00,4,4    //PAGE: fb_ec=0x2;  Address(0x10[4:4],0x10[6:6],)
SPIWrite 0010,40,6,6
SPIWrite 0150,31,0,0
SPIWrite 0150,31,4,4
SPIWrite 0150,31,5,5
SPIWrite 0108,22,0,0
SPIWrite 0108,22,5,5
SPIWrite 0150,b1,7,7
SPIWrite 025e,40,0,7
SPIWrite 025d,00,7,7
SPIWrite 0028,a1,0,0
SPIWrite 0028,a0,0,0
SPIWrite 00a2,00,0,5
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a2,00,0,5
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0010,40,4,4    //PAGE: fb_ec=0x0;  Address(0x10[4:4],0x10[6:6],)
SPIWrite 0010,00,6,6
SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)
SPIWrite 00a3,00,0,7
SPIWrite 00a2,01,0,7
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```
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,14,0,7

\\START: Enabling/Disabling Temp Sensor

SPIWrite 0013,00,0,7    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 03a3,08,0,7    //temp_sense1_sel_input=0x1;(Meaning: );    Address(0x3a0[27:27],)
SPIWrite 03a0,02,0,7    //temp_sense1_en=0x1;   Address(0x3a0[1:1],)
SPIWrite 03a0,02,0,7    //temp_sense1_soft_reset=0x0;   Address(0x3a0[0:0],)
SPIWrite 03a0,0e,0,7    //temp_sense1_div1=0x3;(Meaning: );     Address(0x3a0[3:2],)
SPIWrite 03a0,3e,0,7    //temp_sense1_div2=0x3;(Meaning: );     Address(0x3a0[5:4],)
SPIWrite 03a0,7e,0,7    //temp_sense1_analog_powerup=0x1;(Meaning: );   Address(0x3a0[6:6],)
SPIWrite 0722,02,0,7    //temp_sense_25m_clock_ungate=0x1;(Meaning: );  Address(0x720[17:17],)

\\END: Done enabling/Disabling Temp Sensor


\\END: Completed FB ADC Analog Writes

SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
\\ STEP: analogWrite/step3

\\START: Doing Writes to support AB and CD independent TDD

SPIWrite 0011,10,0,7    //PAGE: rx_ec_q=0x1;    Address(0x11[7:4],)
SPIWrite 0f05,01,0,7
SPIWrite 0f05,05,0,7
SPIWrite 0c75,01,0,7
SPIWrite 0c75,03,0,7
SPIWrite 0c75,83,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0017,01,0,7    //PAGE: dac_1t=0x1;     Address(0x17[3:0],)
SPIWrite 0057,39,0,7
SPIWrite 006d,47,0,7
SPIWrite 0050,04,0,7
SPIWrite 0017,00,0,7    //PAGE: dac_1t=0x0;     Address(0x17[3:0],)
SPIWrite 0011,01,0,7    //PAGE: rx_ec_i=0x1;    Address(0x11[3:0],)
SPIWrite 0c73,80,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,20,0,7    //PAGE: rx_ec_q=0x2;    Address(0x11[7:4],)
SPIWrite 0f05,01,0,7
SPIWrite 0f05,05,0,7
SPIWrite 0c75,01,0,7
SPIWrite 0c75,03,0,7
SPIWrite 0c75,83,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0017,02,0,7    //PAGE: dac_1t=0x2;     Address(0x17[3:0],)
SPIWrite 0057,39,0,7
SPIWrite 006d,47,0,7
SPIWrite 0050,04,0,7
SPIWrite 0017,00,0,7    //PAGE: dac_1t=0x0;     Address(0x17[3:0],)
SPIWrite 0011,02,0,7    //PAGE: rx_ec_i=0x2;    Address(0x11[3:0],)
SPIWrite 0c73,80,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,40,0,7    //PAGE: rx_ec_q=0x4;    Address(0x11[7:4],)
SPIWrite 0f05,01,0,7
SPIWrite 0f05,05,0,7
SPIWrite 0c75,01,0,7
SPIWrite 0c75,03,0,7
SPIWrite 0c75,83,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0017,04,0,7    //PAGE: dac_1t=0x4;     Address(0x17[3:0],)
SPIWrite 0057,39,0,7
SPIWrite 006d,47,0,7
SPIWrite 0050,04,0,7
SPIWrite 0017,00,0,7    //PAGE: dac_1t=0x0;     Address(0x17[3:0],)
SPIWrite 0011,04,0,7    //PAGE: rx_ec_i=0x4;    Address(0x11[3:0],)
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SPIWrite 0c73,80,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0011,80,0,7    //PAGE: rx_ec_q=0x8;    Address(0x11[7:4],)
SPIWrite 0f05,01,0,7
SPIWrite 0f05,05,0,7
SPIWrite 0c75,01,0,7
SPIWrite 0c75,03,0,7
SPIWrite 0c75,83,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0017,08,0,7    //PAGE: dac_1t=0x8;     Address(0x17[3:0],)
SPIWrite 0057,39,0,7
SPIWrite 006d,47,0,7
SPIWrite 0050,04,0,7
SPIWrite 0017,00,0,7    //PAGE: dac_1t=0x0;     Address(0x17[3:0],)
SPIWrite 0011,08,0,7    //PAGE: rx_ec_i=0x8;    Address(0x11[3:0],)
SPIWrite 0c73,80,0,7
SPIWrite 0011,00,0,7    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0014,01,0,7    //PAGE: clktop_2t=0x1;  Address(0x14[1:0],)
SPIWrite 006b,38,0,7    //MASK_PDN_SYNC_CROSS31=0x1;    Address(0x68[29:29],)
SPIWrite 006b,38,0,7    //MASK_PDN_SYNC_RXCML_R=0x1;    Address(0x68[28:28],)
SPIWrite 006b,38,0,7    //MASK_PDN_SYNC_RXCML_L=0x1;    Address(0x68[27:27],)
SPIWrite 006b,3c,0,7    //MASK_PDN_FAST_RXCML_R=0x1;    Address(0x68[26:26],)
SPIWrite 006b,3e,0,7    //MASK_PDN_FAST_RXCML_L=0x1;    Address(0x68[25:25],)
SPIWrite 006b,3f,0,7    //MASK_PDN_FAST_PLL13_CROSS_OUT=0x1;    Address(0x68[24:24],)
SPIWrite 006c,3e,0,7    //MASK_PDN_SYNC_CROSS13=0x1;    Address(0x6c[5:5],)
SPIWrite 006c,3e,0,7    //MASK_PDN_SYNC_TXCML_R=0x1;    Address(0x6c[4:4],)
SPIWrite 006c,3e,0,7    //MASK_PDN_SYNC_TXCML_L=0x1;    Address(0x6c[3:3],)
SPIWrite 006c,3e,0,7    //MASK_PDN_FAST_TXCML_R=0x1;    Address(0x6c[2:2],)
SPIWrite 006c,3e,0,7    //MASK_PDN_FAST_TXCML_L=0x1;    Address(0x6c[1:1],)
SPIWrite 006c,3f,0,7    //MASK_PDN_FAST_PLL31_CROSS_OUT=0x1;    Address(0x6c[0:0],)
SPIWrite 006f,10,0,7    //MASK_PDN_FAST_DCCLKROUTE_FBAB=0x1;    Address(0x6c[28:28],)
SPIWrite 006f,14,0,7    //MASK_PDN_FAST_DCCLKROUTE_RXAB=0x1;    Address(0x6c[26:26],)
SPIWrite 006f,15,0,7    //MASK_PDN_FAST_DCCLKROUTE_TXAB=0x1;    Address(0x6c[24:24],)
SPIWrite 006f,35,0,7    //MASK_PDN_FAST_DCCLKROUTE_FBCD=0x1;    Address(0x6c[29:29],)
SPIWrite 006f,3d,0,7    //MASK_PDN_FAST_DCCLKROUTE_RXCD=0x1;    Address(0x6c[27:27],)
SPIWrite 006f,3f,0,7    //MASK_PDN_FAST_DCCLKROUTE_TXCD=0x1;    Address(0x6c[25:25],)
SPIWrite 0014,00,0,7    //PAGE: clktop_2t=0x0;  Address(0x14[1:0],)
SPIWrite 0017,20,0,7    //PAGE: dac_2t=0x2;     Address(0x17[5:4],)
SPIWrite 002a,08,0,7
SPIWrite 0017,10,0,7    //PAGE: dac_2t=0x1;     Address(0x17[5:4],)
SPIWrite 002a,08,0,7
SPIWrite 0017,20,0,7    //PAGE: dac_2t=0x2;     Address(0x17[5:4],)
SPIWrite 002a,48,0,7
SPIWrite 0017,10,0,7    //PAGE: dac_2t=0x1;     Address(0x17[5:4],)
SPIWrite 002a,48,0,7

\\END: Completed writes to support AB and CD independent TDD

SPIWrite 0017,00,0,7    //PAGE: dac_2t=0x0;     Address(0x17[5:4],)
SPIWrite 0013,10,0,7    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,18,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,07,0,7
SPIWrite 00a6,04,0,7
SPIWrite 00a5,02,0,7
SPIWrite 00a4,00,0,7
SPIWrite 00ab,00,0,7
SPIWrite 00aa,00,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00a8,00,0,7
SPIWrite 0193,12,0,7

SPIPoll 00f0,0,7,7
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SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0011,10,4,7    //PAGE: rx_ec_q=0x1;    Address(0x11[7:4],)
SPIWrite 0281,80,7,7
SPIWrite 0284,40,6,6
SPIWrite 0284,c0,7,7
SPIWrite 0334,33,6,7
SPIWrite 0335,3c,0,2
SPIWrite 0011,00,4,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,01,0,3    //PAGE: rx_ec_i=0x1;    Address(0x11[3:0],)
SPIWrite 0335,3c,0,2
SPIWrite 0281,80,7,7
SPIWrite 0284,40,6,6
SPIWrite 0284,c0,7,7
SPIWrite 0334,33,6,7
SPIWrite 0011,00,0,3    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0012,01,0,3    //PAGE: rx_ec_common=0x1;   Address(0x12[3:0],)
SPIWrite 028a,80,7,7
SPIWrite 0012,00,0,3    //PAGE: rx_ec_common=0x0;   Address(0x12[3:0],)
SPIWrite 0011,20,4,7    //PAGE: rx_ec_q=0x2;    Address(0x11[7:4],)
SPIWrite 0281,80,7,7
SPIWrite 0284,40,6,6
SPIWrite 0284,c0,7,7
SPIWrite 0334,33,6,7
SPIWrite 0335,3c,0,2
SPIWrite 0011,00,4,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,02,0,3    //PAGE: rx_ec_i=0x2;    Address(0x11[3:0],)
SPIWrite 0335,3c,0,2
SPIWrite 0281,80,7,7
SPIWrite 0284,40,6,6
SPIWrite 0284,c0,7,7
SPIWrite 0334,33,6,7
SPIWrite 0011,00,0,3    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0012,02,0,3    //PAGE: rx_ec_common=0x2;   Address(0x12[3:0],)
SPIWrite 028a,80,7,7
SPIWrite 0012,00,0,3    //PAGE: rx_ec_common=0x0;   Address(0x12[3:0],)
SPIWrite 0011,40,4,7    //PAGE: rx_ec_q=0x4;    Address(0x11[7:4],)
SPIWrite 0281,80,7,7
SPIWrite 0284,40,6,6
SPIWrite 0284,c0,7,7
SPIWrite 0334,33,6,7
SPIWrite 0335,3c,0,2
SPIWrite 0011,00,4,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,04,0,3    //PAGE: rx_ec_i=0x4;    Address(0x11[3:0],)
SPIWrite 0335,3c,0,2
SPIWrite 0281,80,7,7
SPIWrite 0284,40,6,6
SPIWrite 0284,c0,7,7
SPIWrite 0334,32,6,7
SPIWrite 0011,00,0,3    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0012,04,0,3    //PAGE: rx_ec_common=0x4;   Address(0x12[3:0],)
SPIWrite 028a,80,7,7
SPIWrite 0012,00,0,3    //PAGE: rx_ec_common=0x0;   Address(0x12[3:0],)
SPIWrite 0011,80,4,7    //PAGE: rx_ec_q=0x8;    Address(0x11[7:4],)
SPIWrite 0281,80,7,7
SPIWrite 0284,40,6,6
SPIWrite 0284,c0,7,7
SPIWrite 0334,32,6,7
SPIWrite 0335,3c,0,2
SPIWrite 0011,00,4,7    //PAGE: rx_ec_q=0x0;    Address(0x11[7:4],)
SPIWrite 0011,08,0,3    //PAGE: rx_ec_i=0x8;    Address(0x11[3:0],)
SPIWrite 0335,3c,0,2
SPIWrite 0281,80,7,7
SPIWrite 0284,40,6,6
SPIWrite 0284,c0,7,7
SPIWrite 0334,31,6,7
SPIWrite 0011,00,0,3    //PAGE: rx_ec_i=0x0;    Address(0x11[3:0],)
SPIWrite 0012,08,0,3    //PAGE: rx_ec_common=0x8;   Address(0x12[3:0],)
SPIWrite 028a,80,7,7
SPIWrite 0012,00,0,7    //PAGE: rx_ec_common=0x0;   Address(0x12[3:0],)
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\\ STEP: jesdConfig/step0

\\START: Configuring Device JESD TX

SPIWrite 0015,01,0,7    //PAGE: rx_jesd=0x3;    Address(0x15[0:0],0x15[4:4],)
SPIWrite 0015,11,0,7
SPIWrite 00b0,04,0,7    //hd_sts_pll_lock_override=0x1;     Address(0xb0[2:2],)
SPIWrite 00b0,0c,0,7    //hd_sts_pll_lock_reg=0x1;  Address(0xb0[3:3],)
SPIWrite 0052,05,0,7    //ddc_bypass_8lanemode_en=0x0;  Address(0x50[20:20],)
SPIWrite 0045,e0,0,7    //init_state=0x1;(Meaning: );   Address(0x44[15:15],)
SPIWrite 0045,e0,0,7    //fifo_init_state=0x1;  Address(0x44[13:13],)
SPIWrite 0045,e0,0,7    //fb_init_state=0x1;(Meaning: );    Address(0x44[14:14],)
SPIWrite 0026,0f,0,7    //jesd_clear_data=0xf;  Address(0x24[19:16],)
SPIWrite 0020,37,0,7    //sysref_jesd_mode=0x1;     Address(0x20[7:5],)
SPIWrite 0020,3f,0,7    //k_m1=0x1f;    Address(0x20[4:0],)
SPIWrite 0021,1f,0,7    //fb_k_m1=0x1f;     Address(0x20[12:8],)
SPIWrite 0043,00,0,7    //jesd_mode=0x0;    Address(0x40[30:24],)
SPIWrite 0044,18,0,7    //fb_jesd_mode=0x18;    Address(0x44[6:0],)
SPIWrite 0076,36,0,7    //adc_jesd_root_clk_div=0x36;   Address(0x74[23:16],)
SPIWrite 00c0,00,0,7    //ddc_rd_clk_ratio_rx1=0x0;     Address(0xc0[4:0],)
SPIWrite 00c0,20,0,7    //ddc_rd_clk_ratio_rx1_override=0x1;    Address(0xc0[5:5],)
SPIWrite 00c1,00,0,7    //ddc_rd_clk_ratio_rx2=0x0;     Address(0xc0[12:8],)
SPIWrite 00c1,20,0,7    //ddc_rd_clk_ratio_rx2_override=0x1;    Address(0xc0[13:13],)
SPIWrite 00c4,01,0,7    //jesd_tx_clk_ratio_rx1=0x1;    Address(0xc4[4:0],)
SPIWrite 00c4,21,0,7    //jesd_tx_clk_ratio_rx1_override=0x1;   Address(0xc4[5:5],)
SPIWrite 00c5,01,0,7    //jesd_tx_clk_ratio_rx2=0x1;    Address(0xc4[12:8],)
SPIWrite 00c5,21,0,7    //jesd_tx_clk_ratio_rx2_override=0x1;   Address(0xc4[13:13],)
SPIWrite 0060,08,0,7    //jesd_system_mode=0x2;     Address(0x60[3:2],)
SPIWrite 0080,01,0,7    //scr_64b_initval=0x1;
Address(0x80[7:0],0x80[15:8],0x80[23:16],0x80[31:24],0x84[7:0],0x84[15:8],0x84[23:16],0x84[25:24]
,)
SPIWrite 0081,00,0,7
SPIWrite 0082,00,0,7
SPIWrite 0083,00,0,7
SPIWrite 0084,00,0,7
SPIWrite 0085,00,0,7
SPIWrite 0086,00,0,7
SPIWrite 0087,00,0,7
SPIWrite 0088,00,0,7    //scr_64b_en=0x0;   Address(0x88[0:0],)
SPIWrite 004f,00,0,7    //jesd_std_sel=0x0;(Meaning: );     Address(0x4c[25:24],)
SPIWrite 005f,08,0,7    //dedicated_rx_fb_lane_mode=0x1;    Address(0x5c[27:27],)
SPIWrite 00ca,01,0,7    //sample_drop_mode_rx1=0x1;     Address(0xc8[19:16],)
SPIWrite 00ca,11,0,7    //sample_drop_mode_rx2=0x1;     Address(0xc8[23:20],)
SPIWrite 0022,00,0,7    //scr=0x0;(Meaning: );  Address(0x20[16:16],)
SPIWrite 0023,00,0,7    //fb_scr=0x0;(Meaning: );   Address(0x20[24:24],)
SPIWrite 0025,0f,0,7    //lane_ena=0xf;     Address(0x24[11:8],)
SPIWrite 0077,04,0,7    //sysref_to_ddc_jesd_clk_div_override=0x1;  Address(0x74[26:26],)
SPIWrite 008f,00,0,7    //init_o_mf_counter=0x0;    Address(0x8c[25:16],)
SPIWrite 008e,00,0,7
SPIWrite 0045,e0,0,7    //init_state=0x1;(Meaning: );   Address(0x44[15:15],)
SPIWrite 0045,e0,0,7    //fifo_init_state=0x1;  Address(0x44[13:13],)
SPIWrite 0045,e0,0,7    //fb_init_state=0x1;(Meaning: );    Address(0x44[14:14],)

\\END: Done configuring Device JESD TX

SPIWrite 0015,10,0,7    //PAGE: rx_jesd=0x0;    Address(0x15[0:0],0x15[4:4],)
SPIWrite 0015,00,0,7
\\ STEP: jesdConfig/step1

\\START: Configuring Device JESD RX

SPIWrite 0015,02,0,7    //PAGE: tx_jesd=0x3;    Address(0x15[1:1],0x15[5:5],)
SPIWrite 0015,22,0,7
SPIWrite 007f,1f,0,7    //k_m1=0x1f;    Address(0x7c[31:24],)
SPIWrite 007e,1f,0,7    //rbd_m1=0x1f;  Address(0x7c[23:16],)
SPIWrite 0020,01,0,7    //init_state_tx0=0x1;(Meaning: );   Address(0x20[0:0],)
SPIWrite 0081,ff,0,7    //jesd_clear_data=0xff;     Address(0x80[15:8],)
SPIWrite 0021,36,0,7    //dac_jesd_root_clk_div=0x36;(Meaning: );   Address(0x20[15:8],)
SPIWrite 013d,00,0,7    //duc_wr_clk_ratio_tx0=0x0;(Meaning: );     Address(0x13c[12:8],)
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SPIWrite 013f,01,0,7    //jesd_rx_clk_ratio_tx0=0x1;(Meaning: );    Address(0x13c[28:24],)
SPIWrite 0024,05,0,7    //jesd_mode_tx0=0x5;(Meaning: );    Address(0x24[4:0],)
SPIWrite 013d,20,0,7    //duc_wr_clk_ratio_tx0_override=0x1;    Address(0x13c[13:13],)
SPIWrite 013f,21,0,7    //jesd_rx_clk_ratio_tx0_override=0x1;   Address(0x13c[29:29],)
SPIWrite 002d,9b,0,7    //spi_txenable=0x1;     Address(0x2c[8:8],)
SPIWrite 0093,ff,0,7    //spidac=0x7fff;    Address(0x90[31:24],0x94[7:0],)
SPIWrite 0094,7f,0,7
SPIWrite 0093,ff,0,7    //spidac=0x7fff;    Address(0x90[31:24],0x94[7:0],)
SPIWrite 0094,7f,0,7
SPIWrite 0092,00,0,7    //spidac_ena=0x0;   Address(0x90[23:23],)
SPIWrite 0092,00,0,7    //spidac_ena=0x0;   Address(0x90[23:23],)
SPIWrite 008b,df,0,7    //sync_request_ena=0xdf;    Address(0x88[31:24],)
SPIWrite 008c,00,0,7    //error_ena=0x0;    Address(0x8c[7:0],)
SPIWrite 0123,7f,0,7    //comma_align_valid_thresh_tx0=0x7f;    Address(0x120[30:24],)
SPIWrite 0148,00,0,7    //jesd_h_ena=0x0;   Address(0x148[1:1],)
SPIWrite 0148,00,0,7    //jesd_c_ena=0x0;   Address(0x148[0:0],)
SPIWrite 007d,12,0,7    //scr=0x0;  Address(0x7c[15:15],)
SPIWrite 007c,0f,0,7    //lane_ena=0xf;     Address(0x7c[7:0],)
SPIWrite 0134,04,0,7    //sysref_to_dac_jesd_clk_div_override=0x1;  Address(0x134[2:2],)
SPIWrite 0020,01,0,7    //init_state_tx0=0x1;(Meaning: );   Address(0x20[0:0],)

\\END: Done configuring Device JESD RX

SPIWrite 0015,20,0,7    //PAGE: tx_jesd=0x0;    Address(0x15[1:1],0x15[5:5],)
SPIWrite 0015,00,0,7

\\EXTERNAL-ACTION: If you have a RX or TX DSA packet to be applied, apply it here.

\\ STEP: calibration/step0

\\START: Sending Sysref to device from Pin/SPI


\\START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 01d4,01,0,7    //pll_reg_spi_req_a=0x1;    Address(0x1d4[0:0],)
SPIWrite 0374,00,0,7    //pll_reg_spi_req_b1=0x0;(Meaning: );   Address(0x374[0:0],)

SPIPoll 01d5,0,0,1


\\Read  pll_reg_spi_a_ack=0x1;  Address(0x1d4[8:8],)


\\END: Done requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0014,01,0,7    //PAGE: clktop_2t=0x1;  Address(0x14[1:0],)
SPIWrite 002c,00,0,7    //TRIM_100N_INT_TXCMLLDOVREF1=0x0;  Address(0x2c[7:5],)

WAIT 0.001

SPIWrite 0014,00,0,7    //PAGE: clktop_2t=0x0;  Address(0x14[1:0],)
SPIWrite 0014,04,0,7    //PAGE: TIMING_CON=0x1;(Meaning: );     Address(0x14[2:2],)
SPIWrite 04d1,00,0,7    //count_len_sysref=0xbf;    Address(0x4d0[15:0],)
SPIWrite 04d0,bf,0,7
SPIWrite 0717,00,0,7    //spare_reg_port=0x0;   Address(0x714[31:0],)
SPIWrite 0716,00,0,7
SPIWrite 0715,00,0,7
SPIWrite 0714,00,0,7
SPIWrite 0717,00,0,7    //spare_reg_port=0x101;     Address(0x714[31:0],)
SPIWrite 0716,00,0,7
SPIWrite 0715,01,0,7
SPIWrite 0714,01,0,7
SPIWrite 0717,00,0,7    //spare_reg_port=0x0;   Address(0x714[31:0],)
SPIWrite 0716,00,0,7
SPIWrite 0715,00,0,7
SPIWrite 0714,00,0,7
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SPIWrite 0014,00,0,7    //PAGE: TIMING_CON=0x0;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0014,08,0,7    //PAGE: pll=0x1;    Address(0x14[7:3],)
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 0051,8e,0,7    //SYS_REF_FROM_PIN_BYPAS=0x1;   Address(0x50[15:15],)
SPIWrite 0051,8e,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x1;    Address(0x50[11:11],)
SPIWrite 0014,10,0,7    //PAGE: pll=0x2;    Address(0x14[7:3],)
SPIWrite 004e,34,0,7    //lcmgen_usespisysref=0x1;  Address(0x4c[18:18],)
SPIWrite 0014,08,0,7    //PAGE: pll=0x1;    Address(0x14[7:3],)
SPIWrite 004e,30,0,7    //lcmgen_div=0xbf;  Address(0x4c[17:2],)
SPIWrite 004d,02,0,7
SPIWrite 004c,fc,0,7
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 004c,fd,0,7    //lcmgen_sync_ena=0x1;  Address(0x4c[0:0],)
SPIWrite 0014,10,0,7    //PAGE: pll=0x2;    Address(0x14[7:3],)
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 0051,8c,0,7    //SYS_REF_FROM_PIN_BYPAS=0x1;   Address(0x50[15:15],)
SPIWrite 0051,8c,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x1;    Address(0x50[11:11],)
SPIWrite 004e,34,0,7    //lcmgen_usespisysref=0x1;  Address(0x4c[18:18],)
SPIWrite 004e,34,0,7    //lcmgen_div=0xbf;  Address(0x4c[17:2],)
SPIWrite 004d,02,0,7
SPIWrite 004c,fc,0,7
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 004c,fd,0,7    //lcmgen_sync_ena=0x1;  Address(0x4c[0:0],)
SPIWrite 0014,20,0,7    //PAGE: pll=0x4;    Address(0x14[7:3],)
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 0051,8e,0,7    //SYS_REF_FROM_PIN_BYPAS=0x1;   Address(0x50[15:15],)
SPIWrite 0051,8e,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x1;    Address(0x50[11:11],)
SPIWrite 0014,10,0,7    //PAGE: pll=0x2;    Address(0x14[7:3],)
SPIWrite 004e,34,0,7    //lcmgen_usespisysref=0x1;  Address(0x4c[18:18],)
SPIWrite 0014,20,0,7    //PAGE: pll=0x4;    Address(0x14[7:3],)
SPIWrite 004e,30,0,7    //lcmgen_div=0xbf;  Address(0x4c[17:2],)
SPIWrite 004d,02,0,7
SPIWrite 004c,fc,0,7
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 004c,fd,0,7    //lcmgen_sync_ena=0x1;  Address(0x4c[0:0],)
SPIWrite 0014,40,0,7    //PAGE: pll=0x8;    Address(0x14[7:3],)
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 0051,8e,0,7    //SYS_REF_FROM_PIN_BYPAS=0x1;   Address(0x50[15:15],)
SPIWrite 0051,8e,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x1;    Address(0x50[11:11],)
SPIWrite 0014,10,0,7    //PAGE: pll=0x2;    Address(0x14[7:3],)
SPIWrite 004e,34,0,7    //lcmgen_usespisysref=0x1;  Address(0x4c[18:18],)
SPIWrite 0014,40,0,7    //PAGE: pll=0x8;    Address(0x14[7:3],)
SPIWrite 004e,30,0,7    //lcmgen_div=0xbf;  Address(0x4c[17:2],)
SPIWrite 004d,02,0,7
SPIWrite 004c,fc,0,7
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 004c,fd,0,7    //lcmgen_sync_ena=0x1;  Address(0x4c[0:0],)
SPIWrite 0014,80,0,7    //PAGE: pll=0x10;   Address(0x14[7:3],)
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 0051,86,0,7    //SYS_REF_FROM_PIN_BYPAS=0x1;   Address(0x50[15:15],)
SPIWrite 0051,8e,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x1;    Address(0x50[11:11],)
SPIWrite 0014,10,0,7    //PAGE: pll=0x2;    Address(0x14[7:3],)
SPIWrite 004e,34,0,7    //lcmgen_usespisysref=0x1;  Address(0x4c[18:18],)
SPIWrite 0014,80,0,7    //PAGE: pll=0x10;   Address(0x14[7:3],)
SPIWrite 004e,30,0,7    //lcmgen_div=0xbf;  Address(0x4c[17:2],)
SPIWrite 004d,02,0,7
SPIWrite 004c,fc,0,7
SPIWrite 004c,fc,0,7    //lcmgen_sync_ena=0x0;  Address(0x4c[0:0],)
SPIWrite 004c,fd,0,7    //lcmgen_sync_ena=0x1;  Address(0x4c[0:0],)

WAIT 0.001

SPIWrite 0014,10,0,7    //PAGE: pll=0x2;    Address(0x14[7:3],)
SPIWrite 004e,34,0,7    //lcmgen_spisysref=0x0;     Address(0x4c[19:19],)
SPIWrite 004e,3c,0,7    //lcmgen_spisysref=0x1;     Address(0x4c[19:19],)
SPIWrite 004e,34,0,7    //lcmgen_spisysref=0x0;     Address(0x4c[19:19],)
SPIWrite 0014,08,0,7    //PAGE: pll=0x1;    Address(0x14[7:3],)
SPIWrite 0051,0e,0,7    //SYS_REF_FROM_PIN_BYPAS=0x0;   Address(0x50[15:15],)
SPIWrite 0051,06,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x0;    Address(0x50[11:11],)
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SPIWrite 0014,10,0,7    //PAGE: pll=0x2;    Address(0x14[7:3],)
SPIWrite 0051,0c,0,7    //SYS_REF_FROM_PIN_BYPAS=0x0;   Address(0x50[15:15],)
SPIWrite 0051,04,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x0;    Address(0x50[11:11],)
SPIWrite 0014,20,0,7    //PAGE: pll=0x4;    Address(0x14[7:3],)
SPIWrite 0051,0e,0,7    //SYS_REF_FROM_PIN_BYPAS=0x0;   Address(0x50[15:15],)
SPIWrite 0051,06,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x0;    Address(0x50[11:11],)
SPIWrite 0014,40,0,7    //PAGE: pll=0x8;    Address(0x14[7:3],)
SPIWrite 0051,0e,0,7    //SYS_REF_FROM_PIN_BYPAS=0x0;   Address(0x50[15:15],)
SPIWrite 0051,06,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x0;    Address(0x50[11:11],)
SPIWrite 0014,80,0,7    //PAGE: pll=0x10;   Address(0x14[7:3],)
SPIWrite 0051,0e,0,7    //SYS_REF_FROM_PIN_BYPAS=0x0;   Address(0x50[15:15],)
SPIWrite 0051,06,0,7    //EN_SYNC_TO_PLLDIG_DIV=0x0;    Address(0x50[11:11],)
SPIWrite 0014,00,0,7    //PAGE: pll=0x0;    Address(0x14[7:3],)
SPIWrite 0014,01,0,7    //PAGE: clktop_2t=0x1;  Address(0x14[1:0],)
SPIWrite 002c,00,0,7    //TRIM_100N_INT_TXCMLLDOVREF1=0x0;  Address(0x2c[7:5],)

\\START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0014,00,0,7    //PAGE: clktop_2t=0x0;  Address(0x14[1:0],)
SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 01d4,00,0,7    //pll_reg_spi_req_a=0x0;    Address(0x1d4[0:0],)
SPIWrite 0374,00,0,7    //pll_reg_spi_req_b1=0x0;(Meaning: );   Address(0x374[0:0],)

WAIT 0.01


\\END: Done requesting/releasing SPI Access to PLL Pages


\\END: Done sending Sysref to device from Pin/SPI


\\START: Staggered TDD Toggle

SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0014,04,0,7    //PAGE: TIMING_CON=0x1;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0124,01,0,7    //use_reg_txon_AB=0x1;  Address(0x124[0:0],)
SPIWrite 0126,01,0,7    //use_reg_rxon_AB=0x1;  Address(0x124[16:16],)
SPIWrite 0128,01,0,7    //use_reg_fbon_AB=0x1;  Address(0x128[0:0],)
SPIWrite 012a,01,0,7    //use_reg_txon_CD=0x1;  Address(0x128[16:16],)
SPIWrite 012c,01,0,7    //use_reg_rxon_CD=0x1;  Address(0x12c[0:0],)
SPIWrite 012e,01,0,7    //use_reg_fbon_CD=0x1;  Address(0x12c[16:16],)
SPIWrite 0127,00,0,7    //reg_for_rxon_AB=0x0;  Address(0x124[24:24],)
SPIWrite 012d,00,0,7    //reg_for_rxon_CD=0x0;  Address(0x12c[8:8],)
SPIWrite 0127,01,0,7    //reg_for_rxon_AB=0x1;  Address(0x124[24:24],)
SPIWrite 012d,01,0,7    //reg_for_rxon_CD=0x1;  Address(0x12c[8:8],)
SPIWrite 0127,00,0,7    //reg_for_rxon_AB=0x0;  Address(0x124[24:24],)
SPIWrite 012d,00,0,7    //reg_for_rxon_CD=0x0;  Address(0x12c[8:8],)
SPIWrite 0125,00,0,7    //reg_for_txon_AB=0x0;  Address(0x124[8:8],)
SPIWrite 012b,00,0,7    //reg_for_txon_CD=0x0;  Address(0x128[24:24],)
SPIWrite 0129,00,0,7    //reg_for_fbon_AB=0x0;  Address(0x128[8:8],)
SPIWrite 012f,00,0,7    //reg_for_fbon_CD=0x0;  Address(0x12c[24:24],)
SPIWrite 0125,01,0,7    //reg_for_txon_AB=0x1;  Address(0x124[8:8],)
SPIWrite 012b,01,0,7    //reg_for_txon_CD=0x1;  Address(0x128[24:24],)
SPIWrite 0129,01,0,7    //reg_for_fbon_AB=0x1;  Address(0x128[8:8],)
SPIWrite 012f,01,0,7    //reg_for_fbon_CD=0x1;  Address(0x12c[24:24],)

\\END: Done Staggered TDD Toggle

SPIWrite 0014,00,0,7    //PAGE: TIMING_CON=0x0;(Meaning: );     Address(0x14[2:2],)
\\ STEP: calibration/step1

\\START: Enabling RX DC correction

SPIWrite 0010,0c,0,7    //PAGE: rx_top=0x3;     Address(0x10[3:2],)
SPIWrite 0401,01,0,7    //dc_freeze_reg=0x1;(Meaning: );    Address(0x400[8:8],)
SPIWrite 0420,00,0,7    //alpha_update_signal=0x0;  Address(0x420[0:0],)
SPIWrite 0420,01,0,7    //alpha_update_signal=0x1;  Address(0x420[0:0],)
SPIWrite 0420,00,0,7    //alpha_update_signal=0x0;  Address(0x420[0:0],)
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SPIWrite 0401,00,0,7    //dc_freeze_reg=0x0;(Meaning: );    Address(0x400[8:8],)
SPIWrite 0400,00,0,7    //bypass=0x0;(Meaning: );   Address(0x400[0:0],)
SPIWrite 0411,01,0,7    //dc_freeze_reg=0x1;(Meaning: );    Address(0x410[8:8],)
SPIWrite 0421,00,0,7    //alpha_update_signal=0x0;  Address(0x420[8:8],)
SPIWrite 0421,01,0,7    //alpha_update_signal=0x1;  Address(0x420[8:8],)
SPIWrite 0421,00,0,7    //alpha_update_signal=0x0;  Address(0x420[8:8],)
SPIWrite 0411,00,0,7    //dc_freeze_reg=0x0;(Meaning: );    Address(0x410[8:8],)
SPIWrite 0410,00,0,7    //bypass=0x0;(Meaning: );   Address(0x410[0:0],)
SPIWrite 0801,01,0,7    //dc_freeze_reg=0x1;(Meaning: );    Address(0x800[8:8],)
SPIWrite 0820,00,0,7    //alpha_update_signal=0x0;  Address(0x820[0:0],)
SPIWrite 0820,01,0,7    //alpha_update_signal=0x1;  Address(0x820[0:0],)
SPIWrite 0820,00,0,7    //alpha_update_signal=0x0;  Address(0x820[0:0],)
SPIWrite 0801,00,0,7    //dc_freeze_reg=0x0;(Meaning: );    Address(0x800[8:8],)
SPIWrite 0800,00,0,7    //bypass=0x0;(Meaning: );   Address(0x800[0:0],)
SPIWrite 0811,01,0,7    //dc_freeze_reg=0x1;(Meaning: );    Address(0x810[8:8],)
SPIWrite 0821,00,0,7    //alpha_update_signal=0x0;  Address(0x820[8:8],)
SPIWrite 0821,01,0,7    //alpha_update_signal=0x1;  Address(0x820[8:8],)
SPIWrite 0821,00,0,7    //alpha_update_signal=0x0;  Address(0x820[8:8],)
SPIWrite 0811,00,0,7    //dc_freeze_reg=0x0;(Meaning: );    Address(0x810[8:8],)
SPIWrite 0810,00,0,7    //bypass=0x0;(Meaning: );   Address(0x810[0:0],)

\\END: Done enabling RX DC correction

SPIWrite 0010,00,0,7    //PAGE: rx_top=0x0;     Address(0x10[3:2],)
\\ STEP: gpioConfig/step0

\\Removing the force on Sync Pin.

SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0555,fd,0,7    //ovr_sel_intpo_dac_sync_n_ab_0=0x0;    Address(0x554[9:9],)
SPIWrite 0555,f5,0,7    //ovr_sel_intpo_dac_sync_n_ab_1=0x0;    Address(0x554[11:11],)
SPIWrite 0555,d5,0,7    //ovr_sel_intpo_dac_sync_n_cd_0=0x0;    Address(0x554[13:13],)
SPIWrite 0555,55,0,7    //ovr_sel_intpo_dac_sync_n_cd_1=0x0;    Address(0x554[15:15],)

\\START: Configuring GPIO

SPIWrite 0538,05,0,7    //preferred_input_sel_gpio_78=0x1;  Address(0x538[4:2],)
SPIWrite 0538,05,0,7    //buf_dir_ctrl_gpio_78=0x1;     Address(0x538[1:0],)
SPIWrite 0550,2a,0,7    //ovr_sel_intpi_tdd_2t_en_cd=0x0;   Address(0x550[7:7],)
SPIWrite 0500,21,0,7    //preferred_output_sel_gpio_64=0x1;     Address(0x500[7:5],)
SPIWrite 0500,22,0,7    //buf_dir_ctrl_gpio_64=0x2;     Address(0x500[1:0],)
SPIWrite 0592,00,0,7    //ovr_sel_intpo_rxd_ext_lnabypass=0x0;  Address(0x590[23:23],)
SPIWrite 0510,21,0,7    //preferred_output_sel_gpio_68=0x1;     Address(0x510[7:5],)
SPIWrite 0510,22,0,7    //buf_dir_ctrl_gpio_68=0x2;     Address(0x510[1:0],)
SPIWrite 0592,00,0,7    //ovr_sel_intpo_rxc_ext_lnabypass=0x0;  Address(0x590[21:21],)
SPIWrite 0518,01,0,7    //preferred_output_sel_gpio_70=0x0;     Address(0x518[7:5],)
SPIWrite 0518,02,0,7    //buf_dir_ctrl_gpio_70=0x2;     Address(0x518[1:0],)
SPIWrite 051a,21,0,7    //crossbar_sel_output_gpio_70=0x21;     Address(0x518[23:16],)
SPIWrite 0587,00,0,7    //ovr_sel_intpo_rxc_digpkdet_hth=0x0;   Address(0x584[25:25],)
SPIWrite 04e4,05,0,7    //preferred_input_sel_gpio_57=0x1;  Address(0x4e4[4:2],)
SPIWrite 04e4,05,0,7    //buf_dir_ctrl_gpio_57=0x1;     Address(0x4e4[1:0],)
SPIWrite 0554,f7,0,7    //ovr_sel_intpi_adc_sync_n_ab_1=0x0;    Address(0x554[3:3],)
SPIWrite 04a4,01,0,7    //preferred_output_sel_gpio_41=0x0;     Address(0x4a4[7:5],)
SPIWrite 04a4,02,0,7    //buf_dir_ctrl_gpio_41=0x2;     Address(0x4a4[1:0],)
SPIWrite 04a6,1e,0,7    //crossbar_sel_output_gpio_41=0x1e;     Address(0x4a4[23:16],)
SPIWrite 0586,00,0,7    //ovr_sel_intpo_rxb_digpkdet_lth=0x0;   Address(0x584[23:23],)
SPIWrite 0458,21,0,7    //preferred_output_sel_gpio_22=0x1;     Address(0x458[7:5],)
SPIWrite 0458,22,0,7    //buf_dir_ctrl_gpio_22=0x2;     Address(0x458[1:0],)
SPIWrite 0571,00,0,7    //ovr_sel_intpo_alarm_2=0x0;    Address(0x570[13:13],)
SPIWrite 0454,05,0,7    //preferred_input_sel_gpio_21=0x1;  Address(0x454[4:2],)
SPIWrite 0454,05,0,7    //buf_dir_ctrl_gpio_21=0x1;     Address(0x454[1:0],)
SPIWrite 056d,02,0,7    //ovr_sel_intpi_global_pdn=0x0;     Address(0x56c[11:11],)
SPIWrite 0420,05,0,7    //preferred_input_sel_gpio_8=0x1;   Address(0x420[4:2],)
SPIWrite 0420,05,0,7    //buf_dir_ctrl_gpio_8=0x1;  Address(0x420[1:0],)
SPIWrite 0551,00,0,7    //ovr_sel_intpi_tdd_1f_en_ab=0x0;   Address(0x550[9:9],)
SPIWrite 0468,05,0,7    //preferred_input_sel_gpio_26=0x1;  Address(0x468[4:2],)
SPIWrite 0468,05,0,7    //buf_dir_ctrl_gpio_26=0x1;     Address(0x468[1:0],)
SPIWrite 0550,22,0,7    //ovr_sel_intpi_tdd_2r_en_cd=0x0;   Address(0x550[3:3],)
SPIWrite 053c,01,0,7    //preferred_output_sel_gpio_79=0x0;     Address(0x53c[7:5],)
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SPIWrite 053c,02,0,7    //buf_dir_ctrl_gpio_79=0x2;     Address(0x53c[1:0],)
SPIWrite 053e,22,0,7    //crossbar_sel_output_gpio_79=0x22;     Address(0x53c[23:16],)
SPIWrite 0587,00,0,7    //ovr_sel_intpo_rxc_digpkdet_lth=0x0;   Address(0x584[27:27],)
SPIWrite 04dc,01,0,7    //preferred_output_sel_gpio_55=0x0;     Address(0x4dc[7:5],)
SPIWrite 04dc,02,0,7    //buf_dir_ctrl_gpio_55=0x2;     Address(0x4dc[1:0],)
SPIWrite 04de,1a,0,7    //crossbar_sel_output_gpio_55=0x1a;     Address(0x4dc[23:16],)
SPIWrite 0586,00,0,7    //ovr_sel_intpo_rxa_digpkdet_lth=0x0;   Address(0x584[19:19],)
SPIWrite 046c,21,0,7    //preferred_output_sel_gpio_27=0x1;     Address(0x46c[7:5],)
SPIWrite 046c,22,0,7    //buf_dir_ctrl_gpio_27=0x2;     Address(0x46c[1:0],)
SPIWrite 0571,00,0,7    //ovr_sel_intpo_alarm_1=0x0;    Address(0x570[11:11],)
SPIWrite 040c,05,0,7    //preferred_input_sel_gpio_3=0x1;   Address(0x40c[4:2],)
SPIWrite 040c,05,0,7    //buf_dir_ctrl_gpio_3=0x1;  Address(0x40c[1:0],)
SPIWrite 0550,02,0,7    //ovr_sel_intpi_tdd_2t_en_ab=0x0;   Address(0x550[5:5],)
SPIWrite 0444,05,0,7    //preferred_input_sel_gpio_17=0x1;  Address(0x444[4:2],)
SPIWrite 0444,05,0,7    //buf_dir_ctrl_gpio_17=0x1;     Address(0x444[1:0],)
SPIWrite 05b0,23,0,7    //ovr_sel_intpi_spib1_clk=0x0;  Address(0x5b0[3:3],)
SPIWrite 0520,22,0,7    //preferred_output_sel_gpio_72=0x1;     Address(0x520[7:5],)
SPIWrite 0520,22,0,7    //buf_dir_ctrl_gpio_72=0x2;     Address(0x520[1:0],)
SPIWrite 0555,55,0,7    //ovr_sel_intpo_dac_sync_n_cd_0=0x0;    Address(0x554[13:13],)
SPIWrite 04c0,05,0,7    //preferred_input_sel_gpio_48=0x1;  Address(0x4c0[4:2],)
SPIWrite 04c0,05,0,7    //buf_dir_ctrl_gpio_48=0x1;     Address(0x4c0[1:0],)
SPIWrite 0554,f5,0,7    //ovr_sel_intpi_adc_sync_n_ab_0=0x0;    Address(0x554[1:1],)
SPIWrite 04e0,01,0,7    //preferred_output_sel_gpio_56=0x0;     Address(0x4e0[7:5],)
SPIWrite 04e0,02,0,7    //buf_dir_ctrl_gpio_56=0x2;     Address(0x4e0[1:0],)
SPIWrite 04e2,1d,0,7    //crossbar_sel_output_gpio_56=0x1d;     Address(0x4e0[23:16],)
SPIWrite 0586,00,0,7    //ovr_sel_intpo_rxb_digpkdet_hth=0x0;   Address(0x584[21:21],)
SPIWrite 051c,01,0,7    //preferred_output_sel_gpio_71=0x0;     Address(0x51c[7:5],)
SPIWrite 051c,02,0,7    //buf_dir_ctrl_gpio_71=0x2;     Address(0x51c[1:0],)
SPIWrite 051e,26,0,7    //crossbar_sel_output_gpio_71=0x26;     Address(0x51c[23:16],)
SPIWrite 0587,00,0,7    //ovr_sel_intpo_rxd_digpkdet_lth=0x0;   Address(0x584[31:31],)
SPIWrite 0534,05,0,7    //preferred_input_sel_gpio_77=0x1;  Address(0x534[4:2],)
SPIWrite 0534,05,0,7    //buf_dir_ctrl_gpio_77=0x1;     Address(0x534[1:0],)
SPIWrite 0552,28,0,7    //ovr_sel_intpi_tdd_1f_en_cd=0x0;   Address(0x550[17:17],)
SPIWrite 0530,05,0,7    //preferred_input_sel_gpio_76=0x1;  Address(0x530[4:2],)
SPIWrite 0530,05,0,7    //buf_dir_ctrl_gpio_76=0x1;     Address(0x530[1:0],)
SPIWrite 0554,d5,0,7    //ovr_sel_intpi_adc_sync_n_cd_0=0x0;    Address(0x554[5:5],)
SPIWrite 04d4,21,0,7    //preferred_output_sel_gpio_53=0x1;     Address(0x4d4[7:5],)
SPIWrite 04d4,22,0,7    //buf_dir_ctrl_gpio_53=0x2;     Address(0x4d4[1:0],)
SPIWrite 0586,00,0,7    //ovr_sel_intpo_rxa_digpkdet_hth=0x0;   Address(0x584[17:17],)
SPIWrite 04cc,05,0,7    //preferred_input_sel_gpio_51=0x1;  Address(0x4cc[4:2],)
SPIWrite 04cc,05,0,7    //buf_dir_ctrl_gpio_51=0x1;     Address(0x4cc[1:0],)
SPIWrite 0550,00,0,7    //ovr_sel_intpi_tdd_2r_en_ab=0x0;   Address(0x550[1:1],)
SPIWrite 04b8,21,0,7    //preferred_output_sel_gpio_46=0x1;     Address(0x4b8[7:5],)
SPIWrite 04b8,22,0,7    //buf_dir_ctrl_gpio_46=0x2;     Address(0x4b8[1:0],)
SPIWrite 0592,00,0,7    //ovr_sel_intpo_rxb_ext_lnabypass=0x0;  Address(0x590[19:19],)
SPIWrite 04a8,21,0,7    //preferred_output_sel_gpio_42=0x1;     Address(0x4a8[7:5],)
SPIWrite 04a8,22,0,7    //buf_dir_ctrl_gpio_42=0x2;     Address(0x4a8[1:0],)
SPIWrite 0592,00,0,7    //ovr_sel_intpo_rxa_ext_lnabypass=0x0;  Address(0x590[17:17],)
SPIWrite 0430,05,0,7    //preferred_input_sel_gpio_12=0x1;  Address(0x430[4:2],)
SPIWrite 0430,05,0,7    //buf_dir_ctrl_gpio_12=0x1;     Address(0x430[1:0],)
SPIWrite 05b0,03,0,7    //ovr_sel_intbipi_spib1_sdi=0x0;    Address(0x5b0[5:5],)
SPIWrite 0438,05,0,7    //preferred_input_sel_gpio_14=0x1;  Address(0x438[4:2],)
SPIWrite 0438,05,0,7    //buf_dir_ctrl_gpio_14=0x1;     Address(0x438[1:0],)
SPIWrite 05b0,01,0,7    //ovr_sel_intpi_spib1_cs_n=0x0;     Address(0x5b0[1:1],)
SPIWrite 042c,21,0,7    //preferred_output_sel_gpio_11=0x1;     Address(0x42c[7:5],)
SPIWrite 042c,22,0,7    //buf_dir_ctrl_gpio_11=0x2;     Address(0x42c[1:0],)
SPIWrite 05b0,01,0,7    //ovr_sel_intpo_spib1_sdo=0x0;  Address(0x5b0[7:7],)
SPIWrite 0524,01,0,7    //preferred_output_sel_gpio_73=0x0;     Address(0x524[7:5],)
SPIWrite 0524,02,0,7    //buf_dir_ctrl_gpio_73=0x2;     Address(0x524[1:0],)
SPIWrite 0526,25,0,7    //crossbar_sel_output_gpio_73=0x25;     Address(0x524[23:16],)
SPIWrite 0587,00,0,7    //ovr_sel_intpo_rxd_digpkdet_hth=0x0;   Address(0x584[29:29],)
SPIWrite 04f4,05,0,7    //preferred_input_sel_gpio_61=0x1;  Address(0x4f4[4:2],)
SPIWrite 04f4,05,0,7    //buf_dir_ctrl_gpio_61=0x1;     Address(0x4f4[1:0],)
SPIWrite 0554,55,0,7    //ovr_sel_intpi_adc_sync_n_cd_1=0x0;    Address(0x554[7:7],)
SPIWrite 04bc,22,0,7    //preferred_output_sel_gpio_47=0x1;     Address(0x4bc[7:5],)
SPIWrite 04bc,22,0,7    //buf_dir_ctrl_gpio_47=0x2;     Address(0x4bc[1:0],)
SPIWrite 0555,55,0,7    //ovr_sel_intpo_dac_sync_n_ab_0=0x0;    Address(0x554[9:9],)

\\END: Done Configuring GPIO
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SPIWrite 025c,00,0,7    //pull_ctrl_gpio_23=0x0;    Address(0x25c[2:0],)
SPIWrite 0270,00,0,7    //pull_ctrl_gpio_28=0x0;    Address(0x270[2:0],)
SPIWrite 0274,00,0,7    //pull_ctrl_gpio_29=0x0;    Address(0x274[2:0],)
SPIWrite 045c,00,0,7    //buf_dir_ctrl_gpio_23=0x0;     Address(0x45c[1:0],)
SPIWrite 0470,00,0,7    //buf_dir_ctrl_gpio_28=0x0;     Address(0x470[1:0],)
SPIWrite 0474,00,0,7    //buf_dir_ctrl_gpio_29=0x0;     Address(0x474[1:0],)

\\START: Configuring Aux ADC

SPIWrite 0100,00,0,7    //auxadc_powerup=0x0;   Address(0x100[0:0],)
SPIWrite 0100,00,0,7    //auxadc_en_conv=0x0;   Address(0x100[1:1],)
SPIWrite 0100,00,0,7    //auxadc_soft_reset=0x0;    Address(0x100[3:3],)
SPIWrite 0106,01,0,7    //auxadc_sar_bit_mode=0x1;(Meaning: );  Address(0x104[16:16],)
SPIWrite 0102,20,0,7    //auxadc_INP_MUX=0x1;(Meaning: );   Address(0x100[23:21],)
SPIWrite 0102,20,0,7    //auxadc_INM_MUX=0x0;(Meaning: );   Address(0x100[20:18],)
SPIWrite 0733,04,0,7    //aux_adc_reg_sar_delay=0x4;    Address(0x730[26:24],)
SPIWrite 0101,08,0,7    //auxadc_clk_div=0x1;(Meaning: );   Address(0x100[12:11],)
SPIWrite 0101,0a,0,7    //auxadc_duty_cycle_clk=0x2;(Meaning: );    Address(0x100[10:8],)
SPIWrite 0108,00,0,7    //auxadc_offset_estim_phase_en=0x0;     Address(0x108[5:5],)
SPIWrite 0105,a0,0,7    //auxadc_sar_averaging=0x5;(Meaning: );     Address(0x104[15:13],)
SPIWrite 0105,a1,0,7    //auxadc_sar_logic_niter=0x1;   Address(0x104[9:8],)
SPIWrite 0106,05,0,7    //auxadc_inp_buf_chop=0x2;(Meaning: );  Address(0x104[18:17],)
SPIWrite 0106,15,0,7    //auxadc_incm_buf_chop=0x2;(Meaning: );     Address(0x104[20:19],)
SPIWrite 0106,95,0,7    //auxadc_inp_buf_mux_ctrl=0x4;(Meaning: );  Address(0x104[23:21],)
SPIWrite 0105,a1,0,7    //auxadc_sar_logic_state_start=0x0;     Address(0x104[12:10],)
SPIWrite 0108,00,0,7    //auxadc_offset_data_out=0x0;   Address(0x108[6:6],)
SPIWrite 0108,00,0,7    //auxadc_offsetvlaue_force_en=0x0;  Address(0x108[4:4],)
SPIWrite 0107,00,0,7
SPIWrite 0108,00,0,7    //auxadc_offset_corr_value_msb=0x0;     Address(0x108[3:0],)
SPIWrite 0730,00,0,7    //aux_adc_reg_cap_code_force_en=0x0;    Address(0x730[6:6],)
SPIWrite 0730,00,0,7    //aux_adc_reg_cap_code_p_force_val=0x0;     Address(0x730[5:0],)
SPIWrite 0731,00,0,7    //aux_adc_reg_res_code1_force_en=0x0;   Address(0x730[13:13],)
SPIWrite 0731,00,0,7    //aux_adc_reg_res_code2_force_en=0x0;   Address(0x730[14:14],)
SPIWrite 0731,00,0,7    //aux_adc_reg_res_code3_force_en=0x0;   Address(0x730[15:15],)
SPIWrite 0731,00,0,7    //aux_adc_reg_res_code1_p_force_val=0x0;    Address(0x730[12:8],)
SPIWrite 0732,00,0,7    //aux_adc_reg_res_code2_p_force_val=0x0;    Address(0x730[20:16],)
SPIWrite 0732,00,0,7    //aux_adc_reg_res_code3_p_force_val=0x0;    Address(0x730[23:21],)
SPIWrite 0103,00,0,7    //auxadc_inp_res_term_imeas=0x0;(Meaning: );    Address(0x100[31:30],)
SPIWrite 0733,04,0,7    //aux_adc_EN_TP=0x0;(Meaning: );    Address(0x730[31:28],)
SPIWrite 0737,00,0,7    //temp_sense2_cfg1=0x0;     Address(0x734[31:0],)
SPIWrite 0736,00,0,7
SPIWrite 0735,00,0,7
SPIWrite 0734,00,0,7
SPIWrite 0104,00,0,7    //auxadc_TM_IN_MUX_SEL=0x0;(Meaning: );     Address(0x104[2:0],)
SPIWrite 0104,00,0,7    //auxadc_TP_IN_MUX_SEL=0x0;(Meaning: );     Address(0x104[5:3],)
SPIWrite 0102,20,0,7

WAIT 0.1

SPIWrite 0100,00,0,7    //auxadc_soft_reset=0x0;    Address(0x100[3:3],)

WAIT 0.1

SPIWrite 0100,02,0,7    //auxadc_en_conv=0x1;   Address(0x100[1:1],)

\\END: Done configuring Aux ADC

SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
\\ STEP: rxIqMc/step0

\\START: Doing RX IQMC Correction


\\START: Doing RX IQMC Correction Configuration

SPIWrite 0018,10,0,7    //PAGE: rx_iqmc=0x1;    Address(0x18[4:4],)
SPIWrite 0348,04,0,7
SPIWrite 0348,44,0,7
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SPIWrite 0018,00,4,4    //PAGE: rx_iqmc=0x0;    Address(0x18[4:4],)
SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,1e,0,7
SPIWrite 00a1,05,0,7
SPIWrite 00a0,02,0,7
SPIWrite 0193,01,0,7

\\Read  macro_opcode_operand=0x1000000;     Address(0x190[31:0],)


SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0x20[4:4],)


\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0x20[5:5],)


\\Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0x20[6:6],)


\\Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0x20[7:7],)


\\Read  MACRO_STATUS_RESULT_0=0x11119e;     Address(0x34[31:0],)

SPIWrite 0013,00,5,5    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
SPIWrite 0018,10,4,4    //PAGE: rx_iqmc=0x1;    Address(0x18[4:4],)
SPIWrite 036c,08,3,3
SPIWrite 036c,0a,0,2
SPIWrite 0381,00,7,7
SPIWrite 0305,00,0,0
SPIWrite 0305,02,1,1
SPIWrite 0341,00,0,3
SPIWrite 0340,04,0,7
SPIWrite 0343,40,6,6
SPIWrite 0334,07,0,6
SPIWrite 0334,87,7,7
SPIWrite 037e,7f,0,6
SPIWrite 037e,ff,7,7
SPIWrite 0335,1c,0,6
SPIWrite 0335,9c,7,7
SPIWrite 0320,14,0,6
SPIWrite 0320,94,7,7
SPIWrite 0321,14,0,6
SPIWrite 0321,94,7,7
SPIWrite 0324,04,0,2
SPIWrite 0324,0c,3,3
SPIWrite 0324,4c,4,6
SPIWrite 0324,cc,7,7
SPIWrite 0342,00,0,7
SPIWrite 0341,c0,4,7
SPIWrite 0343,c0,7,7
SPIWrite 0327,02,0,6
SPIWrite 0327,82,7,7
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SPIWrite 0322,02,0,6
SPIWrite 0322,82,7,7
SPIWrite 0318,08,0,6
SPIWrite 0318,88,7,7
SPIWrite 0348,44,2,2
SPIWrite 0348,44,6,6
SPIWrite 031c,00,0,5
SPIWrite 031c,80,7,7
SPIWrite 030f,03,0,5
SPIWrite 030f,83,7,7
SPIWrite 0350,00,7,7
SPIWrite 034f,00,7,7
SPIWrite 0359,3c,2,6
SPIWrite 035a,01,0,6
SPIWrite 035b,02,0,6
SPIWrite 0359,bc,7,7
SPIWrite 035a,81,7,7
SPIWrite 035b,82,7,7

\\END: Done configuring RX IQMC Correction


\\END: Did RX IQMC Correction

SPIWrite 0018,00,0,7    //PAGE: rx_iqmc=0x0;    Address(0x18[4:4],)
\\ STEP: agcConfig/step0

\\START: Doing AGC Config

SPIWrite 0010,0c,0,7    //PAGE: rx_top=0x3;     Address(0x10[3:2],)
SPIWrite 04cd,00,0,7    //blank_time_rf_det=0x64;   Address(0x4cc[15:0],)
SPIWrite 04cc,64,0,7
SPIWrite 04cf,01,0,7    //blank_time=0x1f4;     Address(0x4cc[31:16],)
SPIWrite 04ce,f4,0,7
SPIWrite 0275,03,0,7    //blank_time_for_ext_comp_change=0x3e8;     Address(0x274[15:0],)
SPIWrite 0274,e8,0,7
SPIWrite 0cd1,02,0,7    //disable_hysterisis=0x1;(Meaning: );   Address(0xcd0[9:9],)
SPIWrite 0cd1,02,0,7    //dig_gain_dis=0x0;     Address(0xcd0[8:8],)
SPIWrite 0cd1,02,0,7    //dig_gain_dis=0x0;     Address(0xcd0[8:8],)
SPIWrite 0a80,b3,0,7    //gain_comp_stg_2_3_dec_chain=0xb3;     Address(0xa80[7:0],)

\\START: Configuring DGC

SPIWrite 0334,07,0,7    //DgcEnRxMode=0x1;(Meaning: );  Address(0x334[0:0],)
SPIWrite 0337,00,0,7    //FltPtMode=0x0;    Address(0x334[24:24],)
SPIWrite 0337,00,0,7    //FltPtFmt=0x0;(Meaning: );     Address(0x334[26:25],)
SPIWrite 0335,1b,0,7    //DgcMode=0x3;(Meaning: );  Address(0x334[10:8],)
SPIWrite 033c,24,0,7    //NBitsCoarseIdx=0x4;(Meaning: );   Address(0x33c[2:0],)
SPIWrite 033c,1c,0,7    //CoarseStep=0x3;(Meaning: );   Address(0x33c[6:3],)
SPIWrite 04f9,00,0,7    //AttnCodeDelay=0x2;    Address(0x4f8[13:0],)
SPIWrite 04f8,02,0,7
SPIWrite 04f1,01,0,7    //UseMinAttnFromAgc=0x1;(Meaning: );    Address(0x4f0[8:8],)
SPIWrite 033d,00,0,7    //CoarseIndexSwapIandQ=0x0;(Meaning: );     Address(0x33c[9:9],)
SPIWrite 033d,00,0,7    //CoarseIndexInvert=0x0;(Meaning: );    Address(0x33c[8:8],)

\\END: Done configuring DGC


\\START: Configuring Small Step Attack Detector

SPIWrite 0209,01,0,7    //small_step_attack_step_size=0x1;  Address(0x208[13:8],)
SPIWrite 0239,0b,0,7    //small_step_attack_sig_th_high=0xb53;  Address(0x238[11:0],)
SPIWrite 0238,53,0,7
SPIWrite 023b,0b,0,7    //small_step_attack_sig_th_low=0xb53;   Address(0x238[27:16],)
SPIWrite 023a,53,0,7
SPIWrite 021a,00,0,7    //small_step_attack_win_len=0x80;   Address(0x218[23:0],)
SPIWrite 0219,00,0,7
SPIWrite 0218,80,0,7
SPIWrite 024e,00,0,7    //small_step_attack_num_hits=0x8;   Address(0x24c[23:0],)
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SPIWrite 024d,00,0,7
SPIWrite 024c,08,0,7
SPIWrite 0200,4a,0,7    //small_step_attack_en=0x1;(Meaning: );     Address(0x200[1:1],)
SPIWrite 0204,0a,0,7    //small_step_attack_det_en=0x1;(Meaning: );     Address(0x204[1:1],)

\\END: Done configuring Small Step Attack Detector


\\START: Configuring Small Step Decay Detector

SPIWrite 020b,01,0,7    //small_step_decay_step_size=0x1;   Address(0x208[29:24],)
SPIWrite 0241,05,0,7    //small_step_decay_sig_th_high=0x50f;   Address(0x240[11:0],)
SPIWrite 0240,0f,0,7
SPIWrite 0243,05,0,7    //small_step_decay_sig_th_low=0x50f;    Address(0x240[27:16],)
SPIWrite 0242,0f,0,7
SPIWrite 0222,02,0,7    //small_step_decay_win_len=0x20000;     Address(0x220[23:0],)
SPIWrite 0221,00,0,7
SPIWrite 0220,00,0,7
SPIWrite 0256,00,0,7    //small_step_decay_num_hits=0x8;    Address(0x254[23:0],)
SPIWrite 0255,00,0,7
SPIWrite 0254,08,0,7
SPIWrite 0200,4a,0,7    //small_step_decay_en=0x1;(Meaning: );  Address(0x200[3:3],)
SPIWrite 0204,0a,0,7    //small_step_decay_det_en=0x1;(Meaning: );  Address(0x204[3:3],)

\\END: Done configuring Small Step Decay Detector


\\START: Configuring Big Step Attack Detector

SPIWrite 0235,0e,0,7    //big_step_attack_sig_th_high=0xe42;    Address(0x234[11:0],)
SPIWrite 0234,42,0,7
SPIWrite 0237,0e,0,7    //big_step_attack_sig_th_low=0xe42;     Address(0x234[27:16],)
SPIWrite 0236,42,0,7
SPIWrite 0216,00,0,7    //big_step_attack_win_len=0x20;     Address(0x214[23:0],)
SPIWrite 0215,00,0,7
SPIWrite 0214,20,0,7
SPIWrite 024a,00,0,7    //big_step_attack_num_hits=0x8;     Address(0x248[23:0],)
SPIWrite 0249,00,0,7
SPIWrite 0248,08,0,7
SPIWrite 0208,03,0,7    //big_step_attack_step_size=0x3;    Address(0x208[5:0],)
SPIWrite 0200,4a,0,7    //big_step_attack_en=0x0;(Meaning: );   Address(0x200[0:0],)
SPIWrite 0204,0a,0,7    //big_step_attack_det_en=0x0;(Meaning: );   Address(0x204[0:0],)

\\END: Done configuring Big Step Attack Detector


\\START: Configuring Big Step Decay Detector

SPIWrite 0cd7,20,0,7    //big_step_decay_syncmode=0x0;  Address(0xcd4[26:26],)
SPIWrite 020a,03,0,7    //big_step_decay_step_size=0x3;     Address(0x208[21:16],)
SPIWrite 023d,04,0,7    //big_step_decay_sig_th_high=0x404;     Address(0x23c[11:0],)
SPIWrite 023c,04,0,7
SPIWrite 023f,04,0,7    //big_step_decay_sig_th_low=0x404;  Address(0x23c[27:16],)
SPIWrite 023e,04,0,7
SPIWrite 021e,00,0,7    //big_step_decay_win_len=0x8000;    Address(0x21c[23:0],)
SPIWrite 021d,80,0,7
SPIWrite 021c,00,0,7
SPIWrite 0252,00,0,7    //big_step_decay_num_hits=0x8;  Address(0x250[23:0],)
SPIWrite 0251,00,0,7
SPIWrite 0250,08,0,7
SPIWrite 0200,4a,0,7    //big_step_decay_en=0x0;(Meaning: );    Address(0x200[2:2],)
SPIWrite 0204,0a,0,7    //big_step_decay_det_en=0x0;(Meaning: );    Address(0x204[2:2],)

\\END: Done configuring Big Step Decay Detector

SPIWrite 0279,00,0,7    //pin_1_select_bits=0x0;    Address(0x278[15:0],)
SPIWrite 0278,00,0,7
SPIWrite 027b,00,0,7    //pin_2_select_bits=0x0;    Address(0x278[31:16],)
SPIWrite 027a,00,0,7
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SPIWrite 027d,00,0,7    //pin_3_select_bits=0x0;    Address(0x27c[15:0],)
SPIWrite 027c,00,0,7
SPIWrite 027f,00,0,7    //pin_4_select_bits=0x0;    Address(0x27c[31:16],)
SPIWrite 027e,00,0,7
SPIWrite 08cd,00,0,7    //blank_time_rf_det=0x64;   Address(0x8cc[15:0],)
SPIWrite 08cc,64,0,7
SPIWrite 08cf,01,0,7    //blank_time=0x1f4;     Address(0x8cc[31:16],)
SPIWrite 08ce,f4,0,7
SPIWrite 0675,03,0,7    //blank_time_for_ext_comp_change=0x3e8;     Address(0x674[15:0],)
SPIWrite 0674,e8,0,7
SPIWrite 0ed1,02,0,7    //disable_hysterisis=0x1;(Meaning: );   Address(0xed0[9:9],)
SPIWrite 0ed1,02,0,7    //dig_gain_dis=0x0;     Address(0xed0[8:8],)
SPIWrite 0ed1,02,0,7    //dig_gain_dis=0x0;     Address(0xed0[8:8],)
SPIWrite 0a81,b3,0,7    //gain_comp_stg_2_3_dec_chain=0xb3;     Address(0xa80[15:8],)

\\START: Configuring DGC

SPIWrite 0734,07,0,7    //DgcEnRxMode=0x1;(Meaning: );  Address(0x734[0:0],)
SPIWrite 0737,00,0,7    //FltPtMode=0x0;    Address(0x734[24:24],)
SPIWrite 0737,00,0,7    //FltPtFmt=0x0;(Meaning: );     Address(0x734[26:25],)
SPIWrite 0735,1b,0,7    //DgcMode=0x3;(Meaning: );  Address(0x734[10:8],)
SPIWrite 073c,24,0,7    //NBitsCoarseIdx=0x4;(Meaning: );   Address(0x73c[2:0],)
SPIWrite 073c,1c,0,7    //CoarseStep=0x3;(Meaning: );   Address(0x73c[6:3],)
SPIWrite 08f9,00,0,7    //AttnCodeDelay=0x2;    Address(0x8f8[13:0],)
SPIWrite 08f8,02,0,7
SPIWrite 08f1,01,0,7    //UseMinAttnFromAgc=0x1;(Meaning: );    Address(0x8f0[8:8],)
SPIWrite 073d,00,0,7    //CoarseIndexSwapIandQ=0x0;(Meaning: );     Address(0x73c[9:9],)
SPIWrite 073d,00,0,7    //CoarseIndexInvert=0x0;(Meaning: );    Address(0x73c[8:8],)

\\END: Done configuring DGC


\\START: Configuring Small Step Attack Detector

SPIWrite 0609,01,0,7    //small_step_attack_step_size=0x1;  Address(0x608[13:8],)
SPIWrite 0639,0b,0,7    //small_step_attack_sig_th_high=0xb53;  Address(0x638[11:0],)
SPIWrite 0638,53,0,7
SPIWrite 063b,0b,0,7    //small_step_attack_sig_th_low=0xb53;   Address(0x638[27:16],)
SPIWrite 063a,53,0,7
SPIWrite 061a,00,0,7    //small_step_attack_win_len=0x80;   Address(0x618[23:0],)
SPIWrite 0619,00,0,7
SPIWrite 0618,80,0,7
SPIWrite 064e,00,0,7    //small_step_attack_num_hits=0x8;   Address(0x64c[23:0],)
SPIWrite 064d,00,0,7
SPIWrite 064c,08,0,7
SPIWrite 0600,4a,0,7    //small_step_attack_en=0x1;(Meaning: );     Address(0x600[1:1],)
SPIWrite 0604,0a,0,7    //small_step_attack_det_en=0x1;(Meaning: );     Address(0x604[1:1],)

\\END: Done configuring Small Step Attack Detector


\\START: Configuring Small Step Decay Detector

SPIWrite 060b,01,0,7    //small_step_decay_step_size=0x1;   Address(0x608[29:24],)
SPIWrite 0641,05,0,7    //small_step_decay_sig_th_high=0x50f;   Address(0x640[11:0],)
SPIWrite 0640,0f,0,7
SPIWrite 0643,05,0,7    //small_step_decay_sig_th_low=0x50f;    Address(0x640[27:16],)
SPIWrite 0642,0f,0,7
SPIWrite 0622,02,0,7    //small_step_decay_win_len=0x20000;     Address(0x620[23:0],)
SPIWrite 0621,00,0,7
SPIWrite 0620,00,0,7
SPIWrite 0656,00,0,7    //small_step_decay_num_hits=0x8;    Address(0x654[23:0],)
SPIWrite 0655,00,0,7
SPIWrite 0654,08,0,7
SPIWrite 0600,4a,0,7    //small_step_decay_en=0x1;(Meaning: );  Address(0x600[3:3],)
SPIWrite 0604,0a,0,7    //small_step_decay_det_en=0x1;(Meaning: );  Address(0x604[3:3],)

\\END: Done configuring Small Step Decay Detector
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\\START: Configuring Big Step Attack Detector

SPIWrite 0635,0e,0,7    //big_step_attack_sig_th_high=0xe42;    Address(0x634[11:0],)
SPIWrite 0634,42,0,7
SPIWrite 0637,0e,0,7    //big_step_attack_sig_th_low=0xe42;     Address(0x634[27:16],)
SPIWrite 0636,42,0,7
SPIWrite 0616,00,0,7    //big_step_attack_win_len=0x20;     Address(0x614[23:0],)
SPIWrite 0615,00,0,7
SPIWrite 0614,20,0,7
SPIWrite 064a,00,0,7    //big_step_attack_num_hits=0x8;     Address(0x648[23:0],)
SPIWrite 0649,00,0,7
SPIWrite 0648,08,0,7
SPIWrite 0608,03,0,7    //big_step_attack_step_size=0x3;    Address(0x608[5:0],)
SPIWrite 0600,4a,0,7    //big_step_attack_en=0x0;(Meaning: );   Address(0x600[0:0],)
SPIWrite 0604,0a,0,7    //big_step_attack_det_en=0x0;(Meaning: );   Address(0x604[0:0],)

\\END: Done configuring Big Step Attack Detector


\\START: Configuring Big Step Decay Detector

SPIWrite 0ed7,20,0,7    //big_step_decay_syncmode=0x0;  Address(0xed4[26:26],)
SPIWrite 060a,03,0,7    //big_step_decay_step_size=0x3;     Address(0x608[21:16],)
SPIWrite 063d,04,0,7    //big_step_decay_sig_th_high=0x404;     Address(0x63c[11:0],)
SPIWrite 063c,04,0,7
SPIWrite 063f,04,0,7    //big_step_decay_sig_th_low=0x404;  Address(0x63c[27:16],)
SPIWrite 063e,04,0,7
SPIWrite 061e,00,0,7    //big_step_decay_win_len=0x8000;    Address(0x61c[23:0],)
SPIWrite 061d,80,0,7
SPIWrite 061c,00,0,7
SPIWrite 0652,00,0,7    //big_step_decay_num_hits=0x8;  Address(0x650[23:0],)
SPIWrite 0651,00,0,7
SPIWrite 0650,08,0,7
SPIWrite 0600,4a,0,7    //big_step_decay_en=0x0;(Meaning: );    Address(0x600[2:2],)
SPIWrite 0604,0a,0,7    //big_step_decay_det_en=0x0;(Meaning: );    Address(0x604[2:2],)

\\END: Done configuring Big Step Decay Detector

SPIWrite 0679,00,0,7    //pin_1_select_bits=0x0;    Address(0x678[15:0],)
SPIWrite 0678,00,0,7
SPIWrite 067b,00,0,7    //pin_2_select_bits=0x0;    Address(0x678[31:16],)
SPIWrite 067a,00,0,7
SPIWrite 067d,00,0,7    //pin_3_select_bits=0x0;    Address(0x67c[15:0],)
SPIWrite 067c,00,0,7
SPIWrite 067f,00,0,7    //pin_4_select_bits=0x0;    Address(0x67c[31:16],)
SPIWrite 067e,00,0,7

\\START: Enabling or disabling Internal AGC

SPIWrite 0264,00,0,7    //ext_agc_mode=0x0;     Address(0x264[1:1],)
SPIWrite 0264,00,0,7    //internal_agc_en=0x0;(Meaning: );  Address(0x264[0:0],)
SPIWrite 0264,01,0,7    //internal_agc_en=0x1;(Meaning: );  Address(0x264[0:0],)

\\END: DOne enabling or disabling Internal AGC


\\START: Enabling or disabling Internal AGC

SPIWrite 0664,00,0,7    //ext_agc_mode=0x0;     Address(0x664[1:1],)
SPIWrite 0664,00,0,7    //internal_agc_en=0x0;(Meaning: );  Address(0x664[0:0],)
SPIWrite 0664,01,0,7    //internal_agc_en=0x1;(Meaning: );  Address(0x664[0:0],)

\\END: DOne enabling or disabling Internal AGC

SPIWrite 0010,00,0,7    //PAGE: rx_top=0x0;     Address(0x10[3:2],)
SPIWrite 0016,30,0,7    //PAGE: dsa=0x3;    Address(0x16[5:4],)
SPIWrite 0040,02,0,7
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\\END: Completed AGC Config

SPIWrite 0016,00,0,7    //PAGE: dsa=0x0;    Address(0x16[5:4],)
\\ STEP: attnSet/step0

\\START: Setting TX DSA Attenuation

SPIWrite 0016,30,0,7    //PAGE: dsa=0x3;    Address(0x16[5:4],)
SPIWrite 0100,01,0,7
SPIWrite 0102,00,0,7
SPIWrite 0102,01,0,7
SPIWrite 0102,00,0,7

\\END: Done setting TX DSA Attenuation


\\START: Setting TX DSA Attenuation

SPIWrite 0120,01,0,7
SPIWrite 0122,00,0,7
SPIWrite 0122,01,0,7
SPIWrite 0122,00,0,7

\\END: Done setting TX DSA Attenuation


\\START: Setting TX DSA Attenuation

SPIWrite 0100,27,0,7
SPIWrite 0102,00,0,7
SPIWrite 0102,01,0,7
SPIWrite 0102,00,0,7

\\END: Done setting TX DSA Attenuation

SPIWrite 0050,00,0,7

\\START: Setting TX DSA Attenuation

SPIWrite 0120,27,0,7
SPIWrite 0122,00,0,7
SPIWrite 0122,01,0,7
SPIWrite 0122,00,0,7

\\END: Done setting TX DSA Attenuation

SPIWrite 00b0,00,0,7
SPIWrite 0150,03,0,7

\\START: Setting TX DSA Attenuation

SPIWrite 0100,27,0,7
SPIWrite 0102,00,0,7
SPIWrite 0102,01,0,7
SPIWrite 0102,00,0,7

\\END: Done setting TX DSA Attenuation

SPIWrite 0050,00,0,7

\\START: Setting TX DSA Attenuation

SPIWrite 0120,27,0,7
SPIWrite 0122,00,0,7
SPIWrite 0122,01,0,7
SPIWrite 0122,00,0,7

\\END: Done setting TX DSA Attenuation
```

```
SPIWrite 00b0,00,0,7
SPIWrite 0150,03,0,7
SPIWrite 0016,00,0,7    //PAGE: dsa=0x0;    Address(0x16[5:4],)
\\ STEP: dacJesdLinkUp/step0

\\START: Clearing All Alarms

SPIWrite 001a,ff,0,7    //alarms_clear=0x1ff;   Address(0x1a[7:0],0x1b[0:0],)
SPIWrite 001b,01,0,7
SPIWrite 001a,00,0,7    //alarms_clear=0x0;     Address(0x1a[7:0],0x1b[0:0],)
SPIWrite 001b,00,0,7
SPIWrite 0013,20,0,7    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIWrite 02e5,20,0,7
SPIWrite 02e5,00,0,7

\\START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0013,00,0,7    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 01d4,01,0,7    //pll_reg_spi_req_a=0x1;    Address(0x1d4[0:0],)
SPIWrite 0374,00,0,7    //pll_reg_spi_req_b1=0x0;(Meaning: );   Address(0x374[0:0],)

SPIPoll 01d5,0,0,1


\\Read  pll_reg_spi_a_ack=0x1;  Address(0x1d4[8:8],)


\\END: Done requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0014,f8,0,7    //PAGE: pll=0x1f;   Address(0x14[7:3],)
SPIWrite 0066,0b,0,7    //lock_lost_rst=0x1;    Address(0x64[19:19],)
SPIWrite 0066,03,0,7    //lock_lost_rst=0x0;    Address(0x64[19:19],)

\\START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0014,00,0,7    //PAGE: pll=0x0;    Address(0x14[7:3],)
SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 01d4,00,0,7    //pll_reg_spi_req_a=0x0;    Address(0x1d4[0:0],)
SPIWrite 0374,00,0,7    //pll_reg_spi_req_b1=0x0;(Meaning: );   Address(0x374[0:0],)

WAIT 0.01


\\END: Done requesting/releasing SPI Access to PLL Pages

SPIWrite 064a,0f,0,7    //pap_alarm_clear=0xf;  Address(0x648[19:16],)
SPIWrite 064a,00,0,7    //pap_alarm_clear=0x0;  Address(0x648[19:16],)

\\END: Done clearing All Alarms

SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
\\ STEP: dacJesdLinkUp/step1
SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,4a,0,7
SPIWrite 0193,31,0,7

\\Read  macro_opcode_operand=0x31000000;    Address(0x190[31:0],)
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SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0x20[4:4],)


\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0x20[5:5],)


\\Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0x20[6:6],)


\\Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0x20[7:7],)


\\Read  MACRO_READY=0x1;    Address(0x20[0:0],)


\\Read  MACRO_ACK=0x1;  Address(0x20[1:1],)


\\Read  MACRO_DONE=0x1;     Address(0x20[2:2],)

SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\START: Enabling RX IQMC Correction

SPIWrite 0013,00,5,5    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,02,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,00,0,7
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,0f,0,7
SPIWrite 0193,38,0,7

\\Read  macro_opcode_operand=0x38000000;    Address(0x190[31:0],)


SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)
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\\Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0x20[4:4],)

\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0x20[5:5],)

\\Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0x20[6:6],)

\\Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0x20[7:7],)

\\Read  MACRO_READY=0x1;    Address(0x20[0:0],)

\\Read  MACRO_ACK=0x1;  Address(0x20[1:1],)

\\Read  MACRO_DONE=0x1;     Address(0x20[2:2],)

SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


WAIT 0.5

SPIWrite 0013,00,5,5    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)
SPIWrite 0010,0c,2,3    //PAGE: rx_top=0x3;     Address(0x10[3:2],)
SPIWrite 0501,00,0,0    //bypass_mode=0x0;(Meaning: );  Address(0x500[8:8],)
SPIWrite 0901,00,0,0    //bypass_mode=0x0;(Meaning: );  Address(0x900[8:8],)
SPIWrite 0500,00,0,0    //bypass_mode=0x0;(Meaning: );  Address(0x500[0:0],)
SPIWrite 0900,00,0,0    //bypass_mode=0x0;(Meaning: );  Address(0x900[0:0],)

\\END: Done enabling RX IQMC Correction


\\START: Disabling TDD overrides

SPIWrite 0010,00,0,7    //PAGE: rx_top=0x0;     Address(0x10[3:2],)
SPIWrite 0014,04,0,7    //PAGE: TIMING_CON=0x1;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0124,00,0,7    //use_reg_txon_AB=0x0;  Address(0x124[0:0],)
SPIWrite 0126,00,0,7    //use_reg_rxon_AB=0x0;  Address(0x124[16:16],)
SPIWrite 0128,00,0,7    //use_reg_fbon_AB=0x0;  Address(0x128[0:0],)
SPIWrite 012a,00,0,7    //use_reg_txon_CD=0x0;  Address(0x128[16:16],)
SPIWrite 012c,00,0,7    //use_reg_rxon_CD=0x0;  Address(0x12c[0:0],)
SPIWrite 012e,00,0,7    //use_reg_fbon_CD=0x0;  Address(0x12c[16:16],)

\\END: Done disabling TDD overrides

SPIWrite 0014,00,0,7    //PAGE: TIMING_CON=0x0;(Meaning: );     Address(0x14[2:2],)
SPIWrite 0015,02,0,7    //PAGE: tx_jesd=0x3;    Address(0x15[1:1],0x15[5:5],)
SPIWrite 0015,22,0,7
SPIWrite 0173,cc,0,7    //alarms_mask=0x15151515cccc0fff;   Address(0x170[31:0],0x174[31:0],)
SPIWrite 0172,cc,0,7
SPIWrite 0171,0f,0,7
SPIWrite 0170,ff,0,7
SPIWrite 0177,15,0,7
SPIWrite 0176,15,0,7
SPIWrite 0175,15,0,7
SPIWrite 0174,15,0,7
SPIWrite 017b,cc,0,7    //alarms_to_pap_mask=0x15151515cccc0fff;
Address(0x178[31:0],0x17c[31:0],)
SPIWrite 017a,cc,0,7
SPIWrite 0179,0f,0,7
SPIWrite 0178,ff,0,7
SPIWrite 017f,15,0,7
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SPIWrite 017e,15,0,7
SPIWrite 017d,15,0,7
SPIWrite 017c,15,0,7
SPIWrite 0015,20,0,7    //PAGE: tx_jesd=0x0;    Address(0x15[1:1],0x15[5:5],)
SPIWrite 0015,00,0,7
SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 064a,f0,0,7    //misc_spi_spare_14=0xf;    Address(0x648[23:20],)
SPIWrite 064a,00,0,7    //misc_spi_spare_14=0x0;    Address(0x648[23:20],)

\\START: Configuring Interrupt Pins

SPIWrite 0119,0f,0,7    //alarm_mask_lsb_for_alarm0=0xf01;  Address(0x118[15:0],)
SPIWrite 0118,01,0,7
SPIWrite 011b,00,0,7    //alarm_mask_msb_for_alarm0=0x0;    Address(0x118[31:16],)
SPIWrite 011a,00,0,7
SPIWrite 011d,00,0,7    //alarm_mask_lsb_for_alarm1=0x20;   Address(0x11c[15:0],)
SPIWrite 011c,20,0,7
SPIWrite 011f,00,0,7    //alarm_mask_msb_for_alarm1=0x0;    Address(0x11c[31:16],)
SPIWrite 011e,00,0,7

\\END: Done configuring Interrupt Pins


\\START: Putting the System to Sleep/Waking it up

SPIWrite 0914,00,0,7    //mask_pdn_high_intr=0x0;   Address(0x914[0:0],)
SPIWrite 0918,00,0,7    //mask_pdn_fall_intr=0x0;   Address(0x918[0:0],)
SPIWrite 0015,00,7,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0013,10,4,4    //PAGE: customer_macro=0x1;(Meaning: );     Address(0x13[4:4],)

SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7
SPIWrite 00a2,08,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,ff,0,7
SPIWrite 0193,39,0,7

SPIPoll 00f0,0,7,7


SPIPoll 00f0,0,0,1

SPIWrite 0193,3a,0,7

SPIPoll 00f0,0,7,7

SPIWrite 0013,00,4,4    //PAGE: customer_macro=0x0;(Meaning: );     Address(0x13[4:4],)
SPIWrite 0013,20,5,5    //PAGE: cm4_macro=0x1;  Address(0x13[5:5],)
SPIReadCheck 0020,3,3,00

\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR=0x0;    Address(0x20[3:3],)


\\Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0x20[4:4],)


\\Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0x20[5:5],)


\\Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0x20[6:6],)


\\Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0x20[7:7],)
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\\END: Done putting the System to Sleep/Waking it up

SPIWrite 0013,00,0,7    //PAGE: cm4_macro=0x0;  Address(0x13[5:5],)

\\END: Device Config Complete

SPIWrite 0010,04,0,7    //PAGE: rx_top=0x1;     Address(0x10[3:2],)
SPIWrite 033d,02,0,7    //CoarseIndexSwapIandQ=0x1;(Meaning: );     Address(0x33c[9:9],)
SPIWrite 073d,02,0,7    //CoarseIndexSwapIandQ=0x1;(Meaning: );     Address(0x73c[9:9],)
SPIWrite 04f9,00,0,7    //AttnCodeDelay=0x6;    Address(0x4f8[13:0],)
SPIWrite 04f8,06,0,7
SPIWrite 08f9,00,0,7    //AttnCodeDelay=0x6;    Address(0x8f8[13:0],)
SPIWrite 08f8,06,0,7
SPIWrite 033e,04,0,7    //FineOffset=0x4;   Address(0x33c[18:16],)
SPIWrite 073e,04,0,7    //FineOffset=0x4;   Address(0x73c[18:16],)
SPIWrite 0010,08,0,7    //PAGE: rx_top=0x2;     Address(0x10[3:2],)
SPIWrite 033d,02,0,7    //CoarseIndexSwapIandQ=0x1;(Meaning: );     Address(0x33c[9:9],)
SPIWrite 073d,02,0,7    //CoarseIndexSwapIandQ=0x1;(Meaning: );     Address(0x73c[9:9],)
SPIWrite 04f9,00,0,7    //AttnCodeDelay=0x6;    Address(0x4f8[13:0],)
SPIWrite 04f8,06,0,7
SPIWrite 08f9,00,0,7    //AttnCodeDelay=0x6;    Address(0x8f8[13:0],)
SPIWrite 08f8,06,0,7
SPIWrite 033e,04,0,7    //FineOffset=0x4;   Address(0x33c[18:16],)
SPIWrite 073e,04,0,7    //FineOffset=0x4;   Address(0x73c[18:16],)
SPIWrite 0010,00,0,7    //PAGE: rx_top=0x0;     Address(0x10[3:2],)
SPIWrite 0015,80,0,7    //PAGE: DIGTOP_MISC=0x1;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0278,03,0,7    //pull_ctrl_gpio_30=0x3;    Address(0x278[2:0],)
SPIWrite 0015,00,0,7    //PAGE: DIGTOP_MISC=0x0;(Meaning: );    Address(0x15[7:7],)
SPIWrite 0015,08,0,7    //PAGE: jesd_subchip=0x1;(Meaning: );   Address(0x15[3:3],)
SPIWrite 0056,04,0,7
SPIWrite 0015,00,0,7    //PAGE: jesd_subchip=0x0;(Meaning: );   Address(0x15[3:3],)

\\Device Bringup is Completed
```