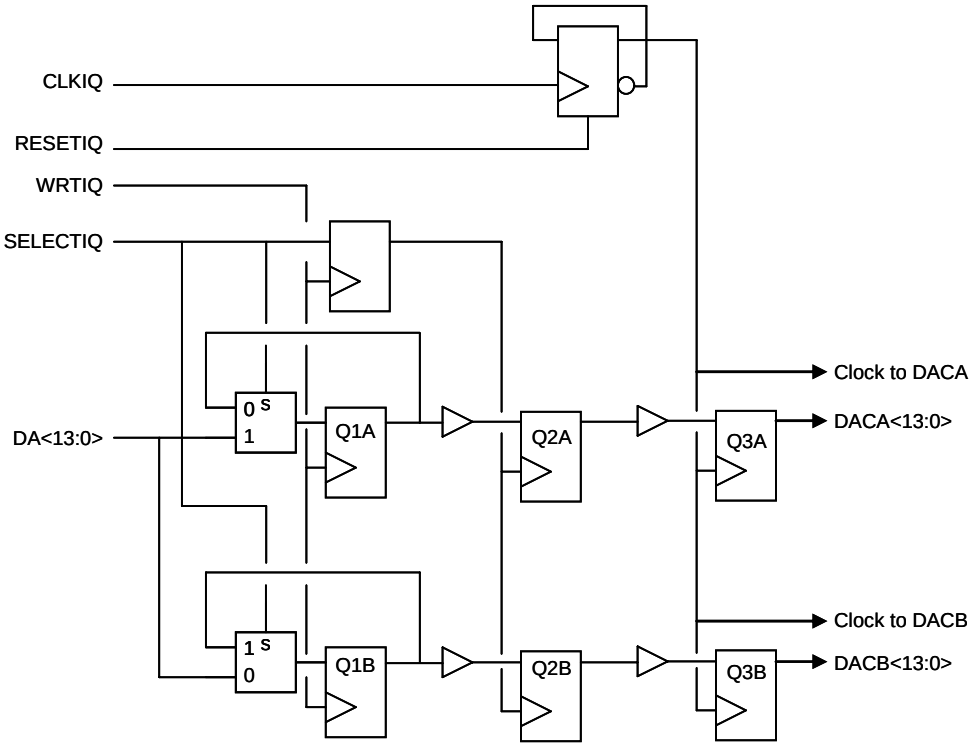
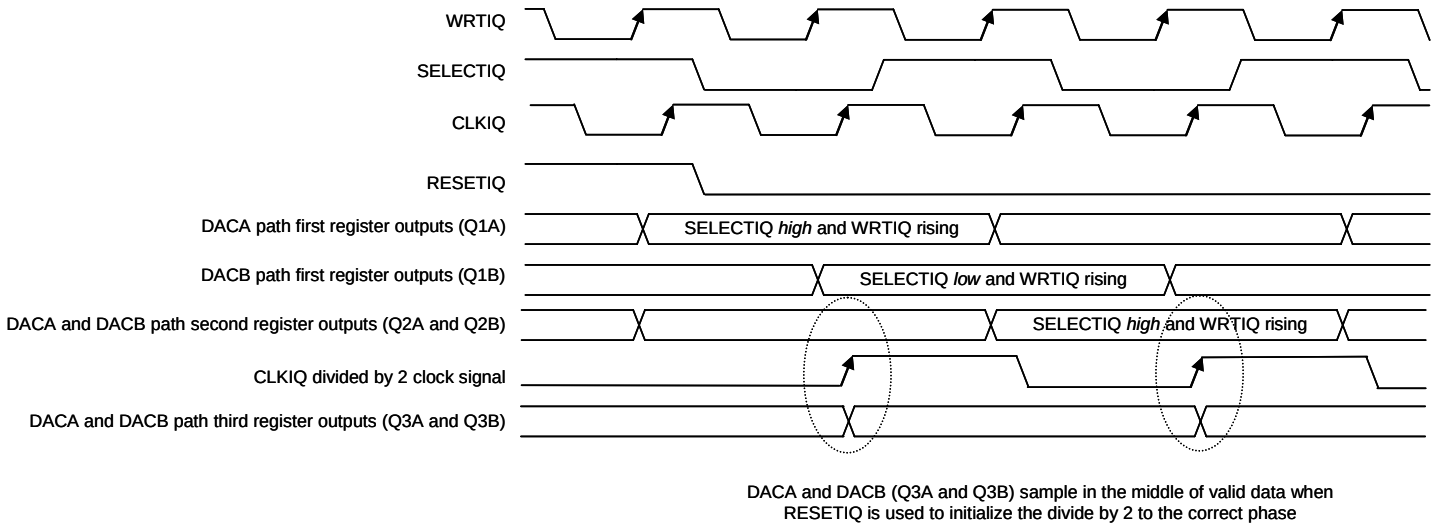
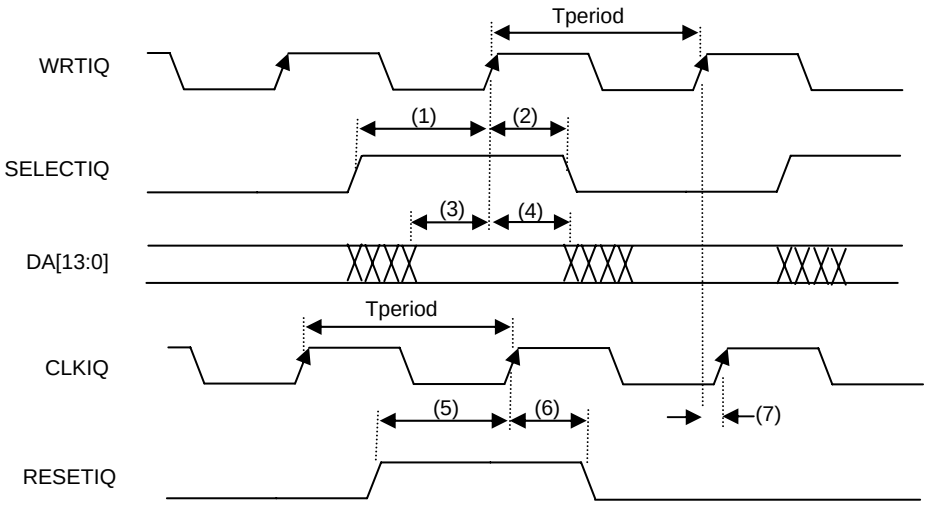
The DAC56X2 family datasheets do not include guaranteed timing numbers for interleaved input data mode. This document describes the internal operation and requirements for interleaved interface mode.



Interleaved Mode Simplified Schematic



Functional Timing Diagram



Interleaved Mode Timing Diagram

Timing no.	Description	Min	Max	Units
(1)	Setup Time: SELECTIQ rising or falling edge to WRTIQ rising edge	2.5		ns
(2)	Hold Time: SELECTIQ rising or falling edge to WRTIQ rising edge	1		ns
(3)	Setup Time: DA[13:0] rising or falling edge to WRTIQ rising edge	1		ns
(4)	Hold Time: DA[13:0] rising or falling edge to WRTIQ rising edge	1		ns
(5)	Setup Time: RESETIQ rising or falling edge to CLKIQ rising edge	1		ns
(6)	Hold Time: RESETIQ rising or falling edge to CLKIQ rising edge	1		ns
(7)	*If RESETIQ is used to initialize the internal CLKIQ divider to the correct phase, CLKIQ and WRTIQ can be connected together.* *If RESETIQ is not used to initialize the internal CLKIQ divider to the correct phase, the system must be designed with enough skew between WRTIQ and CLKIQ (more than 1nS between rising edges) to guarantee successful transfer of data between these two clock zones.*			