12-Bit, Voltage Output
DIGITAL-TO-ANALOG CONVERTER

FEATURES
- LOW POWER: 1.8mW
- UNIPOLAR OR BIPOLAR OPERATION
- SETTLING TIME: 10µs to 0.012%
- 12-BIT LINEARITY AND MONOTONICITY: 
  -40°C to +85°C
- DATA READBACK
- DOUBLE-BUFFERED DATA INPUTS
- 24-LEAD SSOP PACKAGE

APPLICATIONS
- PROCESS CONTROL
- CLOSED-LOOP SERVO-CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS

DESCRIPTION
The DAC7613 is a 12-bit, voltage output digital-to-analog converter with guaranteed 12-bit monotonic performance over the specified temperature range. The DAC7613 accepts a 12-bit parallel input data, has double-buffered DAC input logic and provides a readback mode of the internal input register. An asynchronous reset clears all registers to a mid-scale code of 800_H or to a zero-scale of 000_H. The DAC7613 can operate from a single +5V supply or from +5V and –5V supplies.

Low power and small size makes the DAC7613 ideal for data acquisition systems and closed-loop servo-control. The DAC7613 is available in a plastic SSOP-24 package, and offers guaranteed specifications over the –40°C to +85°C temperature range.
**SPECIFICATION**

At $T_A = -40°C$ to $+85°C$, $V_{DD} = +5V$, $V_{SS} = -5V$, $V_{REFH} = +2.5V$, and $V_{REFL} = -2.5V$, unless otherwise noted.

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<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>DAC7613E</th>
<th>DAC7613EB</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ACCURACY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Linearity Error (1)</td>
<td>$V_{SS} = 0V$ or $-5V$</td>
<td>$\pm 2$</td>
<td>$\pm 1$</td>
<td>LSB(2)</td>
</tr>
<tr>
<td>Differential Linearity Error</td>
<td>$V_{SS} = 0V$ or $-5V$</td>
<td>$\pm 1$</td>
<td>$\pm 1$</td>
<td>LSB</td>
</tr>
<tr>
<td>Monotonicity</td>
<td>$T_{MIN}$ to $T_{MAX}$</td>
<td>12</td>
<td>*</td>
<td>Bits</td>
</tr>
<tr>
<td>Zero-Scale Error</td>
<td>Code = 000$H$</td>
<td>$\pm 4$</td>
<td>*</td>
<td>LSB</td>
</tr>
<tr>
<td>Zero-Scale Drift</td>
<td></td>
<td>2</td>
<td>5</td>
<td>ppm/$^°C$</td>
</tr>
<tr>
<td>Full-Scale Error</td>
<td>Code = FFF$H$</td>
<td>$\pm 4$</td>
<td>*</td>
<td>LS</td>
</tr>
<tr>
<td>Zero-Scale Error</td>
<td>Code = 00A$H$, $V_{SS} = 0V$</td>
<td>$\pm 8$</td>
<td>*</td>
<td>LSB</td>
</tr>
<tr>
<td>Zero-Scale Drift</td>
<td>$V_{SS} = 0V$</td>
<td>5</td>
<td>10</td>
<td>ppm/$^°C$</td>
</tr>
<tr>
<td>Full-Scale Error</td>
<td>Code = FFF$H$, $V_{SS} = 0V$</td>
<td>$\pm 8$</td>
<td>*</td>
<td>LSB</td>
</tr>
<tr>
<td>Power Supply Rejection</td>
<td></td>
<td>30</td>
<td>*</td>
<td>ppm/$V$</td>
</tr>
<tr>
<td><strong>ANALOG OUTPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage Output (3)</td>
<td>$V_{REFL} = 0V$, $V_{SS} = 0V$</td>
<td>0</td>
<td>$V_{REFH}$</td>
<td>*</td>
</tr>
<tr>
<td>Output Current</td>
<td>$V_{SS} = -5V$</td>
<td>$V_{REFL}$</td>
<td>$V_{REFH}$</td>
<td>*</td>
</tr>
<tr>
<td>Load Capacitance</td>
<td>No Oscillation</td>
<td>100</td>
<td>*</td>
<td>pF</td>
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<tr>
<td>Short-Circuit Current</td>
<td>+5, –15</td>
<td>*</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Short-Circuit Duration</td>
<td>Indefinite</td>
<td>*</td>
<td></td>
<td></td>
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<tr>
<td><strong>REFERENCE INPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{REFH}$ Input Range</td>
<td>$V_{SS} = 0V$ or $-5V$</td>
<td>$V_{REFL}$</td>
<td>$+2.5$</td>
<td>*</td>
</tr>
<tr>
<td>$V_{REFL}$ Input Range</td>
<td>$V_{SS} = 0V$</td>
<td>0</td>
<td>$V_{REFH}$</td>
<td>*</td>
</tr>
<tr>
<td>$V_{REFL}$ Input Range</td>
<td>$V_{SS} = -5V$</td>
<td>$-2.5$</td>
<td>$V_{REFH}$</td>
<td>*</td>
</tr>
<tr>
<td><strong>DYNAMIC PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Settling Time (4)</td>
<td>To $\pm 0.012%$</td>
<td>5</td>
<td>10</td>
<td>*</td>
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<tr>
<td>Output Noise Voltage</td>
<td>0Hz to 1MHz</td>
<td>40</td>
<td>*</td>
<td>$nV/\sqrt{Hz}$</td>
</tr>
<tr>
<td><strong>DIGITAL INPUT/OUTPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic Family</td>
<td>CMOS</td>
<td>*</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic Levels</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>$I_{IH} \leq \pm 10\mu A$</td>
<td>0.7 $V_{DD}$</td>
<td>$V_{DD} + 0.3$</td>
<td>*</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>$I_{IL} \leq \pm 10\mu A$</td>
<td>$-0.3$</td>
<td>$0.3 V_{DD}$</td>
<td>*</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>$I_{OH} = -0.8mA$</td>
<td>3.6</td>
<td>$V_{DD}$</td>
<td>*</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>$I_{OL} = 1.6mA$</td>
<td>0.0</td>
<td>0.4</td>
<td>*</td>
</tr>
<tr>
<td>Data Format</td>
<td>Straight Binary</td>
<td>*</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>POWER SUPPLY REQUIREMENTS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>If $V_{SS} = 0V$</td>
<td>4.75</td>
<td>5.25</td>
<td>*</td>
</tr>
<tr>
<td>$V_{SS}$</td>
<td>$-5.25$</td>
<td>$-4.75$</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>$0.35$</td>
<td>0.5</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>$I_{SS}$</td>
<td>$-0.65$</td>
<td>$-0.45$</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>$V_{SS} = -5V$</td>
<td>4</td>
<td>5.75</td>
<td>*</td>
</tr>
<tr>
<td>$V_{SS} = 0V$</td>
<td>1.8</td>
<td>2.5</td>
<td>*</td>
<td>*</td>
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<tr>
<td><strong>TEMPERATURE RANGE</strong></td>
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<td></td>
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<tr>
<td>Specified Performance</td>
<td>$-40$</td>
<td>$+85$</td>
<td>*</td>
<td>*</td>
</tr>
</tbody>
</table>

Notes: (1) If $V_{SS} = 0V$, specification applies at code 00A$H$ and above. (2) LSB means Least Significant Bit, when $V_{REFH} = 2.5V$ and $V_{REFL} = -2.5V$, then one LSB equals 1.22mV. (3) Ideal output voltage, does not take into account zero or full-scale error. (4) If $V_{SS} = -5V$, full-scale 5V step. If $V_{SS} = 0V$, full-scale positive 2.5V step and negative step from code FFF$H$ to 00A$H$. 

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ABSOLUTE MAXIMUM RATINGS(1)

<table>
<thead>
<tr>
<th>Condition</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD to VSS</td>
<td>–0.3V to 11V</td>
</tr>
<tr>
<td>VDD to GND</td>
<td>–0.3V to 5.5V</td>
</tr>
<tr>
<td>VREFL to VSS</td>
<td>–0.3V to (VDD – VSS)</td>
</tr>
<tr>
<td>VDD to VREFH</td>
<td>–0.3V to (VDD – VSS)</td>
</tr>
<tr>
<td>VREFH to VREFL</td>
<td>–0.3V to (VDD – VSS)</td>
</tr>
<tr>
<td>Digital Input Voltage to GND</td>
<td>–0.3V to VDD + 0.3V</td>
</tr>
<tr>
<td>Digital Output Voltage to GND</td>
<td>–0.3V to VDD + 0.3V</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>+150°C</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>–40°C to +85°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>–65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10s)</td>
<td>+300°C</td>
</tr>
</tbody>
</table>

NOTE: (1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>MAXIMUM LINEARITY ERROR (LSB)</th>
<th>MAXIMUM DIFFERENTIAL LINEARITY ERROR (LSB)</th>
<th>PACKAGE</th>
<th>DRAWING NUMBER</th>
<th>SPECIFICATION TEMPERATURE RANGE</th>
<th>ORDERING NUMBER(1)</th>
<th>TRANSPORT MEDIA</th>
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<tbody>
<tr>
<td>DAC7613E</td>
<td>±2</td>
<td>±1</td>
<td>SSOP-24</td>
<td>338</td>
<td>–40°C to +85°C</td>
<td>DAC7613E/1K</td>
<td>Rails</td>
</tr>
<tr>
<td></td>
<td>&quot;</td>
<td>&quot;</td>
<td></td>
<td></td>
<td></td>
<td>DAC7613E/1K</td>
<td>Tape and Reel</td>
</tr>
<tr>
<td>DAC7613EB</td>
<td>±1</td>
<td>±1</td>
<td>SSOP-24</td>
<td>338</td>
<td>–40°C to +85°C</td>
<td>DAC7613EB/1K</td>
<td>Rails</td>
</tr>
<tr>
<td></td>
<td>&quot;</td>
<td>&quot;</td>
<td></td>
<td></td>
<td></td>
<td>DAC7613EB/1K</td>
<td>Tape and Reel</td>
</tr>
</tbody>
</table>

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of “DAC7613E/1K” will get a single 1000-piece Tape and Reel.
## PIN CONFIGURATION

### Pin Configuration Diagram

- **DB11 (MSB)**
- **DB10**
- **DB9**
- **DB8**
- **DB7**
- **DB6**
- **DB5**
- **DB4**
- **DB3**
- **DB2**
- **DB1**
- **DB0 (LSB)**

- **VREFL** Reference Input Voltage Low. Sets minimum output voltage for the DAC.
- **VREFH** Reference Input Voltage High. Sets maximum output voltage for the DAC.
- **VSS** Negative Analog Supply Voltage, 0V or –5V nominal.
- **GND** Ground
- **VDD** Positive Power Supply
- **VOUT** DAC Voltage Output
- **LOADDAC** The selected DAC register becomes transparent when LOADDAC is LOW. It is in the latched state when LOADDAC is HIGH.
- **RESET** Asynchronous Reset Input. Sets the DAC register to either zero-scale (000H) or mid-scale (800H) when LOW. RESETSEL determines which code is active.
- **RESETSEL** When LOW, a LOW on RESET will cause the DAC register to be set to code 000H. When RESETSEL is HIGH, a LOW on RESET will set the registers to code 800H.
- **CS** Chip Select. Active LOW.
- **R/W** Enabled by CS. Controls data read and write from the input register.

### Pin Descriptions

<table>
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<tr>
<th>PIN</th>
<th>LABEL</th>
<th>DESCRIPTION</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>DB11</td>
<td>Data Bit 11, MSB</td>
</tr>
<tr>
<td>2</td>
<td>DB10</td>
<td>Data Bit 10</td>
</tr>
<tr>
<td>3</td>
<td>DB9</td>
<td>Data Bit 9</td>
</tr>
<tr>
<td>4</td>
<td>DB8</td>
<td>Data Bit 8</td>
</tr>
<tr>
<td>5</td>
<td>DB7</td>
<td>Data Bit 7</td>
</tr>
<tr>
<td>6</td>
<td>DB6</td>
<td>Data Bit 6</td>
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<tr>
<td>7</td>
<td>DB5</td>
<td>Data Bit 5</td>
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<tr>
<td>8</td>
<td>DB4</td>
<td>Data Bit 4</td>
</tr>
<tr>
<td>9</td>
<td>DB3</td>
<td>Data Bit 3</td>
</tr>
<tr>
<td>10</td>
<td>DB2</td>
<td>Data Bit 2</td>
</tr>
<tr>
<td>11</td>
<td>DB1</td>
<td>Data Bit 1</td>
</tr>
<tr>
<td>12</td>
<td>DB0</td>
<td>Data Bit 0, LSB</td>
</tr>
<tr>
<td>13</td>
<td>VREFL</td>
<td>Reference Input Voltage Low. Sets minimum output voltage for the DAC.</td>
</tr>
<tr>
<td>14</td>
<td>NIC</td>
<td>Not Internally Connected</td>
</tr>
<tr>
<td>15</td>
<td>VREFH</td>
<td>Reference Input Voltage High. Sets maximum output voltage for the DAC.</td>
</tr>
<tr>
<td>16</td>
<td>VSS</td>
<td>Negative Analog Supply Voltage, 0V or –5V nominal.</td>
</tr>
<tr>
<td>17</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>18</td>
<td>VDD</td>
<td>Positive Power Supply</td>
</tr>
<tr>
<td>19</td>
<td>VOUT</td>
<td>DAC Voltage Output</td>
</tr>
<tr>
<td>20</td>
<td>LOADDAC</td>
<td>The selected DAC register becomes transparent when LOADDAC is LOW. It is in the latched state when LOADDAC is HIGH.</td>
</tr>
<tr>
<td>21</td>
<td>RESET</td>
<td>Asynchronous Reset Input. Sets the DAC register to either zero-scale (000H) or mid-scale (800H) when LOW. RESETSEL determines which code is active.</td>
</tr>
<tr>
<td>22</td>
<td>RESETSEL</td>
<td>When LOW, a LOW on RESET will cause the DAC register to be set to code 000H. When RESETSEL is HIGH, a LOW on RESET will set the registers to code 800H.</td>
</tr>
<tr>
<td>23</td>
<td>CS</td>
<td>Chip Select. Active LOW.</td>
</tr>
<tr>
<td>24</td>
<td>R/W</td>
<td>Enabled by CS. Controls data read and write from the input register.</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CURVES: \( V_{SS} = 0V \)

At \( T_A = +25^\circ\text{C}, V_{DD} = +5V, V_{RERH} = +2.5V, \) and \( V_{REFL} = 0V, \) representative unit, unless otherwise specified.

**LINEARITY ERROR and DIFFERENTIAL LINEARITY ERROR vs CODE**

**DIFFERENTIAL LINEARITY ERROR vs CODE**

**ZERO-SCALE ERROR vs TEMPERATURE**

(Code 010H)

**FULL-SCALE ERROR vs TEMPERATURE**

(Code FFFFH)
TYPICAL PERFORMANCE CURVES: $V_{SS} = -5V$

At $T_A = +25^\circ C$, $V_{DD} = +5V$, $V_{REFH} = +2.5V$, and $V_{REFL} = 0V$, representative unit, unless otherwise specified.
THEORY OF OPERATION

The DAC7613 is a 12-bit, voltage output Digital-to-Analog Converter (DAC). The architecture is a classic R-2R ladder configuration followed by an operational amplifier that serves as a buffer. The minimum voltage output ("zero-scale") and maximum voltage output ("full-scale") are set by the external voltage references (V_{REFL} and V_{REFH}, respectively). The digital input is a 12-bit parallel word and the DAC input register offers a readback capability. The converter can be powered from a single +5V supply or a dual ±5V supply. The device offers a reset function which immediately sets the DAC output voltage and DAC register to mid-scale (code 800H) or to zero-scale (code 000H), depending on the status of the reset selection. See Figures 1 and 2 for the basic operation of the DAC7613.

**FIGURE 1.** Basic Single-Supply Operation of the DAC7613.

**FIGURE 2.** Basic Dual-Supply Operation of the DAC7613.
ANALOG OUTPUTS

When $V_{SS} = -5V$ (dual supply operation), the output amplifier can swing to within 2.25V of the supply rails, guaranteed over the $-40^\circ C$ to $+85^\circ C$ temperature range. With $V_{SS} = 0V$ (single-supply operation), the output can swing to ground. Note that the settling time of the output op amp will be longer with voltages very near ground. Additionally, care must be taken when measuring the zero-scale error when $V_{SS} = 0V$. Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes ($000_{16}$, $001_{16}$, $002_{16}$, etc.) if the output amplifier has a negative offset.

The behavior of the output amplifier can be critical in some applications. Under short-circuit conditions (DAC output shorted to ground), the output amplifier can sink a great deal more current than it can source. See the Specifications table for more details concerning short-circuit current.

REFERENCE INPUTS

The reference inputs, $V_{REFL}$ and $V_{REFH}$, can be any voltage between $V_{SS} + 2.25V$ and $V_{DD} - 2.25V$ provided that $V_{REFH}$ is at least 1.25V greater than $V_{REFL}$. The minimum output of each DAC is equal to $V_{REFL}$ plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to $V_{REFH}$ plus a similar offset voltage. Note that $V_{SS}$ (the negative power supply) must either be connected to ground or must be in the range of $-4.75V$ to $-5.25V$. The voltage on $V_{SS}$ sets several bias points within the converter. If $V_{SS}$ is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the $V_{REFH}$ input depends on the DAC output voltages and can vary from a few microamps to approximately 0.1 milliamp. The $V_{REFH}$ source will not be required to sink current, only source it. Bypassing the reference voltage or voltages with at least a 0.1µF capacitor placed as close to the DAC7613 package is strongly recommended.

DIGITAL INTERFACE

Table I shows the basic control logic for the DAC7613. Note that the internal register is level triggered and not edge triggered. When the appropriate signal is LOW, the register becomes transparent. When this signal is returned HIGH, the digital word currently in the register is latched. The first register (the input register) is triggered via the R/W, and CS inputs. The second register (the DAC register) is transparent when LOADDAC input is pulled LOW.

The double-buffered architecture is mainly designed so that the DAC input register can be written at any time and then the DAC voltage updated by pulling LOADDAC LOW.

<table>
<thead>
<tr>
<th>R/W</th>
<th>CS</th>
<th>RST</th>
<th>LOADDAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
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<td>L</td>
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<td>H</td>
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</tr>
<tr>
<td>X</td>
<td>H</td>
<td>L</td>
<td>X</td>
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</table>

TABLE I. DAC7613 Control Logic Truth Table.
DIGITAL TIMING

Figure 3 and Table II provide detailed timing for the digital interface of the DAC7613.

DIGITAL INPUT CODING

The DAC7613 input data is in Straight Binary format. The output voltage is given by the following equation:

\[ V_{OUT} = V_{REFL} + \left( \frac{V_{REFH} - V_{REFL}}{4096} \right) \cdot N \]  

(1)

where N is the digital input code. This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

![Image of digital input and output timing with tables and diagrams]

TABLE II. Timing Specifications (T_A = –40°C to +85°C).

<table>
<thead>
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<th>TYP</th>
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<td>tOZ</td>
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<td>tRESET</td>
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# PACKAGING INFORMATION

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<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<tr>
<td>DAC7613E</td>
<td>ACTIVE</td>
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<td>DB</td>
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<td>CU NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>DAC7613E</td>
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<td>-40 to 85</td>
<td>DAC7613E</td>
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</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD:** The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS):** TI’s terms “Lead-Free” or “Pb-Free” mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br):** TI defines “Green” to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

![Diagram of reel dimensions](image)

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

![Diagram of quadrant assignments](image)

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0  (mm)</th>
<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
<th>W  (mm)</th>
<th>Pin1 Quadrant</th>
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### TAPE AND REEL BOX DIMENSIONS

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*All dimensions are nominal*
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