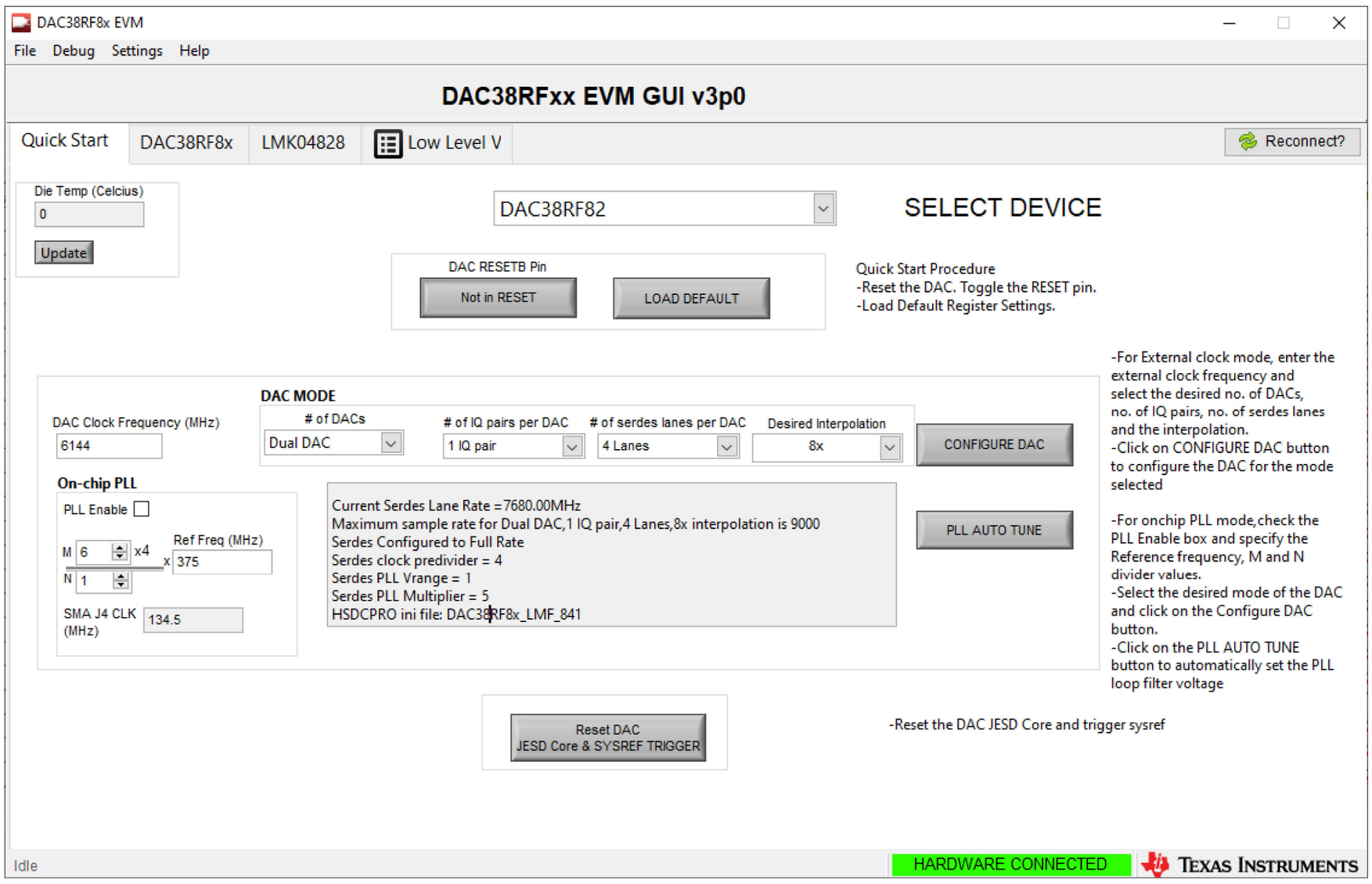
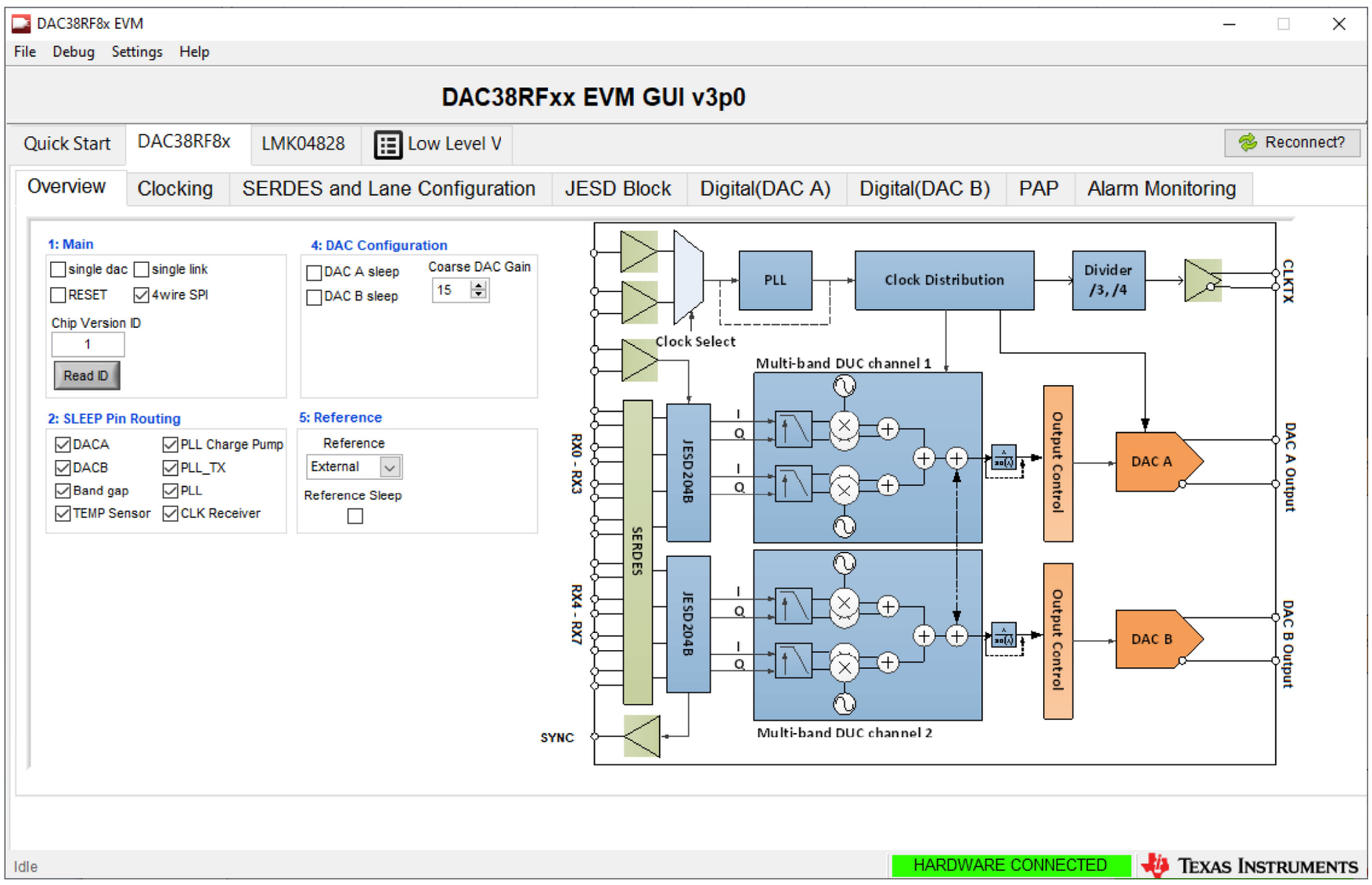

DAC38RF8x EVM
File Debug Settings Help
DAC38RFxx EVM GUI v3p0
Quick Start
DAC38RF8x
LMK04828
Low Level V
Reconnect?
Die Temp (Celcius)
0
Update
DAC38RF82
SELECT DEVICE
DAC RESETB Pin
Not in RESET
LOAD DEFAULT
Quick Start Procedure
-Reset the DAC. Toggle the RESET pin.
-Load Default Register Settings.
DAC MODE
DAC Clock Frequency (MHz)
6144
# of DACs
Dual DAC
# of IQ pairs per DAC
1 IQ pair
# of serdes lanes per DAC
4 Lanes
Desired Interpolation
8x
CONFIGURE DAC
-For External clock mode, enter the external clock frequency and select the desired no. of DACs, no. of IQ pairs, no. of serdes lanes and the interpolation.
-Click on CONFIGURE DAC button to configure the DAC for the mode selected
On-chip PLL
PLL Enable
M 6 x4
N 1
Ref Freq (MHz)
x 375
SMA J4 CLK (MHz)
134.5
Current Serdes Lane Rate =7680.00MHz
Maximum sample rate for Dual DAC,1 IQ pair,4 Lanes,8x interpolation is 9000
Serdes Configured to Full Rate
Serdes clock predivider = 4
Serdes PLL Vrange = 1
Serdes PLL Multiplier = 5
HSDCPRO ini file: DAC38RF8x_LMF_841
PLL AUTO TUNE
-For onchip PLL mode,check the PLL Enable box and specify the Reference frequency, M and N divider values.
-Select the desired mode of the DAC and click on the Configure DAC button.
-Click on the PLL AUTO TUNE button to automatically set the PLL loop filter voltage
Reset DAC
JESD Core & SYSREF TRIGGER
-Reset the DAC JESD Core and trigger sysref
Idle
HARDWARE CONNECTED
Texas Instruments


DAC38RF8x EVM
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Overview
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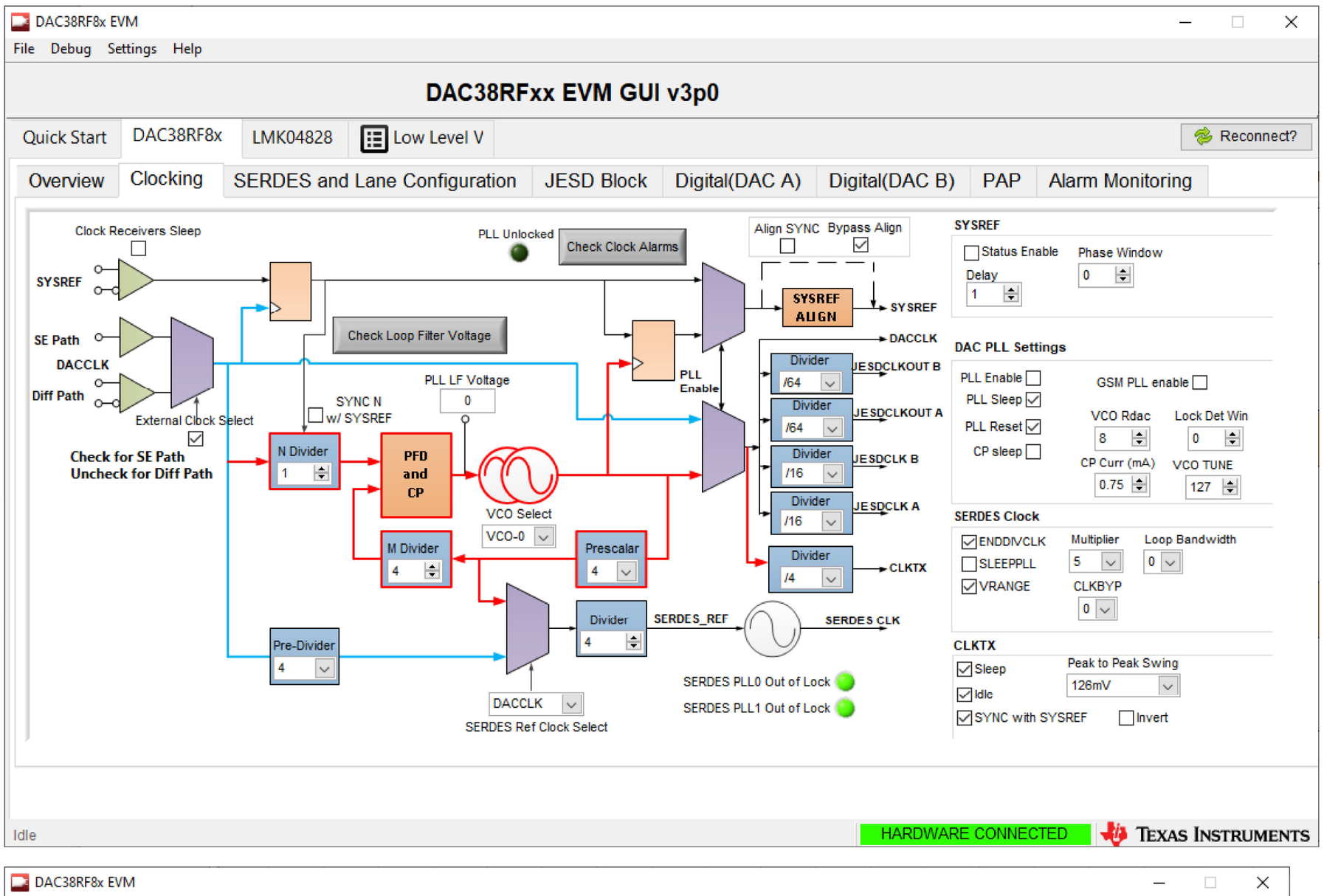
JESD Block
Digital(DAC A)
Digital(DAC B)
PAP
Alarm Monitoring
1: Main
single dac
single link
RESET
4wire SPI
Chip Version ID
1
Read ID
2: SLEEP Pin Routing
DACA
DACB
Band gap
TEMP Sensor
PLL Charge Pump
PLL_TX
PLL
CLK Receiver
4: DAC Configuration
DAC A sleep
DAC B sleep
Coarse DAC Gain
15
5: Reference
Reference
External
Reference Sleep
PLL
Clock Distribution
Divider /3, /4
CLKTX
Clock Select
Multi-band DUC channel 1
Multi-band DUC channel 2
RX0 - RX3
RX4 - RX7
SERDES
JESD204B
JESD204B
I
Q
Output Control
Output Control
DAC A
DAC B
DAC A Output
DAC B Output
SYNC
Idle
HARDWARE CONNECTED
Texas Instruments


DAC38RF8x EVM
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Digital(DAC B)
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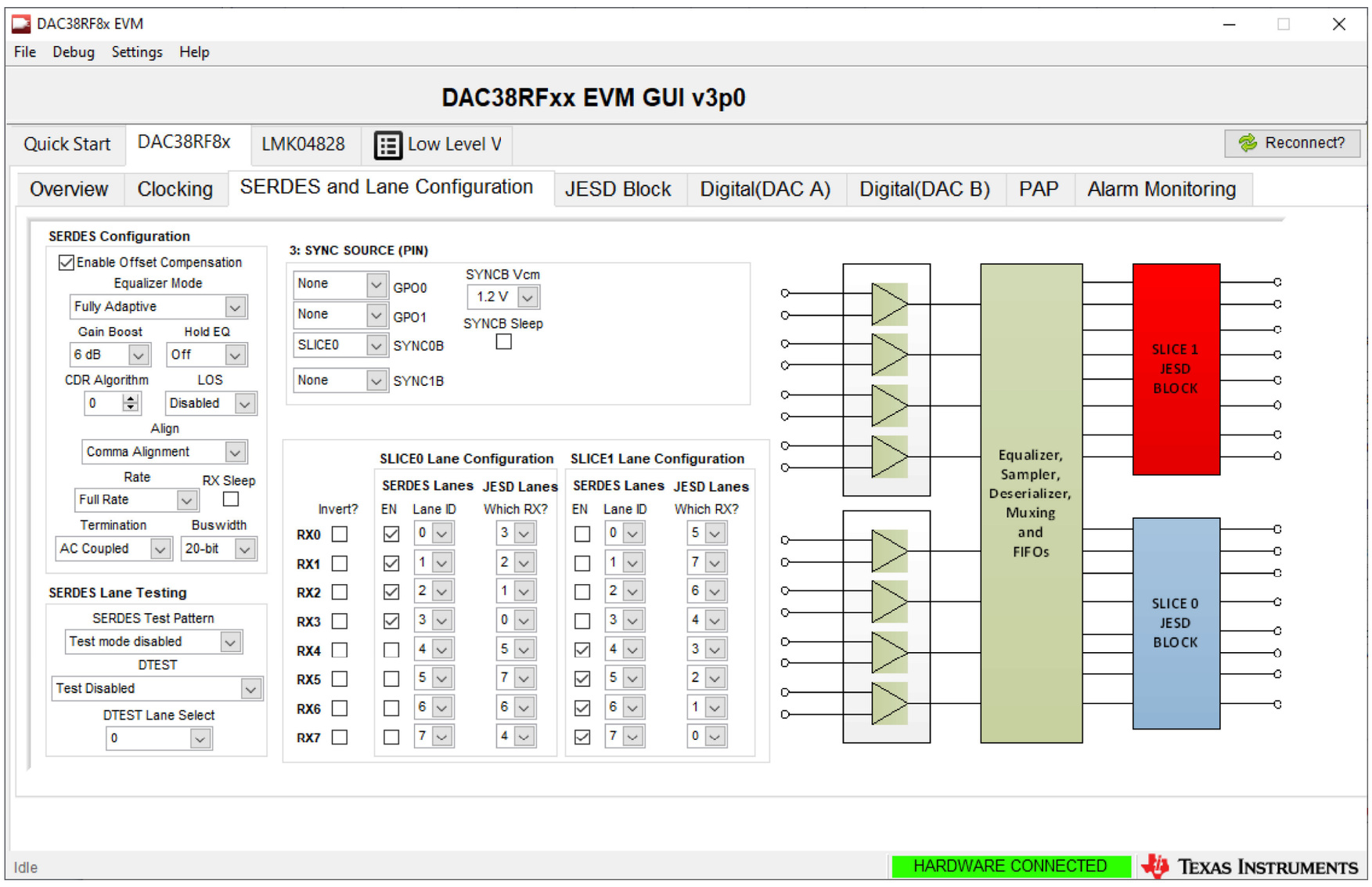
Alarm Monitoring
Clock Receivers Sleep
PLL Unlocked
Check Clock Alarms
Align SYNC
Bypass Align
SYSREF
SE Path
DACCLK
Diff Path
External Clock Select
Check for SE Path
Uncheck for Diff Path
Check Loop Filter Voltage
PLL LF Voltage
SYNC N w/ SYSREF
N Divider
PFD and CP
VCO Select
VCO-0
M Divider
Prescalar
Pre-Divider
PLL Enable
SYSREF ALIGN
DACCLK
Divider /64
JESDCLKOUT B
Divider /64
JESDCLKOUT A
Divider /16
JESDCLK B
Divider /16
JESDCLK A
Divider /4
CLKTX
Divider
SERDES_REF
SERDES CLK
SERDES PLL0 Out of Lock
SERDES PLL1 Out of Lock
SERDES Ref Clock Select
SYSREF
Status Enable
Phase Window
Delay
DAC PLL Settings
PLL Enable
PLL Sleep
PLL Reset
CP sleep
GSM PLL enable
VCO Rdac
Lock Det Win
CP Curr (mA)
VCO TUNE
SERDES Clock
ENDDIVCLK
SLEEPPLL
VRANGE
Multiplier
Loop Bandwidth
CLKBYP
CLKTX
Sleep
Idle
Peak to Peak Swing
126mV
SYNC with SYSREF
Invert
Idle
HARDWARE CONNECTED
Texas Instruments


DAC38RF8x EVM
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Digital(DAC B)
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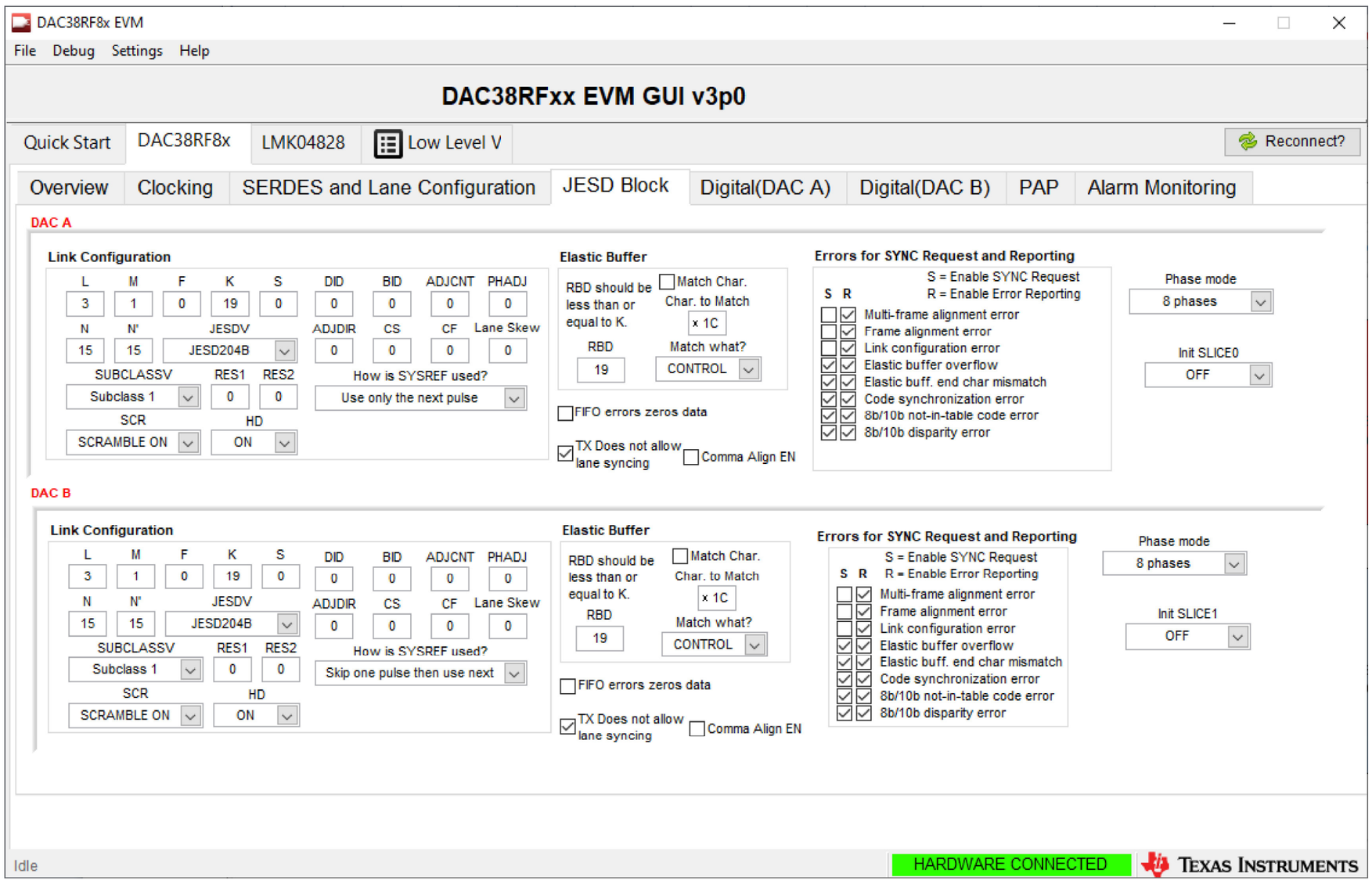
SERDES Configuration
Enable Offset Compensation
Equalizer Mode
Fully Adaptive
Gain Boost
6 dB
Hold EQ
Off
CDR Algorithm
LOS
Disabled
Align
Comma Alignment
Rate
Full Rate
RX Sleep
Termination
AC Coupled
Buswidth
20-bit
SERDES Lane Testing
SERDES Test Pattern
Test mode disabled
DTEST
Test Disabled
DTEST Lane Select
3: SYNC SOURCE (PIN)
None
GPO0
None
GPO1
SLICE0
SYNC0B
None
SYNC1B
SYNCB Vcm
1.2 V
SYNCB Sleep
SLICE0 Lane Configuration
SLICE1 Lane Configuration
SERDES Lanes
JESD Lanes
Invert?
EN
Lane ID
Which RX?
RX0
RX1
RX2
RX3
RX4
RX5
RX6
RX7
Equalizer, Sampler, Deserializer, Muxing and FIFOs
SLICE 1 JESD BLOCK
SLICE 0 JESD BLOCK
Idle
HARDWARE CONNECTED
Texas Instruments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Digital(DAC B)
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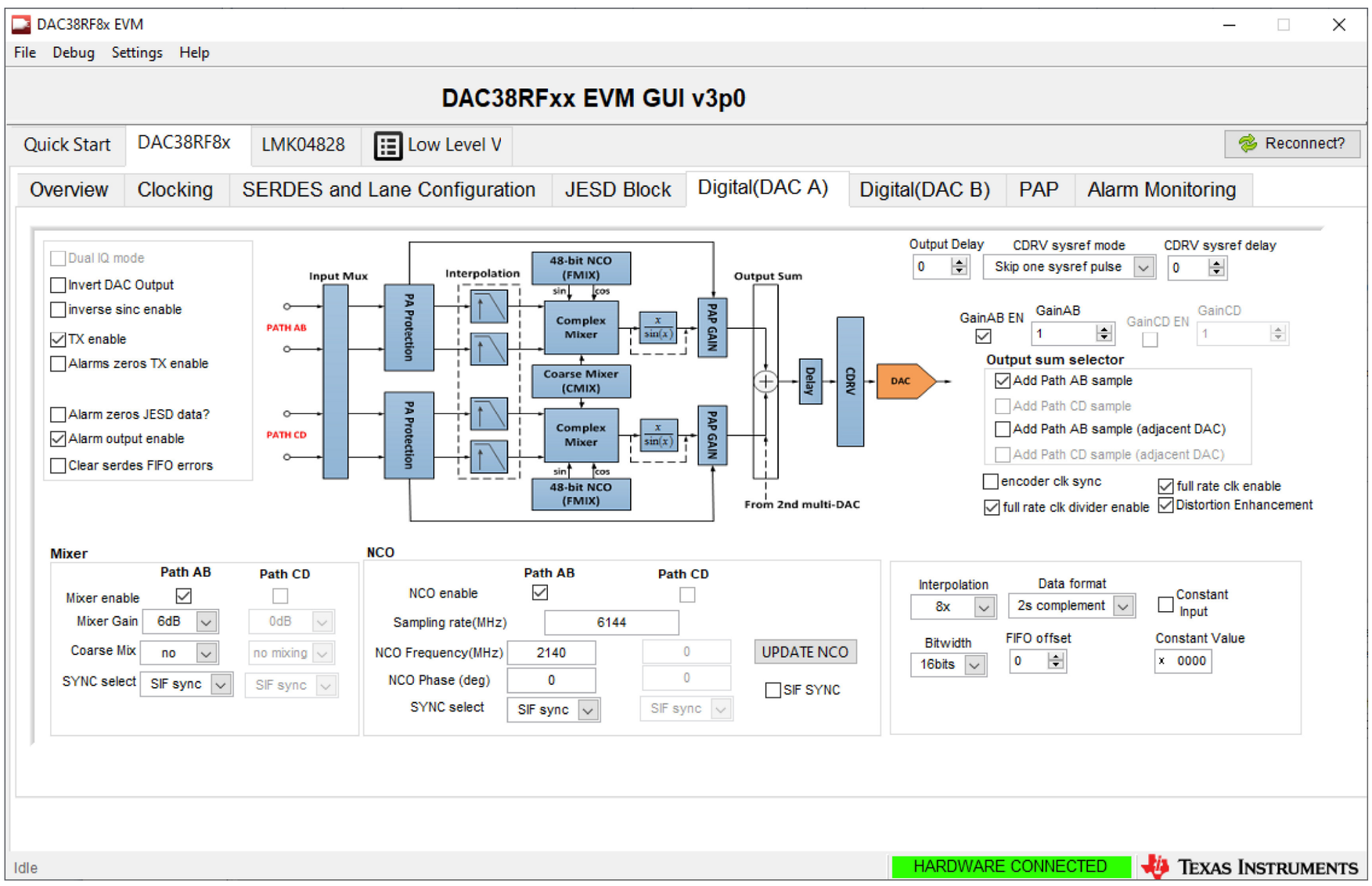
DAC A
Link Configuration
L M F K S DID BID ADJCNT PHADJ
3 1 0 19 0 0 0 0 0
N N' JESDV ADJDIR CS CF Lane Skew
15 15 JESD204B 0 0 0 0
SUBCLASSV RES1 RES2 How is SYSREF used?
Subclass 1 0 0 Use only the next pulse
SCR HD
SCRAMBLE ON ON
Elastic Buffer
RBD should be less than or equal to K.
Match Char.
Char. to Match
x 1C
RBD
19
Match what?
CONTROL
FIFO errors zeros data
TX Does not allow lane syncing
Comma Align EN
Errors for SYNC Request and Reporting
S = Enable SYNC Request
R = Enable Error Reporting
S R
Multi-frame alignment error
Frame alignment error
Link configuration error
Elastic buffer overflow
Elastic buff. end char mismatch
Code synchronization error
8b/10b not-in-table code error
8b/10b disparity error
Phase mode
8 phases
Init SLICE0
OFF
DAC B
Link Configuration
L M F K S DID BID ADJCNT PHADJ
3 1 0 19 0 0 0 0 0
N N' JESDV ADJDIR CS CF Lane Skew
15 15 JESD204B 0 0 0 0
SUBCLASSV RES1 RES2 How is SYSREF used?
Subclass 1 0 0 Skip one pulse then use next
SCR HD
SCRAMBLE ON ON
Elastic Buffer
RBD should be less than or equal to K.
Match Char.
Char. to Match
x 1C
RBD
19
Match what?
CONTROL
FIFO errors zeros data
TX Does not allow lane syncing
Comma Align EN
Errors for SYNC Request and Reporting
S = Enable SYNC Request
R = Enable Error Reporting
S R
Multi-frame alignment error
Frame alignment error
Link configuration error
Elastic buffer overflow
Elastic buff. end char mismatch
Code synchronization error
8b/10b not-in-table code error
8b/10b disparity error
Phase mode
8 phases
Init SLICE1
OFF
Idle
HARDWARE CONNECTED
Texas Instruments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Digital(DAC B)
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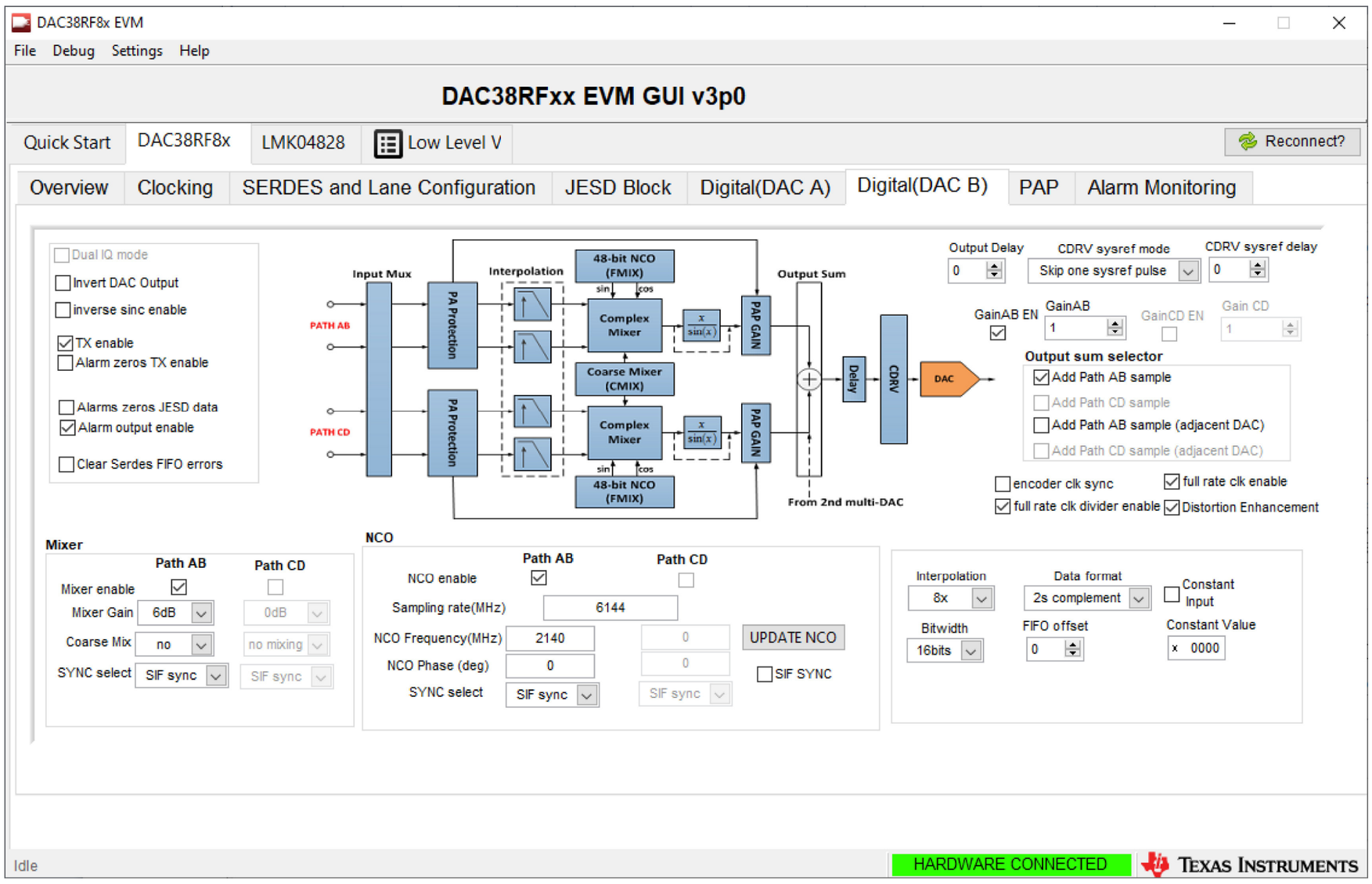
TX enable
Alarms zeros TX enable
Alarm zeros JESD data?
Alarm output enable
Clear serdes FIFO errors
Input Mux
PATH AB
PATH CD
PA Protection
Interpolation
48-bit NCO (FMIX)
sin
cos
Complex Mixer
Coarse Mixer (CMIX)
PAP GAIN
Output Sum
From 2nd multi-DAC
Delay
CDRV
DAC
Output Delay
CDRV sysref mode
Skip one sysref pulse
CDRV sysref delay
GainAB EN
GainAB
GainCD EN
GainCD
Output sum selector
Add Path AB sample
Add Path CD sample
Add Path AB sample (adjacent DAC)
Add Path CD sample (adjacent DAC)
encoder clk sync
full rate clk divider enable
full rate clk enable
Distortion Enhancement
Mixer
Path AB
Path CD
Mixer enable
Mixer Gain
6dB
0dB
Coarse Mix
no
no mixing
SYNC select
SIF sync
NCO
NCO enable
Sampling rate(MHz)
6144
NCO Frequency(MHz)
2140
NCO Phase (deg)
UPDATE NCO
SIF SYNC
Interpolation
8x
Data format
2s complement
Constant Input
Bitwidth
16bits
FIFO offset
Constant Value
x 0000
Idle
HARDWARE CONNECTED
Texas Instruments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TX enable
Alarm zeros TX enable
Alarms zeros JESD data
Alarm output enable
Clear Serdes FIFO errors
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Complex Mixer
Coarse Mixer (CMIX)
PA Protection
PAP GAIN
Output Sum
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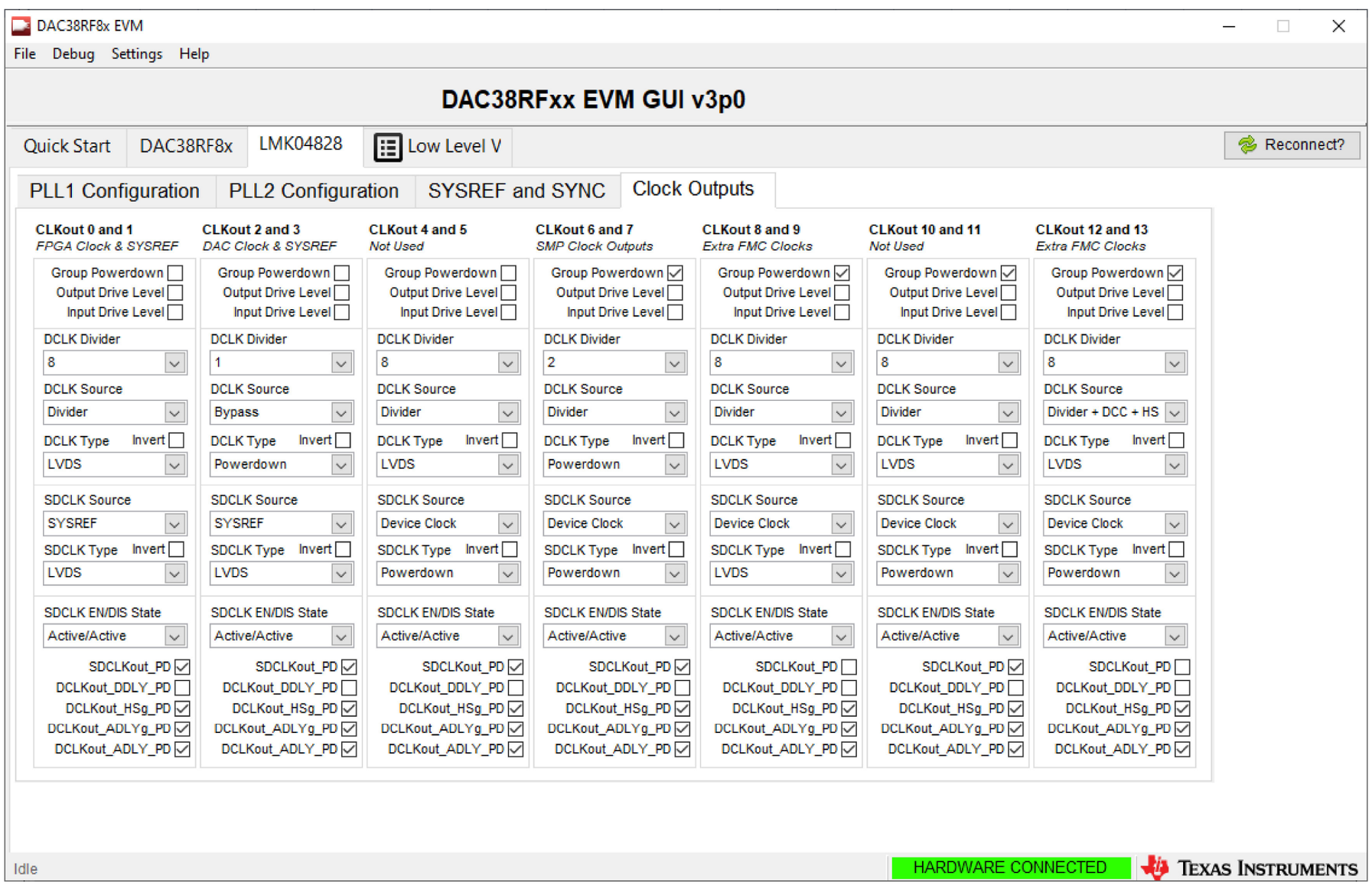
CDRV
DAC
PATH AB
PATH CD
From 2nd multi-DAC
Output Delay
CDRV sysref mode
Skip one sysref pulse
CDRV sysref delay
GainAB EN
GainAB
GainCD EN
Gain CD
Output sum selector
Add Path AB sample
Add Path CD sample
Add Path AB sample (adjacent DAC)
Add Path CD sample (adjacent DAC)
encoder clk sync
full rate clk enable
full rate clk divider enable
Distortion Enhancement
Mixer
Path AB
Path CD
Mixer enable
Mixer Gain
Coarse Mix
SYNC select
NCO
NCO enable
Sampling rate(MHz)
NCO Frequency(MHz)
NCO Phase (deg)
UPDATE NCO
SIF SYNC
Interpolation
Data format
Constant Input
Bitwidth
FIFO offset
Constant Value
Idle
HARDWARE CONNECTED
Texas Instruments


DAC38RF8x EVM
File Debug Settings Help
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PLL1 Configuration
PLL2 Configuration
SYSREF and SYNC
Clock Outputs
CLKout 0 and 1
FPGA Clock & SYSREF
CLKout 2 and 3
DAC Clock & SYSREF
CLKout 4 and 5
Not Used
CLKout 6 and 7
SMP Clock Outputs
CLKout 8 and 9
Extra FMC Clocks
CLKout 10 and 11
Not Used
CLKout 12 and 13
Extra FMC Clocks
Group Powerdown
Output Drive Level
Input Drive Level
DCLK Divider
DCLK Source
DCLK Type
Invert
SDCLK Source
SDCLK Type
SDCLK EN/DIS State
SDCLKout_PD
DCLKout_DDLY_PD
DCLKout_HSg_PD
DCLKout_ADLYg_PD
DCLKout_ADLY_PD
Idle
HARDWARE CONNECTED
Texas Instruments

DAC38RF8x EVM

File Debug Settings Help

# DAC38RFxx EVM GUI v3p0

Quick Start | DAC38RF8x | LMK04828 | Low Level V | Reconnect?

PLL1 Configuration | PLL2 Configuration | SYSREF and SYNC | Clock Outputs

**SYSREF Configuration**

SYSREF Source: SYSREF Continuous
SYSREF Divider: 320
Pulse Count: 8
SYSREF Block PD
SYSREF PD
SYSREF DDLY PD
SYSREF Pulser PD

**Global DDLY**

DDLY Step Count: 0
SYSREF DDLY: 8
SYSREF DDLY EN

**SYNC Configuration**

SYNC Mode: Pin

**Pulsed SYSREF must be configured before triggering will work.**

Trigger SYSREF

SYSREF SYNC Disable
DCLKout0 SYNC Disable
DCLKout2 SYNC Disable
DCLKout4 SYNC Disable
DCLKout6 SYNC Disable
DCLKout8 SYNC Disable
DCLKout10 SYNC Disable
DCLKout12 SYNC Disable
SYNC Pin Polarity
SYNC Enable
SYNC until PLL2 DLD
SYNC until PLL1 DLD

**CLKout Delays**

| CLKout 0 and 1 *FPGA Clock & SYSREF* | CLKout 2 and 3 *DAC Clock & SYSREF* | CLKout 4 and 5 *Not Used* | CLKout 6 and 7 *SMP Clock Outputs* | CLKout 8 and 9 *Extra FMC Clocks* | CLKout 10 and 11 *Not Used* | CLKout 12 and 13 *Extra FMC Clocks* |
|---|---|---|---|---|---|---|
| *DCLK Delay* | *DCLK Delay* | *DCLK Delay* | *DCLK Delay* | *DCLK Delay* | *DCLK Delay* | *DCLK Delay* |
| Dynamic DDLY EN | Dynamic DDLY EN | Dynamic DDLY EN | Dynamic DDLY EN | Dynamic DDLY EN | Dynamic DDLY EN | Dynamic DDLY EN |
| DCLK Continuous? | DCLK Continuous? | DCLK Continuous? | DCLK Continuous? | DCLK Continuous? | DCLK Continuous? | DCLK Continuous? |
| HS | HS | HS | HS | HS | HS | HS |
| # High: 5 | # High: 5 | # High: 5 | # High: 5 | # High: 5 | # High: 5 | # High: 5 |
| # Low: 5 | # Low: 5 | # Low: 5 | # Low: 5 | # Low: 5 | # Low: 5 | # Low: 5 |
| ADLY Input: Divider Only | ADLY Input: Divider Only | ADLY Input: Divider Only | ADLY Input: Divider Only | ADLY Input: Divider Only | ADLY Input: Divider Only | ADLY Input: Divider Only |
| ADLY (ps): 500 | ADLY (ps): 500 | ADLY (ps): 500 | ADLY (ps): 500 | ADLY (ps): 500 | ADLY (ps): 500 | ADLY (ps): 500 |
| *SDCLK Delay* | *SDCLK Delay* | *SDCLK Delay* | *SDCLK Delay* | *SDCLK Delay* | *SDCLK Delay* | *SDCLK Delay* |
| HS | HS | HS | HS | HS | HS | HS |
| ADLY EN | ADLY EN | ADLY EN | ADLY EN | ADLY EN | ADLY EN | ADLY EN |
| DDLY: 0 | DDLY: 0 | DDLY: 0 | DDLY: 0 | DDLY: 0 | DDLY: 0 | DDLY: 0 |
| ADLY (ps): 0 | ADLY (ps): 0 | ADLY (ps): 0 | ADLY (ps): 0 | ADLY (ps): 0 | ADLY (ps): 0 | ADLY (ps): 0 |

Idle | HARDWARE CONNECTED | Texas Instruments

Signal Tap Logic Analyzer - C:/debug/evm_dac_testC1192sysref/prj/jesd204b_ed - jesd204b_ed - [RX_TRANSPORT_DATAOUT.stp]*

File Edit View Project Processing Tools Window Help

Search Intel FPGA

Instance Manager: Ready to acquire

| Instance | Status | Enabled |
|---|---|---|
| auto_signaltap_0 | Not running | ✓ |

JTAG Chain Configuration: JTAG ready

Hardware: USB-BlasterII [USB-1] Setup...

Device: @1: 10AS066H1(.|ES)/10A Scan Chain

Bridge Index: None Detected

>> SOF Manager: ...

log: Trig @ 2021/01/18 14:00:54 (0:0:0.2 elapsed)

click to insert time bar

| Type | Alias | Name | -224 | -223 | -222 | -221 | -220 | -219 | -218 | -217 | -216 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | sysref | | | | | | | | | |
| | | tx_syncn | | | | | | | | | |
| | | xcvr_jesd_tx:i0_xcvr_jesd_tx\|jesd204_tx_pcs_data[255..0] | | | | | | | | | |
| | | xcvr_jesd_tx:i0_xcvr_jesd_tx\|jesd204_tx_pcs_data[255..224] | BECD765Ah | D3B834B9h | 0926FE0Eh | 205FC91Dh | D3A1B938h | 8BDE4221h | D6FE21CEh | 18B53614h | |
| | | xcvr_jesd_tx:i0_xcvr_jesd_tx\|jesd204_tx_pcs_data[223..192] | 49596772h | FA0F2437h | AEBFD1E6h | 8389929Fh | 8B84FC80h | C4B2A396h | 1500ECD7h | 5E4E3D2Ah | |
| | | xcvr_jesd_tx:i0_xcvr_jesd_tx\|jesd204_tx_pcs_data[191..160] | BECD765Ah | D3B834B9h | 0926FE0Eh | 205FC91Dh | D3A1B938h | 8BDE4221h | D6FE21CEh | 18B53614h | |
| | | xcvr_jesd_tx:i0_xcvr_jesd_tx\|jesd204_tx_pcs_data[159..120] | 49596772h | FA0F2437h | AEBFD1E6h | 8389929Fh | 8B84FC80h | C4B2A396h | 1500ECD7h | 5E4E3D2Ah | |
| | | xcvr_jesd_tx:i0_xcvr_jesd_tx\|jesd204_tx_pcs_data[127..96] | BECD765Ah | D3B834B9h | 0926FE0Eh | 205FC91Dh | D3A1B938h | 8BDE4221h | D6FE21CEh | 18B53614h | |
| | | xcvr_jesd_tx:i0_xcvr_jesd_tx\|jesd204_tx_pcs_data[95..64] | 49596772h | FA0F2437h | AEBFD1E6h | 8389929Fh | 8B84FC80h | C4B2A396h | 1500ECD7h | 5E4E3D2Ah | |
| | | xcvr_jesd_tx:i0_xcvr_jesd_tx\|jesd204_tx_pcs_data[63..32] | BECD765Ah | D3B834B9h | 0926FE0Eh | 205FC91Dh | D3A1B938h | 8BDE4221h | D6FE21CEh | 18B53614h | |
| | | xcvr_jesd_tx:i0_xcvr_jesd_tx\|jesd204_tx_pcs_data[31..0] | 49596772h | FA0F2437h | AEBFD1E6h | 8389929Fh | 8B84FC80h | C4B2A396h | 1500ECD7h | 5E4E3D2Ah | |
| | | ...ayer_DAC38RF82_84111:jesd_transport1\|jesd204_tx_link_data[255..0] | | | | | | | | | |
| | | ...C38RF82_84111:jesd_transport1\|jesd204_tx_link_data[255..224] | 38B9A1D3h | 2142DE8Bh | CE21FED6h | 1436B518h | F9FFE379h | A76DDE2Ah | 946E2429h | FF3150E5h | |
| | | ...C38RF82_84111:jesd_transport1\|jesd204_tx_link_data[223..192] | 8080848Bh | 96A3B2C4h | D7EC0015h | 2A3D4E5Eh | 6A747B7Fh | 7F7C756Ch | 5F503F2Ch | 1703EED9h | |
| | | ...C38RF82_84111:jesd_transport1\|jesd204_tx_link_data[191..160] | 38B9A1D3h | 2142DE8Bh | CE21FED6h | 1436B518h | F9FFE379h | A76DDE2Ah | 946E2429h | FF3150E5h | |
| | | ...C38RF82_84111:jesd_transport1\|jesd204_tx_link_data[159..128] | 8080848Bh | 96A3B2C4h | D7EC0015h | 2A3D4E5Eh | 6A747B7Fh | 7F7C756Ch | 5F503F2Ch | 1703EED9h | |
| | | ...C38RF82_84111:jesd_transport1\|jesd204_tx_link_data[127..96] | 38B9A1D3h | 2142DE8Bh | CE21FED6h | 1436B518h | F9FFE379h | A76DDE2Ah | 946E2429h | FF3150E5h | |
| | | ...AC38RF82_84111:jesd_transport1\|jesd204_tx_link_data[95..64] | 8080848Bh | 96A3B2C4h | D7EC0015h | 2A3D4E5Eh | 6A747B7Fh | 7F7C756Ch | 5F503F2Ch | 1703EED9h | |
| | | ...AC38RF82_84111:jesd_transport1\|jesd204_tx_link_data[63..32] | 38B9A1D3h | 2142DE8Bh | CE21FED6h | 1436B518h | F9FFE379h | A76DDE2Ah | 946E2429h | FF3150E5h | |
| | | ...DAC38RF82_84111:jesd_transport1\|jesd204_tx_link_data[31..0] | 8080848Bh | 96A3B2C4h | D7EC0015h | 2A3D4E5Eh | 6A747B7Fh | 7F7C756Ch | 5F503F2Ch | 1703EED9h | |
| | | altera_jesd204:u_jesd204\|jesd204_tx_link_valid | | | | | | | | | |
| | | ...ort_layer_DAC38RF82_84111:jesd_transport1\|dds:ddsi0\|fsin_o[15..0] | 9621h | D7CEh | 2A14h | 6AF9h | 7FA7h | 5F94h | 17FFh | C67Fh | |
| | | ...ort_layer_DAC38RF82_84111:jesd_transport1\|dds:ddsi1\|fsin_o[15..0] | A342h | EC21h | 3D36h | 74FFh | 7C6Dh | 506Eh | 0331h | B4A5h | |
| | | ...ort_layer_DAC38RF82_84111:jesd_transport1\|dds:ddsi2\|fsin_o[15..0] | B2DEh | 00FEh | 4EB5h | 7BE3h | 75DEh | 3F24h | EE50h | A4CBh | |

Data | Setup

auto_signaltap_0