```
//global_soft_reset=0
SPIWrite 0000,a0
//global_soft_reset=1
SPIWrite 0000,20
//global_soft_reset=0
SPIWrite 0000,20
//global_4pin=0
SPIWrite 0000,20
//global_ascend=1
SPIRead 0003

// Read // chip_type: a
SPIRead 0004
SPIRead 0005

// Read // chip_id: 77
SPIRead 0006

// Read // chip_ver: 20
SPIRead 0007
SPIRead 0008
// Read // vendor_id: 451
// Done resetting the Device



WAIT 1

// Doing LMK config

// Done with LMK Config

// Waking up device

SPIWrite 0015,00
//PAGE:jesd_subchip=0(Meaning: );
SPIWrite 0015,80
//PAGE:DIGTOP_MISC=1(Meaning: );
SPIWrite 0600,03
//misc_spi_global_pdn_ctrl=1
SPIWrite 0600,02
//misc_spi_global_pdn_ctrl=0

// Done waking up device
/*********************************************************/
WAIT 10
SPIWrite 07f0,00
//spi_ovr_sys_autoload_chain=0
```

```
SPIWrite 0804,00
//spi_ovr_sys_autoload_chain=0
SPIWrite 07f0,3c
SPIWrite 07f0,3d
SPIWrite 07f0,3f
SPIWrite 07f0,3c
SPIWrite 07f0,00

SPIWrite 0804,3c
SPIWrite 0804,3d
SPIWrite 0804,3f
SPIWrite 0804,3c
SPIWrite 0804,00
//spi_ovr_sys_autoload_chain=0


WAIT 10

SPIRead 0138

// Read // obs_func_spi_chain_autoload_done: f
SPIRead 013c

// Read // obs_func_spi_chain_autoload_error: f
SPIWrite 0135,01
//spi_ovr_sys_clk_gate=1
SPIWrite 0131,01
//spi_ovr_sys_clk_gate=1
SPIWrite 0015,00
//PAGE:jesd_subchip=0(Meaning: );

/***********Step: Top CM4 wakeup******************/

//PAGE:DIGTOP_MISC=0(Meaning: );
SPIWrite 0013,10
//PAGE:customer_macro=1(Meaning: );
SPIWrite 0140,01
SPIWrite 0140,00
SPIWrite 0013,00
//PAGE:customer_macro=0(Meaning: );


/***********Step: Top Patch Download/Apply. Ajay Specific Fw writes******************/

SPIWrite 0012,10
//PAGE:sys_calib_macro_memory=1(Meaning: );
SPIWrite 0040,00
SPIWrite 0020,00
```

SPIWrite 0021,00
SPIWrite 0022,00
SPIWrite 0023,00
SPIWrite 0024,31
SPIWrite 0025,80
SPIWrite 0026,02
SPIWrite 0027,00
SPIWrite 0028,b5
SPIWrite 0029,a4
SPIWrite 002a,6d
SPIWrite 002b,ea
SPIWrite 002c,7d
SPIWrite 002d,19
SPIWrite 002e,ce
SPIWrite 002f,ca
SPIWrite 0030,12
SPIWrite 0031,00
SPIWrite 0032,01
SPIWrite 0033,12
SPIWrite 0034,04
SPIWrite 0035,03
SPIWrite 0036,13
SPIWrite 0037,00
SPIWrite 0038,00
SPIWrite 0039,00
SPIWrite 003a,00
SPIWrite 003b,00
SPIWrite 003c,00
SPIWrite 003d,00
SPIWrite 003e,00
SPIWrite 003f,00
SPIWrite 0040,00
SPIWrite 0041,00
SPIWrite 0042,00
SPIWrite 0043,00
SPIWrite 0044,00
SPIWrite 0045,00
SPIWrite 0046,00
SPIWrite 0047,00
SPIWrite 0048,00
SPIWrite 0049,00
SPIWrite 004a,00
SPIWrite 004b,00
SPIWrite 004c,00
SPIWrite 004d,00
SPIWrite 004e,00
SPIWrite 004f,00
SPIWrite 0050,38

SPIWrite 0051,b5
SPIWrite 0052,31
SPIWrite 0053,4a
SPIWrite 0054,31
SPIWrite 0055,49
SPIWrite 0056,11
SPIWrite 0057,60
SPIWrite 0058,40
SPIWrite 0059,4b
SPIWrite 005a,93
SPIWrite 005b,65
SPIWrite 005c,9d
SPIWrite 005d,20
SPIWrite 005e,50
SPIWrite 005f,60
SPIWrite 0060,2f
SPIWrite 0061,49
SPIWrite 0062,91
SPIWrite 0063,60
SPIWrite 0064,3e
SPIWrite 0065,4b
SPIWrite 0066,13
SPIWrite 0067,66
SPIWrite 0068,2e
SPIWrite 0069,49
SPIWrite 006a,d1
SPIWrite 006b,60
SPIWrite 006c,3d
SPIWrite 006d,4b
SPIWrite 006e,93
SPIWrite 006f,66
SPIWrite 0070,2d
SPIWrite 0071,49
SPIWrite 0072,11
SPIWrite 0073,61
SPIWrite 0074,3c
SPIWrite 0075,4b
SPIWrite 0076,53
SPIWrite 0077,67
SPIWrite 0078,2c
SPIWrite 0079,49
SPIWrite 007a,51
SPIWrite 007b,61
SPIWrite 007c,00
SPIWrite 007d,20
SPIWrite 007e,d0
SPIWrite 007f,61
SPIWrite 0080,10

SPIWrite 0081,62
SPIWrite 0082,50
SPIWrite 0083,62
SPIWrite 0084,90
SPIWrite 0085,62
SPIWrite 0086,50
SPIWrite 0087,63
SPIWrite 0088,29
SPIWrite 0089,49
SPIWrite 008a,91
SPIWrite 008b,61
SPIWrite 008c,29
SPIWrite 008d,49
SPIWrite 008e,d1
SPIWrite 008f,62
SPIWrite 0090,29
SPIWrite 0091,49
SPIWrite 0092,11
SPIWrite 0093,63
SPIWrite 0094,35
SPIWrite 0095,4b
SPIWrite 0096,c2
SPIWrite 0097,f8
SPIWrite 0098,80
SPIWrite 0099,30
SPIWrite 009a,28
SPIWrite 009b,49
SPIWrite 009c,91
SPIWrite 009d,63
SPIWrite 009e,28
SPIWrite 009f,49
SPIWrite 00a0,d1
SPIWrite 00a1,63
SPIWrite 00a2,28
SPIWrite 00a3,49
SPIWrite 00a4,11
SPIWrite 00a5,64
SPIWrite 00a6,28
SPIWrite 00a7,49
SPIWrite 00a8,51
SPIWrite 00a9,64
SPIWrite 00aa,28
SPIWrite 00ab,49
SPIWrite 00ac,91
SPIWrite 00ad,64
SPIWrite 00ae,28
SPIWrite 00af,49
SPIWrite 00b0,d1

SPIWrite 00b1,64
SPIWrite 00b2,28
SPIWrite 00b3,49
SPIWrite 00b4,11
SPIWrite 00b5,65
SPIWrite 00b6,28
SPIWrite 00b7,49
SPIWrite 00b8,51
SPIWrite 00b9,65
SPIWrite 00ba,d1
SPIWrite 00bb,65
SPIWrite 00bc,51
SPIWrite 00bd,66
SPIWrite 00be,d1
SPIWrite 00bf,66
SPIWrite 00c0,11
SPIWrite 00c1,67
SPIWrite 00c2,91
SPIWrite 00c3,67
SPIWrite 00c4,d1
SPIWrite 00c5,67
SPIWrite 00c6,c2
SPIWrite 00c7,f8
SPIWrite 00c8,84
SPIWrite 00c9,10
SPIWrite 00ca,29
SPIWrite 00cb,49
SPIWrite 00cc,c1
SPIWrite 00cd,f8
SPIWrite 00ce,08
SPIWrite 00cf,29
SPIWrite 00d0,0c
SPIWrite 00d1,22
SPIWrite 00d2,c0
SPIWrite 00d3,f2
SPIWrite 00d4,00
SPIWrite 00d5,02
SPIWrite 00d6,52
SPIWrite 00d7,1e
SPIWrite 00d8,fd
SPIWrite 00d9,d1
SPIWrite 00da,00
SPIWrite 00db,bf
SPIWrite 00dc,00
SPIWrite 00dd,bf
SPIWrite 00de,80
SPIWrite 00df,22
SPIWrite 00e0,24

SPIWrite 00e1,4b
SPIWrite 00e2,0a
SPIWrite 00e3,70
SPIWrite 00e4,28
SPIWrite 00e5,25
SPIWrite 00e6,1d
SPIWrite 00e7,70
SPIWrite 00e8,4a
SPIWrite 00e9,70
SPIWrite 00ea,98
SPIWrite 00eb,80
SPIWrite 00ec,0a
SPIWrite 00ed,24
SPIWrite 00ee,5c
SPIWrite 00ef,80
SPIWrite 00f0,8a
SPIWrite 00f1,70
SPIWrite 00f2,c8
SPIWrite 00f3,70
SPIWrite 00f4,08
SPIWrite 00f5,71
SPIWrite 00f6,48
SPIWrite 00f7,71
SPIWrite 00f8,88
SPIWrite 00f9,71
SPIWrite 00fa,0a
SPIWrite 00fb,72
SPIWrite 00fc,0a
SPIWrite 00fd,74
SPIWrite 00fe,1f
SPIWrite 00ff,4d
SPIWrite 0100,ca
SPIWrite 0101,74
SPIWrite 0102,1d
SPIWrite 0103,49
SPIWrite 0104,1e
SPIWrite 0105,4a
SPIWrite 0106,c1
SPIWrite 0107,f8
SPIWrite 0108,b4
SPIWrite 0109,50
SPIWrite 010a,1e
SPIWrite 010b,48
SPIWrite 010c,c1
SPIWrite 010d,f8
SPIWrite 010e,b8
SPIWrite 010f,20
SPIWrite 0110,1d

SPIWrite 0111,49
SPIWrite 0112,01
SPIWrite 0113,60
SPIWrite 0114,38
SPIWrite 0115,bd
SPIWrite 0116,c0
SPIWrite 0117,46
SPIWrite 0118,00
SPIWrite 0119,30
SPIWrite 011a,01
SPIWrite 011b,20
SPIWrite 011c,00
SPIWrite 011d,7c
SPIWrite 011e,01
SPIWrite 011f,20
SPIWrite 0120,a9
SPIWrite 0121,d4
SPIWrite 0122,01
SPIWrite 0123,00
SPIWrite 0124,c5
SPIWrite 0125,d4
SPIWrite 0126,01
SPIWrite 0127,00
SPIWrite 0128,b7
SPIWrite 0129,d4
SPIWrite 012a,01
SPIWrite 012b,00
SPIWrite 012c,e1
SPIWrite 012d,d4
SPIWrite 012e,01
SPIWrite 012f,00
SPIWrite 0130,7f
SPIWrite 0131,d4
SPIWrite 0132,01
SPIWrite 0133,00
SPIWrite 0134,8d
SPIWrite 0135,d4
SPIWrite 0136,01
SPIWrite 0137,00
SPIWrite 0138,d3
SPIWrite 0139,d4
SPIWrite 013a,01
SPIWrite 013b,00
SPIWrite 013c,9b
SPIWrite 013d,d4
SPIWrite 013e,01
SPIWrite 013f,00
SPIWrite 0140,8b

SPIWrite 0141,d4
SPIWrite 0142,01
SPIWrite 0143,00
SPIWrite 0144,cd
SPIWrite 0145,d8
SPIWrite 0146,01
SPIWrite 0147,00
SPIWrite 0148,27
SPIWrite 0149,d7
SPIWrite 014a,01
SPIWrite 014b,00
SPIWrite 014c,33
SPIWrite 014d,d5
SPIWrite 014e,01
SPIWrite 014f,00
SPIWrite 0150,9b
SPIWrite 0151,82
SPIWrite 0152,02
SPIWrite 0153,00
SPIWrite 0154,b7
SPIWrite 0155,82
SPIWrite 0156,02
SPIWrite 0157,00
SPIWrite 0158,31
SPIWrite 0159,d5
SPIWrite 015a,01
SPIWrite 015b,00
SPIWrite 015c,fd
SPIWrite 015d,d4
SPIWrite 015e,01
SPIWrite 015f,00
SPIWrite 0160,2d
SPIWrite 0161,17
SPIWrite 0162,01
SPIWrite 0163,00
SPIWrite 0164,3d
SPIWrite 0165,d5
SPIWrite 0166,01
SPIWrite 0167,00
SPIWrite 0168,33
SPIWrite 0169,d6
SPIWrite 016a,01
SPIWrite 016b,00
SPIWrite 016c,39
SPIWrite 016d,d7
SPIWrite 016e,01
SPIWrite 016f,00
SPIWrite 0170,00

SPIWrite 0171,e4
SPIWrite 0172,00
SPIWrite 0173,e0
SPIWrite 0174,00
SPIWrite 0175,00
SPIWrite 0176,01
SPIWrite 0177,20
SPIWrite 0178,24
SPIWrite 0179,59
SPIWrite 017a,00
SPIWrite 017b,20
SPIWrite 017c,6d
SPIWrite 017d,81
SPIWrite 017e,02
SPIWrite 017f,00
SPIWrite 0180,7d
SPIWrite 0181,81
SPIWrite 0182,02
SPIWrite 0183,00
SPIWrite 0184,b0
SPIWrite 0185,54
SPIWrite 0186,00
SPIWrite 0187,20
SPIWrite 0188,97
SPIWrite 0189,82
SPIWrite 018a,02
SPIWrite 018b,00
SPIWrite 018c,08
SPIWrite 018d,b5
SPIWrite 018e,d8
SPIWrite 018f,f7
SPIWrite 0190,69
SPIWrite 0191,f8
SPIWrite 0192,31
SPIWrite 0193,48
SPIWrite 0194,31
SPIWrite 0195,49
SPIWrite 0196,00
SPIWrite 0197,78
SPIWrite 0198,08
SPIWrite 0199,70
SPIWrite 019a,08
SPIWrite 019b,bd
SPIWrite 019c,30
SPIWrite 019d,48
SPIWrite 019e,f8
SPIWrite 019f,b5
SPIWrite 01a0,4f

SPIWrite 01a1,f0
SPIWrite 01a2,22
SPIWrite 01a3,41
SPIWrite 01a4,41
SPIWrite 01a5,f2
SPIWrite 01a6,14
SPIWrite 01a7,0c
SPIWrite 01a8,b1
SPIWrite 01a9,f9
SPIWrite 01aa,48
SPIWrite 01ab,20
SPIWrite 01ac,1c
SPIWrite 01ad,f8
SPIWrite 01ae,00
SPIWrite 01af,70
SPIWrite 01b0,91
SPIWrite 01b1,f8
SPIWrite 01b2,4a
SPIWrite 01b3,30
SPIWrite 01b4,12
SPIWrite 01b5,f1
SPIWrite 01b6,18
SPIWrite 01b7,0f
SPIWrite 01b8,04
SPIWrite 01b9,db
SPIWrite 01ba,00
SPIWrite 01bb,2a
SPIWrite 01bc,04
SPIWrite 01bd,dd
SPIWrite 01be,d1
SPIWrite 01bf,10
SPIWrite 01c0,c9
SPIWrite 01c1,b2
SPIWrite 01c2,02
SPIWrite 01c3,e0
SPIWrite 01c4,6f
SPIWrite 01c5,f0
SPIWrite 01c6,17
SPIWrite 01c7,02
SPIWrite 01c8,00
SPIWrite 01c9,21
SPIWrite 01ca,24
SPIWrite 01cb,4c
SPIWrite 01cc,24
SPIWrite 01cd,78
SPIWrite 01ce,8c
SPIWrite 01cf,42
SPIWrite 01d0,b8

SPIWrite 01d1,bf
SPIWrite 01d2,21
SPIWrite 01d3,1c
SPIWrite 01d4,a2
SPIWrite 01d5,eb
SPIWrite 01d6,c1
SPIWrite 01d7,02
SPIWrite 01d8,18
SPIWrite 01d9,32
SPIWrite 01da,d2
SPIWrite 01db,b2
SPIWrite 01dc,c0
SPIWrite 01dd,2a
SPIWrite 01de,a8
SPIWrite 01df,bf
SPIWrite 01e0,bf
SPIWrite 01e1,22
SPIWrite 01e2,5c
SPIWrite 01e3,08
SPIWrite 01e4,0a
SPIWrite 01e5,d3
SPIWrite 01e6,ac
SPIWrite 01e7,f1
SPIWrite 01e8,10
SPIWrite 01e9,06
SPIWrite 01ea,87
SPIWrite 01eb,f0
SPIWrite 01ec,01
SPIWrite 01ed,05
SPIWrite 01ee,34
SPIWrite 01ef,1d
SPIWrite 01f0,21
SPIWrite 01f1,54
SPIWrite 01f2,05
SPIWrite 01f3,f0
SPIWrite 01f4,01
SPIWrite 01f5,05
SPIWrite 01f6,35
SPIWrite 01f7,54
SPIWrite 01f8,64
SPIWrite 01f9,1c
SPIWrite 01fa,22
SPIWrite 01fb,54
SPIWrite 01fc,9c
SPIWrite 01fd,08
SPIWrite 01fe,0a
SPIWrite 01ff,d3
SPIWrite 0200,ac

SPIWrite 0201,f1
SPIWrite 0202,0f
SPIWrite 0203,06
SPIWrite 0204,87
SPIWrite 0205,f0
SPIWrite 0206,01
SPIWrite 0207,05
SPIWrite 0208,74
SPIWrite 0209,1d
SPIWrite 020a,21
SPIWrite 020b,54
SPIWrite 020c,05
SPIWrite 020d,f0
SPIWrite 020e,01
SPIWrite 020f,05
SPIWrite 0210,35
SPIWrite 0211,54
SPIWrite 0212,64
SPIWrite 0213,1c
SPIWrite 0214,22
SPIWrite 0215,54
SPIWrite 0216,dc
SPIWrite 0217,08
SPIWrite 0218,0a
SPIWrite 0219,d3
SPIWrite 021a,ac
SPIWrite 021b,f1
SPIWrite 021c,0e
SPIWrite 021d,06
SPIWrite 021e,87
SPIWrite 021f,f0
SPIWrite 0220,01
SPIWrite 0221,05
SPIWrite 0222,b4
SPIWrite 0223,1d
SPIWrite 0224,21
SPIWrite 0225,54
SPIWrite 0226,05
SPIWrite 0227,f0
SPIWrite 0228,01
SPIWrite 0229,05
SPIWrite 022a,35
SPIWrite 022b,54
SPIWrite 022c,64
SPIWrite 022d,1c
SPIWrite 022e,22
SPIWrite 022f,54
SPIWrite 0230,1c

SPIWrite 0231,09
SPIWrite 0232,0a
SPIWrite 0233,d3
SPIWrite 0234,ac
SPIWrite 0235,f1
SPIWrite 0236,0d
SPIWrite 0237,06
SPIWrite 0238,87
SPIWrite 0239,f0
SPIWrite 023a,01
SPIWrite 023b,05
SPIWrite 023c,f4
SPIWrite 023d,1d
SPIWrite 023e,21
SPIWrite 023f,54
SPIWrite 0240,05
SPIWrite 0241,f0
SPIWrite 0242,01
SPIWrite 0243,05
SPIWrite 0244,35
SPIWrite 0245,54
SPIWrite 0246,64
SPIWrite 0247,1c
SPIWrite 0248,22
SPIWrite 0249,54
SPIWrite 024a,27
SPIWrite 024b,b1
SPIWrite 024c,05
SPIWrite 024d,48
SPIWrite 024e,00
SPIWrite 024f,68
SPIWrite 0250,04
SPIWrite 0251,46
SPIWrite 0252,18
SPIWrite 0253,46
SPIWrite 0254,a0
SPIWrite 0255,47
SPIWrite 0256,f8
SPIWrite 0257,bd
SPIWrite 0258,4a
SPIWrite 0259,00
SPIWrite 025a,00
SPIWrite 025b,a2
SPIWrite 025c,00
SPIWrite 025d,00
SPIWrite 025e,01
SPIWrite 025f,20
SPIWrite 0260,d8

SPIWrite 0261,33
SPIWrite 0262,00
SPIWrite 0263,20
SPIWrite 0264,64
SPIWrite 0265,57
SPIWrite 0266,00
SPIWrite 0267,20
SPIWrite 0268,00
SPIWrite 0269,21
SPIWrite 026a,4f
SPIWrite 026b,f0
SPIWrite 026c,2e
SPIWrite 026d,42
SPIWrite 026e,82
SPIWrite 026f,f8
SPIWrite 0270,a2
SPIWrite 0271,19
SPIWrite 0272,01
SPIWrite 0273,20
SPIWrite 0274,82
SPIWrite 0275,f8
SPIWrite 0276,a2
SPIWrite 0277,09
SPIWrite 0278,00
SPIWrite 0279,bf
SPIWrite 027a,82
SPIWrite 027b,f8
SPIWrite 027c,a2
SPIWrite 027d,19
SPIWrite 027e,82
SPIWrite 027f,f8
SPIWrite 0280,c2
SPIWrite 0281,1b
SPIWrite 0282,82
SPIWrite 0283,f8
SPIWrite 0284,c2
SPIWrite 0285,0b
SPIWrite 0286,00
SPIWrite 0287,bf
SPIWrite 0288,82
SPIWrite 0289,f8
SPIWrite 028a,c2
SPIWrite 028b,1b
SPIWrite 028c,4f
SPIWrite 028d,f0
SPIWrite 028e,2f
SPIWrite 028f,43
SPIWrite 0290,83

SPIWrite 0291,f8
SPIWrite 0292,a2
SPIWrite 0293,19
SPIWrite 0294,83
SPIWrite 0295,f8
SPIWrite 0296,a2
SPIWrite 0297,09
SPIWrite 0298,00
SPIWrite 0299,bf
SPIWrite 029a,83
SPIWrite 029b,f8
SPIWrite 029c,a2
SPIWrite 029d,19
SPIWrite 029e,83
SPIWrite 029f,f8
SPIWrite 02a0,c2
SPIWrite 02a1,1b
SPIWrite 02a2,83
SPIWrite 02a3,f8
SPIWrite 02a4,c2
SPIWrite 02a5,0b
SPIWrite 02a6,00
SPIWrite 02a7,bf
SPIWrite 02a8,12
SPIWrite 02a9,4a
SPIWrite 02aa,10
SPIWrite 02ab,88
SPIWrite 02ac,83
SPIWrite 02ad,f8
SPIWrite 02ae,c2
SPIWrite 02af,1b
SPIWrite 02b0,40
SPIWrite 02b1,1c
SPIWrite 02b2,10
SPIWrite 02b3,80
SPIWrite 02b4,70
SPIWrite 02b5,47
SPIWrite 02b6,00
SPIWrite 02b7,20
SPIWrite 02b8,70
SPIWrite 02b9,47
SPIWrite 02ba,10
SPIWrite 02bb,b5
SPIWrite 02bc,0e
SPIWrite 02bd,4c
SPIWrite 02be,d4
SPIWrite 02bf,f8
SPIWrite 02c0,c0

SPIWrite 02c1,01
SPIWrite 02c2,80
SPIWrite 02c3,47
SPIWrite 02c4,0b
SPIWrite 02c5,48
SPIWrite 02c6,d4
SPIWrite 02c7,f8
SPIWrite 02c8,08
SPIWrite 02c9,14
SPIWrite 02ca,80
SPIWrite 02cb,1e
SPIWrite 02cc,00
SPIWrite 02cd,88
SPIWrite 02ce,88
SPIWrite 02cf,47
SPIWrite 02d0,ff
SPIWrite 02d1,f7
SPIWrite 02d2,ca
SPIWrite 02d3,ff
SPIWrite 02d4,10
SPIWrite 02d5,bd
SPIWrite 02d6,10
SPIWrite 02d7,b5
SPIWrite 02d8,07
SPIWrite 02d9,4c
SPIWrite 02da,d4
SPIWrite 02db,f8
SPIWrite 02dc,c4
SPIWrite 02dd,01
SPIWrite 02de,80
SPIWrite 02df,47
SPIWrite 02e0,04
SPIWrite 02e1,48
SPIWrite 02e2,d4
SPIWrite 02e3,f8
SPIWrite 02e4,08
SPIWrite 02e5,14
SPIWrite 02e6,80
SPIWrite 02e7,1e
SPIWrite 02e8,00
SPIWrite 02e9,88
SPIWrite 02ea,88
SPIWrite 02eb,47
SPIWrite 02ec,ff
SPIWrite 02ed,f7
SPIWrite 02ee,bc
SPIWrite 02ef,ff
SPIWrite 02f0,10

```
SPIWrite 02f1,bd
SPIWrite 02f2,c0
SPIWrite 02f3,46
SPIWrite 02f4,04
SPIWrite 02f5,00
SPIWrite 02f6,01
SPIWrite 02f7,20
SPIWrite 02f8,08
SPIWrite 02f9,53
SPIWrite 02fa,00
SPIWrite 02fb,20
SPIWrite 0012,00
//PAGE:sys_calib_macro_memory=0(Meaning: );
SPIWrite 0013,10
//PAGE:customer_macro=1(Meaning: );
SPIRead 00f3
SPIRead 00f2
SPIRead 00f1
SPIRead 00f0


// Read // cm4_wr_spi_rf0: 0x1
SPIWrite 00a3,10
SPIWrite 00a2,00
SPIWrite 00a1,00
SPIWrite 00a0,00
SPIWrite 00a7,00
SPIWrite 00a6,00
SPIWrite 00a5,00
SPIWrite 00a4,00
SPIWrite 0193,81
SPIWrite 0192,00
SPIWrite 0191,00
SPIWrite 0190,00
SPIRead 00f3
SPIRead 00f2
SPIRead 00f1
SPIRead 00f0


// Read // cm4_wr_spi_rf0: 0x7
SPIRead 00f3
SPIRead 00f2
SPIRead 00f1
SPIRead 00f0


// Read // cm4_wr_spi_rf0: 0x7
```

```
SPIWrite 0013,00
//PAGE:customer_macro=0(Meaning: );
SPIWrite 0013,20
//PAGE:cm4_macro=1
SPIRead 0020


// Read // MACRO_READY: 0x1
SPIRead 0020


// Read // MACRO_ACK: 0x1
SPIRead 0020


// Read // MACRO_DONE: 0x1
SPIRead 0020


// Read // MACRO_ERROR: 0x0
SPIWrite 0013,00
//PAGE:cm4_macro=0
SPIWrite 0013,10
//PAGE:customer_macro=1(Meaning: );
SPIRead 00f3
SPIRead 00f2
SPIRead 00f1
SPIRead 00f0


// Read // cm4_wr_spi_rf0: 0x7
SPIWrite 00a3,10
SPIWrite 00a2,00
SPIWrite 00a1,00
SPIWrite 00a0,01
SPIWrite 00a7,00
SPIWrite 00a6,00
SPIWrite 00a5,00
SPIWrite 00a4,00
SPIWrite 0193,81
SPIWrite 0192,00
SPIWrite 0191,00
SPIWrite 0190,00
SPIRead 00f3
SPIRead 00f2
SPIRead 00f1
SPIRead 00f0
```

// Read // cm4_wr_spi_rf0: 0x7
SPIRead 00f3
SPIRead 00f2
SPIRead 00f1
SPIRead 00f0

// Read // cm4_wr_spi_rf0: 0x7
SPIWrite 0013,00
//PAGE:customer_macro=0(Meaning:);
SPIWrite 0013,20
//PAGE:cm4_macro=1
SPIRead 0020

// Read // MACRO_READY: 0x1
SPIRead 0020

// Read // MACRO_ACK: 0x1
SPIRead 0020

// Read // MACRO_DONE: 0x1
SPIRead 0020

// Read // MACRO_ERROR: 0x0
SPIWrite 0013,00

//Step: Run TX DSA Gain swap Macro.
SPIWrite 0013,10
SPIWrite 00A3,00
SPIWrite 00A2,00
SPIWrite 00A1,00
SPIWrite 00A0,01
SPIWrite 00A7,00
SPIWrite 00A6,00
SPIWrite 00A5,00
SPIWrite 00A4,0F
SPIWrite 0193,42
SPIWrite 0192,00
SPIWrite 0191,00
SPIWrite 0190,00
SPIWrite 0013,00
SPIWrite 0013,20

```
WAIT 5
SPIRead 0020
SPIWrite 0013,00



SPIWrite 0013,10
//PAGE:customer_macro=1(Meaning: );
SPIWrite 0140,00
SPIWrite 0144,00
SPIWrite 0013,00
//PAGE:customer_macro=0(Meaning: );
SPIWrite 0013,02
//PAGE:cm4top_dram=1(Meaning: );
SPIWrite 3490,ff
SPIWrite 3491,ff
SPIWrite 3492,ff
SPIWrite 3493,ff
SPIWrite 0013,00
//PAGE:cm4top_dram=0(Meaning: );
SPIWrite 0013,10
//PAGE:customer_macro=1(Meaning: );
SPIWrite 0140,00
SPIWrite 0144,00
SPIWrite 0013,00
//PAGE:customer_macro=0(Meaning: );
SPIWrite 0013,02
//PAGE:cm4top_dram=1(Meaning: );
SPIWrite 3494,00
SPIWrite 3495,00
SPIWrite 3496,00
SPIWrite 3497,00
SPIWrite 0013,00
//PAGE:cm4top_dram=0(Meaning: );
SPIWrite 0013,10
//PAGE:customer_macro=1(Meaning: );
SPIWrite 0140,00
SPIWrite 0144,00
SPIWrite 0013,00
//PAGE:customer_macro=0(Meaning: );
SPIWrite 0013,02
//PAGE:cm4top_dram=1(Meaning: );
SPIWrite 349c,ff
SPIWrite 349d,ff
SPIWrite 349e,ff
SPIWrite 349f,7f
SPIWrite 0013,00
```

```
//PAGE:cm4top_dram=0(Meaning: );
SPIWrite 0013,10
//PAGE:customer_macro=1(Meaning: );
SPIWrite 0140,00
SPIWrite 0144,00
SPIWrite 0013,00
//PAGE:customer_macro=0(Meaning: );
SPIWrite 0013,02
//PAGE:cm4top_dram=1(Meaning: );
SPIWrite 3498,00
SPIWrite 3499,00
SPIWrite 349a,00
SPIWrite 349b,80
SPIWrite 0013,00
```

```
//**********Step: Relinquishing access to CM4***********//
// CM4 access to PLL Pages
SPIWrite 0015,80
//PAGE:DIGTOP_MISC=1(Meaning: );
SPIWrite 01d4,00
SPIWrite 0374,00
//pll_reg_spi_req_a=1
SPIRead 01d5

SPIWrite 0015,00
//PAGE:DIGTOP_MISC=0(Meaning: );
// Done requesting/releasing SPI Access to PLL Pages


//**********Step: TXCD Page same as PG1P0***********//
//PG1P1: TX DSA writes to make TXCD DSA page look like PG1P0
SPIWrite 0015,80
SPIWrite 0649,80
SPIWrite 0015,00

//Step:Tx DSA en_byp_change_pulse=1
SPIWrite 0016,30
SPIWrite 09A3,01
SPIWrite 0bc3,01
SPIWrite 0016,00
```

```
//**********Step: Temperature Sensor(Internal Use)**********//
//PG1P1:
SPIWrite 0015,80
SPIWrite 03a3,08
SPIWrite 0015,00


//**********Step: Setting DSA phase error range to 100deg**********//
SPIWrite 0013,02
SPIWrite 3515,64
SPIWrite 0013,00

//******************Band Specific Start***************//
//Band 2=2.6G
//**********Step: Setting global Variable. TempSacle,TempMax,TempMin, Packet
Reload=1,Nyq=4**********//
PG1P1: Set global variables for fuse packet Load Nyquist=2
SPIWrite 0013,02
SPIWrite 3ed8,20
SPIWrite 3eda,CE
SPIWrite 3edb,FF
SPIWrite 3edc,7F
SPIWrite 3edd,00
SPIWrite 3F2c,01
SPIWrite 3F2d,01
SPIWrite 3F2e,01
SPIWrite 3F2f,01
SPIWrite 0013,00


//******************Band Specific Stop*****************//

//**********Step: Converter Rate coniguration Macro: 48X**********//
//PG1P1: Configuration for 48X, 54X, 56X modes only for packet Load. Configure 48X 2949.12M
SPIWrite 0013,10
SPIWrite 00A3,00
SPIWrite 00A2,00
SPIWrite 00A1,00
SPIWrite 00A0,00
SPIWrite 0193,25
SPIWrite 0192,00
SPIWrite 0191,00
SPIWrite 0190,00

SPIWrite 0013,20

WAIT 5
SPIRead 0020
```

```
// Read // MACRO_STATUS_RESULT_0: 7
SPIWrite 0013,00
//**********Step: Interface Rate configuration Macro: 4X for Rx,8X for Tx and Fb**********//
// Read // cm4_wr_spi_rf0: 0x7
SPIWrite 0013,10
SPIWrite 00a3,05
SPIWrite 00a2,04
SPIWrite 00a1,05
SPIWrite 00a0,04
SPIWrite 00a7,00
SPIWrite 00a6,00
SPIWrite 00a5,04
SPIWrite 00a4,04
SPIWrite 0193,26
SPIWrite 0192,00
SPIWrite 0191,00
SPIWrite 0190,00
SPIWrite 0013,00
//PAGE:customer_macro=0(Meaning: );
SPIWrite 0013,20
WAIT 5

SPIRead 0020
SPIWrite 0013,00

//**********Step: Fuse Packet Load (Only PLL)**********//
//PG1P1: Packet Load through MCU

SPIWrite 0013,10
SPIWrite 00A3,00
SPIWrite 00A2,1F
SPIWrite 00A1,7D
SPIWrite 00A0,00
SPIWrite 00A7,08
SPIWrite 00A6,09
SPIWrite 00A5,02
SPIWrite 00A4,00
SPIWrite 0193,12
SPIWrite 0192,00
SPIWrite 0191,00
SPIWrite 0190,00
SPIWrite 0013,00

SPIWrite 0013,20
//PAGE:cm4_macro=1
WAIT 5
SPIRead 0020
// Read // MACRO_STATUS_RESULT_0: 7
```

```
SPIWrite 0013,00

//**********Step: Start Temperature compensation process Macro**********//
//Temperature Tracking of Trim
SPIWrite 0013,10
SPIWrite 00A3,00
SPIWrite 00A2,00
SPIWrite 00A1,01
SPIWrite 00A0,01
SPIWrite 0193,14
SPIWrite 0192,00
SPIWrite 0191,00
SPIWrite 0190,00


SPIWrite 0013,20
//PAGE:cm4_macro=1
WAIT 5
SPIRead 0020
// Read // MACRO_STATUS_RESULT_0: 7
SPIWrite 0013,00


//Requesting/releasing SPI Access to PLL Pages
SPIWrite 0015,80
//PAGE:DIGTOP_MISC=1(Meaning: );
SPIWrite 01d4,01
WAIT 1
//pll_reg_spi_req_a=1
SPIRead 01d5


// Read // pll_reg_spi_a_ack: 1(Meaning: access acknowledge)


SPIWrite 0015,00
//PAGE:DIGTOP_MISC=0(Meaning: );
// Done requesting/releasing SPI Access to PLL Pages

// Configure PLL0
SPIWrite 0014,08
//PAGE:pll=1
SPIWrite 004b,33
//PLL_SPARE0=cc000
SPIWrite 004a,00
SPIWrite 0049,00
SPIWrite 005e,97
//EN_VCO=1
```

SPIWrite 0028,15
//N=15
SPIWrite 0036,15
//N_to_CAL=15
SPIWrite 0035,08
//CAL_CONTROL=8
SPIWrite 0051,06
//CTL_REF_DIV=1(Meaning:);
SPIWrite 0050,40
SPIWrite 0051,06
//EN_DIV8_CLK_TO_PLLDIG=1
SPIWrite 0051,06
//EN_CLK_TO_PLLDIG=1
SPIWrite 0051,0e
//EN_SYNC_TO_PLLDIG_DIV=1
SPIWrite 003c,40
//CTL_DIV_23_45=0
SPIWrite 005e,97
//EN_FRAC_N_MODE=1
SPIWrite 0033,03
//EN_FRAC_MODE=1
SPIWrite 003f,0c
//CTL_TEST_MUX=0
SPIWrite 0049,01
//EN_VCO_PKDET=1
SPIWrite 0048,2f
//VCO_PKDT_BIAS=7
SPIWrite 0044,27
//CTL_VCO_IB_GM=7
SPIWrite 0043,4c
//CTL_VCO_IB_TAIL=c
SPIWrite 0043,0c
//CTL_VCO_IB_GM_SLOPE=0
SPIWrite 0042,04
//CTL_VCO_IB_TAIL_SLOPE=0
SPIWrite 0046,00
//CTL_VCO_IB_GM1=0
SPIWrite 0040,28
//CTL_VB_VAR_SLOPE=0
SPIWrite 002e,00
//F=7980
SPIWrite 002d,70
SPIWrite 002c,80
SPIWrite 0032,03
//D=3c000
SPIWrite 0031,c0
SPIWrite 0030,00
SPIWrite 0033,03

```
//F_order=1
SPIWrite 0039,40
//EN_LOCK_DETECT=1
SPIWrite 003f,14
//CTL_PFD_DEL=2
SPIWrite 003f,12
//CTL_OUT_DIV=2
SPIWrite 003c,40
//CTL_LDO_ANA=4
SPIWrite 003d,24
//CTL_LDO_RF=4
SPIWrite 0052,10
//CTL_FBDIV_LDO_PROG=8
SPIWrite 003a,08
//CTL_CP_IREF=2
SPIWrite 003b,30
//CTL_CP_IOUT=3
SPIWrite 0034,03
//lock_acc=3
SPIWrite 0034,0f
//lock_cnt=3
SPIWrite 0034,1f
//lock_err=1
SPIWrite 0066,04
//lock_rst=1
SPIWrite 0066,00
//lock_rst=0
SPIWrite 0066,08
//lock_lost_rst=1
SPIWrite 0066,00
//lock_lost_rst=0
SPIWrite 0034,1f
//EN_CAL=0
SPIWrite 0034,5f
//EN_CAL=1

WAIT 2

AFE77xx_GLOBAL
SPIWrite 005e,9f
//EN_I_OFFSET=1
SPIWrite 003c,40
//CTL_I_OFST_UP_DN=0
SPIWrite 0065,12
//CTL_I_OFST_REF=1
SPIWrite 003c,44
//CTL_I_OFFSET=1
```

```
// SPIPoll 0062,7,7,1


AFE77xx_GLOBAL
SPIRead 0062


// Read // lock: 0x1


SPIWrite 0014,00


AFE77xx_GLOBAL
SPIWrite 0014,10
//PAGE:pll=2
SPIWrite 005e,97
//EN_VCO=1
SPIWrite 0028,12
//N=12
SPIWrite 0036,12
//N_to_CAL=12
SPIWrite 0035,08
//CAL_CONTROL=8
SPIWrite 0051,06
//CTL_REF_DIV=1(Meaning: );
SPIWrite 0050,40
SPIWrite 0051,06
//EN_DIV8_CLK_TO_PLLDIG=1
SPIWrite 0051,06
//EN_CLK_TO_PLLDIG=1
SPIWrite 0051,0e
//EN_SYNC_TO_PLLDIG_DIV=1
SPIWrite 003c,40
//CTL_DIV_23_45=0
SPIWrite 005e,96
//EN_FRAC_N_MODE=0
SPIWrite 0033,02
//EN_FRAC_MODE=0
SPIWrite 003f,0c
//CTL_TEST_MUX=0
SPIWrite 0049,01
//EN_VCO_PKDET=1
SPIWrite 0048,2f
//VCO_PKDT_BIAS=7
SPIWrite 0044,27
//CTL_VCO_IB_GM=7
```

```
SPIWrite 0043,4c
//CTL_VCO_IB_TAIL=c
SPIWrite 0043,0c
//CTL_VCO_IB_GM_SLOPE=0
SPIWrite 0042,04
//CTL_VCO_IB_TAIL_SLOPE=0
SPIWrite 0046,00
//CTL_VCO_IB_GM1=0
SPIWrite 0040,28
//CTL_VB_VAR_SLOPE=0
SPIWrite 002e,00
//F=0
SPIWrite 002d,00
SPIWrite 002c,00
SPIWrite 0032,02
//D=20000
SPIWrite 0031,00
SPIWrite 0030,00
SPIWrite 0033,02
//F_order=1
SPIWrite 0039,40
//EN_LOCK_DETECT=1
SPIWrite 003f,14
//CTL_PFD_DEL=2
SPIWrite 003f,13
//CTL_OUT_DIV=3
SPIWrite 003c,40
//CTL_LDO_ANA=4
SPIWrite 003d,24
//CTL_LDO_RF=4
SPIWrite 0052,10
//CTL_FBDIV_LDO_PROG=8
SPIWrite 003a,04
//CTL_CP_IREF=1
SPIWrite 003b,10
//CTL_CP_IOUT=1
SPIWrite 0034,03
//lock_acc=3
SPIWrite 0034,0f
//lock_cnt=3
SPIWrite 0034,1f
//lock_err=1
SPIWrite 0066,04
//lock_rst=1
SPIWrite 0066,00
//lock_rst=0
SPIWrite 0066,08
//lock_lost_rst=1
```

```
SPIWrite 0066,00
//lock_lost_rst=0
SPIWrite 0034,1f
//EN_CAL=0
SPIWrite 0034,5f
//EN_CAL=1

WAIT 2

AFE77xx_GLOBAL
SPIWrite 005e,96
//EN_I_OFFSET=0


// SPIPoll 0062,7,7,1


AFE77xx_GLOBAL
SPIRead 0062


// Read // lock: 0x1
SPIWrite 0051,0c
//EN_DIV8_CLK_TO_PLLDIG=0


// END: Done configuring PLL


AFE77xx_GLOBAL
SPIWrite 0014,00
//PAGE:pll=0

// END: Done configuring PLL
//**********Step: Power down Unused PLL**********//


// Powers up/down the PLL2
SPIWrite 0014,20
//PAGE:pll=4
SPIWrite 005e,17
//EN_VCO=0


// Powers up/down the PLL3
SPIWrite 0014,40
//PAGE:pll=8
SPIWrite 005e,17
```

```
//EN_VCO=0


// Powers up/down the PLL4
SPIWrite 0014,80
//PAGE:pll=10
SPIWrite 005e,17
//EN_VCO=0
SPIWrite 0014,00
//PAGE:pll=0


//**********Step: Cm4 Clock Enable clock, Enable Dither, Switch to PLL Clock**********//
SPIWrite 0013,20
//PAGE:cm4_macro=1
SPIWrite 0084,21
SPIWrite 0084,61
SPIWrite 0084,21
SPIWrite 0084,21
SPIWrite 0084,01
SPIWrite 0088,01
SPIWrite 0013,00

//**********Step: Packet Load(2.6GLO: (0,4,7,10,11,17,20)) using CM4 (All fixed and Flexi
Packets)**********//
SPIWrite 00a3,00
SPIWrite 00a2,00
SPIWrite 00a1,00
SPIWrite 00a0,00
SPIWrite 00a7,04
SPIWrite 00a6,00
SPIWrite 00a5,07
SPIWrite 00a4,00
SPIWrite 00ab,11
SPIWrite 00aa,0b
SPIWrite 00a9,0a
SPIWrite 00a8,07
SPIWrite 00af,00
SPIWrite 00ae,00
SPIWrite 00ad,00
SPIWrite 00ac,14
SPIWrite 0193,12
SPIWrite 0192,00
SPIWrite 0191,00
SPIWrite 0190,00
SPIWrite 0013,00

SPIWrite 0013,20
```

```
//PAGE:cm4_macro=1
WAIT 5
SPIRead 0020
// Read // MACRO_STATUS_RESULT_0: 7
SPIWrite 0013,00
/*********************************************************/

// Doing Top level initialization
//**********Step: Setting Serdes Clock divider**********//
//PAGE:cm4_macro=0
SPIWrite 0018,01
//PAGE:ana_4t4r=1(Meaning: );
SPIWrite 0050,00
SPIWrite 0054,00
SPIWrite 0050,18
SPIWrite 0054,18
SPIWrite 0018,00


//**********Step: Setting Rx DSA codes to values**********//
//PAGE:ana_4t4r=0(Meaning: );
SPIWrite 0016,30
//PAGE:dsa=3
SPIWrite 0180,01
SPIWrite 0677,01
SPIWrite 0676,f0
SPIWrite 0675,03
SPIWrite 0674,e0
SPIWrite 067b,01
SPIWrite 067a,f0
SPIWrite 0679,03
SPIWrite 0678,21
SPIWrite 067f,01
SPIWrite 067e,f0
SPIWrite 067d,02
SPIWrite 067c,82
SPIWrite 0683,01
SPIWrite 0682,f0
SPIWrite 0681,02
SPIWrite 0680,23
SPIWrite 0687,01
SPIWrite 0686,f0
SPIWrite 0685,01
SPIWrite 0684,c4
SPIWrite 068b,01
SPIWrite 068a,f0
SPIWrite 0689,01
SPIWrite 0688,85
```

SPIWrite 068f,01
SPIWrite 068e,f0
SPIWrite 068d,01
SPIWrite 068c,46
SPIWrite 0693,01
SPIWrite 0692,f0
SPIWrite 0691,01
SPIWrite 0690,27
SPIWrite 0697,01
SPIWrite 0696,e0
SPIWrite 0695,01
SPIWrite 0694,08
SPIWrite 069b,01
SPIWrite 069a,e0
SPIWrite 0699,00
SPIWrite 0698,e9
SPIWrite 069f,01
SPIWrite 069e,f0
SPIWrite 069d,00
SPIWrite 069c,ca
SPIWrite 06a3,01
SPIWrite 06a2,f0
SPIWrite 06a1,00
SPIWrite 06a0,ab
SPIWrite 06a7,01
SPIWrite 06a6,f0
SPIWrite 06a5,00
SPIWrite 06a4,8c
SPIWrite 06ab,01
SPIWrite 06aa,f0
SPIWrite 06a9,00
SPIWrite 06a8,8d
SPIWrite 06af,01
SPIWrite 06ae,f0
SPIWrite 06ad,00
SPIWrite 06ac,6e
SPIWrite 06b3,01
SPIWrite 06b2,f0
SPIWrite 06b1,00
SPIWrite 06b0,6f
SPIWrite 06b7,01
SPIWrite 06b6,d0
SPIWrite 06b5,00
SPIWrite 06b4,70
SPIWrite 06bb,01
SPIWrite 06ba,b0
SPIWrite 06b9,00
SPIWrite 06b8,71

SPIWrite 06bf,01
SPIWrite 06be,80
SPIWrite 06bd,00
SPIWrite 06bc,72
SPIWrite 06c3,01
SPIWrite 06c2,50
SPIWrite 06c1,00
SPIWrite 06c0,73
SPIWrite 06c7,01
SPIWrite 06c6,20
SPIWrite 06c5,00
SPIWrite 06c4,74
SPIWrite 06cb,00
SPIWrite 06ca,60
SPIWrite 06c9,00
SPIWrite 06c8,75
SPIWrite 06cf,00
SPIWrite 06ce,20
SPIWrite 06cd,00
SPIWrite 06cc,76
SPIWrite 06d3,00
SPIWrite 06d2,00
SPIWrite 06d1,00
SPIWrite 06d0,77
SPIWrite 06d7,00
SPIWrite 06d6,00
SPIWrite 06d5,00
SPIWrite 06d4,78
SPIWrite 06db,00
SPIWrite 06da,40
SPIWrite 06d9,00
SPIWrite 06d8,59
SPIWrite 06df,00
SPIWrite 06de,00
SPIWrite 06dd,00
SPIWrite 06dc,5a
SPIWrite 06e3,00
SPIWrite 06e2,00
SPIWrite 06e1,00
SPIWrite 06e0,5b
SPIWrite 06e7,00
SPIWrite 06e6,00
SPIWrite 06e5,00
SPIWrite 06e4,5c
SPIWrite 06eb,01
SPIWrite 06ea,30
SPIWrite 06e9,00
SPIWrite 06e8,3d

SPIWrite 06ef,00
SPIWrite 06ee,f0
SPIWrite 06ed,00
SPIWrite 06ec,3e
SPIWrite 06f3,00
SPIWrite 06f2,f0
SPIWrite 06f1,00
SPIWrite 06f0,3e
SPIWrite 06f7,00
SPIWrite 06f6,f0
SPIWrite 06f5,00
SPIWrite 06f4,3e
SPIWrite 06fb,00
SPIWrite 06fa,f0
SPIWrite 06f9,00
SPIWrite 06f8,3e
SPIWrite 06ff,00
SPIWrite 06fe,f0
SPIWrite 06fd,00
SPIWrite 06fc,3e
SPIWrite 0703,00
SPIWrite 0702,f0
SPIWrite 0701,00
SPIWrite 0700,3e
SPIWrite 0707,00
SPIWrite 0706,f0
SPIWrite 0705,00
SPIWrite 0704,3e
SPIWrite 0317,01
SPIWrite 0316,f0
SPIWrite 0315,03
SPIWrite 0314,e0
SPIWrite 031b,01
SPIWrite 031a,f0
SPIWrite 0319,03
SPIWrite 0318,21
SPIWrite 031f,01
SPIWrite 031e,f0
SPIWrite 031d,02
SPIWrite 031c,82
SPIWrite 0323,01
SPIWrite 0322,f0
SPIWrite 0321,02
SPIWrite 0320,23
SPIWrite 0327,01
SPIWrite 0326,f0
SPIWrite 0325,01
SPIWrite 0324,c4

SPIWrite 032b,01
SPIWrite 032a,f0
SPIWrite 0329,01
SPIWrite 0328,85
SPIWrite 032f,01
SPIWrite 032e,f0
SPIWrite 032d,01
SPIWrite 032c,46
SPIWrite 0333,01
SPIWrite 0332,f0
SPIWrite 0331,01
SPIWrite 0330,27
SPIWrite 0337,01
SPIWrite 0336,e0
SPIWrite 0335,01
SPIWrite 0334,08
SPIWrite 033b,01
SPIWrite 033a,e0
SPIWrite 0339,00
SPIWrite 0338,e9
SPIWrite 033f,01
SPIWrite 033e,f0
SPIWrite 033d,00
SPIWrite 033c,ca
SPIWrite 0343,01
SPIWrite 0342,f0
SPIWrite 0341,00
SPIWrite 0340,ab
SPIWrite 0347,01
SPIWrite 0346,f0
SPIWrite 0345,00
SPIWrite 0344,8c
SPIWrite 034b,01
SPIWrite 034a,f0
SPIWrite 0349,00
SPIWrite 0348,8d
SPIWrite 034f,01
SPIWrite 034e,f0
SPIWrite 034d,00
SPIWrite 034c,6e
SPIWrite 0353,01
SPIWrite 0352,f0
SPIWrite 0351,00
SPIWrite 0350,6f
SPIWrite 0357,01
SPIWrite 0356,d0
SPIWrite 0355,00
SPIWrite 0354,70

SPIWrite 035b,01
SPIWrite 035a,b0
SPIWrite 0359,00
SPIWrite 0358,71
SPIWrite 035f,01
SPIWrite 035e,80
SPIWrite 035d,00
SPIWrite 035c,72
SPIWrite 0363,01
SPIWrite 0362,50
SPIWrite 0361,00
SPIWrite 0360,73
SPIWrite 0367,01
SPIWrite 0366,20
SPIWrite 0365,00
SPIWrite 0364,74
SPIWrite 036b,00
SPIWrite 036a,60
SPIWrite 0369,00
SPIWrite 0368,75
SPIWrite 036f,00
SPIWrite 036e,20
SPIWrite 036d,00
SPIWrite 036c,76
SPIWrite 0373,00
SPIWrite 0372,00
SPIWrite 0371,00
SPIWrite 0370,77
SPIWrite 0377,00
SPIWrite 0376,00
SPIWrite 0375,00
SPIWrite 0374,78
SPIWrite 037b,00
SPIWrite 037a,40
SPIWrite 0379,00
SPIWrite 0378,59
SPIWrite 037f,00
SPIWrite 037e,00
SPIWrite 037d,00
SPIWrite 037c,5a
SPIWrite 0383,00
SPIWrite 0382,00
SPIWrite 0381,00
SPIWrite 0380,5b
SPIWrite 0387,00
SPIWrite 0386,00
SPIWrite 0385,00
SPIWrite 0384,5c

SPIWrite 038b,01
SPIWrite 038a,30
SPIWrite 0389,00
SPIWrite 0388,3d
SPIWrite 038f,00
SPIWrite 038e,f0
SPIWrite 038d,00
SPIWrite 038c,3e
SPIWrite 0393,00
SPIWrite 0392,f0
SPIWrite 0391,00
SPIWrite 0390,3e
SPIWrite 0397,00
SPIWrite 0396,f0
SPIWrite 0395,00
SPIWrite 0394,3e
SPIWrite 039b,00
SPIWrite 039a,f0
SPIWrite 0399,00
SPIWrite 0398,3e
SPIWrite 039f,00
SPIWrite 039e,f0
SPIWrite 039d,00
SPIWrite 039c,3e
SPIWrite 03a3,00
SPIWrite 03a2,f0
SPIWrite 03a1,00
SPIWrite 03a0,3e
SPIWrite 03a7,00
SPIWrite 03a6,f0
SPIWrite 03a5,00
SPIWrite 03a4,3e

SPIWrite 02fb,00
SPIWrite 065b,00
SPIWrite 02fd,00
SPIWrite 065d,00
SPIWrite 02fe,00
SPIWrite 0305,00
SPIWrite 030e,00
SPIWrite 065e,00
SPIWrite 0665,00
SPIWrite 066e,00
SPIWrite 0040,03
SPIWrite 0311,00
SPIWrite 0671,00
SPIWrite 02c8,01
SPIWrite 02d0,01

SPIWrite 0630,01
SPIWrite 09a8,ff
SPIWrite 09b0,ff
SPIWrite 09b8,ff
SPIWrite 09c0,ff
SPIWrite 09c8,ff
SPIWrite 09d0,ff
SPIWrite 09d8,ff
SPIWrite 09e0,ff
SPIWrite 09e8,ff
SPIWrite 09f0,ff
SPIWrite 09f8,ff
SPIWrite 0a00,ff
SPIWrite 0a08,ff
SPIWrite 0a10,ff
SPIWrite 0a18,ff
SPIWrite 0a20,ff
SPIWrite 0a28,ff
SPIWrite 0a30,ff
SPIWrite 0a38,ff
SPIWrite 0a40,ff
SPIWrite 0a48,ff
SPIWrite 0a50,ff
SPIWrite 0a58,ff
SPIWrite 0a60,ff
SPIWrite 0a68,ff
SPIWrite 0a70,ff
SPIWrite 0a78,ff
SPIWrite 0a80,ff
SPIWrite 0a88,ff
SPIWrite 0a90,ff
SPIWrite 0a98,ff
SPIWrite 0aa0,ff
SPIWrite 0aa8,ff
SPIWrite 0ab0,fe
SPIWrite 0ab8,fc
SPIWrite 0ac0,f8
SPIWrite 0ac8,f0
SPIWrite 0ad0,e0
SPIWrite 0ad8,c0
SPIWrite 0ae0,80
SPIWrite 09af,ff
SPIWrite 09ae,ff
SPIWrite 09ad,ff
SPIWrite 09ac,ff
SPIWrite 09b7,ff
SPIWrite 09b6,ff
SPIWrite 09b5,ff

SPIWrite 09b4,fe
SPIWrite 09bf,ff
SPIWrite 09be,ff
SPIWrite 09bd,ff
SPIWrite 09bc,fc
SPIWrite 09c7,ff
SPIWrite 09c6,ff
SPIWrite 09c5,ff
SPIWrite 09c4,f8
SPIWrite 09cf,ff
SPIWrite 09ce,ff
SPIWrite 09cd,ff
SPIWrite 09cc,f0
SPIWrite 09d7,ff
SPIWrite 09d6,ff
SPIWrite 09d5,ff
SPIWrite 09d4,e0
SPIWrite 09df,ff
SPIWrite 09de,ff
SPIWrite 09dd,ff
SPIWrite 09dc,c0
SPIWrite 09e7,ff
SPIWrite 09e6,ff
SPIWrite 09e5,ff
SPIWrite 09e4,80
SPIWrite 09ef,ff
SPIWrite 09ee,ff
SPIWrite 09ed,ff
SPIWrite 09ec,00
SPIWrite 09f7,ff
SPIWrite 09f6,ff
SPIWrite 09f5,fe
SPIWrite 09f4,00
SPIWrite 09ff,ff
SPIWrite 09fe,ff
SPIWrite 09fd,fc
SPIWrite 09fc,00
SPIWrite 0a07,ff
SPIWrite 0a06,ff
SPIWrite 0a05,f8
SPIWrite 0a04,00
SPIWrite 0a0f,ff
SPIWrite 0a0e,ff
SPIWrite 0a0d,f0
SPIWrite 0a0c,00
SPIWrite 0a17,ff
SPIWrite 0a16,ff
SPIWrite 0a15,e0

SPIWrite 0a14,00
SPIWrite 0a1f,ff
SPIWrite 0a1e,ff
SPIWrite 0a1d,c0
SPIWrite 0a1c,00
SPIWrite 0a27,ff
SPIWrite 0a26,ff
SPIWrite 0a25,80
SPIWrite 0a24,00
SPIWrite 0a2f,ff
SPIWrite 0a2e,ff
SPIWrite 0a2d,00
SPIWrite 0a2c,00
SPIWrite 0a37,ff
SPIWrite 0a36,fe
SPIWrite 0a35,00
SPIWrite 0a34,00
SPIWrite 0a3f,ff
SPIWrite 0a3e,fc
SPIWrite 0a3d,00
SPIWrite 0a3c,00
SPIWrite 0a47,ff
SPIWrite 0a46,f8
SPIWrite 0a45,00
SPIWrite 0a44,00
SPIWrite 0a4f,ff
SPIWrite 0a4e,f0
SPIWrite 0a4d,00
SPIWrite 0a4c,00
SPIWrite 0a57,ff
SPIWrite 0a56,e0
SPIWrite 0a55,00
SPIWrite 0a54,00
SPIWrite 0a5f,ff
SPIWrite 0a5e,c0
SPIWrite 0a5d,00
SPIWrite 0a5c,00
SPIWrite 0a67,ff
SPIWrite 0a66,80
SPIWrite 0a65,00
SPIWrite 0a64,00
SPIWrite 0a6f,ff
SPIWrite 0a6e,00
SPIWrite 0a6d,00
SPIWrite 0a6c,00
SPIWrite 0a77,fe
SPIWrite 0a76,00
SPIWrite 0a75,00

SPIWrite 0a74,00
SPIWrite 0a7f,fc
SPIWrite 0a7e,00
SPIWrite 0a7d,00
SPIWrite 0a7c,00
SPIWrite 0a87,f8
SPIWrite 0a86,00
SPIWrite 0a85,00
SPIWrite 0a84,00
SPIWrite 0a8f,f0
SPIWrite 0a8e,00
SPIWrite 0a8d,00
SPIWrite 0a8c,00
SPIWrite 0a97,e0
SPIWrite 0a96,00
SPIWrite 0a95,00
SPIWrite 0a94,00
SPIWrite 0a9f,c0
SPIWrite 0a9e,00
SPIWrite 0a9d,00
SPIWrite 0a9c,00
SPIWrite 0aa7,80
SPIWrite 0aa6,00
SPIWrite 0aa5,00
SPIWrite 0aa4,00
SPIWrite 0aaf,00
SPIWrite 0aae,00
SPIWrite 0aad,00
SPIWrite 0aac,00
SPIWrite 0ab7,00
SPIWrite 0ab6,00
SPIWrite 0ab5,00
SPIWrite 0ab4,00
SPIWrite 0abf,00
SPIWrite 0abe,00
SPIWrite 0abd,00
SPIWrite 0abc,00
SPIWrite 0ac7,00
SPIWrite 0ac6,00
SPIWrite 0ac5,00
SPIWrite 0ac4,00
SPIWrite 0acf,00
SPIWrite 0ace,00
SPIWrite 0acd,00
SPIWrite 0acc,00
SPIWrite 0ad7,00
SPIWrite 0ad6,00
SPIWrite 0ad5,00

SPIWrite 0ad4,00
SPIWrite 0adf,00
SPIWrite 0ade,00
SPIWrite 0add,00
SPIWrite 0adc,00
SPIWrite 0ae7,00
SPIWrite 0ae6,00
SPIWrite 0ae5,00
SPIWrite 0ae4,00
SPIWrite 0bc8,ff
SPIWrite 0bd0,ff
SPIWrite 0bd8,ff
SPIWrite 0be0,ff
SPIWrite 0be8,ff
SPIWrite 0bf0,ff
SPIWrite 0bf8,ff
SPIWrite 0c00,ff
SPIWrite 0c08,ff
SPIWrite 0c10,ff
SPIWrite 0c18,ff
SPIWrite 0c20,ff
SPIWrite 0c28,ff
SPIWrite 0c30,ff
SPIWrite 0c38,ff
SPIWrite 0c40,ff
SPIWrite 0c48,ff
SPIWrite 0c50,ff
SPIWrite 0c58,ff
SPIWrite 0c60,ff
SPIWrite 0c68,ff
SPIWrite 0c70,ff
SPIWrite 0c78,ff
SPIWrite 0c80,ff
SPIWrite 0c88,ff
SPIWrite 0c90,ff
SPIWrite 0c98,ff
SPIWrite 0ca0,ff
SPIWrite 0ca8,ff
SPIWrite 0cb0,ff
SPIWrite 0cb8,ff
SPIWrite 0cc0,ff
SPIWrite 0cc8,ff
SPIWrite 0cd0,fe
SPIWrite 0cd8,fc
SPIWrite 0ce0,f8
SPIWrite 0ce8,f0
SPIWrite 0cf0,e0
SPIWrite 0cf8,c0

SPIWrite 0d00,80
SPIWrite 0bcf,ff
SPIWrite 0bce,ff
SPIWrite 0bcd,ff
SPIWrite 0bcc,ff
SPIWrite 0bd7,ff
SPIWrite 0bd6,ff
SPIWrite 0bd5,ff
SPIWrite 0bd4,fe
SPIWrite 0bdf,ff
SPIWrite 0bde,ff
SPIWrite 0bdd,ff
SPIWrite 0bdc,fc
SPIWrite 0be7,ff
SPIWrite 0be6,ff
SPIWrite 0be5,ff
SPIWrite 0be4,f8
SPIWrite 0bef,ff
SPIWrite 0bee,ff
SPIWrite 0bed,ff
SPIWrite 0bec,f0
SPIWrite 0bf7,ff
SPIWrite 0bf6,ff
SPIWrite 0bf5,ff
SPIWrite 0bf4,e0
SPIWrite 0bff,ff
SPIWrite 0bfe,ff
SPIWrite 0bfd,ff
SPIWrite 0bfc,c0
SPIWrite 0c07,ff
SPIWrite 0c06,ff
SPIWrite 0c05,ff
SPIWrite 0c04,80
SPIWrite 0c0f,ff
SPIWrite 0c0e,ff
SPIWrite 0c0d,ff
SPIWrite 0c0c,00
SPIWrite 0c17,ff
SPIWrite 0c16,ff
SPIWrite 0c15,fe
SPIWrite 0c14,00
SPIWrite 0c1f,ff
SPIWrite 0c1e,ff
SPIWrite 0c1d,fc
SPIWrite 0c1c,00
SPIWrite 0c27,ff
SPIWrite 0c26,ff
SPIWrite 0c25,f8

SPIWrite 0c24,00
SPIWrite 0c2f,ff
SPIWrite 0c2e,ff
SPIWrite 0c2d,f0
SPIWrite 0c2c,00
SPIWrite 0c37,ff
SPIWrite 0c36,ff
SPIWrite 0c35,e0
SPIWrite 0c34,00
SPIWrite 0c3f,ff
SPIWrite 0c3e,ff
SPIWrite 0c3d,c0
SPIWrite 0c3c,00
SPIWrite 0c47,ff
SPIWrite 0c46,ff
SPIWrite 0c45,80
SPIWrite 0c44,00
SPIWrite 0c4f,ff
SPIWrite 0c4e,ff
SPIWrite 0c4d,00
SPIWrite 0c4c,00
SPIWrite 0c57,ff
SPIWrite 0c56,fe
SPIWrite 0c55,00
SPIWrite 0c54,00
SPIWrite 0c5f,ff
SPIWrite 0c5e,fc
SPIWrite 0c5d,00
SPIWrite 0c5c,00
SPIWrite 0c67,ff
SPIWrite 0c66,f8
SPIWrite 0c65,00
SPIWrite 0c64,00
SPIWrite 0c6f,ff
SPIWrite 0c6e,f0
SPIWrite 0c6d,00
SPIWrite 0c6c,00
SPIWrite 0c77,ff
SPIWrite 0c76,e0
SPIWrite 0c75,00
SPIWrite 0c74,00
SPIWrite 0c7f,ff
SPIWrite 0c7e,c0
SPIWrite 0c7d,00
SPIWrite 0c7c,00
SPIWrite 0c87,ff
SPIWrite 0c86,80
SPIWrite 0c85,00

SPIWrite 0c84,00
SPIWrite 0c8f,ff
SPIWrite 0c8e,00
SPIWrite 0c8d,00
SPIWrite 0c8c,00
SPIWrite 0c97,fe
SPIWrite 0c96,00
SPIWrite 0c95,00
SPIWrite 0c94,00
SPIWrite 0c9f,fc
SPIWrite 0c9e,00
SPIWrite 0c9d,00
SPIWrite 0c9c,00
SPIWrite 0ca7,f8
SPIWrite 0ca6,00
SPIWrite 0ca5,00
SPIWrite 0ca4,00
SPIWrite 0caf,f0
SPIWrite 0cae,00
SPIWrite 0cad,00
SPIWrite 0cac,00
SPIWrite 0cb7,e0
SPIWrite 0cb6,00
SPIWrite 0cb5,00
SPIWrite 0cb4,00
SPIWrite 0cbf,c0
SPIWrite 0cbe,00
SPIWrite 0cbd,00
SPIWrite 0cbc,00
SPIWrite 0cc7,80
SPIWrite 0cc6,00
SPIWrite 0cc5,00
SPIWrite 0cc4,00
SPIWrite 0ccf,00
SPIWrite 0cce,00
SPIWrite 0ccd,00
SPIWrite 0ccc,00
SPIWrite 0cd7,00
SPIWrite 0cd6,00
SPIWrite 0cd5,00
SPIWrite 0cd4,00
SPIWrite 0cdf,00
SPIWrite 0cde,00
SPIWrite 0cdd,00
SPIWrite 0cdc,00
SPIWrite 0ce7,00
SPIWrite 0ce6,00
SPIWrite 0ce5,00

SPIWrite 0ce4,00
SPIWrite 0cef,00
SPIWrite 0cee,00
SPIWrite 0ced,00
SPIWrite 0cec,00
SPIWrite 0cf7,00
SPIWrite 0cf6,00
SPIWrite 0cf5,00
SPIWrite 0cf4,00
SPIWrite 0cff,00
SPIWrite 0cfe,00
SPIWrite 0cfd,00
SPIWrite 0cfc,00
SPIWrite 0d07,00
SPIWrite 0d06,00
SPIWrite 0d05,00
SPIWrite 0d04,00
SPIWrite 09a2,00
SPIWrite 09a2,01
SPIWrite 09a2,00
SPIWrite 0bc2,00
SPIWrite 0bc2,01
SPIWrite 0bc2,00
SPIWrite 0101,18
SPIWrite 0121,18
SPIWrite 0103,01
SPIWrite 0123,01
SPIWrite 0100,01
SPIWrite 0102,00
SPIWrite 0102,01
SPIWrite 0102,00
SPIWrite 0100,00
SPIWrite 0102,00
SPIWrite 0102,01
SPIWrite 0102,00
SPIWrite 0120,01
SPIWrite 0122,00
SPIWrite 0122,01
SPIWrite 0122,00
SPIWrite 0120,00
SPIWrite 0122,00
SPIWrite 0122,01
SPIWrite 0122,00
SPIWrite 0103,00
SPIWrite 0123,00
SPIWrite 0155,0f
SPIWrite 0994,01
SPIWrite 0bb4,01

SPIWrite 0df2,04
SPIWrite 0df1,80
SPIWrite 0df0,00
SPIWrite 0df6,05
SPIWrite 0df5,0c
SPIWrite 0df4,56
SPIWrite 0dfa,05
SPIWrite 0df9,98
SPIWrite 0df8,9e
SPIWrite 0dfe,07
SPIWrite 0dfd,20
SPIWrite 0dfc,f3
SPIWrite 0e02,08
SPIWrite 0e01,a9
SPIWrite 0e00,33
SPIWrite 0e06,0a
SPIWrite 0e05,ad
SPIWrite 0e04,80
SPIWrite 0e0a,0d
SPIWrite 0e09,31
SPIWrite 0e08,c9
SPIWrite 0e0e,0f
SPIWrite 0e0d,b9
SPIWrite 0e0c,f1
SPIWrite 0e12,13
SPIWrite 0e11,ba
SPIWrite 0e10,42
SPIWrite 0e16,1a
SPIWrite 0e15,3e
SPIWrite 0e14,6b
SPIWrite 0e1a,25
SPIWrite 0e19,42
SPIWrite 0e18,8b
SPIWrite 0e1e,29
SPIWrite 0e1d,ca
SPIWrite 0e1c,a3
SPIWrite 0e22,29
SPIWrite 0e21,d2
SPIWrite 0e20,c1
SPIWrite 0e26,29
SPIWrite 0e25,d2
SPIWrite 0e24,eb
SPIWrite 0e2a,29
SPIWrite 0e29,db
SPIWrite 0e28,01
SPIWrite 0e2e,29
SPIWrite 0e2d,df
SPIWrite 0e2c,1b

SPIWrite 0e32,29
SPIWrite 0e31,e3
SPIWrite 0e30,33
SPIWrite 0e36,29
SPIWrite 0e35,e7
SPIWrite 0e34,45
SPIWrite 0e3a,29
SPIWrite 0e39,eb
SPIWrite 0e38,58
SPIWrite 0e3e,29
SPIWrite 0e3d,ef
SPIWrite 0e3c,67
SPIWrite 0e42,29
SPIWrite 0e41,f3
SPIWrite 0e40,77
SPIWrite 0e46,29
SPIWrite 0e45,f3
SPIWrite 0e44,77
SPIWrite 0e4a,29
SPIWrite 0e49,f3
SPIWrite 0e48,77
SPIWrite 0e4e,29
SPIWrite 0e4d,f3
SPIWrite 0e4c,77
SPIWrite 0e52,29
SPIWrite 0e51,f3
SPIWrite 0e50,77
SPIWrite 0e56,29
SPIWrite 0e55,f3
SPIWrite 0e54,77
SPIWrite 0e5a,29
SPIWrite 0e59,f3
SPIWrite 0e58,77
SPIWrite 0e5e,29
SPIWrite 0e5d,f3
SPIWrite 0e5c,77
SPIWrite 0e62,29
SPIWrite 0e61,f3
SPIWrite 0e60,77
SPIWrite 0e66,29
SPIWrite 0e65,f3
SPIWrite 0e64,77
SPIWrite 0e6a,29
SPIWrite 0e69,f3
SPIWrite 0e68,77
SPIWrite 0e6e,29
SPIWrite 0e6d,f3
SPIWrite 0e6c,77

SPIWrite 0dd1,01

// Done Top level initialization

//**********Step: Setting up PLL Mux**********//
// Configuring PLL Mux

SPIWrite 0016,00
//PAGE:dsa=0
SPIWrite 0014,01
//PAGE:clktop_2t=1
SPIWrite 0064,00
//CTL_SEL_CLK_MUX_CROSS_PLL_TOP_1P8_L=0(Meaning:);
SPIWrite 0064,00
//CTL_SEL_CLK_MUX_CROSS_PLL_TOP_1P8_R=0(Meaning:);
SPIWrite 0062,01
//CTL_SEL_CLK_MUX_CROSS_PLL_BOT_L=1(Meaning:);
SPIWrite 0062,03
//CTL_SEL_CLK_MUX_CROSS_PLL_BOT_R=1(Meaning:);
SPIWrite 0071,00
//SEL_CLK_MUX_RX_1P8_L=0(Meaning:);
SPIWrite 0071,00
//SEL_CLK_MUX_RX_1P8_R=0(Meaning:);
SPIWrite 0071,00
//SEL_CLK_MUX_TX_1P8_L=0(Meaning:);
SPIWrite 0071,00
//SEL_CLK_MUX_TX_1P8_R=0(Meaning:);
SPIWrite 0060,01
//CTL_EN_CROSS_PLL_BLOCK_1P8=1(Meaning:);
SPIWrite 0060,01
//CTL_SEL_CROSS_PLL_DIR_1P8=0(Meaning:);

// Done configuring PLL Mux

//**********Step: Setting Credo Access modes**********//

SPIWrite 0014,00
//PAGE:clktop_2t=0
SPIWrite 0015,08
//PAGE:jesd_subchip=1(Meaning:);

```
SPIWrite 0020,07
SPIWrite 0020,07
SPIWrite 0021,12
SPIWrite 0022,12
SPIWrite 0021,12
SPIWrite 0022,12
SPIWrite 0021,12
SPIWrite 0022,12
SPIWrite 0015,00
//PAGE:jesd_subchip=0(Meaning: );


//**********Step: Credo reset: All Reset, CPU reset**********//


SPIWrite 0015,04
//PAGE:SERDES=1
SPIWrite 0015,04
SPIWrite 7007,00
//BUS_WIDTH_LANE3=0
SPIWrite 7006,00
SPIWrite 7007,00
//BUS_WIDTH_LANE2=0
SPIWrite 7006,00
SPIWrite 7007,00
//BUS_WIDTH_LANE1=0
SPIWrite 7006,00
SPIWrite 7007,00
//BUS_WIDTH_LANE0=0
SPIWrite 7006,00
SPIWrite 0015,00
//PAGE:SERDES=2
SPIWrite 0015,40
SPIWrite 7007,00
//BUS_WIDTH_LANE3=0
SPIWrite 7006,00
SPIWrite 7007,00
//BUS_WIDTH_LANE2=0
SPIWrite 7006,00
SPIWrite 7007,00
//BUS_WIDTH_LANE1=0
SPIWrite 7006,00
SPIWrite 7007,00
//BUS_WIDTH_LANE0=0
SPIWrite 7006,00
SPIWrite 0015,44
//PAGE:SERDES=1
```

```
SPIWrite 0015,04
SPIWrite 701b,08
//DOMAIN_RESET=888
SPIWrite 701a,88
SPIWrite 701b,00
//DOMAIN_RESET=0
SPIWrite 701a,00
SPIWrite 701b,07
//DOMAIN_RESET=777
SPIWrite 701a,77
SPIWrite 701b,00
//DOMAIN_RESET=0
SPIWrite 701a,00
SPIWrite 0015,00
//PAGE:SERDES=2
SPIWrite 0015,40
SPIWrite 701b,08
//DOMAIN_RESET=888
SPIWrite 701a,88
SPIWrite 701b,00
//DOMAIN_RESET=0
SPIWrite 701a,00
SPIWrite 701b,07
//DOMAIN_RESET=777
SPIWrite 701a,77
SPIWrite 701b,00
//DOMAIN_RESET=0
SPIWrite 701a,00
SPIWrite 0015,00
// Done Resetting Serdes



SPIWrite 0015,40
//PAGE:SERDES=0
SPIWrite 0015,00
SPIWrite 0015,08
//PAGE:jesd_subchip=1(Meaning: );
SPIWrite 0021,12
SPIWrite 0022,12
SPIWrite 0015,00
//PAGE:jesd_subchip=0(Meaning: );



AFE77xx_GLOBAL
SPIWrite 0015,44
//PAGE:SERDES=1
```

```
SPIWrite 0015,04
SPIWrite 701b,08
//DOMAIN_RESET=888
SPIWrite 701a,88
SPIWrite 701b,00
//DOMAIN_RESET=0
SPIWrite 701a,00
SPIWrite 701b,07
//DOMAIN_RESET=777
SPIWrite 701a,77
SPIWrite 701b,00
//DOMAIN_RESET=0
SPIWrite 701a,00
SPIWrite 0015,00
//PAGE:SERDES=2
SPIWrite 0015,40
SPIWrite 701b,08
//DOMAIN_RESET=888
SPIWrite 701a,88
SPIWrite 701b,00
//DOMAIN_RESET=0
SPIWrite 701a,00
SPIWrite 701b,07
//DOMAIN_RESET=777
SPIWrite 701a,77
SPIWrite 701b,00
//DOMAIN_RESET=0
SPIWrite 701a,00

//**********Step: SRAM Bist enable for FW download issue**********//

//SRAM BIST Enable
SPIWrite 0015,44
SPIWrite 702F,C0
SPIWrite 702E,00


//**********Step: Preparing Credo for Firmware re Download**********//

//PAGE:SERDES=3
SPIWrite 0015,44
SPIWrite 7029,ff
SPIWrite 7028,f0


WAIT 10
```

AFE77xx_GLOBAL
SPIWrite 701b,0a
SPIWrite 701a,aa

WAIT 10

AFE77xx_GLOBAL
SPIWrite 701b,00
SPIWrite 701a,00

WAIT 10

SPIWrite 702F,00
SPIWrite 702E,00

SPIWrite 0015,00

//**********Step: Static Credo Writes(for 25G serdes)**********//

// Configuring the SERDES

SPIWrite 0015,04
//PAGE:SERDES=3
SPIWrite 0015,44
SPIWrite 7007,00
SPIWrite 7006,00
SPIWrite 49ff,fd
SPIWrite 49fe,b0
SPIWrite 49ed,1d
SPIWrite 49ec,c0
SPIWrite 49e7,52
SPIWrite 49e6,26
SPIWrite 49e5,6e
SPIWrite 49e4,b6
SPIWrite 49df,a8
SPIWrite 49de,28
SPIWrite 49eb,63
SPIWrite 49ea,98
SPIWrite 49e9,b2
SPIWrite 49e8,44
SPIWrite 49fd,63
SPIWrite 49fc,98
SPIWrite 49fb,b2

SPIWrite 49fa,48
SPIWrite 49f9,4a
SPIWrite 49f8,44
SPIWrite 49f7,6d
SPIWrite 49f6,b6
SPIWrite 49d9,6c
SPIWrite 49d8,06
SPIWrite 41ff,88
SPIWrite 41fe,c8
SPIWrite 4095,74
SPIWrite 4094,60
SPIWrite 4141,03
SPIWrite 4140,01
SPIWrite 4097,06
SPIWrite 4096,db
SPIWrite 4001,10
SPIWrite 4000,6b
SPIWrite 4003,64
SPIWrite 4002,80
SPIWrite 4005,62
SPIWrite 4004,00
SPIWrite 4007,7b
SPIWrite 4006,33
SPIWrite 4009,70
SPIWrite 4008,0a
SPIWrite 400b,bd
SPIWrite 400a,68
SPIWrite 400d,76
SPIWrite 400c,2d
SPIWrite 400f,66
SPIWrite 400e,ab
SPIWrite 4011,d0
SPIWrite 4010,08
SPIWrite 4013,00
SPIWrite 4012,18
SPIWrite 4015,66
SPIWrite 4014,2c
SPIWrite 4017,3d
SPIWrite 4016,15
SPIWrite 4019,00
SPIWrite 4018,80
SPIWrite 401b,00
SPIWrite 401a,02
SPIWrite 401d,34
SPIWrite 401c,00
SPIWrite 401f,00
SPIWrite 401e,00
SPIWrite 4021,10

SPIWrite 4020,1a
SPIWrite 4039,03
SPIWrite 4038,40
SPIWrite 403b,00
SPIWrite 403a,e0
SPIWrite 403d,00
SPIWrite 403c,00
SPIWrite 403f,00
SPIWrite 403e,80
SPIWrite 4077,00
SPIWrite 4076,00
SPIWrite 4079,00
SPIWrite 4078,00
SPIWrite 407b,00
SPIWrite 407a,00
SPIWrite 407d,00
SPIWrite 407c,00
SPIWrite 4083,9f
SPIWrite 4082,df
SPIWrite 4085,b3
SPIWrite 4084,c0
SPIWrite 408f,08
SPIWrite 408e,31
SPIWrite 4091,05
SPIWrite 4090,18
SPIWrite 4093,f5
SPIWrite 4092,e7
SPIWrite 4095,74
SPIWrite 4094,60
SPIWrite 4097,06
SPIWrite 4096,db
SPIWrite 4141,03
SPIWrite 4140,01
SPIWrite 41e7,00
SPIWrite 41e6,80
SPIWrite 41e9,fc
SPIWrite 41e8,00
SPIWrite 41eb,9f
SPIWrite 41ea,fe
SPIWrite 41ed,46
SPIWrite 41ec,00
SPIWrite 41ef,10
SPIWrite 41ee,00
SPIWrite 41f1,68
SPIWrite 41f0,64
SPIWrite 41f3,92
SPIWrite 41f2,30
SPIWrite 41f5,00

SPIWrite 41f4,00
SPIWrite 41f7,6d
SPIWrite 41f6,87
SPIWrite 41f9,6d
SPIWrite 41f8,b6
SPIWrite 41fb,42
SPIWrite 41fa,46
SPIWrite 41fd,62
SPIWrite 41fc,7c
SPIWrite 41ff,88
SPIWrite 41fe,c8
SPIWrite 4201,10
SPIWrite 4200,6b
SPIWrite 4203,64
SPIWrite 4202,80
SPIWrite 4205,62
SPIWrite 4204,00
SPIWrite 4207,7b
SPIWrite 4206,33
SPIWrite 4209,70
SPIWrite 4208,0a
SPIWrite 420b,bd
SPIWrite 420a,68
SPIWrite 420d,76
SPIWrite 420c,2d
SPIWrite 420f,66
SPIWrite 420e,ab
SPIWrite 4211,d0
SPIWrite 4210,08
SPIWrite 4213,00
SPIWrite 4212,18
SPIWrite 4215,66
SPIWrite 4214,2c
SPIWrite 4217,3d
SPIWrite 4216,15
SPIWrite 4219,00
SPIWrite 4218,80
SPIWrite 421b,00
SPIWrite 421a,02
SPIWrite 421d,34
SPIWrite 421c,00
SPIWrite 421f,00
SPIWrite 421e,00
SPIWrite 4221,10
SPIWrite 4220,1a
SPIWrite 4239,03
SPIWrite 4238,40
SPIWrite 423b,00

SPIWrite 423a,e0
SPIWrite 423d,00
SPIWrite 423c,00
SPIWrite 423f,00
SPIWrite 423e,80
SPIWrite 4277,00
SPIWrite 4276,00
SPIWrite 4279,00
SPIWrite 4278,00
SPIWrite 427b,00
SPIWrite 427a,00
SPIWrite 427d,00
SPIWrite 427c,00
SPIWrite 4283,9f
SPIWrite 4282,df
SPIWrite 4285,b3
SPIWrite 4284,c0
SPIWrite 428f,08
SPIWrite 428e,31
SPIWrite 4291,05
SPIWrite 4290,18
SPIWrite 4293,f5
SPIWrite 4292,e7
SPIWrite 4295,74
SPIWrite 4294,60
SPIWrite 4297,06
SPIWrite 4296,db
SPIWrite 4341,03
SPIWrite 4340,01
SPIWrite 43e7,00
SPIWrite 43e6,80
SPIWrite 43e9,fc
SPIWrite 43e8,00
SPIWrite 43eb,9f
SPIWrite 43ea,fe
SPIWrite 43ed,46
SPIWrite 43ec,00
SPIWrite 43ef,10
SPIWrite 43ee,00
SPIWrite 43f1,68
SPIWrite 43f0,64
SPIWrite 43f3,92
SPIWrite 43f2,30
SPIWrite 43f5,00
SPIWrite 43f4,00
SPIWrite 43f7,6d
SPIWrite 43f6,87
SPIWrite 43f9,6d

SPIWrite 43f8,b6
SPIWrite 43fb,42
SPIWrite 43fa,46
SPIWrite 43fd,62
SPIWrite 43fc,7c
SPIWrite 43ff,88
SPIWrite 43fe,c8
SPIWrite 4401,10
SPIWrite 4400,6b
SPIWrite 4403,64
SPIWrite 4402,80
SPIWrite 4405,62
SPIWrite 4404,00
SPIWrite 4407,7b
SPIWrite 4406,33
SPIWrite 4409,70
SPIWrite 4408,0a
SPIWrite 440b,bd
SPIWrite 440a,68
SPIWrite 440d,76
SPIWrite 440c,2d
SPIWrite 440f,66
SPIWrite 440e,ab
SPIWrite 4411,d0
SPIWrite 4410,08
SPIWrite 4413,00
SPIWrite 4412,18
SPIWrite 4415,66
SPIWrite 4414,2c
SPIWrite 4417,3d
SPIWrite 4416,15
SPIWrite 4419,00
SPIWrite 4418,80
SPIWrite 441b,00
SPIWrite 441a,02
SPIWrite 441d,34
SPIWrite 441c,00
SPIWrite 441f,00
SPIWrite 441e,00
SPIWrite 4421,10
SPIWrite 4420,1a
SPIWrite 4439,03
SPIWrite 4438,40
SPIWrite 443b,00
SPIWrite 443a,e0
SPIWrite 443d,00
SPIWrite 443c,00
SPIWrite 443f,00

SPIWrite 443e,80
SPIWrite 4477,00
SPIWrite 4476,00
SPIWrite 4479,00
SPIWrite 4478,00
SPIWrite 447b,00
SPIWrite 447a,00
SPIWrite 447d,00
SPIWrite 447c,00
SPIWrite 4483,9f
SPIWrite 4482,df
SPIWrite 4485,b3
SPIWrite 4484,c0
SPIWrite 448f,08
SPIWrite 448e,31
SPIWrite 4491,05
SPIWrite 4490,18
SPIWrite 4493,f5
SPIWrite 4492,e7
SPIWrite 4495,74
SPIWrite 4494,60
SPIWrite 4497,06
SPIWrite 4496,db
SPIWrite 4541,03
SPIWrite 4540,01
SPIWrite 45e7,00
SPIWrite 45e6,80
SPIWrite 45e9,fc
SPIWrite 45e8,00
SPIWrite 45eb,9f
SPIWrite 45ea,fe
SPIWrite 45ed,46
SPIWrite 45ec,00
SPIWrite 45ef,10
SPIWrite 45ee,00
SPIWrite 45f1,68
SPIWrite 45f0,64
SPIWrite 45f3,92
SPIWrite 45f2,30
SPIWrite 45f5,00
SPIWrite 45f4,00
SPIWrite 45f7,6d
SPIWrite 45f6,87
SPIWrite 45f9,6d
SPIWrite 45f8,b6
SPIWrite 45fb,42
SPIWrite 45fa,46
SPIWrite 45fd,62

SPIWrite 45fc,7c
SPIWrite 45ff,88
SPIWrite 45fe,c8
SPIWrite 4601,10
SPIWrite 4600,6b
SPIWrite 4603,64
SPIWrite 4602,80
SPIWrite 4605,62
SPIWrite 4604,00
SPIWrite 4607,7b
SPIWrite 4606,33
SPIWrite 4609,70
SPIWrite 4608,0a
SPIWrite 460b,bd
SPIWrite 460a,68
SPIWrite 460d,76
SPIWrite 460c,2d
SPIWrite 460f,66
SPIWrite 460e,ab
SPIWrite 4611,d0
SPIWrite 4610,08
SPIWrite 4613,00
SPIWrite 4612,18
SPIWrite 4615,66
SPIWrite 4614,2c
SPIWrite 4617,3d
SPIWrite 4616,15
SPIWrite 4619,00
SPIWrite 4618,80
SPIWrite 461b,00
SPIWrite 461a,02
SPIWrite 461d,34
SPIWrite 461c,00
SPIWrite 461f,00
SPIWrite 461e,00
SPIWrite 4621,10
SPIWrite 4620,1a
SPIWrite 4639,03
SPIWrite 4638,40
SPIWrite 463b,00
SPIWrite 463a,e0
SPIWrite 463d,00
SPIWrite 463c,00
SPIWrite 463f,00
SPIWrite 463e,80
SPIWrite 4677,00
SPIWrite 4676,00
SPIWrite 4679,00

SPIWrite 4678,00
SPIWrite 467b,00
SPIWrite 467a,00
SPIWrite 467d,00
SPIWrite 467c,00
SPIWrite 4683,9f
SPIWrite 4682,df
SPIWrite 4685,b3
SPIWrite 4684,c0
SPIWrite 468f,08
SPIWrite 468e,31
SPIWrite 4691,05
SPIWrite 4690,18
SPIWrite 4693,f5
SPIWrite 4692,e7
SPIWrite 4695,74
SPIWrite 4694,60
SPIWrite 4697,06
SPIWrite 4696,db
SPIWrite 4741,03
SPIWrite 4740,01
SPIWrite 47e7,00
SPIWrite 47e6,80
SPIWrite 47e9,fc
SPIWrite 47e8,00
SPIWrite 47eb,9f
SPIWrite 47ea,fe
SPIWrite 47ed,46
SPIWrite 47ec,00
SPIWrite 47ef,10
SPIWrite 47ee,00
SPIWrite 47f1,68
SPIWrite 47f0,64
SPIWrite 47f3,92
SPIWrite 47f2,30
SPIWrite 47f5,00
SPIWrite 47f4,00
SPIWrite 47f7,6d
SPIWrite 47f6,87
SPIWrite 47f9,6d
SPIWrite 47f8,b6
SPIWrite 47fb,42
SPIWrite 47fa,46
SPIWrite 47fd,62
SPIWrite 47fc,7c
SPIWrite 47ff,88
SPIWrite 47fe,c8

```
SPIWrite 49b4,47
SPIWrite 49b5,47
//Added Writes for Serdes Pll
SPIWrite 7007,00
//BUS_WIDTH_LANE0=0
SPIWrite 7006,00
SPIWrite 7007,00
//BUS_WIDTH_LANE1=0
SPIWrite 7006,00
SPIWrite 7007,00
//BUS_WIDTH_LANE2=0
SPIWrite 7006,00
SPIWrite 7007,00
//BUS_WIDTH_LANE3=0
SPIWrite 7006,00
SPIWrite 0015,00
//PAGE:SERDES=0

SPIWrite 0015,44
SPIWrite 49F5,72
SPIWrite 49F4,C0
SPIWrite 49F7,79
SPIWrite 49F6,B6
SPIWrite 49F9,4A
SPIWrite 49F8,44
SPIWrite 49FB,B2
SPIWrite 49FA,48
SPIWrite 49FD,63
SPIWrite 49FC,98
SPIWrite 41FD,62
SPIWrite 41FC,7C
SPIWrite 41FB,42
SPIWrite 41FA,46
SPIWrite 41F9,DB
SPIWrite 41F8,36
SPIWrite 41F7,6D
SPIWrite 41F6,87
SPIWrite 41F3,92
SPIWrite 41F2,30
SPIWrite 41F1,68
SPIWrite 41F0,64
SPIWrite 41EF,10
SPIWrite 41EE,00
SPIWrite 43FD,62
SPIWrite 43FC,7C
SPIWrite 43FB,42
SPIWrite 43FA,46
SPIWrite 43F9,DB
```

SPIWrite 43F8,36
SPIWrite 43F7,6D
SPIWrite 43F6,87
SPIWrite 43F3,92
SPIWrite 43F2,30
SPIWrite 43F1,68
SPIWrite 43F0,64
SPIWrite 43EF,10
SPIWrite 43EE,00
SPIWrite 45FD,62
SPIWrite 45FC,7C
SPIWrite 45FB,42
SPIWrite 45FA,46
SPIWrite 45F9,DB
SPIWrite 45F8,36
SPIWrite 45F7,6D
SPIWrite 45F6,87
SPIWrite 45F3,92
SPIWrite 45F2,30
SPIWrite 45F1,68
SPIWrite 45F0,64
SPIWrite 45EF,10
SPIWrite 45EE,00
SPIWrite 47FD,62
SPIWrite 47FC,7C
SPIWrite 47FB,42
SPIWrite 47FA,46
SPIWrite 47F9,DB
SPIWrite 47F8,36
SPIWrite 47F7,6D
SPIWrite 47F6,87
SPIWrite 47F3,92
SPIWrite 47F2,30
SPIWrite 47F1,68
SPIWrite 47F0,64
SPIWrite 47EF,10
SPIWrite 47EE,00
SPIWrite 0015,00
// Done configuring the SERDES

//**********Step: Loading Cerdo Firmeare using Macro**********//

// Loading Serdes Firmware

SPIWrite 0015,08
SPIWrite 0021,1A

```
SPIWrite 0022,1A
SPIWrite 0015,00
SPIWrite 0013,10
SPIWrite 00A3,00
SPIWrite 00A2,01
SPIWrite 00A1,03
SPIWrite 00A0,00
SPIWrite 0193,82
SPIWrite 0192,00
SPIWrite 0191,00
SPIWrite 0190,00
SPIWrite 0013,00
WAIT 5
SPIWrite 0013,20
WAIT 5
SPIRead 20
SPIWrite 0013,0

SPIWrite 0015,08
SPIWrite 0021,1A
SPIWrite 0022,1A
SPIWrite 0015,00
SPIWrite 0013,10
SPIWrite 00A3,00
SPIWrite 00A2,01
SPIWrite 00A1,03
SPIWrite 00A0,01
SPIWrite 0193,82
SPIWrite 0192,00
SPIWrite 0191,00
SPIWrite 0190,00
SPIWrite 0013,00
WAIT 5
SPIWrite 0013,20
WAIT 5
SPIRead 20
SPIWrite 0013,0

SPIWrite 0015,08
SPIWrite 0021,12
SPIWrite 0022,12
SPIWrite 0015,0


// Done loading Serdes Firmware

//**********Step: Logic Reset after firmware download**********//
```

```
SPIWrite 0015,44
SPIWrite 701b,07
SPIWrite 701a,77
//DOMAIN_RESET=777
SPIWrite 701b,00
SPIWrite 701a,00
//DOMAIN_RESET=777
SPIWrite 0015,00

WAIT 5

SPIWrite 0015,04
SPIRead F029
SPIRead F029
SPIRead F028
SPIRead F028
SPIWrite 0015,40
SPIRead F029
SPIRead F029
SPIRead F028
SPIRead F028
SPIWrite 0015,00

//**********Step: Disabling unused serdes lanes**********//

//Lane power down
SPIWrite 0015,44
SPIWrite 47fd,62
SPIWrite 47fc,78
SPIWrite 45fd,62
SPIWrite 45fc,78

SPIWrite 47f7,6d
SPIWrite 47f6,83
SPIWrite 45f7,6d
SPIWrite 45f6,83

SPIWrite 47eb,1f
SPIWrite 47ea,fe
SPIWrite 45eb,1f
SPIWrite 45ea,fe

SPIWrite 47ff,08
SPIWrite 47fe,c8
SPIWrite 45ff,08
SPIWrite 45fe,c8
SPIWrite 0015,00
```

```
//**********Step: JESD subchip configurations**********//
SPIWrite 0015,08
//PAGE:jesd_subchip=1(Meaning: );
//Check
SPIWrite 005b,01
SPIWrite 0066,22
SPIWrite 0067,33


// Configuring JESD TX Lane Mux

SPIWrite 00c4,43
SPIWrite 00c5,02
SPIWrite 00c6,51
SPIWrite 00c7,76
SPIWrite 00c8,43
SPIWrite 00c9,02
SPIWrite 00ca,51
SPIWrite 00cb,76


// Done configuring JESD TX Lane Mux




// Configuring JESD RX Lane Mux
SPIWrite 00cc,43
SPIWrite 00cd,02
SPIWrite 00ce,51
SPIWrite 00cf,76
SPIWrite 00d0,43
SPIWrite 00d1,02
SPIWrite 00d2,51
SPIWrite 00d3,76


// Done configuring JESD RX Lane Mux


//Check
SPIWrite 0032,10
SPIWrite 0035,10
SPIWrite 0030,10
SPIWrite 0031,10
SPIWrite 0033,10
```

SPIWrite 0034,10

// Configuring the Data Muxes

SPIWrite 0044,50
SPIWrite 0044,50
SPIWrite 0044,50
SPIWrite 0044,50
SPIWrite 0045,fa
SPIWrite 0045,fa
SPIWrite 0045,fa
SPIWrite 0045,fa
SPIWrite 0046,fa
SPIWrite 0046,fa
SPIWrite 0046,fa
SPIWrite 0046,fa
SPIWrite 0047,50
SPIWrite 0047,50
SPIWrite 0047,50
SPIWrite 0047,50
SPIWrite 003a,e4
SPIWrite 003a,e4
SPIWrite 003a,e4
SPIWrite 003a,e4
SPIWrite 003b,e4
SPIWrite 003b,e4
SPIWrite 003b,e4
SPIWrite 003b,e4
SPIWrite 003c,00
SPIWrite 003c,00
SPIWrite 003d,11
SPIWrite 003d,11
SPIWrite 003e,44
SPIWrite 003e,44
SPIWrite 003f,55
SPIWrite 003f,55
SPIWrite 0036,d8
SPIWrite 0036,d8
SPIWrite 0036,d8
SPIWrite 0036,d8
SPIWrite 0037,d8
SPIWrite 0037,d8
SPIWrite 0037,d8
SPIWrite 0037,d8
SPIWrite 0040,44

SPIWrite 0040,44
SPIWrite 0041,55
SPIWrite 0041,55
SPIWrite 0042,00
SPIWrite 0042,00
SPIWrite 0043,11
SPIWrite 0043,11
SPIWrite 0038,d8
SPIWrite 0038,d8
SPIWrite 0038,d8
SPIWrite 0038,d8
SPIWrite 0039,d8
SPIWrite 0039,d8
SPIWrite 0039,d8
SPIWrite 0039,d8
SPIWrite 0040,44
SPIWrite 0040,44
SPIWrite 0041,55
SPIWrite 0041,55
SPIWrite 0042,00
SPIWrite 0042,00
SPIWrite 0043,11
SPIWrite 0043,11

// Done configuring the Data Muxes

// Configuring JESDTX Sync Mux
SPIWrite 0054,24
SPIWrite 0054,04
SPIWrite 0054,00
SPIWrite 0054,00

// Done configuring JESDTX Sync Mux

// Configuring JESDRX Sync Mux

SPIWrite 0061,01
SPIWrite 0061,03
SPIWrite 0061,07
SPIWrite 0061,0f
SPIWrite 0061,0e
SPIWrite 0061,0c
SPIWrite 0061,08
SPIWrite 0061,00
SPIWrite 0055,e0
SPIWrite 0055,e0
SPIWrite 0055,20
SPIWrite 0055,00
SPIWrite 0015,00

// Done configuring JESDRX Sync Mux

// START: Setting FIFO and dither in JESD

SPIWrite 0015,08
AFE77xx_GLOBAL
SPIWrite 0032,10
SPIWrite 0035,10
SPIWrite 0030,10
SPIWrite 0031,10
SPIWrite 0033,10
SPIWrite 0034,10
SPIWrite 009c,01
SPIWrite 009d,00
SPIWrite 009e,01
SPIWrite 009f,00
SPIWrite 00a4,01
SPIWrite 00a5,00
SPIWrite 00a0,01
SPIWrite 00a1,00
SPIWrite 00a2,01
SPIWrite 00a3,00
SPIWrite 00a6,01
SPIWrite 00a7,00
SPIWrite 005b,01
SPIWrite 00a8,01
SPIWrite 00a8,03
SPIWrite 00a8,13
SPIWrite 00a8,17
SPIWrite 00a8,1f
SPIWrite 00a8,3f
SPIWrite 0015,00

// END: Done Setting FIFO and dither in JESD

```
//**********Step: Doing RX, TX and FB Digital Chain Config.**********//

AFE77xx_GLOBAL
SPIWrite 0013,10
//PAGE:customer_macro=1(Meaning: );
SPIRead 00f3
SPIRead 00f2
SPIRead 00f1
SPIRead 00f0


// Read // cm4_wr_spi_rf0: 0x7
SPIWrite 00a3,00
SPIWrite 00a2,01
SPIWrite 00a1,01
SPIWrite 00a0,01
SPIWrite 00a7,00
SPIWrite 00a6,00
SPIWrite 00a5,00
SPIWrite 00a4,00
SPIWrite 0193,31
SPIWrite 0192,00
SPIWrite 0191,00
SPIWrite 0190,00
SPIRead 0193
SPIRead 0192
SPIRead 0191
SPIRead 0190
WAIT 10

// Read // macro_opcode_operand: 0x31000000
SPIRead 00f3
SPIRead 00f2
SPIRead 00f1
SPIRead 00f0


// Read // cm4_wr_spi_rf0: 0x7
SPIWrite 0013,00
//PAGE:customer_macro=0(Meaning: );
SPIWrite 0013,20
//PAGE:cm4_macro=1
SPIRead 0020

SPIWrite 0013,00
```

```
//Set Fb Nco Word
SPIWrite 0016,40
//Disable Mixer correction. Backward compatibilty
SPIWrite 010c,00

//e1400000
SPIWrite 0107,e1
SPIWrite 0106,40
SPIWrite 0105,00
SPIWrite 0104,00
SPIWrite 0016,00

//*********Async Fifo Pointer setting********//
SPIWrite 0013,00
//PAGE:customer_macro=0(Meaning: );
SPIWrite 0016,40
//PAGE:fb_top=1
SPIWrite 015b,03
//FBAsyncFIFORdPtrVal=3
SPIWrite 0016,80
//PAGE:fb_top=2
SPIWrite 015b,03
//FBAsyncFIFORdPtrVal=3
SPIWrite 0016,00
//PAGE:fb_top=0
SPIWrite 0010,04
//PAGE:rx_top=1
SPIWrite 0120,01
//RxDecAsyncFIFORdPtrLoad=1
SPIWrite 0010,08
//PAGE:rx_top=2
SPIWrite 0120,01
//RxDecAsyncFIFORdPtrLoad=1
SPIWrite 0010,00
//PAGE:rx_top=0
SPIWrite 0010,01
//PAGE:tx_top=1
SPIWrite 010d,01
//RdPtrOffDigOutAsyncFIFO=1
SPIWrite 0010,02
//PAGE:tx_top=2
SPIWrite 010d,01
//RdPtrOffDigOutAsyncFIFO=1
SPIWrite 0010,01
//PAGE:tx_top=1
SPIWrite 010b,00
//RdPtrOffDigInpAsyncFIFO=0
SPIWrite 0010,02
```

```
//PAGE:tx_top=2
SPIWrite 010b,00
//RdPtrOffDigInpAsyncFIFO=0
SPIWrite 0010,00
//PAGE:tx_top=0

///Adjust Rx Dig Gain
SPIWrite 0010,04
//PAGE:rx_top=1
SPIWrite 0af9,01
//pdn_in=1(Meaning: );
SPIWrite 0afb,01
//pdn_in=1(Meaning: );
SPIWrite 0a50,33
//gain_component_n=33
SPIWrite 0a51,33
//gain_component_n=33
SPIWrite 0a52,33
//gain_component_n=33
SPIWrite 0a53,33
//gain_component_n=33
SPIWrite 0a56,0e
//gain_corrector_bypass=0(Meaning: );
SPIWrite 0a56,0c
//gain_corrector_bypass=0(Meaning: );
SPIWrite 0a56,08
//gain_corrector_bypass=0(Meaning: );
SPIWrite 0a56,00
//gain_corrector_bypass=0(Meaning: );
SPIWrite 0a54,01
//rx1_unit_gain_mode=1(Meaning: );
SPIWrite 0a54,03
//rx2_unit_gain_mode=1(Meaning: );
SPIWrite 0c6b,00
//coef_update_signal=0
SPIWrite 0c73,00
//coef_update_signal=0
SPIWrite 0e6b,00
//coef_update_signal=0
SPIWrite 0e73,00
//coef_update_signal=0
SPIWrite 0c6b,01
//coef_update_signal=1
SPIWrite 0c73,01
//coef_update_signal=1
SPIWrite 0e6b,01
//coef_update_signal=1
SPIWrite 0e73,01
```

```
//coef_update_signal=1
SPIWrite 0c6b,00
//coef_update_signal=0
SPIWrite 0c73,00
//coef_update_signal=0
SPIWrite 0e6b,00
//coef_update_signal=0
SPIWrite 0e73,00
//coef_update_signal=0
SPIWrite 0010,08
//PAGE:rx_top=2
SPIWrite 0af9,01
//pdn_in=1(Meaning: );
SPIWrite 0afb,01
//pdn_in=1(Meaning: );
SPIWrite 0a50,33
//gain_component_n=33
SPIWrite 0a51,33
//gain_component_n=33
SPIWrite 0a52,33
//gain_component_n=33
SPIWrite 0a53,33
//gain_component_n=33
SPIWrite 0a56,0e
//gain_corrector_bypass=0(Meaning: );
SPIWrite 0a56,0c
//gain_corrector_bypass=0(Meaning: );
SPIWrite 0a56,08
//gain_corrector_bypass=0(Meaning: );
SPIWrite 0a56,00
//gain_corrector_bypass=0(Meaning: );
SPIWrite 0a54,01
//rx1_unit_gain_mode=1(Meaning: );
SPIWrite 0a54,03
//rx2_unit_gain_mode=1(Meaning: );
SPIWrite 0c6b,00
//coef_update_signal=0
SPIWrite 0c73,00
//coef_update_signal=0
SPIWrite 0e6b,00
//coef_update_signal=0
SPIWrite 0e73,00
//coef_update_signal=0
SPIWrite 0c6b,01
//coef_update_signal=1
SPIWrite 0c73,01
//coef_update_signal=1
SPIWrite 0e6b,01
```

```
//coef_update_signal=1
SPIWrite 0e73,01
//coef_update_signal=1
SPIWrite 0c6b,00
//coef_update_signal=0
SPIWrite 0c73,00
//coef_update_signal=0
SPIWrite 0e6b,00
//coef_update_signal=0
SPIWrite 0e73,00
//coef_update_signal=0


AFE77xx_GLOBAL
SPIWrite 0010,00
//PAGE:rx_top=0

// END: Completed RX, TX and FB Digital Chain Config.


//**********Step: Timing Controller initialization**********//
SPIWrite 0014,04
//PAGE:TIMING_CON=1(Meaning: );
SPIWrite 04e7,00
//enable_multi_sysref=0
SPIWrite 04c4,00
//mode_2t2r=0
SPIWrite 04c5,00
//fdd_mode=0
SPIWrite 0206,06
//force_tg_txAB=0
SPIWrite 0206,04
//force_tg_rxAB=0
SPIWrite 0206,00
//force_tg_fbAB=0
SPIWrite 036a,06
//force_tg_txCD=0
SPIWrite 036a,04
//force_tg_rxCD=0
SPIWrite 036a,00
//force_tg_fbCD=0
SPIWrite 04dc,80
//force_pll_txAB=0
SPIWrite 04dd,0d
//force_pll_txCD=0
SPIWrite 04dc,00
//force_pll_rxAB=0
SPIWrite 04dd,09
```

```
//force_pll_rxCD=0
SPIWrite 04dd,08
//force_pll_fbAB=0
SPIWrite 04dd,00
//force_pll_fbCD=0
SPIWrite 0110,00
//fb_vswr_pin_valid_cha=0
SPIWrite 0111,00
//fb_vswr_pin_valid_chc=0
SPIWrite 0118,00

//use_reg_for_tx_gswap_rxtxlo=0
//SPIWrite 0155,0f
//4Channel
//SPIWrite 011b,01
//TX SWAP 4T4R
SPIWrite 011c,01
//use_reg_for_txdsalatch=1
SPIWrite 0121,00
//en_reg_for_gswap=0
SPIWrite 0106,0f
//chsel_gswap=0f
SPIWrite 0114,00
//fb_ncosel_pin_valid_cha=0
SPIWrite 0115,00
//fb_ncosel_pin_valid_chc=0
SPIWrite 071f,90
//override_val_fbmuxsel=24
SPIWrite 071f,93
//override_fb_muxsel=3
SPIWrite 04c6,01
//dc_pll_sync_mode=1
SPIWrite 0014,00

//**********Step: Clock top writes**********//
//PAGE:TIMING_CON=0(Meaning: );
SPIWrite 0014,01
//PAGE:clktop_2t=1
SPIWrite 005c,10
//CTL_SEL_CM_BIAS_R_SHRT_RXCML_1P8=1
SPIWrite 005c,18
//CTL_FORCE_LDO_FILT_RXCML_1P8=1
SPIWrite 005c,1c
//CTL_FORCE_CASCODEFILT_RXCML_1P8=1
SPIWrite 005c,1e
//CTL_FORCE_BIASFILT_RXCML_1P8=1
```

```
SPIWrite 0014,00
//PAGE:clktop_2t=0


//**********Step: TDD pin override internally and Toggle**********//
// Overriding TDD Pins internally
SPIWrite 0014,04
//PAGE:TIMING_CON=1(Meaning: );
SPIWrite 0124,01
//use_reg_txon_AB=1
SPIWrite 0126,01
//use_reg_rxon_AB=1
SPIWrite 0128,01
//use_reg_fbon_AB=1
SPIWrite 012a,01
//use_reg_txon_CD=1
SPIWrite 012c,01
//use_reg_rxon_CD=1
SPIWrite 012e,01
//use_reg_fbon_CD=1
SPIWrite 0125,00
//reg_for_txon_AB=0
SPIWrite 0127,00
//reg_for_rxon_AB=0
SPIWrite 0129,00
//reg_for_fbon_AB=0
SPIWrite 012b,00
//reg_for_txon_CD=0
SPIWrite 012d,00
//reg_for_rxon_CD=0
SPIWrite 012f,00
//reg_for_fbon_CD=0


// Done overriding TDD Pins internally




// Overriding TDD Pins internally


SPIWrite 0124,01
//use_reg_txon_AB=1
SPIWrite 0126,01
//use_reg_rxon_AB=1
```

```
SPIWrite 0128,01
//use_reg_fbon_AB=1
SPIWrite 012a,01
//use_reg_txon_CD=1
SPIWrite 012c,01
//use_reg_rxon_CD=1
SPIWrite 012e,01
//use_reg_fbon_CD=1
SPIWrite 0125,01
//reg_for_txon_AB=1
SPIWrite 0127,01
//reg_for_rxon_AB=1
SPIWrite 0129,01
//reg_for_fbon_AB=1
SPIWrite 012b,01
//reg_for_txon_CD=1
SPIWrite 012d,01
//reg_for_rxon_CD=1
SPIWrite 012f,01
//reg_for_fbon_CD=1
SPIWrite 0014,00
// Done overriding TDD Pins internally



//**********Step: Doing DAC analog writes**********//
// Doing DAC Analog Writes
SPIWrite 0017,0f
//PAGE:dac_1t=f
SPIWrite 00bc,05
SPIWrite 00bc,55
SPIWrite 00bd,0a
SPIWrite 00bd,aa
SPIWrite 00be,14
SPIWrite 00bf,19
SPIWrite 00c0,19
SPIWrite 0052,14
SPIWrite 0052,b4
SPIWrite 0054,0a
SPIWrite 0055,14
SPIWrite 0056,19
SPIWrite 0057,19
SPIWrite 0040,08
SPIWrite 0040,18
SPIWrite 003f,00
SPIWrite 003e,00
SPIWrite 003d,00
```

SPIWrite 003c,03
SPIWrite 007b,03
SPIWrite 007a,ff
SPIWrite 007e,03
SPIWrite 007d,ff
SPIWrite 0081,03
SPIWrite 0080,ff
SPIWrite 0085,03
SPIWrite 0084,ff
SPIWrite 0089,00
SPIWrite 0088,03
SPIWrite 008d,00
SPIWrite 008c,03
SPIWrite 0091,01
SPIWrite 0090,ff
SPIWrite 0095,00
SPIWrite 0094,1f
SPIWrite 00c1,1e
SPIWrite 00c2,32
SPIWrite 006e,0a
SPIWrite 006e,aa
SPIWrite 0041,28
SPIWrite 0042,0a
SPIWrite 0042,aa
SPIWrite 0043,0a
SPIWrite 0043,aa
SPIWrite 0044,0a
SPIWrite 006f,0a
SPIWrite 0045,03
SPIWrite 0046,03
SPIWrite 0062,08
SPIWrite 0062,88
SPIWrite 0063,08
SPIWrite 0063,88
SPIWrite 0065,40
SPIWrite 0066,40
SPIWrite 0067,40
SPIWrite 0068,40
SPIWrite 0069,40
SPIWrite 006a,40
SPIWrite 006b,40
SPIWrite 006c,40
SPIWrite 0064,04
SPIWrite 0064,44
SPIWrite 00c8,05
SPIWrite 00c8,55
SPIWrite 00c9,02
SPIWrite 00c9,22

SPIWrite 00c9,08
SPIWrite 00c9,88
SPIWrite 00d5,e4
SPIWrite 00d8,e4
SPIWrite 00d6,1f
SPIWrite 00d7,1f
SPIWrite 00d9,a0
SPIWrite 00da,a0
SPIWrite 00af,92
SPIWrite 00ad,0f
SPIWrite 00b0,1f
SPIWrite 00a7,ff
SPIWrite 00a6,ff
SPIWrite 00a5,ff
SPIWrite 00a4,ff
SPIWrite 00a8,ff
SPIWrite 00ae,06
SPIWrite 00cb,ff
SPIWrite 00cc,ff
SPIWrite 00d5,b8
SPIWrite 00d8,b8
SPIWrite 006f,0a
SPIWrite 006f,aa
SPIWrite 006d,06
SPIWrite 006d,46
SPIWrite 0047,03
//IMD3
SPIWrite 009C,02
SPIWrite 009F,78
SPIWrite 009E,00
SPIWrite 0017,00

//PG1P1: Improved Time Variation of QMC
SPIWrite 0017,0F
SPIWrite 0065,7F
SPIWrite 0067,7F
SPIWrite 0069,7F
SPIWrite 006B,7F
SPIWrite 0066,7F
SPIWrite 0068,7F
SPIWrite 006A,7F
SPIWrite 006C,7F
SPIWrite 0062,02
SPIWrite 0062,22
SPIWrite 0063,02
SPIWrite 0063,22
SPIWrite 0064,07
SPIWrite 0064,77

```
SPIWrite 0047,03
SPIWrite 0017,00

// Completed DAC Analog Writes


//**********Step: Doing RX ADC analog writes**********//
// Doing RX ADC Analog Writes
SPIWrite 0011,0f
//PAGE:rx_ec_i=f
//SPIWrite 0334,30
//SPIWrite 0308,06
//SPIWrite 0335,38
//SPIWrite 0334,31
//SPIWrite 0309,0b
//SPIWrite 030a,03
SPIWrite 029d,03
SPIWrite 029d,1b
SPIWrite 029e,00
SPIWrite 029d,db
SPIWrite 0299,03
SPIWrite 029e,30
SPIWrite 029f,0c
SPIWrite 029f,6c
SPIWrite 02a0,03
SPIWrite 029e,30
SPIWrite 029f,6d
SPIWrite 02a0,13
//SPIWrite 0330,0e
//SPIWrite 0331,17
//SPIWrite 0332,08
//SPIWrite 04a0,04
SPIWrite 0011,00
//PAGE:rx_ec_i=0
SPIWrite 0011,f0
//PAGE:rx_ec_q=f
//SPIWrite 0334,30
//SPIWrite 0308,06
//SPIWrite 0335,38
//SPIWrite 0334,31
//SPIWrite 0309,0b
//SPIWrite 030a,03
SPIWrite 029d,03
SPIWrite 029d,1b
SPIWrite 029e,00
SPIWrite 029d,db
SPIWrite 0299,03
SPIWrite 029e,30
```

```
SPIWrite 029f,0c
SPIWrite 029f,6c
SPIWrite 02a0,03
SPIWrite 029e,30
SPIWrite 029f,6d
SPIWrite 02a0,13
//SPIWrite 0330,0e
//SPIWrite 0331,17
//SPIWrite 0332,08
//SPIWrite 04a0,04
SPIWrite 0011,00
//PAGE:rx_ec_q=0
SPIWrite 0011,0f
//PAGE:rx_ec_i=f
SPIWrite 0500,03
SPIWrite 0500,03
SPIWrite 0011,00
//PAGE:rx_ec_i=0
SPIWrite 0011,f0
//PAGE:rx_ec_q=f
SPIWrite 0500,03
SPIWrite 0500,03
SPIWrite 0011,00
//PAGE:rx_ec_q=0
SPIWrite 0011,10
//PAGE:rx_ec_q=1
SPIWrite 0293,02
SPIWrite 0011,20
//PAGE:rx_ec_q=2
SPIWrite 0293,02
SPIWrite 0011,40
//PAGE:rx_ec_q=4
SPIWrite 0293,02
SPIWrite 0011,80
//PAGE:rx_ec_q=8
SPIWrite 0293,02
SPIWrite 0011,00
//PAGE:rx_ec_q=0
SPIWrite 0011,0f
//PAGE:rx_ec_i=f
SPIWrite 0c70,08
SPIWrite 0c70,18
SPIWrite 0103,80
SPIWrite 0011,00
//PAGE:rx_ec_i=0
SPIWrite 0011,10
//PAGE:rx_ec_q=1
SPIWrite 0c74,02
```

```
SPIWrite 0103,80
SPIWrite 0011,00
//PAGE:rx_ec_q=0
SPIWrite 0011,01
//PAGE:rx_ec_i=1
SPIWrite 049f,00
SPIWrite 049e,00
SPIWrite 049f,04
SPIWrite 049e,01
SPIWrite 049d,00
SPIWrite 049c,01
SPIWrite 049c,00
SPIWrite 049d,00
SPIWrite 04a2,00
SPIWrite 04a2,01
SPIWrite 04a2,00
SPIWrite 049c,01

WAIT 5


SPIWrite 049c,00

WAIT 5


SPIWrite 049d,02
SPIWrite 0011,00
//PAGE:rx_ec_i=0
SPIWrite 0011,10
//PAGE:rx_ec_q=1
SPIWrite 049f,00
SPIWrite 049e,00
SPIWrite 049f,04
SPIWrite 049e,01
SPIWrite 049d,00
SPIWrite 049c,01
SPIWrite 049c,00
SPIWrite 049d,00
SPIWrite 04a2,00
SPIWrite 04a2,01
SPIWrite 04a2,00
SPIWrite 049c,01
```

WAIT 5

SPIWrite 049c,00

WAIT 5

SPIWrite 049d,02
SPIWrite 0011,00
//PAGE:rx_ec_q=0
SPIWrite 0011,02
//PAGE:rx_ec_i=2
SPIWrite 049f,00
SPIWrite 049e,00
SPIWrite 049f,04
SPIWrite 049e,01
SPIWrite 049d,00
SPIWrite 049c,01
SPIWrite 049c,00
SPIWrite 049d,00
SPIWrite 04a2,00
SPIWrite 04a2,01
SPIWrite 04a2,00
SPIWrite 049c,01

WAIT 5

SPIWrite 049c,00

WAIT 5

SPIWrite 049d,02
SPIWrite 0011,00
//PAGE:rx_ec_i=0
SPIWrite 0011,20
//PAGE:rx_ec_q=2
SPIWrite 049f,00

SPIWrite 049e,00
SPIWrite 049f,04
SPIWrite 049e,01
SPIWrite 049d,00
SPIWrite 049c,01
SPIWrite 049c,00
SPIWrite 049d,00
SPIWrite 04a2,00
SPIWrite 04a2,01
SPIWrite 04a2,00
SPIWrite 049c,01

WAIT 5

SPIWrite 049c,00

WAIT 5

SPIWrite 049d,02
SPIWrite 0011,00
//PAGE:rx_ec_q=0
SPIWrite 0011,04
//PAGE:rx_ec_i=4
SPIWrite 049f,00
SPIWrite 049e,00
SPIWrite 049f,04
SPIWrite 049e,01
SPIWrite 049d,00
SPIWrite 049c,01
SPIWrite 049c,00
SPIWrite 049d,00
SPIWrite 04a2,00
SPIWrite 04a2,01
SPIWrite 04a2,00
SPIWrite 049c,01

WAIT 5

SPIWrite 049c,00

WAIT 5

SPIWrite 049d,02
SPIWrite 0011,00
//PAGE:rx_ec_i=0
SPIWrite 0011,40
//PAGE:rx_ec_q=4
SPIWrite 049f,00
SPIWrite 049e,00
SPIWrite 049f,04
SPIWrite 049e,01
SPIWrite 049d,00
SPIWrite 049c,01
SPIWrite 049c,00
SPIWrite 049d,00
SPIWrite 04a2,00
SPIWrite 04a2,01
SPIWrite 04a2,00
SPIWrite 049c,01

WAIT 5

SPIWrite 049c,00

WAIT 5

SPIWrite 049d,02
SPIWrite 0011,00
//PAGE:rx_ec_q=0
SPIWrite 0011,08
//PAGE:rx_ec_i=8
SPIWrite 049f,00
SPIWrite 049e,00
SPIWrite 049f,04
SPIWrite 049e,01
SPIWrite 049d,00
SPIWrite 049c,01
SPIWrite 049c,00

SPIWrite 049d,00
SPIWrite 04a2,00
SPIWrite 04a2,01
SPIWrite 04a2,00
SPIWrite 049c,01

WAIT 5

SPIWrite 049c,00

WAIT 5

SPIWrite 049d,02
SPIWrite 0011,00
//PAGE:rx_ec_i=0
SPIWrite 0011,80
//PAGE:rx_ec_q=8
SPIWrite 049f,00
SPIWrite 049e,00
SPIWrite 049f,04
SPIWrite 049e,01
SPIWrite 049d,00
SPIWrite 049c,01
SPIWrite 049c,00
SPIWrite 049d,00
SPIWrite 04a2,00
SPIWrite 04a2,01
SPIWrite 04a2,00
SPIWrite 049c,01

WAIT 5

SPIWrite 049c,00

WAIT 5

```
SPIWrite 049d,02
SPIWrite 0011,00
//PAGE:rx_ec_q=0
SPIWrite 0011,0f
//PAGE:rx_ec_i=f
SPIWrite 0c70,10
SPIWrite 0c70,00
SPIWrite 0103,00
SPIWrite 0011,00
//PAGE:rx_ec_i=0
SPIWrite 0011,10
//PAGE:rx_ec_q=1
SPIWrite 0c74,00
SPIWrite 0103,00
SPIWrite 0011,00
//PAGE:rx_ec_q=0
SPIWrite 0011,0f
//PAGE:rx_ec_i=f
SPIWrite 0500,02
SPIWrite 0500,00
SPIWrite 050a,01
SPIWrite 0502,01
SPIWrite 0011,00
//PAGE:rx_ec_i=0
SPIWrite 0011,f0
//PAGE:rx_ec_q=f
SPIWrite 0500,02
SPIWrite 0500,00
SPIWrite 050a,01
SPIWrite 0502,01
SPIWrite 0011,00
//PAGE:rx_ec_q=0
SPIWrite 0012,0f
//PAGE:rx_ec_common=f
SPIWrite 04c4,20
SPIWrite 0012,00
//PAGE:rx_ec_common=0


// Completed RX ADC Analog Writes


//**********Step: Doing FB ADC analog writes**********//
// Doing FB ADC Analog Writes
SPIWrite 0010,10
//PAGE:fb_ec=1
SPIWrite 0010,10
SPIWrite 00b0,03
```

```
SPIWrite 0188,09
SPIWrite 0140,28
SPIWrite 0138,28
SPIWrite 0190,09
SPIWrite 0168,39
SPIWrite 0160,39
SPIWrite 0119,32
SPIWrite 0121,32
SPIWrite 0129,32
SPIWrite 0131,32
SPIWrite 0119,32
SPIWrite 0121,32
SPIWrite 0129,32
SPIWrite 0131,32
SPIWrite 0010,00
//PAGE:fb_ec=0
SPIWrite 0010,00
SPIWrite 0010,20
//PAGE:fb_ana=1
//SPIWrite 0010,20
//SPIWrite 0085,08
//SPIWrite 0010,00
//PAGE:fb_ana=0
SPIWrite 0010,00
SPIWrite 0010,00
//PAGE:fb_ec=2
SPIWrite 0010,40
SPIWrite 00b0,03
SPIWrite 0188,09
SPIWrite 0140,28
SPIWrite 0138,28
SPIWrite 0190,09
SPIWrite 0168,39
SPIWrite 0160,39
SPIWrite 0119,32
SPIWrite 0121,32
SPIWrite 0129,32
SPIWrite 0131,32
SPIWrite 0119,32
SPIWrite 0121,32
SPIWrite 0129,32
SPIWrite 0131,32
SPIWrite 0010,40
//PAGE:fb_ec=0
SPIWrite 0010,00
SPIWrite 0010,00
//PAGE:fb_ana=2
//SPIWrite 0010,80
```

```
//SPIWrite 0085,08
//SPIWrite 0010,a0
//PAGE:fb_ana=1
SPIWrite 0010,20
SPIWrite 0102,08
SPIWrite 0010,00
//PAGE:fb_ana=2
SPIWrite 0010,80
SPIWrite 0102,08
SPIWrite 0010,80
//PAGE:fb_ana=0
SPIWrite 0010,00
SPIWrite 0017,10
//PAGE:dac_2t=1
SPIWrite 002e,04
SPIWrite 0017,20
//PAGE:dac_2t=2
SPIWrite 002e,04
SPIWrite 0017,00
//PAGE:dac_2t=0
SPIWrite 0017,40
//PAGE:ana_2r=1
SPIWrite 003f,20
SPIWrite 003f,26
SPIWrite 0017,80
//PAGE:ana_2r=2
SPIWrite 003f,20
SPIWrite 003f,26
SPIWrite 0017,00
//PAGE:ana_2r=0

//FLVDD increase for FB to ?V
SPIWrite 0010,20
SPIWrite 0095,01
SPIWrite 0094,c0
SPIWrite 0010,00

SPIWrite 0010,20
//PAGE:fb_ana=1
SPIWrite 0010,20
SPIWrite 0080,10
SPIWrite 0080,18
SPIWrite 0010,00
//PAGE:fb_ana=2
SPIWrite 0010,80
SPIWrite 0080,10
SPIWrite 0080,18
SPIWrite 0010,a0
```

```
//PAGE:fb_ana=1
SPIWrite 0010,20
SPIWrite 009a,01
SPIWrite 0010,00
//PAGE:fb_ana=2
SPIWrite 0010,80
SPIWrite 009a,01
SPIWrite 0010,80
//PAGE:fb_ana=0
SPIWrite 0010,00

//FB
SPIWrite 0010,50
//PAGE:fb_ec=3
SPIWrite 0028,a1

WAIT 10
SPIWrite 0028,a0
SPIWrite 0010,00
//PAGE:fb_ec=0

//OVR Comparator calib
SPIWrite 0010,50
SPIWrite 00a0,01
WAIT 100
SPIWrite 00a0,00
SPIWrite 0010,00


// Completed FB ADC Analog Writes


//**********Step: Doing JESD TX configuration**********//

// Configuring Device JESD TX
SPIWrite 0015,01
//PAGE:rx_jesd=3
SPIWrite 0015,11
SPIWrite 00b0,04
//hd_sts_pll_lock_override=1
SPIWrite 00b0,0c
//hd_sts_pll_lock_reg=1
SPIWrite 00dc,02
//lc_init_state_serdesfifo_spi_ovr=0
SPIWrite 00dd,00
//lc_gearbox_init_state=0
SPIWrite 0052,05
//ddc_bypass_8lanemode_en=0
```

```
SPIWrite 0045,e0
//init_state=1
SPIWrite 0045,e0
//fifo_init_state=1
SPIWrite 0045,e0
//fb_init_state=1
SPIWrite 0026,0f
//jesd_clear_data=f
SPIWrite 0020,37
//sysref_jesd_mode=1
SPIWrite 0020,3f
//k_m1=1f
SPIWrite 0021,1f
//fb_k_m1=1f
SPIWrite 0043,10
//jesd_mode=10
SPIWrite 0044,15
//fb_jesd_mode=15
SPIWrite 0076,00
//adc_jesd_root_clk_div=0
SPIWrite 00c0,10
//ddc_rd_clk_ratio_rx1=10
SPIWrite 00c0,30
//ddc_rd_clk_ratio_rx1_override=1
SPIWrite 00c1,10
//ddc_rd_clk_ratio_rx2=10
SPIWrite 00c1,30
//ddc_rd_clk_ratio_rx2_override=1
SPIWrite 00c4,00
//jesd_tx_clk_ratio_rx1=0
SPIWrite 00c4,20
//jesd_tx_clk_ratio_rx1_override=1
SPIWrite 00c5,00
//jesd_tx_clk_ratio_rx2=0
SPIWrite 00c5,20
//jesd_tx_clk_ratio_rx2_override=1
SPIWrite 0060,08
//jesd_system_mode=2
SPIWrite 0080,01
//scr_64b_initval=1
SPIWrite 0081,00
SPIWrite 0082,00
SPIWrite 0083,00
SPIWrite 0084,00
SPIWrite 0085,00
SPIWrite 0086,00
SPIWrite 0087,00
SPIWrite 0088,01
```

```
//scr_64b_en=1
SPIWrite 004f,01
//jesd_std_sel=1
SPIWrite 005f,00
//dedicated_rx_fb_lane_mode=0
SPIWrite 00ca,01
//sample_drop_mode_rx1=1
SPIWrite 00ca,11
//sample_drop_mode_rx2=1
SPIWrite 0022,01
//scr=1
SPIWrite 0023,01
//fb_scr=1
SPIWrite 0025,03
//lane_ena=3
SPIWrite 0015,10
//PAGE:rx_jesd=0
SPIWrite 0025,00
//lane_ena=0
SPIWrite 0015,00
// Done configuring Device JESD TX



//**********Step: Doing JESD RX configuration**********//
// Configuring Device JESD RX
SPIWrite 0015,02
//PAGE:tx_jesd=3
SPIWrite 0015,22
SPIWrite 0123,7F
//comma_align_valid_thresh_tx0=127

SPIWrite 007f,1f
//k_m1=1f
SPIWrite 007e,0a
//rbd_m1=0a
SPIWrite 0020,01
//init_state_tx0=1
SPIWrite 0081,ff
//jesd_clear_data=ff
SPIWrite 0023,0b
//lc_gearbox_init_state_ovr=1(Meaning: );
SPIWrite 0023,09
//lc_gearbox_init_state=0(Meaning: );
SPIWrite 0021,00
//dac_jesd_root_clk_div=0
SPIWrite 013d,10
```

```
//duc_wr_clk_ratio_tx0=10
SPIWrite 013f,00
//jesd_rx_clk_ratio_tx0=0
SPIWrite 0024,09
//jesd_mode_tx0=9
SPIWrite 013d,30
//duc_wr_clk_ratio_tx0_override=1
SPIWrite 013f,20
//jesd_rx_clk_ratio_tx0_override=1
SPIWrite 002d,9b
//spi_txenable=1
SPIWrite 0093,ff
//spidac=7fff
SPIWrite 0094,7f
SPIWrite 0093,ff
//spidac=7fff
SPIWrite 0094,7f
SPIWrite 0092,00
//spidac_ena=0
SPIWrite 0092,00
//spidac_ena=0
SPIWrite 008b,df
//sync_request_ena=df
SPIWrite 0148,00
//jesd_c_ena=0
SPIWrite 0148,02
//jesd_h_ena=1
SPIWrite 007d,92
//scr=1
SPIWrite 007c,03
//lane_ena=3
SPIWrite 0015,20
//PAGE:tx_jesd=0
SPIWrite 007c,00
//lane_ena=0
SPIWrite 0015,00

// Done configuring Device JESD RX



//**********Step: Doing GPIO configuration**********//
// Configuring GPIO for internal AGC Mode
SPIWrite 0015,80
//PAGE:DIGTOP_MISC=1(Meaning: );
SPIWrite 07e9,00
//parallel_apb_mode_input=0(Meaning: );
SPIWrite 07e9,00
```

```
//parallel_apb_mode_output=0(Meaning: );
SPIWrite 07e9,00
//parallel_memory_access_mode_input=0(Meaning: );
SPIWrite 07e9,00
//parallel_memory_access_mode_output=0(Meaning: );
SPIWrite 0400,01
//buf_dir_ctrl_gpio_0=1
SPIWrite 0400,01
//preferred_input_sel_gpio_0=0
SPIWrite 0400,01
//preferred_output_sel_gpio_0=0
SPIWrite 0401,4e
//crossbar_sel_input_gpio_0=4e
SPIWrite 0402,00
//crossbar_sel_output_gpio_0=0
SPIWrite 0403,00
//activ_bir_dir_ctrl_gpio_0=0
SPIWrite 0404,01
//buf_dir_ctrl_gpio_1=1
SPIWrite 0404,05
//preferred_input_sel_gpio_1=1
SPIWrite 0404,05
//preferred_output_sel_gpio_1=0
SPIWrite 0405,00
//crossbar_sel_input_gpio_1=0
SPIWrite 0406,00
//crossbar_sel_output_gpio_1=0
SPIWrite 0407,00
//activ_bir_dir_ctrl_gpio_1=0
SPIWrite 0408,01
//buf_dir_ctrl_gpio_2=1
SPIWrite 0408,05
//preferred_input_sel_gpio_2=1
SPIWrite 0408,05
//preferred_output_sel_gpio_2=0
SPIWrite 0409,00
//crossbar_sel_input_gpio_2=0
SPIWrite 040a,00
//crossbar_sel_output_gpio_2=0
SPIWrite 040b,00
//activ_bir_dir_ctrl_gpio_2=0
SPIWrite 040c,01
//buf_dir_ctrl_gpio_3=1
SPIWrite 040c,05
//preferred_input_sel_gpio_3=1
SPIWrite 040c,05
//preferred_output_sel_gpio_3=0
SPIWrite 040d,00
```

```
//crossbar_sel_input_gpio_3=0
SPIWrite 040e,00
//crossbar_sel_output_gpio_3=0
SPIWrite 040f,00
//activ_bir_dir_ctrl_gpio_3=0
SPIWrite 0410,01
//buf_dir_ctrl_gpio_4=1
SPIWrite 0410,05
//preferred_input_sel_gpio_4=1
SPIWrite 0410,05
//preferred_output_sel_gpio_4=0
SPIWrite 0411,00
//crossbar_sel_input_gpio_4=0
SPIWrite 0412,00
//crossbar_sel_output_gpio_4=0
SPIWrite 0413,00
//activ_bir_dir_ctrl_gpio_4=0
SPIWrite 0414,01
//buf_dir_ctrl_gpio_5=1
SPIWrite 0414,05
//preferred_input_sel_gpio_5=1
SPIWrite 0414,05
//preferred_output_sel_gpio_5=0
SPIWrite 0415,00
//crossbar_sel_input_gpio_5=0
SPIWrite 0416,00
//crossbar_sel_output_gpio_5=0
SPIWrite 0417,00
//activ_bir_dir_ctrl_gpio_5=0
SPIWrite 0418,01
//buf_dir_ctrl_gpio_6=1
SPIWrite 0418,05
//preferred_input_sel_gpio_6=1
SPIWrite 0418,05
//preferred_output_sel_gpio_6=0
SPIWrite 0419,00
//crossbar_sel_input_gpio_6=0
SPIWrite 041a,00
//crossbar_sel_output_gpio_6=0
SPIWrite 041b,00
//activ_bir_dir_ctrl_gpio_6=0
SPIWrite 041c,01
//buf_dir_ctrl_gpio_7=1
SPIWrite 041c,05
//preferred_input_sel_gpio_7=1
SPIWrite 041c,05
//preferred_output_sel_gpio_7=0
SPIWrite 041d,00
```

```
//crossbar_sel_input_gpio_7=0
SPIWrite 041e,00
//crossbar_sel_output_gpio_7=0
SPIWrite 041f,00
//activ_bir_dir_ctrl_gpio_7=0
SPIWrite 0420,01
//buf_dir_ctrl_gpio_8=1
SPIWrite 0420,05
//preferred_input_sel_gpio_8=1
SPIWrite 0420,05
//preferred_output_sel_gpio_8=0
SPIWrite 0421,00
//crossbar_sel_input_gpio_8=0
SPIWrite 0422,00
//crossbar_sel_output_gpio_8=0
SPIWrite 0423,00
//activ_bir_dir_ctrl_gpio_8=0
SPIWrite 0424,02
//buf_dir_ctrl_gpio_9=2
SPIWrite 0424,02
//preferred_input_sel_gpio_9=0
SPIWrite 0424,22
//preferred_output_sel_gpio_9=1
SPIWrite 0425,00
//crossbar_sel_input_gpio_9=0
SPIWrite 0426,00
//crossbar_sel_output_gpio_9=0
SPIWrite 0427,0a
//activ_bir_dir_ctrl_gpio_9=5
SPIWrite 0428,00
//buf_dir_ctrl_gpio_10=0
SPIWrite 0428,00
//preferred_input_sel_gpio_10=0
SPIWrite 0429,00
//crossbar_sel_input_gpio_10=0
SPIWrite 0428,00
//preferred_output_sel_gpio_10=0
SPIWrite 042a,00
//crossbar_sel_output_gpio_10=0
SPIWrite 042b,00
//activ_bir_dir_ctrl_gpio_10=0
SPIWrite 042c,02
//buf_dir_ctrl_gpio_11=2
SPIWrite 042c,02
//preferred_input_sel_gpio_11=0
SPIWrite 042c,22
//preferred_output_sel_gpio_11=1
SPIWrite 042d,00
```

```
//crossbar_sel_input_gpio_11=0
SPIWrite 042e,00
//crossbar_sel_output_gpio_11=0
SPIWrite 042f,0e
//activ_bir_dir_ctrl_gpio_11=7
SPIWrite 0430,01
//buf_dir_ctrl_gpio_12=1
SPIWrite 0430,05
//preferred_input_sel_gpio_12=1
SPIWrite 0430,05
//preferred_output_sel_gpio_12=0
SPIWrite 0431,00
//crossbar_sel_input_gpio_12=0
SPIWrite 0432,00
//crossbar_sel_output_gpio_12=0
SPIWrite 0433,00
//activ_bir_dir_ctrl_gpio_12=0
SPIWrite 0434,00
//buf_dir_ctrl_gpio_13=0
SPIWrite 0434,00
//preferred_input_sel_gpio_13=0
SPIWrite 0435,00
//crossbar_sel_input_gpio_13=0
SPIWrite 0434,00
//preferred_output_sel_gpio_13=0
SPIWrite 0436,00
//crossbar_sel_output_gpio_13=0
SPIWrite 0437,00
//activ_bir_dir_ctrl_gpio_13=0
SPIWrite 0438,01
//buf_dir_ctrl_gpio_14=1
SPIWrite 0438,05
//preferred_input_sel_gpio_14=1
SPIWrite 0438,05
//preferred_output_sel_gpio_14=0
SPIWrite 0439,00
//crossbar_sel_input_gpio_14=0
SPIWrite 043a,00
//crossbar_sel_output_gpio_14=0
SPIWrite 043b,00
//activ_bir_dir_ctrl_gpio_14=0
SPIWrite 043c,00
//buf_dir_ctrl_gpio_15=0
SPIWrite 043c,00
//preferred_input_sel_gpio_15=0
SPIWrite 043d,00
//crossbar_sel_input_gpio_15=0
SPIWrite 043c,00
```

```
//preferred_output_sel_gpio_15=0
SPIWrite 043e,00
//crossbar_sel_output_gpio_15=0
SPIWrite 043f,00
//activ_bir_dir_ctrl_gpio_15=0
SPIWrite 0440,00
//buf_dir_ctrl_gpio_16=0
SPIWrite 0440,00
//preferred_input_sel_gpio_16=0
SPIWrite 0441,00
//crossbar_sel_input_gpio_16=0
SPIWrite 0440,00
//preferred_output_sel_gpio_16=0
SPIWrite 0442,00
//crossbar_sel_output_gpio_16=0
SPIWrite 0443,00
//activ_bir_dir_ctrl_gpio_16=0
SPIWrite 0444,01
//buf_dir_ctrl_gpio_17=1
SPIWrite 0444,05
//preferred_input_sel_gpio_17=1
SPIWrite 0444,05
//preferred_output_sel_gpio_17=0
SPIWrite 0445,00
//crossbar_sel_input_gpio_17=0
SPIWrite 0446,00
//crossbar_sel_output_gpio_17=0
SPIWrite 0447,00
//activ_bir_dir_ctrl_gpio_17=0
SPIWrite 0448,01
//buf_dir_ctrl_gpio_18=1
SPIWrite 0448,05
//preferred_input_sel_gpio_18=1
SPIWrite 0448,05
//preferred_output_sel_gpio_18=0
SPIWrite 0449,00
//crossbar_sel_input_gpio_18=0
SPIWrite 044a,00
//crossbar_sel_output_gpio_18=0
SPIWrite 044b,00
//activ_bir_dir_ctrl_gpio_18=0
SPIWrite 044c,00
//buf_dir_ctrl_gpio_19=0
SPIWrite 044c,00
//preferred_input_sel_gpio_19=0
SPIWrite 044d,00
//crossbar_sel_input_gpio_19=0
SPIWrite 044c,00
```

```
//preferred_output_sel_gpio_19=0
SPIWrite 044e,00
//crossbar_sel_output_gpio_19=0
SPIWrite 044f,00
//activ_bir_dir_ctrl_gpio_19=0
SPIWrite 0450,01
//buf_dir_ctrl_gpio_20=1
SPIWrite 0450,05
//preferred_input_sel_gpio_20=1
SPIWrite 0450,05
//preferred_output_sel_gpio_20=0
SPIWrite 0451,00
//crossbar_sel_input_gpio_20=0
SPIWrite 0452,00
//crossbar_sel_output_gpio_20=0
SPIWrite 0453,00
//activ_bir_dir_ctrl_gpio_20=0
SPIWrite 0454,01
//buf_dir_ctrl_gpio_21=1
SPIWrite 0454,05
//preferred_input_sel_gpio_21=1
SPIWrite 0454,05
//preferred_output_sel_gpio_21=0
SPIWrite 0455,00
//crossbar_sel_input_gpio_21=0
SPIWrite 0456,00
//crossbar_sel_output_gpio_21=0
SPIWrite 0457,00
//activ_bir_dir_ctrl_gpio_21=0
SPIWrite 0458,02
//buf_dir_ctrl_gpio_22=2
SPIWrite 0458,02
//preferred_input_sel_gpio_22=0
SPIWrite 0458,22
//preferred_output_sel_gpio_22=1
SPIWrite 0459,00
//crossbar_sel_input_gpio_22=0
SPIWrite 045a,00
//crossbar_sel_output_gpio_22=0
SPIWrite 045b,00
//activ_bir_dir_ctrl_gpio_22=0
SPIWrite 045c,00
//buf_dir_ctrl_gpio_23=0
SPIWrite 045c,00
//preferred_input_sel_gpio_23=0
SPIWrite 045d,00
//crossbar_sel_input_gpio_23=0
SPIWrite 045c,00
```

```
//preferred_output_sel_gpio_23=0
SPIWrite 045e,00
//crossbar_sel_output_gpio_23=0
SPIWrite 045f,00
//activ_bir_dir_ctrl_gpio_23=0
SPIWrite 0460,00
//buf_dir_ctrl_gpio_24=0
SPIWrite 0460,00
//preferred_input_sel_gpio_24=0
SPIWrite 0461,00
//crossbar_sel_input_gpio_24=0
SPIWrite 0460,00
//preferred_output_sel_gpio_24=0
SPIWrite 0462,00
//crossbar_sel_output_gpio_24=0
SPIWrite 0463,00
//activ_bir_dir_ctrl_gpio_24=0
SPIWrite 0464,00
//buf_dir_ctrl_gpio_25=0
SPIWrite 0464,00
//preferred_input_sel_gpio_25=0
SPIWrite 0465,00
//crossbar_sel_input_gpio_25=0
SPIWrite 0464,00
//preferred_output_sel_gpio_25=0
SPIWrite 0466,00
//crossbar_sel_output_gpio_25=0
SPIWrite 0467,00
//activ_bir_dir_ctrl_gpio_25=0
SPIWrite 0468,01
//buf_dir_ctrl_gpio_26=1
SPIWrite 0468,05
//preferred_input_sel_gpio_26=1
SPIWrite 0468,05
//preferred_output_sel_gpio_26=0
SPIWrite 0469,00
//crossbar_sel_input_gpio_26=0
SPIWrite 046a,00
//crossbar_sel_output_gpio_26=0
SPIWrite 046b,00
//activ_bir_dir_ctrl_gpio_26=0
SPIWrite 046c,02
//buf_dir_ctrl_gpio_27=2
SPIWrite 046c,02
//preferred_input_sel_gpio_27=0
SPIWrite 046c,22
//preferred_output_sel_gpio_27=1
SPIWrite 046d,00
```

```
//crossbar_sel_input_gpio_27=0
SPIWrite 046e,00
//crossbar_sel_output_gpio_27=0
SPIWrite 046f,00
//activ_bir_dir_ctrl_gpio_27=0
SPIWrite 0470,00
//buf_dir_ctrl_gpio_28=0
SPIWrite 0470,00
//preferred_input_sel_gpio_28=0
SPIWrite 0471,00
//crossbar_sel_input_gpio_28=0
SPIWrite 0470,00
//preferred_output_sel_gpio_28=0
SPIWrite 0472,00
//crossbar_sel_output_gpio_28=0
SPIWrite 0473,00
//activ_bir_dir_ctrl_gpio_28=0
SPIWrite 0474,00
//buf_dir_ctrl_gpio_29=0
SPIWrite 0474,00
//preferred_input_sel_gpio_29=0
SPIWrite 0475,00
//crossbar_sel_input_gpio_29=0
SPIWrite 0474,00
//preferred_output_sel_gpio_29=0
SPIWrite 0476,00
//crossbar_sel_output_gpio_29=0
SPIWrite 0477,00
//activ_bir_dir_ctrl_gpio_29=0
SPIWrite 0478,00
//buf_dir_ctrl_gpio_30=0
SPIWrite 0478,00
//preferred_input_sel_gpio_30=0
SPIWrite 0479,00
//crossbar_sel_input_gpio_30=0
SPIWrite 0478,00
//preferred_output_sel_gpio_30=0
SPIWrite 047a,00
//crossbar_sel_output_gpio_30=0
SPIWrite 047b,00
//activ_bir_dir_ctrl_gpio_30=0
SPIWrite 047c,00
//buf_dir_ctrl_gpio_31=0
SPIWrite 047c,00
//preferred_input_sel_gpio_31=0
SPIWrite 047d,00
//crossbar_sel_input_gpio_31=0
SPIWrite 047c,00
```

```
//preferred_output_sel_gpio_31=0
SPIWrite 047e,00
//crossbar_sel_output_gpio_31=0
SPIWrite 047f,00
//activ_bir_dir_ctrl_gpio_31=0
SPIWrite 0480,00
//buf_dir_ctrl_gpio_32=0
SPIWrite 0480,00
//preferred_input_sel_gpio_32=0
SPIWrite 0481,00
//crossbar_sel_input_gpio_32=0
SPIWrite 0480,00
//preferred_output_sel_gpio_32=0
SPIWrite 0482,00
//crossbar_sel_output_gpio_32=0
SPIWrite 0483,00
//activ_bir_dir_ctrl_gpio_32=0
SPIWrite 0484,00
//buf_dir_ctrl_gpio_33=0
SPIWrite 0484,00
//preferred_input_sel_gpio_33=0
SPIWrite 0485,00
//crossbar_sel_input_gpio_33=0
SPIWrite 0484,00
//preferred_output_sel_gpio_33=0
SPIWrite 0486,00
//crossbar_sel_output_gpio_33=0
SPIWrite 0487,00
//activ_bir_dir_ctrl_gpio_33=0
SPIWrite 0488,00
//buf_dir_ctrl_gpio_34=0
SPIWrite 0488,00
//preferred_input_sel_gpio_34=0
SPIWrite 0489,00
//crossbar_sel_input_gpio_34=0
SPIWrite 0488,00
//preferred_output_sel_gpio_34=0
SPIWrite 048a,00
//crossbar_sel_output_gpio_34=0
SPIWrite 048b,00
//activ_bir_dir_ctrl_gpio_34=0
SPIWrite 048c,01
//buf_dir_ctrl_gpio_35=1
SPIWrite 048c,05
//preferred_input_sel_gpio_35=1
SPIWrite 048c,05
//preferred_output_sel_gpio_35=0
SPIWrite 048d,00
```

```
//crossbar_sel_input_gpio_35=0
SPIWrite 048e,00
//crossbar_sel_output_gpio_35=0
SPIWrite 048f,00
//activ_bir_dir_ctrl_gpio_35=0
SPIWrite 0490,00
//buf_dir_ctrl_gpio_36=0
SPIWrite 0490,00
//preferred_input_sel_gpio_36=0
SPIWrite 0491,00
//crossbar_sel_input_gpio_36=0
SPIWrite 0490,00
//preferred_output_sel_gpio_36=0
SPIWrite 0492,00
//crossbar_sel_output_gpio_36=0
SPIWrite 0493,00
//activ_bir_dir_ctrl_gpio_36=0
SPIWrite 0494,00
//buf_dir_ctrl_gpio_37=0
SPIWrite 0494,00
//preferred_input_sel_gpio_37=0
SPIWrite 0495,00
//crossbar_sel_input_gpio_37=0
SPIWrite 0494,00
//preferred_output_sel_gpio_37=0
SPIWrite 0496,00
//crossbar_sel_output_gpio_37=0
SPIWrite 0497,00
//activ_bir_dir_ctrl_gpio_37=0
SPIWrite 0498,00
//buf_dir_ctrl_gpio_38=0
SPIWrite 0498,00
//preferred_input_sel_gpio_38=0
SPIWrite 0499,00
//crossbar_sel_input_gpio_38=0
SPIWrite 0498,00
//preferred_output_sel_gpio_38=0
SPIWrite 049a,00
//crossbar_sel_output_gpio_38=0
SPIWrite 049b,00
//activ_bir_dir_ctrl_gpio_38=0
SPIWrite 049c,00
//buf_dir_ctrl_gpio_39=0
SPIWrite 049c,00
//preferred_input_sel_gpio_39=0
SPIWrite 049d,00
//crossbar_sel_input_gpio_39=0
SPIWrite 049c,00
```

```
//preferred_output_sel_gpio_39=0
SPIWrite 049e,00
//crossbar_sel_output_gpio_39=0
SPIWrite 049f,00
//activ_bir_dir_ctrl_gpio_39=0
SPIWrite 04a0,01
//buf_dir_ctrl_gpio_40=1
SPIWrite 04a0,05
//preferred_input_sel_gpio_40=1
SPIWrite 04a0,05
//preferred_output_sel_gpio_40=0
SPIWrite 04a1,00
//crossbar_sel_input_gpio_40=0
SPIWrite 04a2,00
//crossbar_sel_output_gpio_40=0
SPIWrite 04a3,00
//activ_bir_dir_ctrl_gpio_40=0
SPIWrite 04a4,02
//buf_dir_ctrl_gpio_41=2
SPIWrite 04a4,02
//preferred_input_sel_gpio_41=0
SPIWrite 04a4,42
//preferred_output_sel_gpio_41=2
SPIWrite 04a5,00
//crossbar_sel_input_gpio_41=0
SPIWrite 04a6,00
//crossbar_sel_output_gpio_41=0
SPIWrite 04a7,00
//activ_bir_dir_ctrl_gpio_41=0
SPIWrite 04a8,02
//buf_dir_ctrl_gpio_42=2
SPIWrite 04a8,02
//preferred_input_sel_gpio_42=0
SPIWrite 04a8,22
//preferred_output_sel_gpio_42=1
SPIWrite 04a9,00
//crossbar_sel_input_gpio_42=0
SPIWrite 04aa,00
//crossbar_sel_output_gpio_42=0
SPIWrite 04ab,00
//activ_bir_dir_ctrl_gpio_42=0
SPIWrite 04ac,00
//buf_dir_ctrl_gpio_43=0
SPIWrite 04ac,00
//preferred_input_sel_gpio_43=0
SPIWrite 04ad,00
//crossbar_sel_input_gpio_43=0
SPIWrite 04ac,00
```

```
//preferred_output_sel_gpio_43=0
SPIWrite 04ae,00
//crossbar_sel_output_gpio_43=0
SPIWrite 04af,00
//activ_bir_dir_ctrl_gpio_43=0
SPIWrite 04b0,02
//buf_dir_ctrl_gpio_44=2
SPIWrite 04b0,02
//preferred_input_sel_gpio_44=0
SPIWrite 04b0,42
//preferred_output_sel_gpio_44=2
SPIWrite 04b1,00
//crossbar_sel_input_gpio_44=0
SPIWrite 04b2,00
//crossbar_sel_output_gpio_44=0
SPIWrite 04b3,00
//activ_bir_dir_ctrl_gpio_44=0
SPIWrite 04b4,00
//buf_dir_ctrl_gpio_45=0
SPIWrite 04b4,00
//preferred_input_sel_gpio_45=0
SPIWrite 04b5,00
//crossbar_sel_input_gpio_45=0
SPIWrite 04b4,00
//preferred_output_sel_gpio_45=0
SPIWrite 04b6,00
//crossbar_sel_output_gpio_45=0
SPIWrite 04b7,00
//activ_bir_dir_ctrl_gpio_45=0
SPIWrite 04b8,02
//buf_dir_ctrl_gpio_46=2
SPIWrite 04b8,02
//preferred_input_sel_gpio_46=0
SPIWrite 04b8,22
//preferred_output_sel_gpio_46=1
SPIWrite 04b9,00
//crossbar_sel_input_gpio_46=0
SPIWrite 04ba,00
//crossbar_sel_output_gpio_46=0
SPIWrite 04bb,00
//activ_bir_dir_ctrl_gpio_46=0
SPIWrite 04bc,02
//buf_dir_ctrl_gpio_47=2
SPIWrite 04bc,02
//preferred_input_sel_gpio_47=0
SPIWrite 04bc,22
//preferred_output_sel_gpio_47=1
SPIWrite 04bd,00
```

```
//crossbar_sel_input_gpio_47=0
SPIWrite 04be,00
//crossbar_sel_output_gpio_47=0
SPIWrite 04bf,00
//activ_bir_dir_ctrl_gpio_47=0
SPIWrite 04c0,01
//buf_dir_ctrl_gpio_48=1
SPIWrite 04c0,05
//preferred_input_sel_gpio_48=1
SPIWrite 04c0,05
//preferred_output_sel_gpio_48=0
SPIWrite 04c1,00
//crossbar_sel_input_gpio_48=0
SPIWrite 04c2,00
//crossbar_sel_output_gpio_48=0
SPIWrite 04c3,00
//activ_bir_dir_ctrl_gpio_48=0
SPIWrite 04c4,02
//buf_dir_ctrl_gpio_49=2
SPIWrite 04c4,02
//preferred_input_sel_gpio_49=0
SPIWrite 04c4,22
//preferred_output_sel_gpio_49=1
SPIWrite 04c5,00
//crossbar_sel_input_gpio_49=0
SPIWrite 04c6,00
//crossbar_sel_output_gpio_49=0
SPIWrite 04c7,00
//activ_bir_dir_ctrl_gpio_49=0
SPIWrite 04c8,00
//buf_dir_ctrl_gpio_50=0
SPIWrite 04c8,00
//preferred_input_sel_gpio_50=0
SPIWrite 04c9,00
//crossbar_sel_input_gpio_50=0
SPIWrite 04c8,00
//preferred_output_sel_gpio_50=0
SPIWrite 04ca,00
//crossbar_sel_output_gpio_50=0
SPIWrite 04cb,00
//activ_bir_dir_ctrl_gpio_50=0
SPIWrite 04cc,01
//buf_dir_ctrl_gpio_51=1
SPIWrite 04cc,05
//preferred_input_sel_gpio_51=1
SPIWrite 04cc,05
//preferred_output_sel_gpio_51=0
SPIWrite 04cd,00
```

```
//crossbar_sel_input_gpio_51=0
SPIWrite 04ce,00
//crossbar_sel_output_gpio_51=0
SPIWrite 04cf,00
//activ_bir_dir_ctrl_gpio_51=0
SPIWrite 04d0,02
//buf_dir_ctrl_gpio_52=2
SPIWrite 04d0,02
//preferred_input_sel_gpio_52=0
SPIWrite 04d0,42
//preferred_output_sel_gpio_52=2
SPIWrite 04d1,00
//crossbar_sel_input_gpio_52=0
SPIWrite 04d2,00
//crossbar_sel_output_gpio_52=0
SPIWrite 04d3,00
//activ_bir_dir_ctrl_gpio_52=0
SPIWrite 04d4,02
//buf_dir_ctrl_gpio_53=2
SPIWrite 04d4,02
//preferred_input_sel_gpio_53=0
SPIWrite 04d4,42
//preferred_output_sel_gpio_53=2
SPIWrite 04d5,00
//crossbar_sel_input_gpio_53=0
SPIWrite 04d6,00
//crossbar_sel_output_gpio_53=0
SPIWrite 04d7,00
//activ_bir_dir_ctrl_gpio_53=0
SPIWrite 04d8,00
//buf_dir_ctrl_gpio_54=0
SPIWrite 04d8,00
//preferred_input_sel_gpio_54=0
SPIWrite 04d9,00
//crossbar_sel_input_gpio_54=0
SPIWrite 04d8,00
//preferred_output_sel_gpio_54=0
SPIWrite 04da,00
//crossbar_sel_output_gpio_54=0
SPIWrite 04db,00
//activ_bir_dir_ctrl_gpio_54=0
SPIWrite 04dc,02
//buf_dir_ctrl_gpio_55=2
SPIWrite 04dc,02
//preferred_input_sel_gpio_55=0
SPIWrite 04dc,42
//preferred_output_sel_gpio_55=2
SPIWrite 04dd,00
```

```
//crossbar_sel_input_gpio_55=0
SPIWrite 04de,00
//crossbar_sel_output_gpio_55=0
SPIWrite 04df,00
//activ_bir_dir_ctrl_gpio_55=0
SPIWrite 04e0,02
//buf_dir_ctrl_gpio_56=2
SPIWrite 04e0,02
//preferred_input_sel_gpio_56=0
SPIWrite 04e0,42
//preferred_output_sel_gpio_56=2
SPIWrite 04e1,00
//crossbar_sel_input_gpio_56=0
SPIWrite 04e2,00
//crossbar_sel_output_gpio_56=0
SPIWrite 04e3,00
//activ_bir_dir_ctrl_gpio_56=0
SPIWrite 04e4,01
//buf_dir_ctrl_gpio_57=1
SPIWrite 04e4,05
//preferred_input_sel_gpio_57=1
SPIWrite 04e4,05
//preferred_output_sel_gpio_57=0
SPIWrite 04e5,00
//crossbar_sel_input_gpio_57=0
SPIWrite 04e6,00
//crossbar_sel_output_gpio_57=0
SPIWrite 04e7,00
//activ_bir_dir_ctrl_gpio_57=0
SPIWrite 04e8,02
//buf_dir_ctrl_gpio_58=2
SPIWrite 04e8,02
//preferred_input_sel_gpio_58=0
SPIWrite 04e8,22
//preferred_output_sel_gpio_58=1
SPIWrite 04e9,00
//crossbar_sel_input_gpio_58=0
SPIWrite 04ea,00
//crossbar_sel_output_gpio_58=0
SPIWrite 04eb,00
//activ_bir_dir_ctrl_gpio_58=0
SPIWrite 04ec,02
//buf_dir_ctrl_gpio_59=2
SPIWrite 04ec,02
//preferred_input_sel_gpio_59=0
SPIWrite 04ec,22
//preferred_output_sel_gpio_59=1
SPIWrite 04ed,00
```

```
//crossbar_sel_input_gpio_59=0
SPIWrite 04ee,00
//crossbar_sel_output_gpio_59=0
SPIWrite 04ef,00
//activ_bir_dir_ctrl_gpio_59=0
SPIWrite 04f0,02
//buf_dir_ctrl_gpio_60=2
SPIWrite 04f0,02
//preferred_input_sel_gpio_60=0
SPIWrite 04f0,42
//preferred_output_sel_gpio_60=2
SPIWrite 04f1,00
//crossbar_sel_input_gpio_60=0
SPIWrite 04f2,00
//crossbar_sel_output_gpio_60=0
SPIWrite 04f3,00
//activ_bir_dir_ctrl_gpio_60=0
SPIWrite 04f4,01
//buf_dir_ctrl_gpio_61=1
SPIWrite 04f4,05
//preferred_input_sel_gpio_61=1
SPIWrite 04f4,05
//preferred_output_sel_gpio_61=0
SPIWrite 04f5,00
//crossbar_sel_input_gpio_61=0
SPIWrite 04f6,00
//crossbar_sel_output_gpio_61=0
SPIWrite 04f7,00
//activ_bir_dir_ctrl_gpio_61=0
SPIWrite 04f8,00
//buf_dir_ctrl_gpio_62=0
SPIWrite 04f8,00
//preferred_input_sel_gpio_62=0
SPIWrite 04f9,00
//crossbar_sel_input_gpio_62=0
SPIWrite 04f8,00
//preferred_output_sel_gpio_62=0
SPIWrite 04fa,00
//crossbar_sel_output_gpio_62=0
SPIWrite 04fb,00
//activ_bir_dir_ctrl_gpio_62=0
SPIWrite 04fc,02
//buf_dir_ctrl_gpio_63=2
SPIWrite 04fc,02
//preferred_input_sel_gpio_63=0
SPIWrite 04fc,22
//preferred_output_sel_gpio_63=1
SPIWrite 04fd,00
```

```
//crossbar_sel_input_gpio_63=0
SPIWrite 04fe,00
//crossbar_sel_output_gpio_63=0
SPIWrite 04ff,00
//activ_bir_dir_ctrl_gpio_63=0
SPIWrite 0500,02
//buf_dir_ctrl_gpio_64=2
SPIWrite 0500,02
//preferred_input_sel_gpio_64=0
SPIWrite 0500,22
//preferred_output_sel_gpio_64=1
SPIWrite 0501,00
//crossbar_sel_input_gpio_64=0
SPIWrite 0502,00
//crossbar_sel_output_gpio_64=0
SPIWrite 0503,00
//activ_bir_dir_ctrl_gpio_64=0
SPIWrite 0504,02
//buf_dir_ctrl_gpio_65=2
SPIWrite 0504,02
//preferred_input_sel_gpio_65=0
SPIWrite 0504,22
//preferred_output_sel_gpio_65=1
SPIWrite 0505,00
//crossbar_sel_input_gpio_65=0
SPIWrite 0506,00
//crossbar_sel_output_gpio_65=0
SPIWrite 0507,00
//activ_bir_dir_ctrl_gpio_65=0
SPIWrite 0508,02
//buf_dir_ctrl_gpio_66=2
SPIWrite 0508,02
//preferred_input_sel_gpio_66=0
SPIWrite 0508,42
//preferred_output_sel_gpio_66=2
SPIWrite 0509,00
//crossbar_sel_input_gpio_66=0
SPIWrite 050a,00
//crossbar_sel_output_gpio_66=0
SPIWrite 050b,00
//activ_bir_dir_ctrl_gpio_66=0
SPIWrite 050c,00
//buf_dir_ctrl_gpio_67=0
SPIWrite 050c,00
//preferred_input_sel_gpio_67=0
SPIWrite 050d,00
//crossbar_sel_input_gpio_67=0
SPIWrite 050c,00
```

```
//preferred_output_sel_gpio_67=0
SPIWrite 050e,00
//crossbar_sel_output_gpio_67=0
SPIWrite 050f,00
//activ_bir_dir_ctrl_gpio_67=0
SPIWrite 0510,02
//buf_dir_ctrl_gpio_68=2
SPIWrite 0510,02
//preferred_input_sel_gpio_68=0
SPIWrite 0510,22
//preferred_output_sel_gpio_68=1
SPIWrite 0511,00
//crossbar_sel_input_gpio_68=0
SPIWrite 0512,00
//crossbar_sel_output_gpio_68=0
SPIWrite 0513,00
//activ_bir_dir_ctrl_gpio_68=0
SPIWrite 0514,00
//buf_dir_ctrl_gpio_69=0
SPIWrite 0514,00
//preferred_input_sel_gpio_69=0
SPIWrite 0515,00
//crossbar_sel_input_gpio_69=0
SPIWrite 0514,00
//preferred_output_sel_gpio_69=0
SPIWrite 0516,00
//crossbar_sel_output_gpio_69=0
SPIWrite 0517,00
//activ_bir_dir_ctrl_gpio_69=0
SPIWrite 0518,02
//buf_dir_ctrl_gpio_70=2
SPIWrite 0518,02
//preferred_input_sel_gpio_70=0
SPIWrite 0518,42
//preferred_output_sel_gpio_70=2
SPIWrite 0519,00
//crossbar_sel_input_gpio_70=0
SPIWrite 051a,00
//crossbar_sel_output_gpio_70=0
SPIWrite 051b,00
//activ_bir_dir_ctrl_gpio_70=0
SPIWrite 051c,02
//buf_dir_ctrl_gpio_71=2
SPIWrite 051c,02
//preferred_input_sel_gpio_71=0
SPIWrite 051c,42
//preferred_output_sel_gpio_71=2
SPIWrite 051d,00
```

```
//crossbar_sel_input_gpio_71=0
SPIWrite 051e,00
//crossbar_sel_output_gpio_71=0
SPIWrite 051f,00
//activ_bir_dir_ctrl_gpio_71=0
SPIWrite 0520,02
//buf_dir_ctrl_gpio_72=2
SPIWrite 0520,02
//preferred_input_sel_gpio_72=0
SPIWrite 0520,22
//preferred_output_sel_gpio_72=1
SPIWrite 0521,00
//crossbar_sel_input_gpio_72=0
SPIWrite 0522,00
//crossbar_sel_output_gpio_72=0
SPIWrite 0523,00
//activ_bir_dir_ctrl_gpio_72=0
SPIWrite 0524,02
//buf_dir_ctrl_gpio_73=2
SPIWrite 0524,02
//preferred_input_sel_gpio_73=0
SPIWrite 0524,42
//preferred_output_sel_gpio_73=2
SPIWrite 0525,00
//crossbar_sel_input_gpio_73=0
SPIWrite 0526,00
//crossbar_sel_output_gpio_73=0
SPIWrite 0527,00
//activ_bir_dir_ctrl_gpio_73=0
SPIWrite 0528,02
//buf_dir_ctrl_gpio_74=2
SPIWrite 0528,02
//preferred_input_sel_gpio_74=0
SPIWrite 0528,22
//preferred_output_sel_gpio_74=1
SPIWrite 0529,00
//crossbar_sel_input_gpio_74=0
SPIWrite 052a,00
//crossbar_sel_output_gpio_74=0
SPIWrite 052b,00
//activ_bir_dir_ctrl_gpio_74=0
SPIWrite 052c,00
//buf_dir_ctrl_gpio_75=0
SPIWrite 052c,00
//preferred_input_sel_gpio_75=0
SPIWrite 052d,00
//crossbar_sel_input_gpio_75=0
SPIWrite 052c,00
```

```
//preferred_output_sel_gpio_75=0
SPIWrite 052e,00
//crossbar_sel_output_gpio_75=0
SPIWrite 052f,00
//activ_bir_dir_ctrl_gpio_75=0
SPIWrite 0530,01
//buf_dir_ctrl_gpio_76=1
SPIWrite 0530,05
//preferred_input_sel_gpio_76=1
SPIWrite 0530,05
//preferred_output_sel_gpio_76=0
SPIWrite 0531,00
//crossbar_sel_input_gpio_76=0
SPIWrite 0532,00
//crossbar_sel_output_gpio_76=0
SPIWrite 0533,00
//activ_bir_dir_ctrl_gpio_76=0
SPIWrite 0534,01
//buf_dir_ctrl_gpio_77=1
SPIWrite 0534,05
//preferred_input_sel_gpio_77=1
SPIWrite 0534,05
//preferred_output_sel_gpio_77=0
SPIWrite 0535,00
//crossbar_sel_input_gpio_77=0
SPIWrite 0536,00
//crossbar_sel_output_gpio_77=0
SPIWrite 0537,00
//activ_bir_dir_ctrl_gpio_77=0
SPIWrite 0538,01
//buf_dir_ctrl_gpio_78=1
SPIWrite 0538,05
//preferred_input_sel_gpio_78=1
SPIWrite 0538,05
//preferred_output_sel_gpio_78=0
SPIWrite 0539,00
//crossbar_sel_input_gpio_78=0
SPIWrite 053a,00
//crossbar_sel_output_gpio_78=0
SPIWrite 053b,00
//activ_bir_dir_ctrl_gpio_78=0
SPIWrite 053c,02
//buf_dir_ctrl_gpio_79=2
SPIWrite 053c,02
//preferred_input_sel_gpio_79=0
SPIWrite 053c,42
//preferred_output_sel_gpio_79=2
SPIWrite 053d,00
```

```
//crossbar_sel_input_gpio_79=0
SPIWrite 053e,00
//crossbar_sel_output_gpio_79=0
SPIWrite 053f,00
//activ_bir_dir_ctrl_gpio_79=0
SPIWrite 0577,aa
//ovr_sel_intpi_rxdsa_gain_sw=0
SPIWrite 057e,2a
//ovr_sel_intpi_tx_fb_loop_3=0
SPIWrite 05b2,23
//ovr_sel_intpi_spib2_clk=0
SPIWrite 0550,8a
//ovr_sel_intpi_tdd_2t_en_ab=0
SPIWrite 057e,22
//ovr_sel_intpi_tx_fb_loop_1=0
SPIWrite 057e,02
//ovr_sel_intpi_tx_fb_loop_2=0
SPIWrite 05b2,03
//ovr_sel_intbipi_spib2_sdi=0
SPIWrite 05b2,01
//ovr_sel_intpi_spib2_cs_n=0
SPIWrite 0551,00
//ovr_sel_intpi_tdd_1f_en_ab=0
SPIWrite 05b0,0b
//ovr_sel_intbipi_spib1_sdi=0
SPIWrite 05b0,09
//ovr_sel_intpi_spib1_cs_n=0
SPIWrite 05b0,01
//ovr_sel_intpi_spib1_clk=0
SPIWrite 057e,00
//ovr_sel_intpi_tx_fb_loop_0=0
SPIWrite 0552,22
//ovr_sel_intpi_fb_nco_sw=0
SPIWrite 056d,02
//ovr_sel_intpi_global_pdn=0
SPIWrite 0550,82
//ovr_sel_intpi_tdd_2r_en_cd=0
SPIWrite 057c,2a
//ovr_sel_intpi_tx2dsa_gain_sw_rxtxlo=0
SPIWrite 057c,0a
//ovr_sel_intpi_tx1dsa_gain_sw_rxtxlo=0
SPIWrite 0554,fd
//ovr_sel_intpi_adc_sync_n_ab_0=0
SPIWrite 0550,80
//ovr_sel_intpi_tdd_2r_en_ab=0
SPIWrite 0554,f5
//ovr_sel_intpi_adc_sync_n_ab_1=0
SPIWrite 0554,75
```

```
//ovr_sel_intpi_adc_sync_n_cd_1=0
SPIWrite 0554,55
//ovr_sel_intpi_adc_sync_n_cd_0=0
SPIWrite 0552,20
//ovr_sel_intpi_tdd_1f_en_cd=0
SPIWrite 0550,00
//ovr_sel_intpi_tdd_2t_en_cd=0
SPIWrite 0015,00

// Done configuring GPIO for internal AGC Mode



//**********Step: Setting up TDD pin invalid mode definition**********//


// If 105 is 0, when both RX and FB En is 1, RX is selected
// If 105 is 1, when both RX and FB En is 1, FB is selected
SPIWrite 0014,04
SPIWrite 0105,01
SPIWrite 0014,00

//**********Step: Changing Input buffer strength for GPIO0,GPIO20 **********//
SPIWrite 0015,80
SPIWrite 0201,01
SPIWrite 0251,01
SPIWrite 02A1,01
SPIWrite 02F1,01
SPIWrite 0015,00



// Clearing JESD TX Init States
// Done clearing Sysref Flags
// Sending Sysref to device from Pin/SPI
// Reading the JESD RX states to check if link is established
// Clearing JESD RX Data and alarms
// Clearing JESD RX Data and alarms


//**********Step: Doing SPI sysref**********//

AFE77xx_GLOBAL
SPIWrite 0014,04
//PAGE:TIMING_CON=1(Meaning: );
SPIWrite 04d1,00
//count_len_sysref=bf
SPIWrite 04d0,bf
```

```
SPIWrite 0717,00
//spare_reg_port=101
SPIWrite 0716,00
SPIWrite 0715,01
SPIWrite 0714,01
SPIWrite 0717,00
//spare_reg_port=0
SPIWrite 0716,00
SPIWrite 0715,00
SPIWrite 0714,00
SPIWrite 0014,00
//PAGE:TIMING_CON=0(Meaning: );
SPIWrite 0014,10
//PAGE:pll=2
SPIWrite 0051,04
//EN_SYNC_TO_PLLDIG_DIV=0
SPIWrite 0051,84
//SYS_REF_FROM_PIN_BYPAS=1
SPIWrite 0014,e8
//PAGE:pll=1d
SPIWrite 0051,06
//EN_SYNC_TO_PLLDIG_DIV=0
SPIWrite 0051,86
//SYS_REF_FROM_PIN_BYPAS=1
SPIWrite 0014,f8
//PAGE:pll=1f
SPIWrite 004e,34
//lcmgen_usespisysref=1
SPIWrite 004e,34
//lcmgen_div=bf
SPIWrite 004d,02
SPIWrite 004c,fd
SPIWrite 004c,fc
//lcmgen_sync_ena=0
SPIWrite 004c,fd
//lcmgen_sync_ena=1

SPIWrite 004e,34
//lcmgen_spisysref=0
SPIWrite 004e,3c
//lcmgen_spisysref=1
SPIWrite 004e,34
//lcmgen_spisysref=0
SPIWrite 004e,30
SPIWrite 0014,00
//PAGE:pll=0
SPIWrite 0014,10
//PAGE:pll=2
```

```
SPIWrite 0051,04
SPIWrite 0014,e8
//PAGE:pll=1d
SPIWrite 0051,06
SPIWrite 0014,00
//PAGE:pll=0


//**********Step:**********//

SPIWrite 0018,10
SPIWrite 0348,44
SPIWrite 0018,00


//**********Step: SPI access to CM4**********//
// Requesting/releasing SPI Access to PLL Pages
SPIWrite 0015,80
//PAGE:DIGTOP_MISC=1(Meaning: );
SPIWrite 01d4,00
//pll_reg_spi_req_a=0

WAIT 5

SPIRead 01d5
// Read // pll_reg_spi_a_ack: 0x1(Meaning: access acknowledge)


// Done requesting/releasing SPI Access to PLL Pages

AFE77xx_GLOBAL
SPIWrite 0015,00

//**********Step: Get FW version: Check any updates**********//
//PAGE:DIGTOP_MISC=0(Meaning: );
SPIWrite 0013,10
//PAGE:customer_macro=1(Meaning: );
SPIWrite 00a3,00
SPIWrite 00a2,00
SPIWrite 00a1,00
SPIWrite 00a0,02
SPIWrite 0193,01
SPIWrite 0192,00
SPIWrite 0191,00
SPIWrite 0190,00
SPIWrite 0013,00
//PAGE:customer_macro=0(Meaning: );
SPIWrite 0013,20
```

```
//PAGE:cm4_macro=1
WAIT 5
SPIRead 0020
SPIRead 0254

// Read // MACRO_STATUS_RESULT_0: 0x10109a
SPIWrite 0013,00


//PAGE:cm4_macro=0
//**********Step: Updated QMC static writes**********//
//PG1P1: Updated Rx QMC writes
SPIWrite 0018,10
//PAGE:rx_iqmc=1
SPIWrite 0018,10
SPIWrite 0381,00
SPIWrite 0305,00
SPIWrite 0305,02
SPIWrite 0341,00
SPIWrite 0340,04
SPIWrite 0343,40
SPIWrite 0334,07
SPIWrite 0334,87
SPIWrite 037E,7F
SPIWrite 037E,FF
SPIWrite 0335,1C
SPIWrite 0335,9C
SPIWrite 0320,14
SPIWrite 0320,94
SPIWrite 0321,14
SPIWrite 0321,94
SPIWrite 0324,04
SPIWrite 0324,0C
SPIWrite 0324,4C
SPIWrite 0324,CC
SPIWrite 0342,00
SPIWrite 0341,C0
SPIWrite 0343,C0
SPIWrite 0327,02
SPIWrite 0327,82
SPIWrite 0322,02
SPIWrite 0322,82
SPIWrite 0318,08
SPIWrite 0318,88
SPIWrite 0348,04
SPIWrite 0348,44
SPIWrite 031C,00
SPIWrite 031C,80
```

```
SPIWrite 030F,03
SPIWrite 030F,83
SPIWrite 0350,00
SPIWrite 034F,00
SPIWrite 0359,3C
SPIWrite 035A,01
SPIWrite 035B,02
SPIWrite 0359,BC
SPIWrite 035A,81
SPIWrite 035B,82
SPIWrite 0018,00


//**********Step: Enable Clock to RX QMC**********//
//PAGE:rx_iqmc=0
SPIWrite 0015,80
//PAGE:DIGTOP_MISC=1(Meaning: );
SPIWrite 0365,01
//rxiqmc_cm4_divider_outclk_en=1(Meaning: clock is gated);
SPIWrite 0366,01
//rxiqmc_cm4_divider_reset=1(Meaning: divider is under reset);
SPIWrite 0364,04
//rxiqmc_cm4_dither_mode_en=1(Meaning: enable);
SPIWrite 0364,06
//rxiqmc_cm4_clk_div_sel=2(Meaning: reserved);
SPIWrite 0366,00
//rxiqmc_cm4_divider_reset=0(Meaning: divider is running);
SPIWrite 0365,00
//rxiqmc_cm4_divider_outclk_en=0(Meaning: clock is running);
SPIWrite 0015,00
//PAGE:DIGTOP_MISC=0(Meaning: );



//**********Step: Macro to reset RX IQMC**********//

SPIWrite 0013,10
//PAGE:customer_macro=1(Meaning: );
SPIWrite 00a3,00
SPIWrite 00a2,00
SPIWrite 00a1,00
SPIWrite 00a0,00
SPIWrite 00a7,00
SPIWrite 00a6,00
SPIWrite 00a5,00
SPIWrite 00a4,4a
SPIWrite 0193,31
SPIWrite 0192,00
```

```
SPIWrite 0191,00
SPIWrite 0190,00

SPIWrite 0013,00
//PAGE:customer_macro=0(Meaning: );
SPIWrite 0013,20
//PAGE:cm4_macro=1
WAIT 10
WAIT 10
SPIRead 0020
SPIRead 0254
// Read // MACRO_ERROR: 0x0

SPIWrite 0013,00
//PAGE:cm4_macro=0


//Done RX IQMC Correction


//**********Step: **********//
SPIWrite 0014,04
SPIWrite 0528,00
SPIWrite 0523,00
SPIWrite 0014,00

//Doing LO correction

// Requesting/releasing SPI Access to PLL Pages

AFE77xx_GLOBAL
SPIWrite 0018,00
//PAGE:rx_iqmc_dram=0x0
SPIWrite 0015,80
//PAGE:DIGTOP_MISC=0x1(Meaning: );
SPIWrite 01d4,01
//pll_reg_spi_req_a=0x1
SPIRead 01d5

// Read // pll_reg_spi_a_ack: 0x1(Meaning: access acknowledge)

SPIWrite 0015,00

// Done requesting/releasing SPI Access to PLL Pages

//**********Step: Enable RX LO correction **********//

SPIWrite 0010,0c
```

```
//PAGE:rx_top=3
SPIWrite 0401,01
//dc_freeze_reg=1(Meaning: );
SPIWrite 0420,00
//alpha_update_signal=0
SPIWrite 0420,01
//alpha_update_signal=1
SPIWrite 0420,00
//alpha_update_signal=0
SPIWrite 0401,00
//dc_freeze_reg=0(Meaning: );
SPIWrite 0400,00
//bypass=0(Meaning: );
SPIWrite 0411,01
//dc_freeze_reg=1(Meaning: );
SPIWrite 0421,00
//alpha_update_signal=0
SPIWrite 0421,01
//alpha_update_signal=1
SPIWrite 0421,00
//alpha_update_signal=0
SPIWrite 0411,00
//dc_freeze_reg=0(Meaning: );
SPIWrite 0410,00
//bypass=0(Meaning: );
SPIWrite 0801,01
//dc_freeze_reg=1(Meaning: );
SPIWrite 0820,00
//alpha_update_signal=0
SPIWrite 0820,01
//alpha_update_signal=1
SPIWrite 0820,00
//alpha_update_signal=0
SPIWrite 0801,00
//dc_freeze_reg=0(Meaning: );
SPIWrite 0800,00
//bypass=0(Meaning: );
SPIWrite 0811,01
//dc_freeze_reg=1(Meaning: );
SPIWrite 0821,00
//alpha_update_signal=0
SPIWrite 0821,01
//alpha_update_signal=1
SPIWrite 0821,00
//alpha_update_signal=0
SPIWrite 0811,00
//dc_freeze_reg=0(Meaning: );
SPIWrite 0810,00
```

```
//bypass=0(Meaning: );
SPIWrite 0010,00


//Done LO correction

/Doing AAGC Correction
//**********Step: Static writes for AAGC configuration**********//

SPIWrite 0016,30
//PAGE:dsa=3 DSA SPI
SPIWrite 0040,02
SPIWrite 0016,00
//PAGE:dsa=0
SPIWrite 0010,0c
//PAGE:rx_top=3
SPIWrite 04cd,00
//blank_time_rf_det=64
SPIWrite 04cc,64
SPIWrite 04cf,01
//blank_time=1f4
SPIWrite 04ce,f4
SPIWrite 0275,03
//blank_time_for_ext_comp_change=3e8
SPIWrite 0274,e8
SPIWrite 0cd1,02
//disable_hysterisis=1(Meaning: );
SPIWrite 0cd1,02
//dig_gain_dis=0
SPIWrite 0a80,5b
//gain_comp_stg_2_3_dec_chain=5b
SPIWrite 0cd0,00
SPIWrite 020c,01
SPIWrite 0224,06
SPIWrite 0245,20
SPIWrite 0244,3a
SPIWrite 0200,5a
SPIWrite 0204,1a
SPIWrite 08cd,00
//blank_time_rf_det=64
SPIWrite 08cc,64
SPIWrite 08cf,01
//blank_time=1f4
SPIWrite 08ce,f4
SPIWrite 0675,03
//blank_time_for_ext_comp_change=3e8
SPIWrite 0674,e8
SPIWrite 0ed1,02
```

```
//disable_hysterisis=1(Meaning: );
SPIWrite 0ed1,02
//dig_gain_dis=0
SPIWrite 0a81,5b
//gain_comp_stg_2_3_dec_chain=5b
SPIWrite 0ed0,00
SPIWrite 060c,01
SPIWrite 0624,06
SPIWrite 0645,20
SPIWrite 0644,3a
SPIWrite 0600,5a
SPIWrite 0604,1a


// Configuring DGC

//**********Step: Static writes for DGC configuration(12 bit Dynamic ALC)**********//
SPIWrite 0334,07
//DgcEnRxMode=0(Meaning: );
SPIWrite 0336,02
//DynCoarseIdx12BitModeSel=1
SPIWrite 0337,00
//FltPtMode=0
SPIWrite 0337,00
//FltPtFmt=0(Meaning: );
SPIWrite 0335,1e
//DgcMode=6(Meaning: );
SPIWrite 0341,00
//bypass_fine_gain_delay=0x0
SPIWrite 033c,23
//NBitsCoarseIdx=3(Meaning: );
SPIWrite 033c,33
//CoarseStep=6(Meaning: );
SPIWrite 04f9,00
//AttnCodeDelay=0x55
SPIWrite 04f8,55
SPIWrite 04f1,01
//UseMinAttnFromAgc=1(Meaning: );
SPIWrite 033d,00
//CoarseIndexSwapIandQ=0(Meaning: );
SPIWrite 033d,00
//CoarseIndexInvert=0(Meaning: );


// Done configuring DGC
```

// Configuring DGC

SPIWrite 0734,07
//DgcEnRxMode=0(Meaning:);
SPIWrite 0736,02
//DynCoarseIdx12BitModeSel=1
SPIWrite 0737,00
//FltPtMode=0
SPIWrite 0737,00
//FltPtFmt=0(Meaning:);
SPIWrite 0735,1e
//DgcMode=6(Meaning:);
SPIWrite 0741,00
//bypass_fine_gain_delay=0x0
SPIWrite 073c,23
//NBitsCoarseIdx=3(Meaning:);
SPIWrite 073c,33
//CoarseStep=6(Meaning:);
SPIWrite 08f9,00
//AttnCodeDelay=0x55
SPIWrite 08f8,55
SPIWrite 08f1,01
//UseMinAttnFromAgc=1(Meaning:);
SPIWrite 073d,00
//CoarseIndexSwapIandQ=0(Meaning:);
SPIWrite 073d,00
//CoarseIndexInvert=0(Meaning:);

// Done configuring DGC

// Configuring Small Step Attack Detector

SPIWrite 0209,01
//small_step_attack_step_size=1
SPIWrite 0239,06
//small_step_attack_sig_th_high=65a
SPIWrite 0238,5a
SPIWrite 023b,06
//small_step_attack_sig_th_low=65a
SPIWrite 023a,5a
SPIWrite 021a,00

```
//small_step_attack_win_len=40
SPIWrite 0219,00
SPIWrite 0218,40
SPIWrite 024e,00
//small_step_attack_num_hits=8
SPIWrite 024d,00
SPIWrite 024c,08
SPIWrite 0200,5a
//small_step_attack_en=1(Meaning: );
SPIWrite 0204,1a
//small_step_attack_det_en=1(Meaning: );


// Done configuring Small Step Attack Detector



// Configuring Small Step Attack Detector


SPIWrite 0609,01
//small_step_attack_step_size=1
SPIWrite 0639,06
//small_step_attack_sig_th_high=65a
SPIWrite 0638,5a
SPIWrite 063b,06
//small_step_attack_sig_th_low=65a
SPIWrite 063a,5a
SPIWrite 061a,00
//small_step_attack_win_len=40
SPIWrite 0619,00
SPIWrite 0618,40
SPIWrite 064e,00
//small_step_attack_num_hits=8
SPIWrite 064d,00
SPIWrite 064c,08
SPIWrite 0600,5a
//small_step_attack_en=1(Meaning: );
SPIWrite 0604,1a
//small_step_attack_det_en=1(Meaning: );


// Done configuring Small Step Attack Detector
```

// Configuring Small Step Decay Detector

SPIWrite 020b,01
//small_step_decay_step_size=1
SPIWrite 0241,03
//small_step_decay_sig_th_high=32f
SPIWrite 0240,2f
SPIWrite 0243,03
//small_step_decay_sig_th_low=32f
SPIWrite 0242,2f
SPIWrite 0222,02
//small_step_decay_win_len=20000
SPIWrite 0221,00
SPIWrite 0220,00
SPIWrite 0256,00
//small_step_decay_num_hits=8
SPIWrite 0255,00
SPIWrite 0254,08
SPIWrite 0200,5a
//small_step_decay_en=1(Meaning:);
SPIWrite 0204,1a
//small_step_decay_det_en=1(Meaning:);

// Done configuring Small Step Decay Detector

// Configuring Small Step Decay Detector

SPIWrite 060b,01
//small_step_decay_step_size=1
SPIWrite 0641,03
//small_step_decay_sig_th_high=32f
SPIWrite 0640,2f
SPIWrite 0643,03
//small_step_decay_sig_th_low=32f
SPIWrite 0642,2f
SPIWrite 0622,02
//small_step_decay_win_len=20000
SPIWrite 0621,00
SPIWrite 0620,00
SPIWrite 0656,00
//small_step_decay_num_hits=8
SPIWrite 0655,00
SPIWrite 0654,08
SPIWrite 0600,5a

```
//small_step_decay_en=1(Meaning: );
SPIWrite 0604,1a
//small_step_decay_det_en=1(Meaning: );
// Done configuring Small Step Decay Detector


//**********Step: Ext LNA control**********//

// Configuring External LNA Control
SPIWrite 0202,02
//ext_lna_cntl_en=1(Meaning: );
//gain0=200
SPIWrite 0291,02
SPIWrite 0290,00
SPIWrite 0276,02
//ext_lna_gain_margin=2

SPIWrite 0602,02
//ext_lna_cntl_en=1(Meaning: );
//gain0=200
SPIWrite 0691,02
SPIWrite 0690,00
SPIWrite 0676,02
//ext_lna_gain_margin=2

SPIWrite 0010,00
//PAGE:rx_top=0
// Done configuring External LNA Control

//Done AAGC Correction

//**********Step: Setting TX DSA attenuation**********//

// Setting TX DSA Attenuation

SPIWrite 0016,30
//PAGE:dsa=3
SPIWrite 0100,01
SPIWrite 0102,00
SPIWrite 0102,01
SPIWrite 0102,00

// Done setting TX DSA Attenuation


// Setting TX DSA Attenuation

SPIWrite 0120,01
```

SPIWrite 0122,00
SPIWrite 0122,01
SPIWrite 0122,00

// Done setting TX DSA Attenuation

// Setting TX DSA Attenuation

SPIWrite 0100,00
SPIWrite 0102,00
SPIWrite 0102,01
SPIWrite 0102,00

// Done setting TX DSA Attenuation

// Setting TX DSA Attenuation

SPIWrite 0120,00
SPIWrite 0122,00
SPIWrite 0122,01
SPIWrite 0122,00
SPIWrite 0016,00

// Done setting TX DSA Attenuation

//Set TX Digital Gain to Zero
SPIWrite 0016,30
SPIWrite 0101,18
SPIWrite 0121,18
SPIWrite 0016,00

SPIWrite 0013,10
SPIWrite 00A3,00
SPIWrite 00A2,00
SPIWrite 00A1,00
SPIWrite 00A0,01
SPIWrite 0193,44
SPIWrite 0192,00
SPIWrite 0191,00
SPIWrite 0190,00
SPIWrite 0013,00

SPIWrite 0013,20

WAIT 5
SPIRead 0020
// Read // MACRO_STATUS_RESULT_0: 7
SPIWrite 0013,00

SPIWrite 0015,22
SPIWrite 008c,00
SPIWrite 0015,00

SPIWrite 0014,08
SPIWrite 004b,33
SPIWrite 004a,00
SPIWrite 0014,00

SPIWrite 0010,03
SPIWrite 0614,60
SPIWrite 0614,61
SPIWrite 0613,03
SPIWrite 0612,FF
SPIWrite 0611,FF
SPIWrite 0610,FF
SPIWrite 0615,01
SPIWrite 0615,00
SPIWrite 0010,00

//Lane Reset
SPIWrite 0015,44
SPIWrite 4001,90
SPIWrite 4000,6b
SPIWrite 4001,10
SPIWrite 4000,6b

SPIWrite 4201,90
SPIWrite 4200,6b
SPIWrite 4201,10
SPIWrite 4200,6b

SPIWrite 4401,90
SPIWrite 4400,6b
SPIWrite 4401,10
SPIWrite 4400,6b

```
SPIWrite 4601,90
SPIWrite 4600,6b
SPIWrite 4601,10
SPIWrite 4600,6b

SPIWrite 0015,00


SPIWrite 0014,f8
SPIWrite 0066,08
SPIWrite 0066,00
SPIWrite 0014,00



//Match latency between slicer and data
SPIWrite 0010,0c
//Needed for all DGC mode..
SPIWrite 04f8,01
SPIWrite 04f9,00
SPIWrite 08f8,01
SPIWrite 08f9,00
//Bypass the delay in coarse gain(slicer)
//Default is 1
SPIWrite 0341,00
//Default is 1
SPIWrite 0741,00
SPIWrite 0010,00

//Match latency in between data path and gain application
SPIWrite 0010,0c
SPIWrite 04f8,3b
SPIWrite 04f9,00
SPIWrite 08f8,3b
SPIWrite 08f9,00
SPIWrite 0010,00


SPIWrite 0019,1c

/*****************************TX RX SWAP*************************/

//5619_TIROC_ECPRI_2P6
BOARDTYPE 0x45260013

//5319_TIROC_ECPRI_2P6
BOARDTYPE 0x4526010E
```

```
//TX_VGA_Swap Choose TXD
SPIWrite 0016,30
SPIWrite 0155,08
SPIWrite 0016,00
//Set TXAB DSA_SwapValue
SPIWrite 0016,10
SPIWrite 0104,0a
SPIWrite 0124,0a
SPIWrite 0016,00
//Set TXCD DSA_SwapValue
SPIWrite 0016,20
SPIWrite 0104,0a
SPIWrite 0124,0a
SPIWrite 0016,00
// Done

//RX_VGA_Swap Choose TXD
SPIWrite 0014,04
SPIWrite 0106,08
SPIWrite 0014,00
//Set RXAB DSA_SwapValue
SPIWrite 0016,10
SPIWrite 005c,0a
SPIWrite 00bc,0a
SPIWrite 0016,00
//Set RXCD DSA_SwapValue
SPIWrite 0016,20
SPIWrite 005c,0a
SPIWrite 00bc,0a
SPIWrite 0016,00

//The value of 0x0268 0x668 same as 0x005c 0x00bc
SPIWrite 0010,0C
SPIWrite 0268,0a
SPIWrite 0668,0a
SPIWrite 0010,00
// Done

//Doning INT&Alarm
//Set INT PIN Mask
SPIWrite 0015,80
//INT1 for JEDS and SerDes
SPIWrite 011b,00
SPIWrite 011a,00
SPIWrite 0119,00
SPIWrite 0118,01
//INT2 for PLL1 and PLL2
```

```
SPIWrite 011f,00
SPIWrite 011e,00
SPIWrite 011d,03
SPIWrite 011c,00
//Close Page
SPIWrite 0015,00

//Set Alarm Mask --Only Use JESD0
//JESD0
SPIWrite 0015,02
SPIWrite 0170,0a
SPIWrite 0171,c7
SPIWrite 0172,00
SPIWrite 0173,ff
SPIWrite 0174,27
SPIWrite 0175,27
SPIWrite 0176,ff
SPIWrite 0177,ff
SPIWrite 0178,0a
SPIWrite 0179,c7
SPIWrite 017a,00
SPIWrite 017b,ff
SPIWrite 017c,27
SPIWrite 017d,27
SPIWrite 017e,ff
SPIWrite 017f,ff
SPIWrite 0015,00

//JESD1
SPIWrite 0015,20
SPIWrite 0170,0a
SPIWrite 0171,fe
SPIWrite 0172,ff
SPIWrite 0173,ff
SPIWrite 0174,ff
SPIWrite 0175,ff
SPIWrite 0176,ff
SPIWrite 0177,ff
SPIWrite 0178,ff
SPIWrite 0179,ff
SPIWrite 017a,ff
SPIWrite 017b,ff
SPIWrite 017c,ff
SPIWrite 017d,ff
SPIWrite 017e,ff
SPIWrite 017f,ff
SPIWrite 0015,00
```

```
//JESD1 TX
SPIWrite 0015,10
SPIWrite 005e,0f
SPIWrite 0015,00

//JESD0 TX
SPIWrite 0015,01
SPIWrite 005e,0c
SPIWrite 0015,00

//Done INT&Alarm

//Set LnaBypassPolarity
SPIWrite 0015,80
SPIWrite 0192,00
SPIWrite 0015,00


//Low Latency Start
//Step: Enable FB IMD Trim
//SPIWrite 0016,C0
//SPIWrite 01a9,00
//SPIWrite 019c,01
//SPIWrite 0016,00
//Low Latency Stop


//High Latency Start
//******************Band Specific Start*****************//
//******************Packet Reload*****************//
//Band 2=2.6G
//**********Step: Packet Load(2.6GLO: (0,4,7,10,11,17,20)) using CM4 (All fixed and Flexi
Packets)**********//
SPIWrite 0013,10
SPIWrite 00A3,00
SPIWrite 00A2,00
SPIWrite 00A1,00
SPIWrite 00A0,00
SPIWrite 00A7,04
SPIWrite 00A6,00
SPIWrite 00A5,07
SPIWrite 00A4,00
SPIWrite 00AB,11
SPIWrite 00AA,0b
SPIWrite 00A9,0a
SPIWrite 00A8,07
SPIWrite 00AF,00
SPIWrite 00AE,00
```

```
SPIWrite 00AD,00
SPIWrite 00AC,14
SPIWrite 0193,12
SPIWrite 0192,00
SPIWrite 0191,00
SPIWrite 0190,00
SPIWrite 0013,00

SPIWrite 0013,20
//PAGE:cm4_macro=1
WAIT 5
SPIRead 0020
// Read // MACRO_STATUS_RESULT_0: 7
SPIWrite 0013,00


//******************Enable Digital Corrections*****************//
Step: Enable TX IQ Mismatch Trim
SPIWrite 0010,03
SPIWrite 0830,06
SPIWrite 0650,02
SPIWrite 0831,28
SPIWrite 0833,00
SPIWrite 0832,01
SPIWrite 0832,00

SPIWrite 0890,06
SPIWrite 06E4,02
SPIWrite 0891,28
SPIWrite 0893,00
SPIWrite 0892,01
SPIWrite 0892,00
SPIWrite 0010,00



//Step: Enable FB IMD Trim
SPIWrite 0016,C0
SPIWrite 01a9,01
SPIWrite 019c,00
SPIWrite 0016,00


//Step: Enable RX QMC fixed correction
SPIWrite 0010,0C

//Channel A and C
SPIWrite 0901,00
```

SPIWrite 0D72,00
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,01
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,02
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,03
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,04
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,05
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,06
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,07
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,08
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,09
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,0A
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,0B
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00

SPIWrite 0D72,0C
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,0D
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,0E
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,0F
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,10
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,11
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,12
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,13
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,14
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,15
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,16
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,17
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00

SPIWrite 0D72,18
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,19
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,1A
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,1B
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,1C
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,1D
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,1E
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,1F
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,20
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,21
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,22
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,23
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00

SPIWrite 0D72,24
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,25
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,26
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,27
SPIWrite 0D73,00
SPIWrite 0D73,01
SPIWrite 0D73,00
SPIWrite 0D72,00

//Channel B and D
SPIWrite 0501,00
SPIWrite 0B72,00
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,01
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,02
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,03
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,04
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,05
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,06
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00

SPIWrite 0B72,07
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,08
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,09
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,0A
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,0B
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,0C
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,0D
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,0E
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,0F
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,10
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,11
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,12
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00

SPIWrite 0B72,13
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,14
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,15
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,16
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,17
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,18
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,19
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,1A
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,1B
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,1C
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,1D
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,1E
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00

SPIWrite 0B72,1F
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,20
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,21
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,22
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,23
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,24
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,25
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,26
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,27
SPIWrite 0B73,00
SPIWrite 0B73,01
SPIWrite 0B73,00
SPIWrite 0B72,00

SPIWrite 0010,00

//RX IMD Enable
SPIWrite 0010,0C
SPIWrite 0E10,04
SPIWrite 0E11,01
SPIWrite 0E11,00
SPIWrite 0C10,04
SPIWrite 0C11,01
SPIWrite 0C11,00

```
SPIWrite 0010,00

//RX Droop Enable
SPIWrite 0010,0C
SPIWrite 0A57,00
SPIWrite 0A57,00
SPIWrite 0A57,00
SPIWrite 0A57,00
SPIWrite 0C6B,00
SPIWrite 0C6B,01
SPIWrite 0C6B,00
SPIWrite 0C73,00
SPIWrite 0C73,01
SPIWrite 0C73,00
SPIWrite 0E6B,00
SPIWrite 0E6B,01
SPIWrite 0E6B,00
SPIWrite 0E73,00
SPIWrite 0E73,01
SPIWrite 0E73,00
SPIWrite 0010,00

//High Latency Stop


//****** RX noise floor debug. Added in low latency******//
SPIWrite 0014,01
SPIWrite 006c,1e
SPIWrite 0014,00


SPIWrite 0015,44
SPIWrite 49e9,a2
SPIWrite 49e8,44
SPIWrite 49fb,a2
SPIWrite 49fa,48
SPIWrite 0015,00

////**********Step: Enable Tx DSA gain swap macro patch**********//
SPIWrite 0013,10
SPIWrite 00A3,00
SPIWrite 00A2,00
SPIWrite 00A1,00
SPIWrite 00A0,01
SPIWrite 00A7,00
SPIWrite 00A6,00
SPIWrite 00A5,00
SPIWrite 00A4,0F
```

```
SPIWrite 0193,42
SPIWrite 0192,00
SPIWrite 0191,00
SPIWrite 0190,00
SPIWrite 0013,00
SPIWrite 0013,20
WAIT 5
SPIRead 0020
SPIWrite 0013,00

//fbDsaCodesPopulate
SPIWrite 0016,30
SPIWrite 0DF2,00
SPIWrite 0DF1,00
SPIWrite 0DF0,00
SPIWrite 0DF6,00
SPIWrite 0DF5,84
SPIWrite 0DF4,88
SPIWrite 0DFA,01
SPIWrite 0DF9,10
SPIWrite 0DF8,A0
SPIWrite 0DFE,02
SPIWrite 0DFD,98
SPIWrite 0DFC,AB
SPIWrite 0E02,04
SPIWrite 0E01,20
SPIWrite 0E00,CB
SPIWrite 0E06,06
SPIWrite 0E05,24
SPIWrite 0E04,FC
SPIWrite 0E0A,08
SPIWrite 0E09,A9
SPIWrite 0E08,23
SPIWrite 0E0E,0B
SPIWrite 0E0D,31
SPIWrite 0E0C,36
SPIWrite 0E12,0F
SPIWrite 0E11,31
SPIWrite 0E10,6E
SPIWrite 0E16,15
SPIWrite 0E15,B5
SPIWrite 0E14,66
SPIWrite 0E1A,20
SPIWrite 0E19,BA
SPIWrite 0E18,E8
SPIWrite 0E1E,25
SPIWrite 0E1D,42
SPIWrite 0E1C,C2
```

SPIWrite 0E22,25
SPIWrite 0E21,4A
SPIWrite 0E20,DA
SPIWrite 0E26,25
SPIWrite 0E25,4B
SPIWrite 0E24,02
SPIWrite 0E2A,25
SPIWrite 0E29,53
SPIWrite 0E28,15
SPIWrite 0E2E,25
SPIWrite 0E2D,57
SPIWrite 0E2C,2B
SPIWrite 0E32,25
SPIWrite 0E31,5B
SPIWrite 0E30,40
SPIWrite 0E36,25
SPIWrite 0E35,5F
SPIWrite 0E34,53
SPIWrite 0E3A,25
SPIWrite 0E39,63
SPIWrite 0E38,64
SPIWrite 0E3E,25
SPIWrite 0E3D,67
SPIWrite 0E3C,74
SPIWrite 0E42,25
SPIWrite 0E41,6B
SPIWrite 0E40,81
SPIWrite 0E46,25
SPIWrite 0E45,6B
SPIWrite 0E44,81
SPIWrite 0E4A,25
SPIWrite 0E49,6B
SPIWrite 0E48,81
SPIWrite 0E4E,25
SPIWrite 0E4D,6B
SPIWrite 0E4C,81
SPIWrite 0E52,25
SPIWrite 0E51,6B
SPIWrite 0E50,81
SPIWrite 0E56,25
SPIWrite 0E55,6B
SPIWrite 0E54,81
SPIWrite 0E5A,25
SPIWrite 0E59,6B
SPIWrite 0E58,81
SPIWrite 0E5E,25
SPIWrite 0E5D,6B
SPIWrite 0E5C,81

SPIWrite 0E62,25
SPIWrite 0E61,6B
SPIWrite 0E60,81
SPIWrite 0E66,25
SPIWrite 0E65,6B
SPIWrite 0E64,81
SPIWrite 0E6A,25
SPIWrite 0E69,6B
SPIWrite 0E68,81
SPIWrite 0E6E,25
SPIWrite 0E6D,6B
SPIWrite 0E6C,81
SPIWrite 0DD1,01
SPIWrite 0016,00