DGC Verification FAQ:

1. In debug phase only, without enable AGC, but manually configure slicer value, to let customer ASIC to verify the slicer index transmit operation only in 12bit dynamic ALC mode, please provide the register write.

Ans: This can be done using below steps

   a. Use *alcStepSizeDgc(U32 ulChan, U32 stepSize)* from C library to program step size. *ulChan* is 0,1,2,3 for RX A, RxB, RxC, RxD respectively. *stepSize* is the step value from 0 to 6dB
   b. Use *OnlyEnableInternalAgc(U32 ulChan, U32 ulEnable)* from C library to disable AGC. *ulChan* is 0,1,2,3 for RX A, RxB, RxC, RxD respectively. *ulEnable* should be set to 0.
   c. Send ALC frame

```
# RXA/C
AFE77xx_RegWrite(0,0x0010,0xC);
AFE77xx_RegWrite(0,0x0460,0);
AFE77xx_RegWrite(0,0x0460,1);
AFE77xx_RegWrite(0,0x0010,0x0);
# RXB/D
AFE77xx_RegWrite(0,0x0010,0xC);
AFE77xx_RegWrite(0,0x0860,0);
AFE77xx_RegWrite(0,0x0860,1);
AFE77xx_RegWrite(0,0x0010,0x0);
```

2. Register read LNA bypass status

Ans: Use *getAgcLnaStatus(U32 ulChan)* from C library. *ulChan* is 0,1,2,3 for RxA, RxB, RxC, RxD. Returns 1 if Lna is Bypass else 0

3. Register read DSA index

Ans: Use *getCurrentAgcAttenuation(U32 ulChan)* from C library. *ulChan* is 0,1,2,3 for RxA, RxB, RxC, RxD