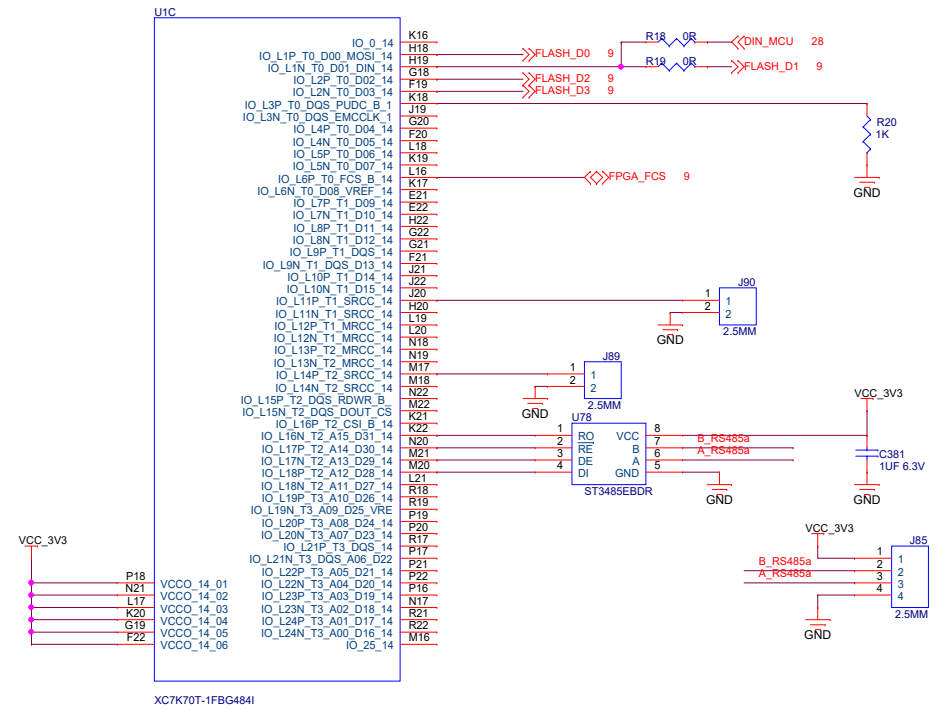
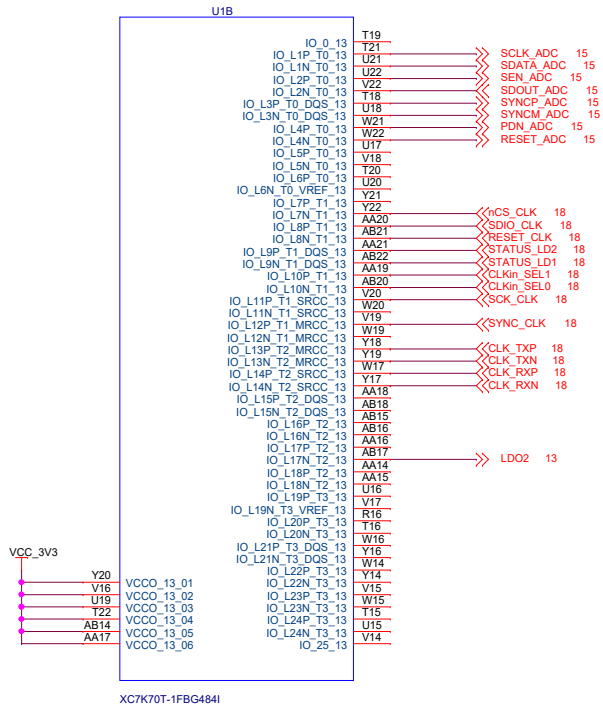
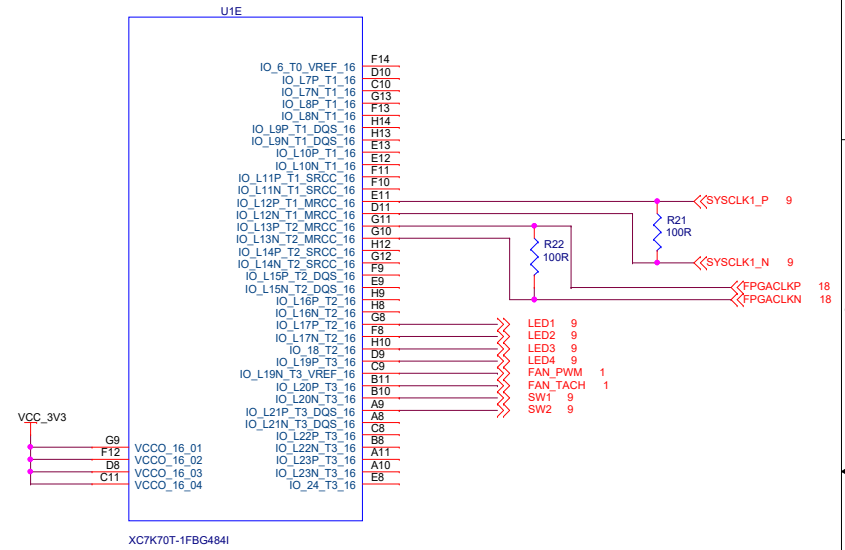
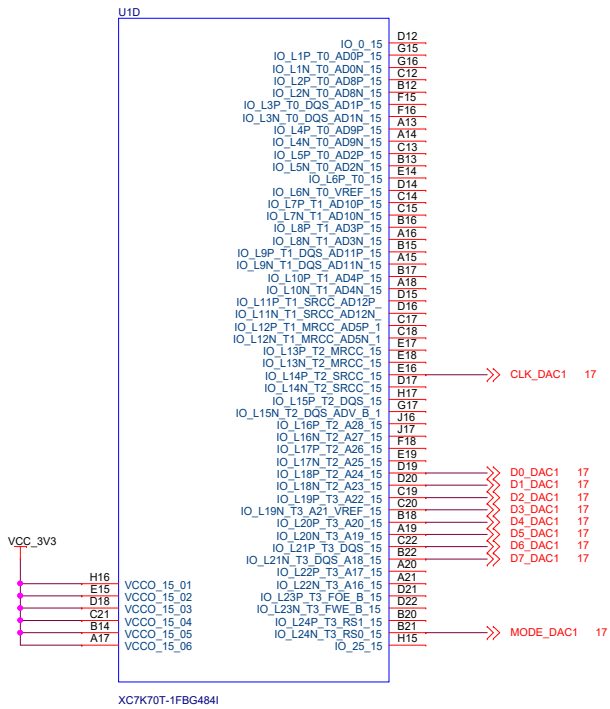


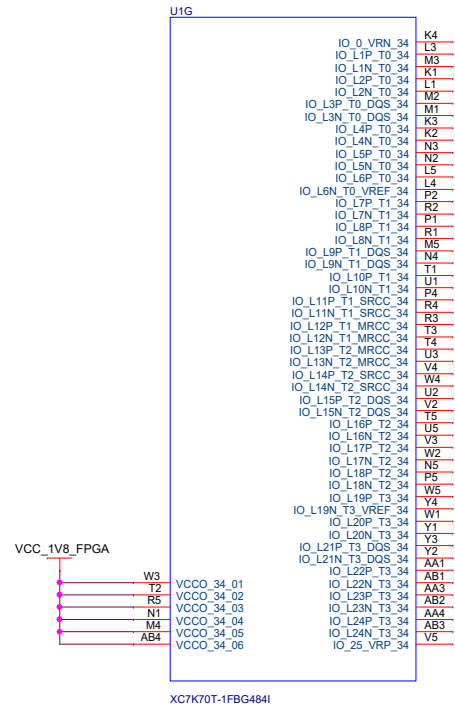
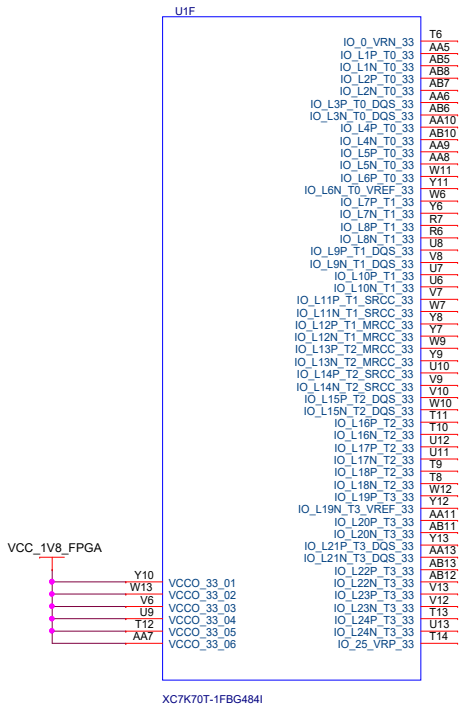
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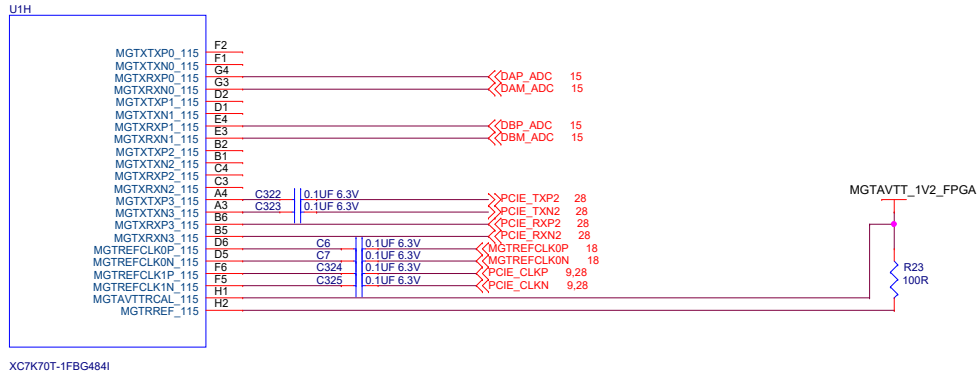
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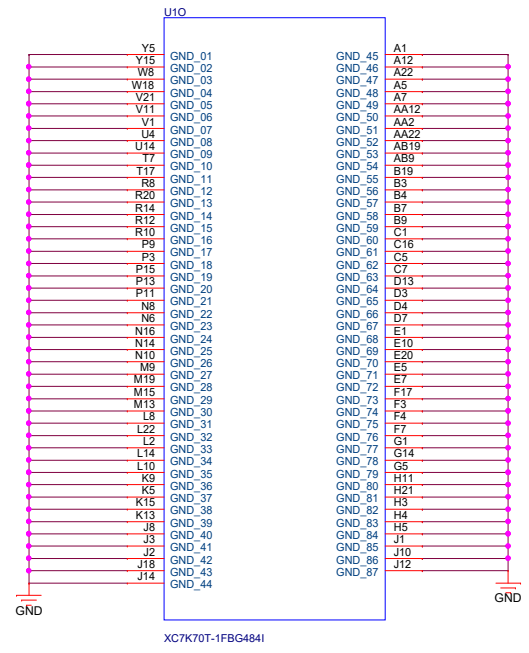
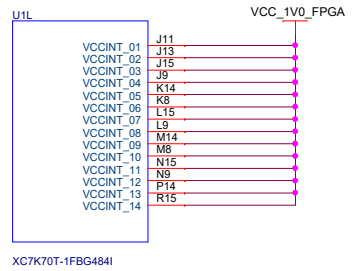
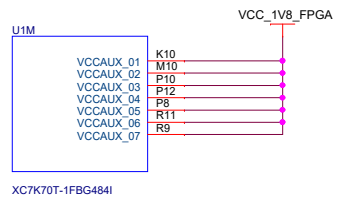
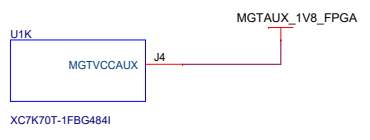
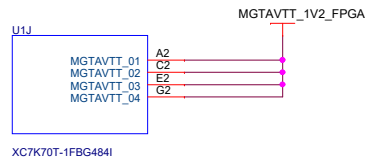
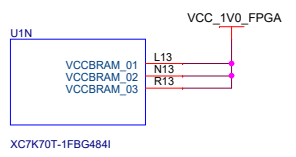
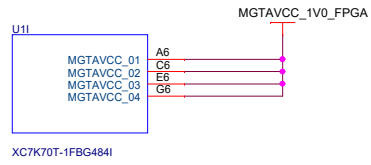
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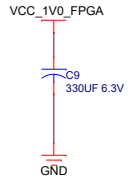
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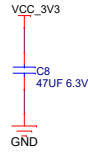
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BYPASS CAPACITORS

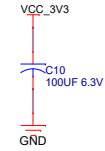
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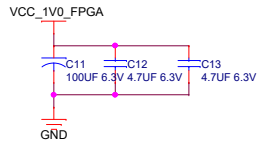
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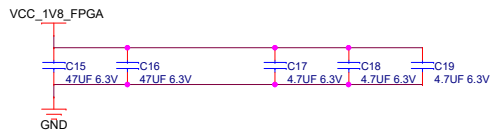
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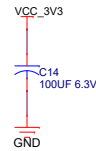
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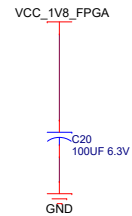
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Banks 16 3.3V VCCO



Banks 33, 34 1.5V VCCO

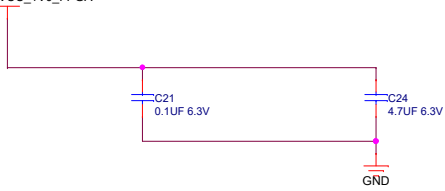


FPGA Bypass Capacitors

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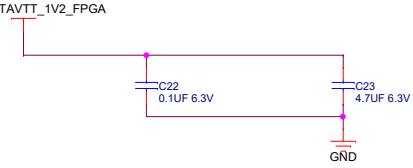
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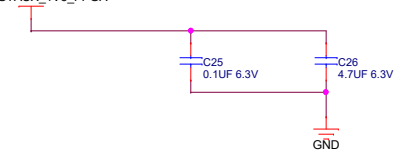
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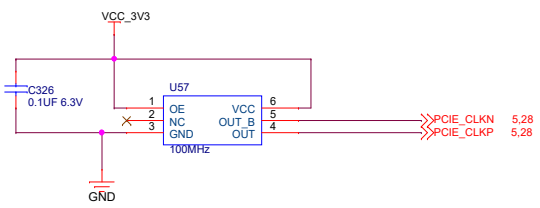
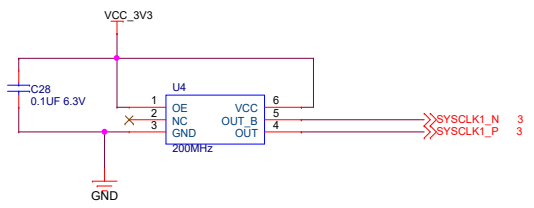
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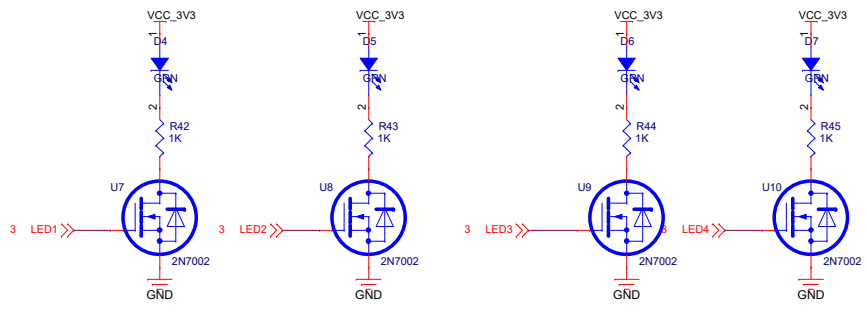
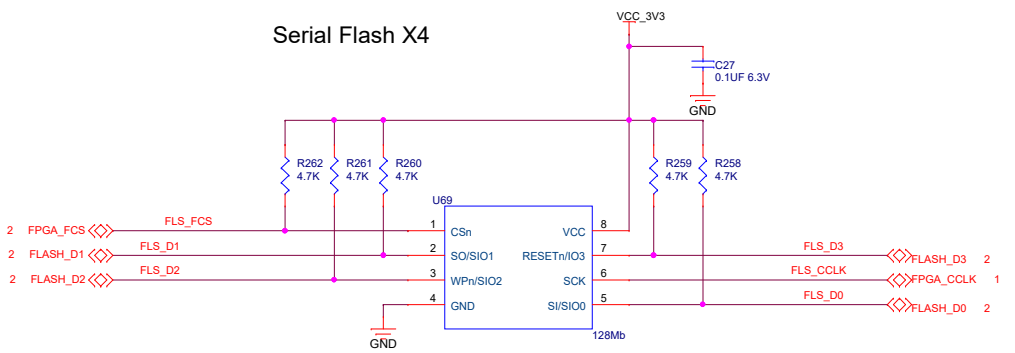


FPGA MGT Bypass Capacitors

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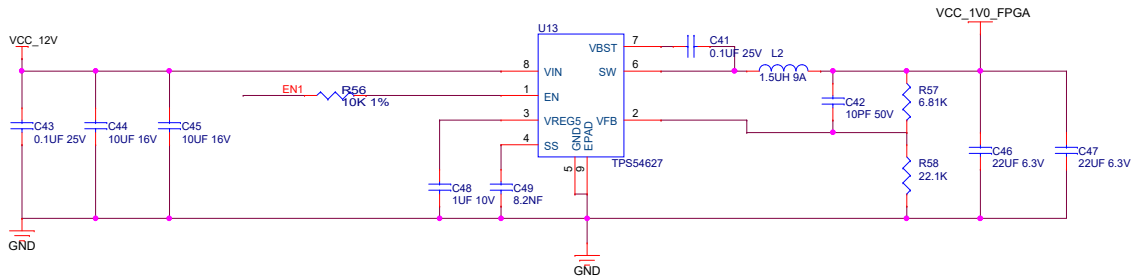
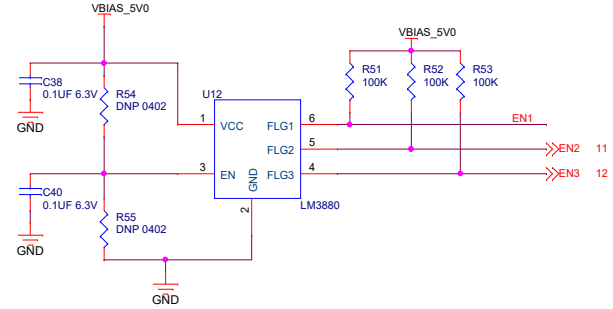
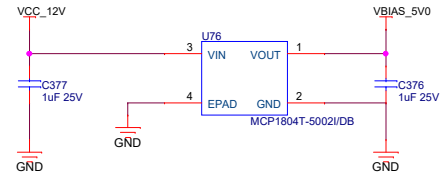
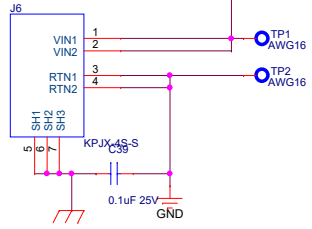
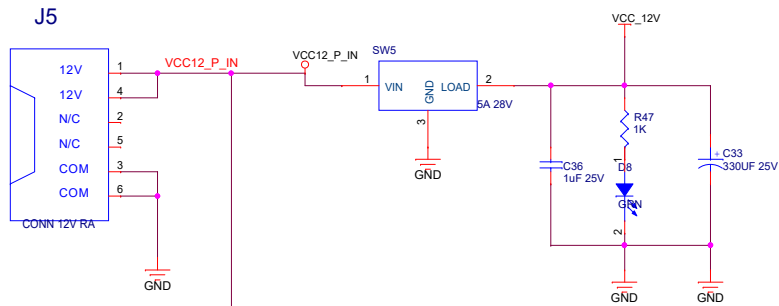


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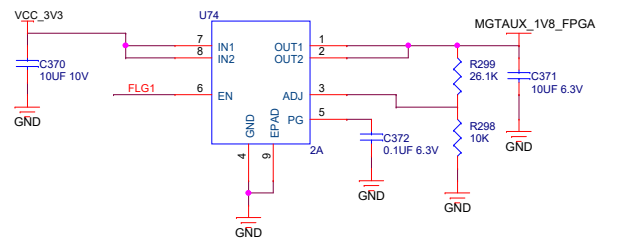
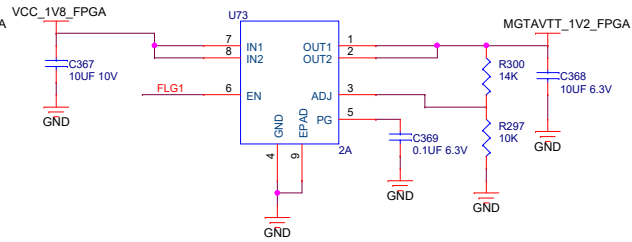
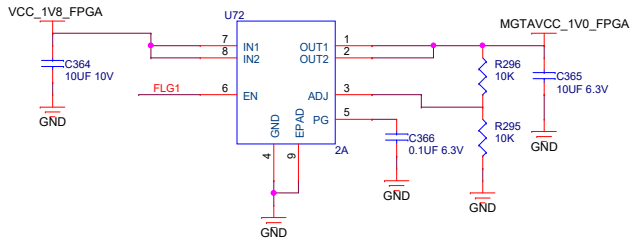
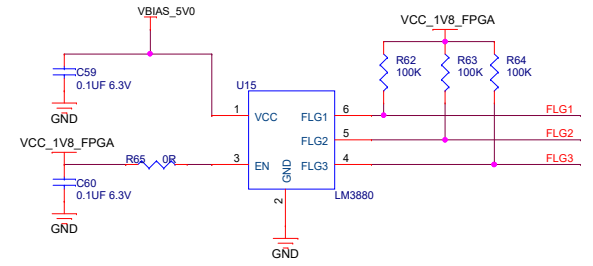
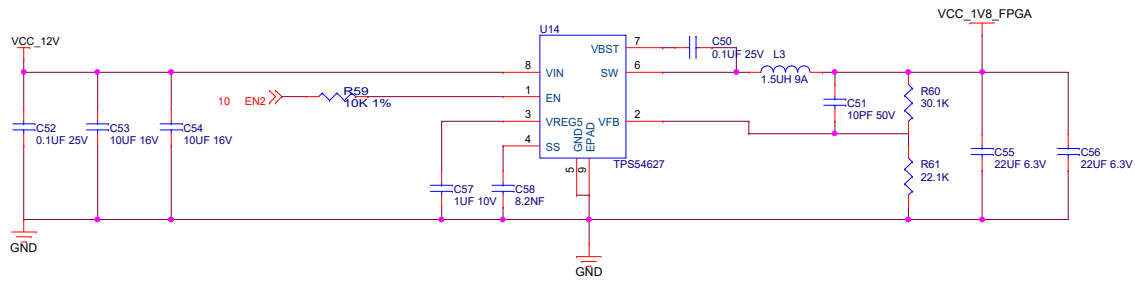


FPGA JTAG, Clock, Flash, Buttons

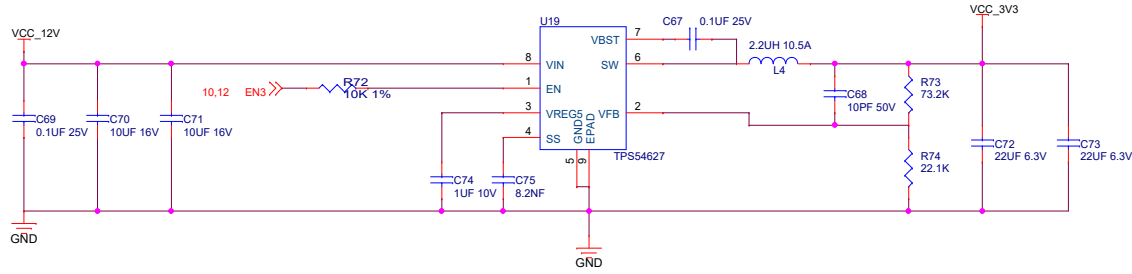
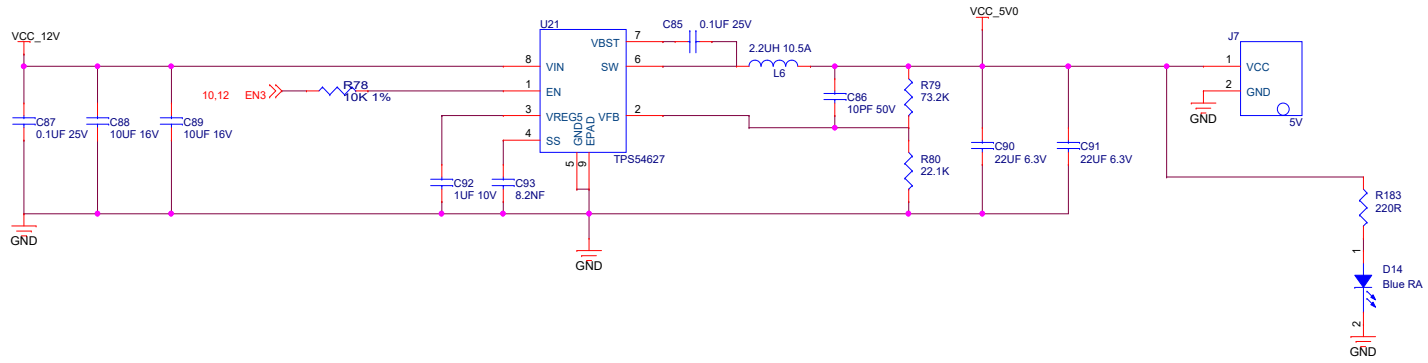
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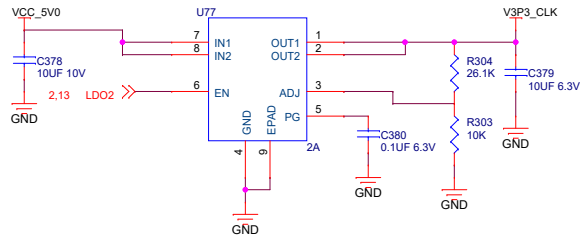
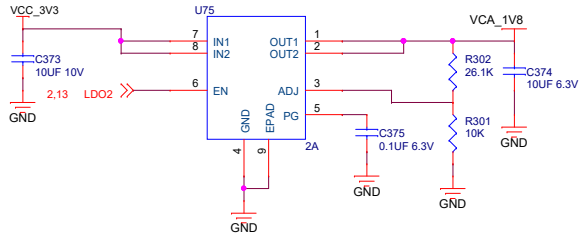
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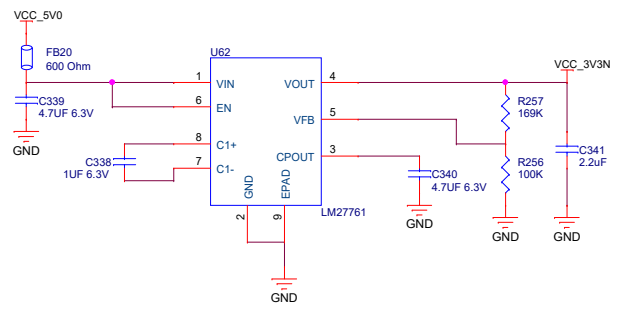
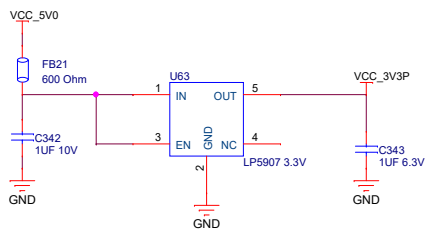
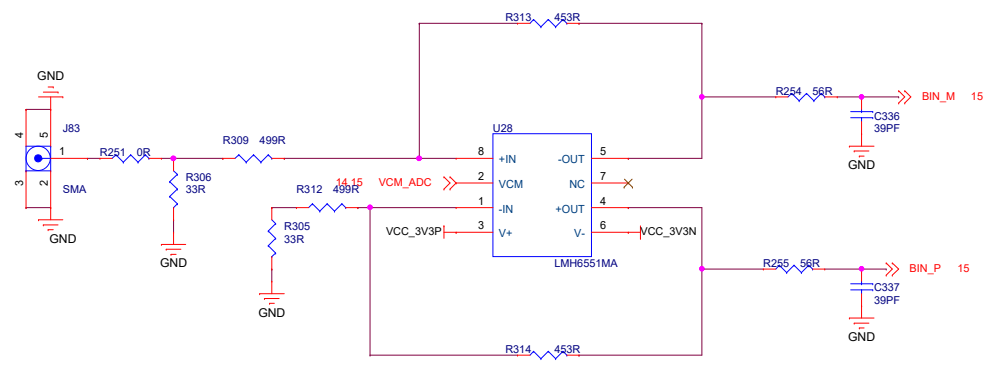
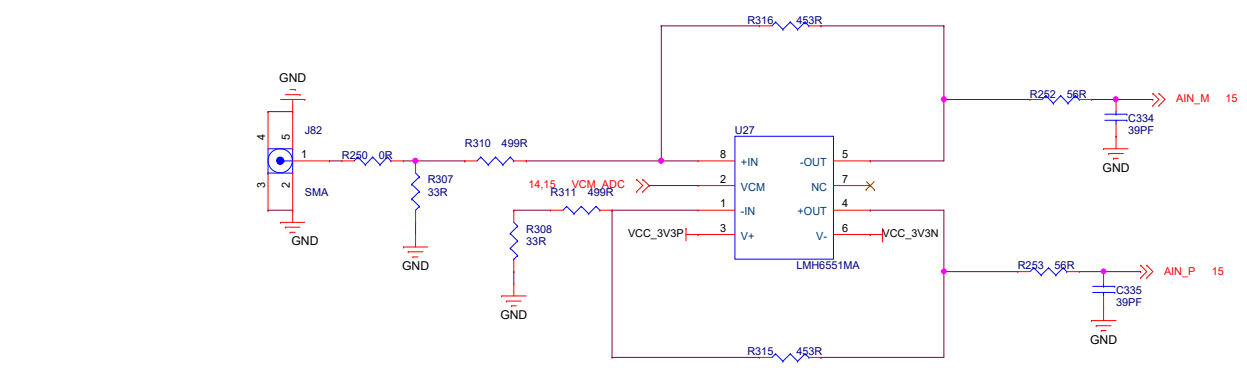
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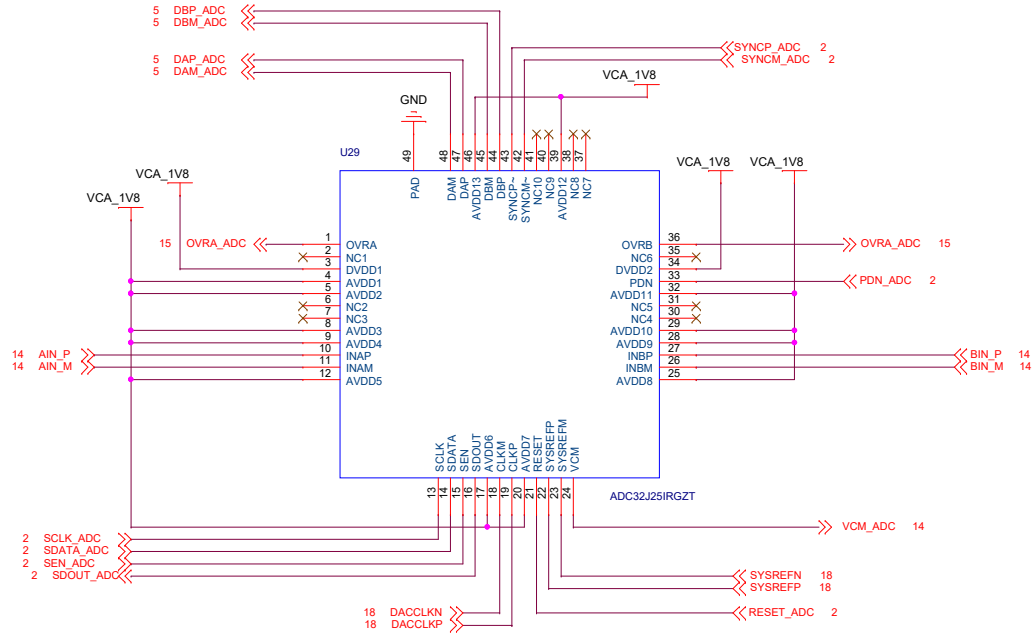
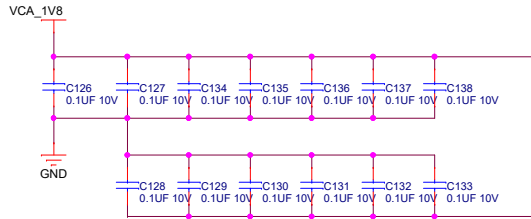
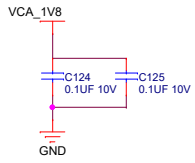
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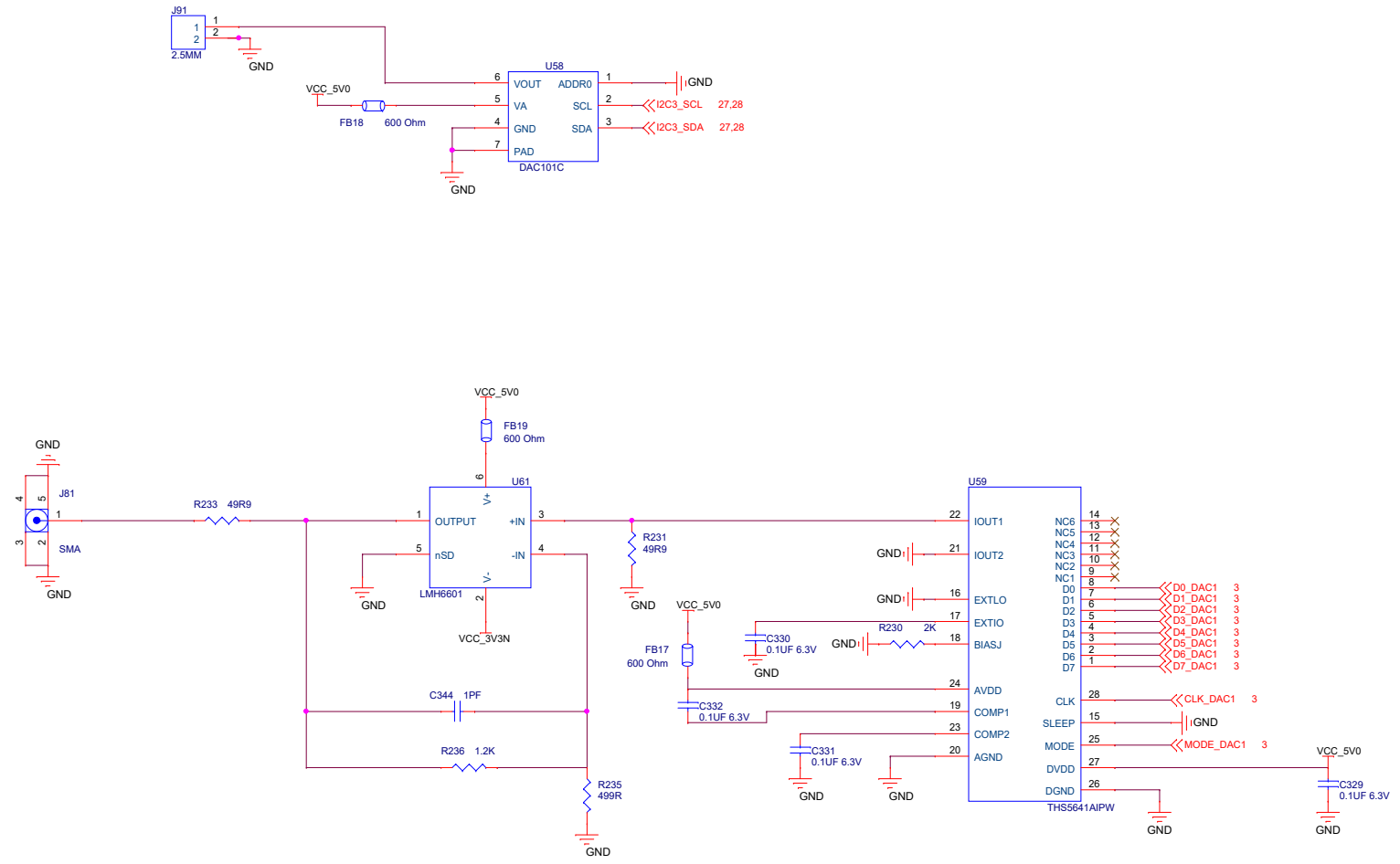
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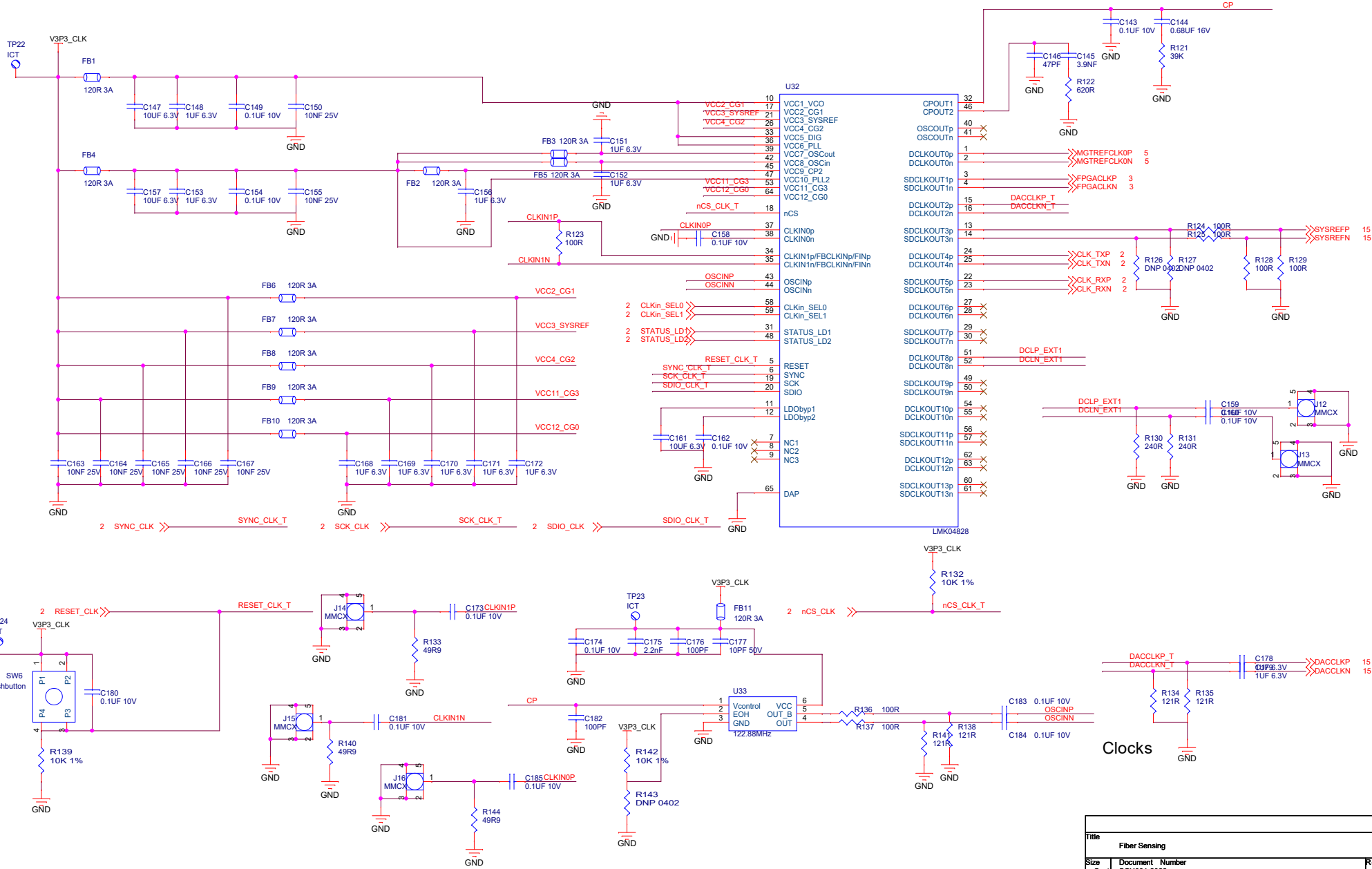
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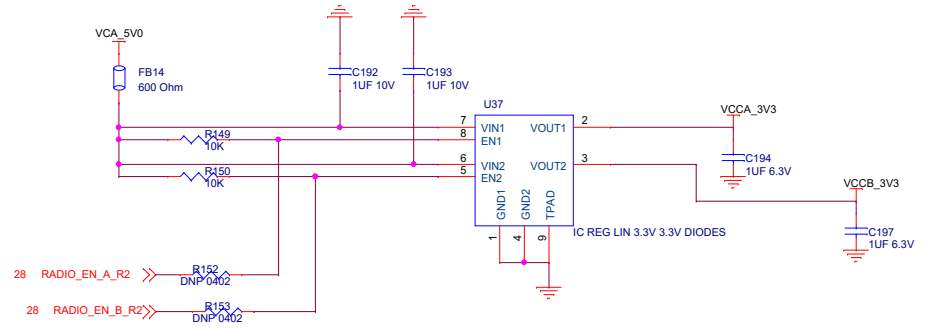
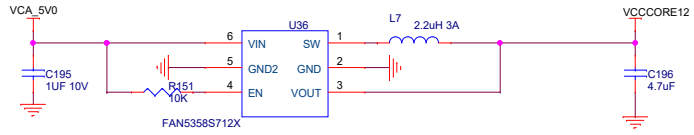
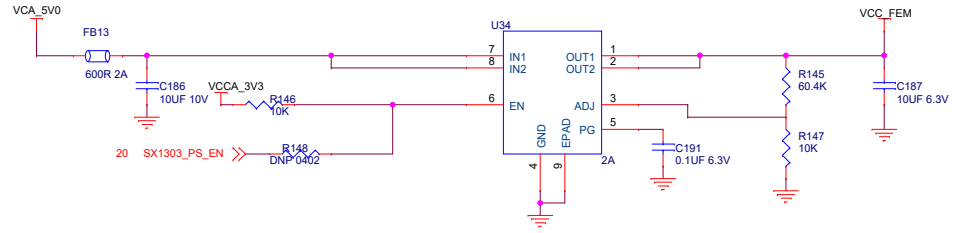
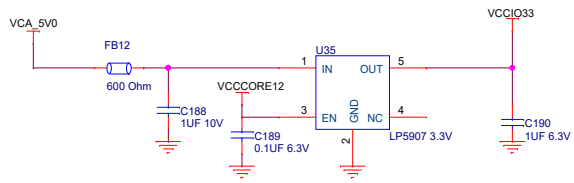


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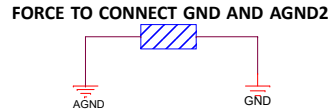
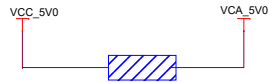


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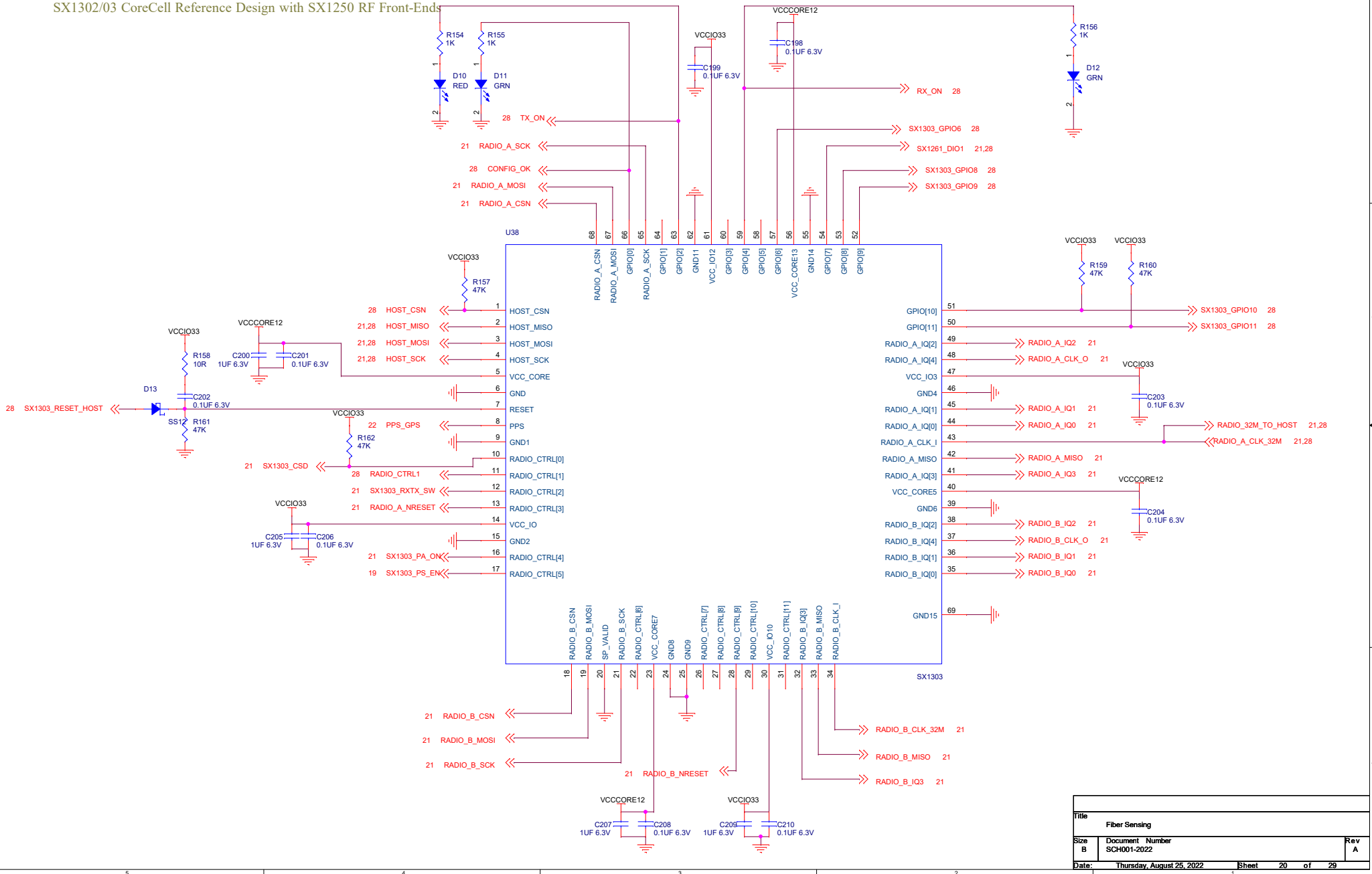


**HOW TO CONNECT gnd TO AGND2?
VIA STICING?
CONNECT POWER PLANE?**



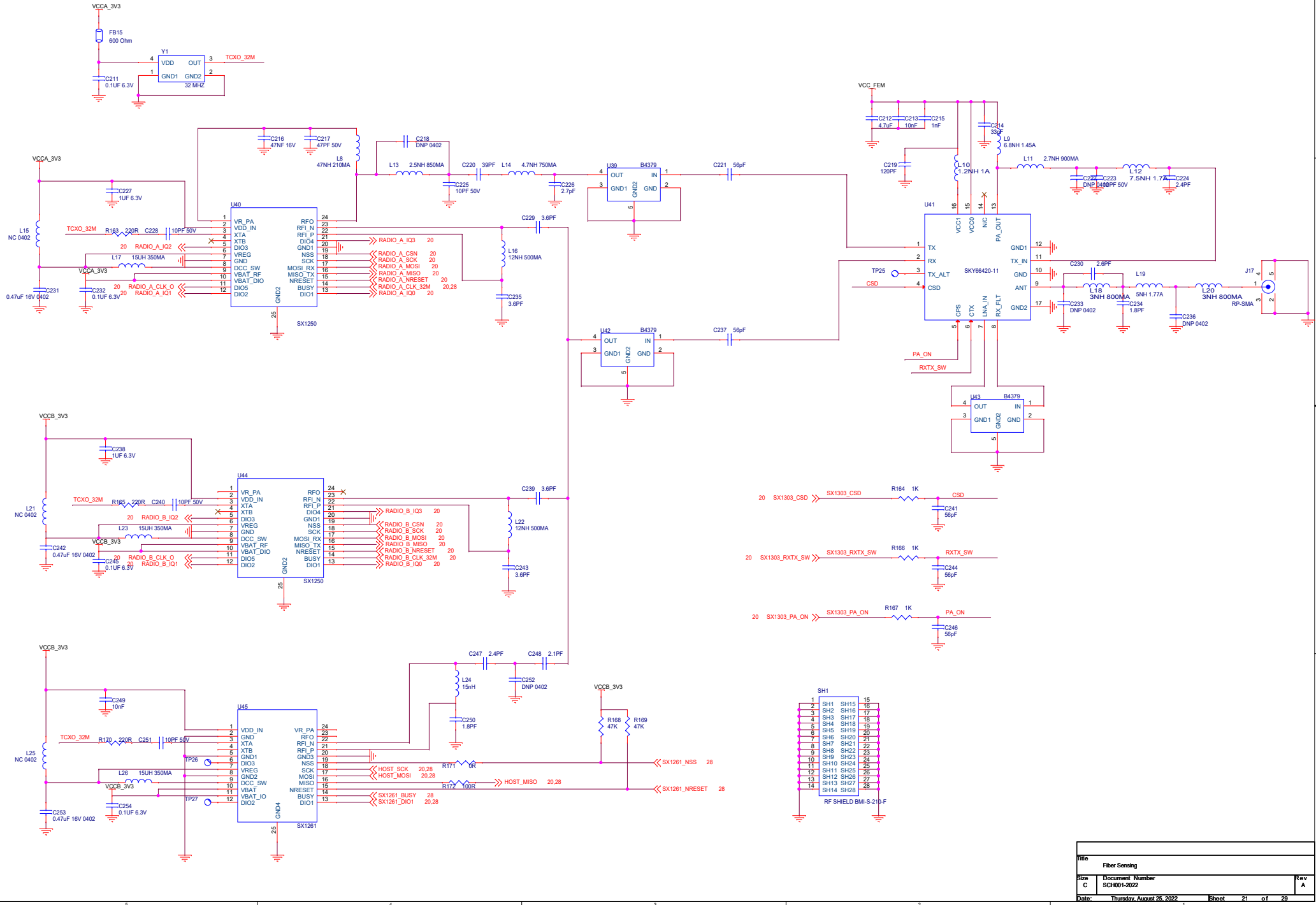
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SX1302/03 CoreCell Reference Design with SX1250 RF Front-Ends

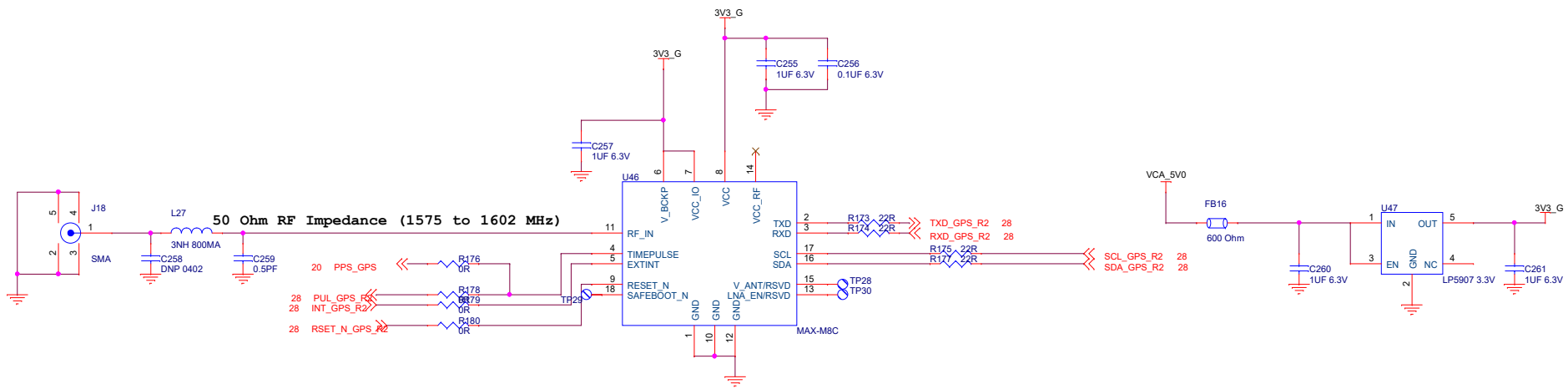


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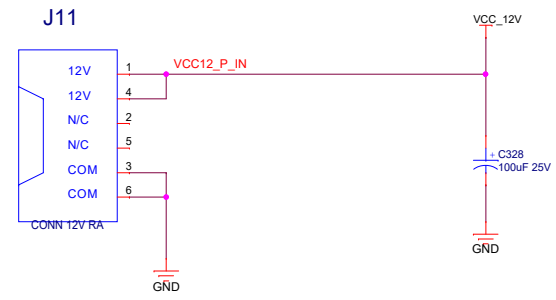
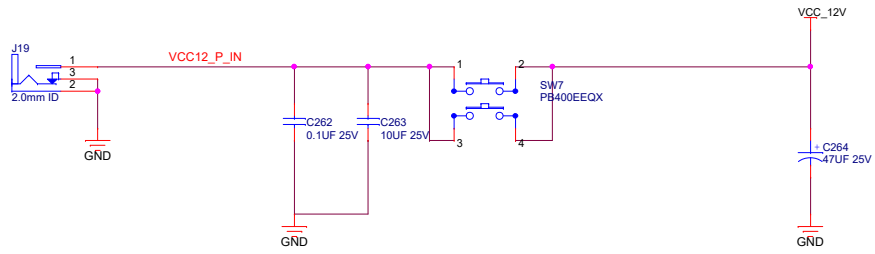
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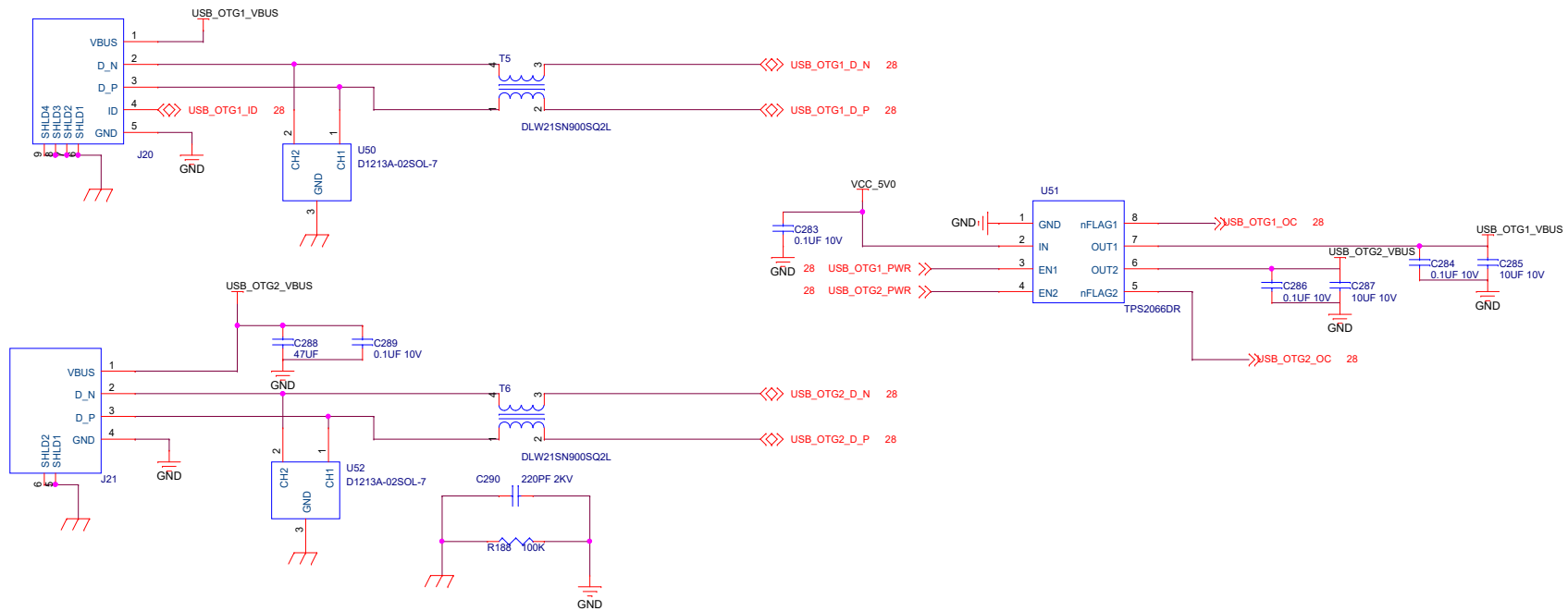
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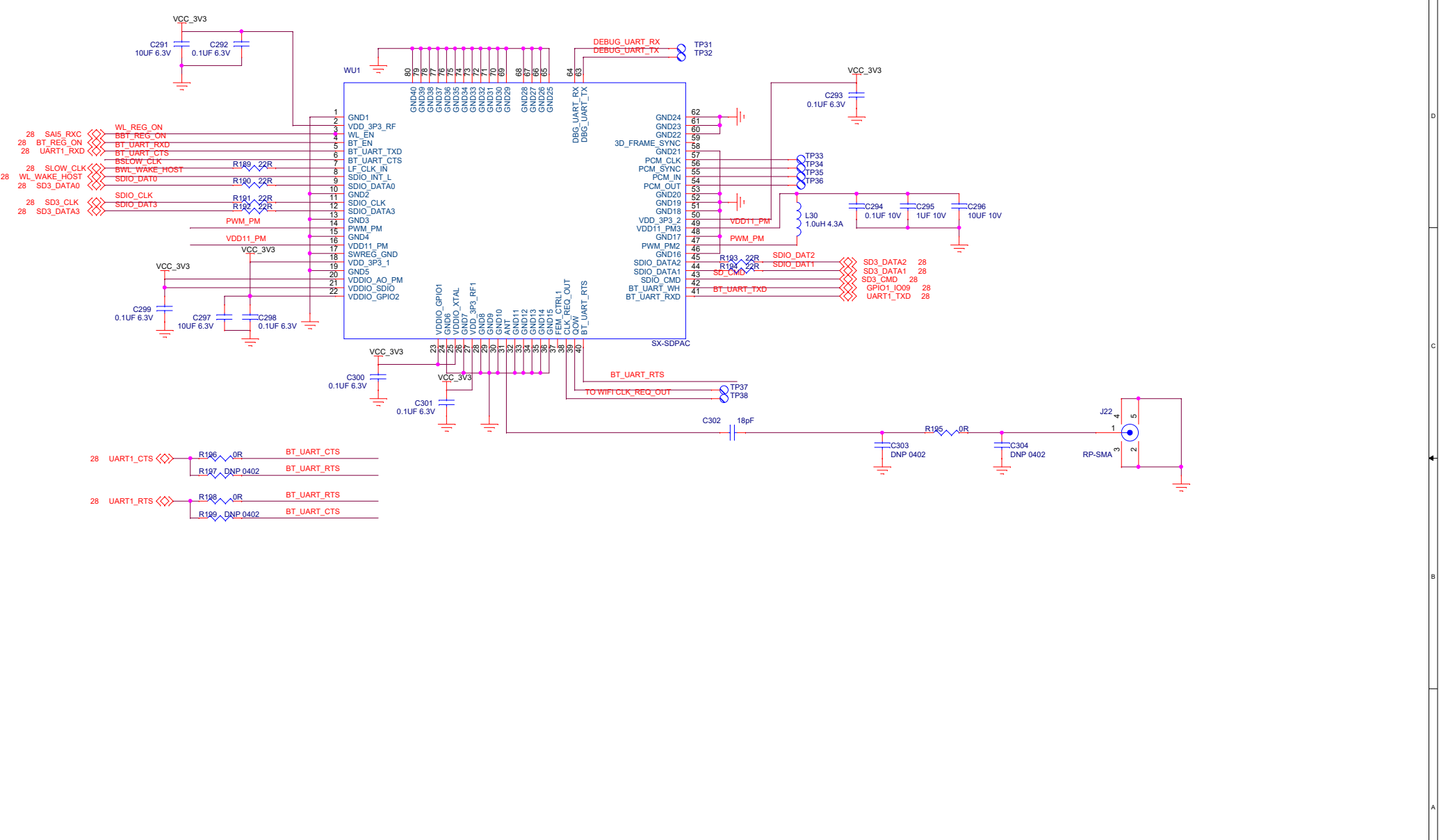
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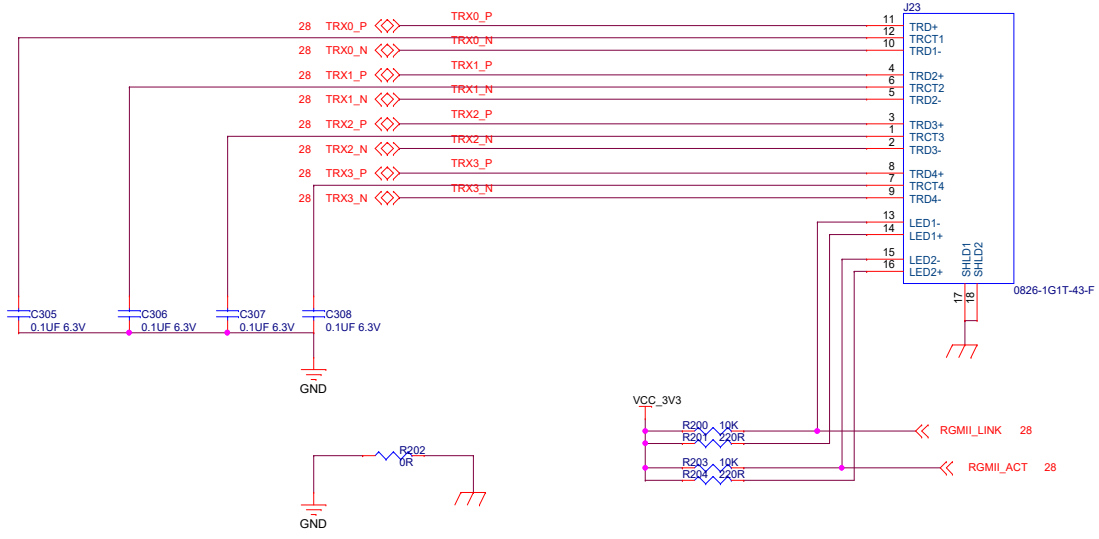
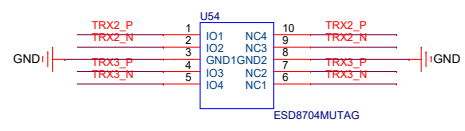
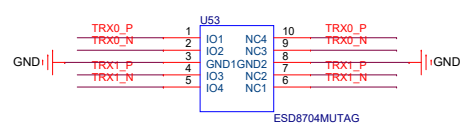
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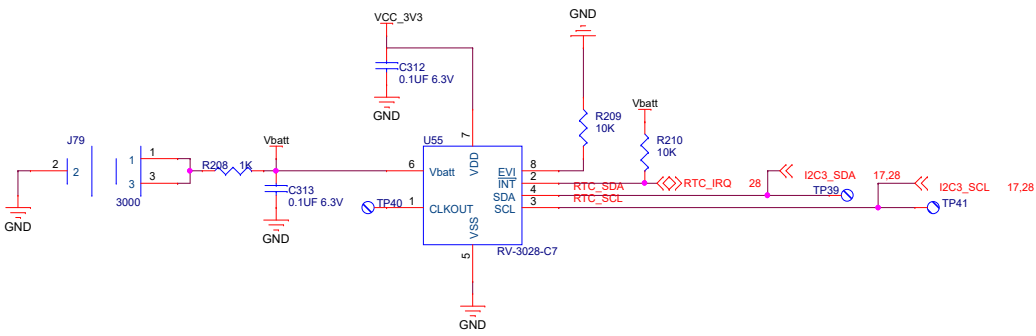
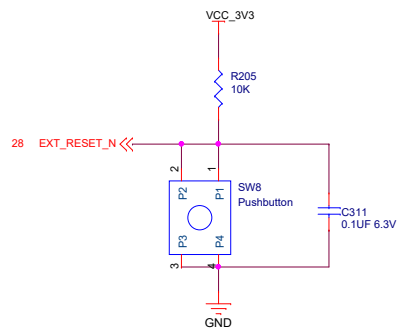
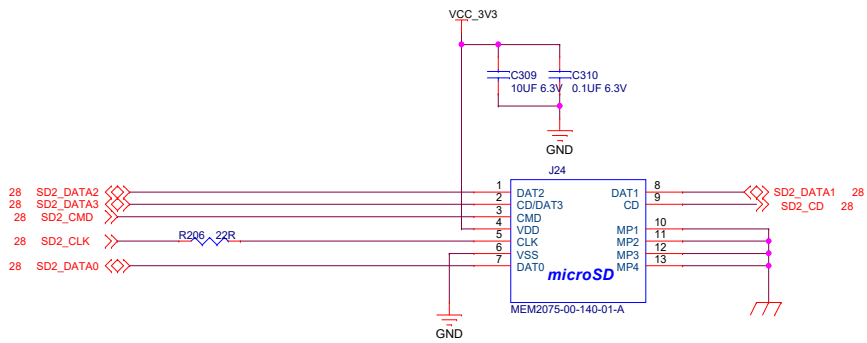
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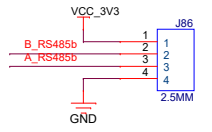
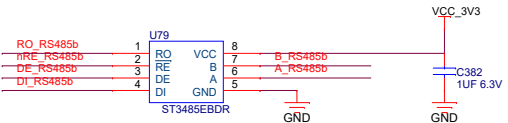
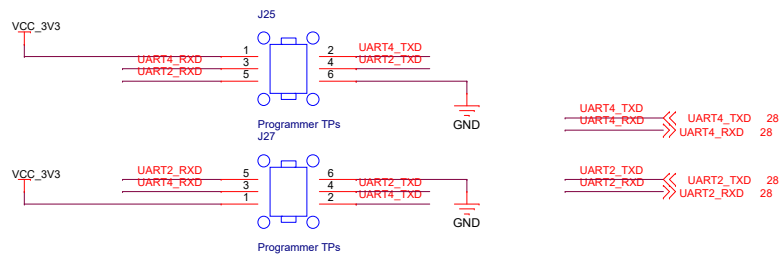
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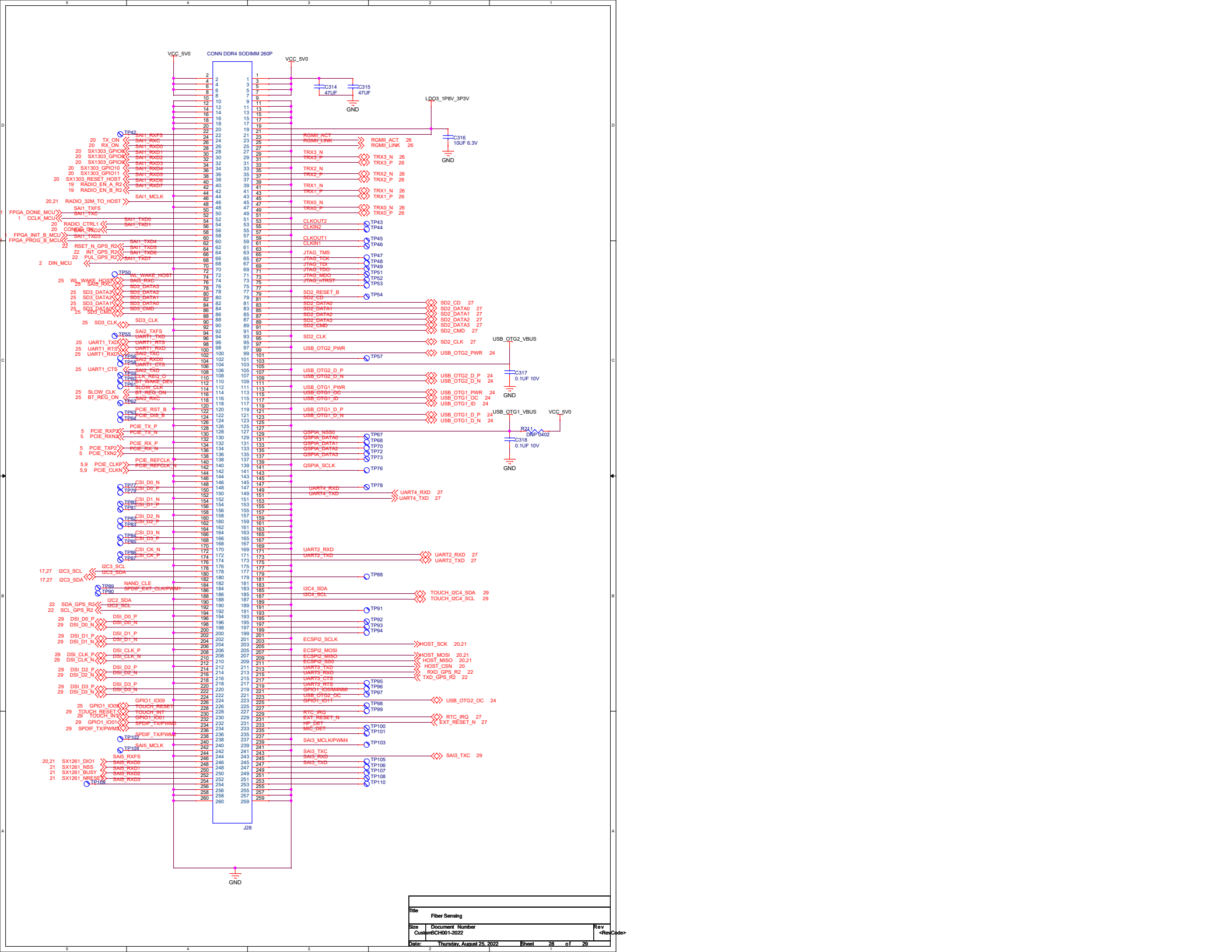
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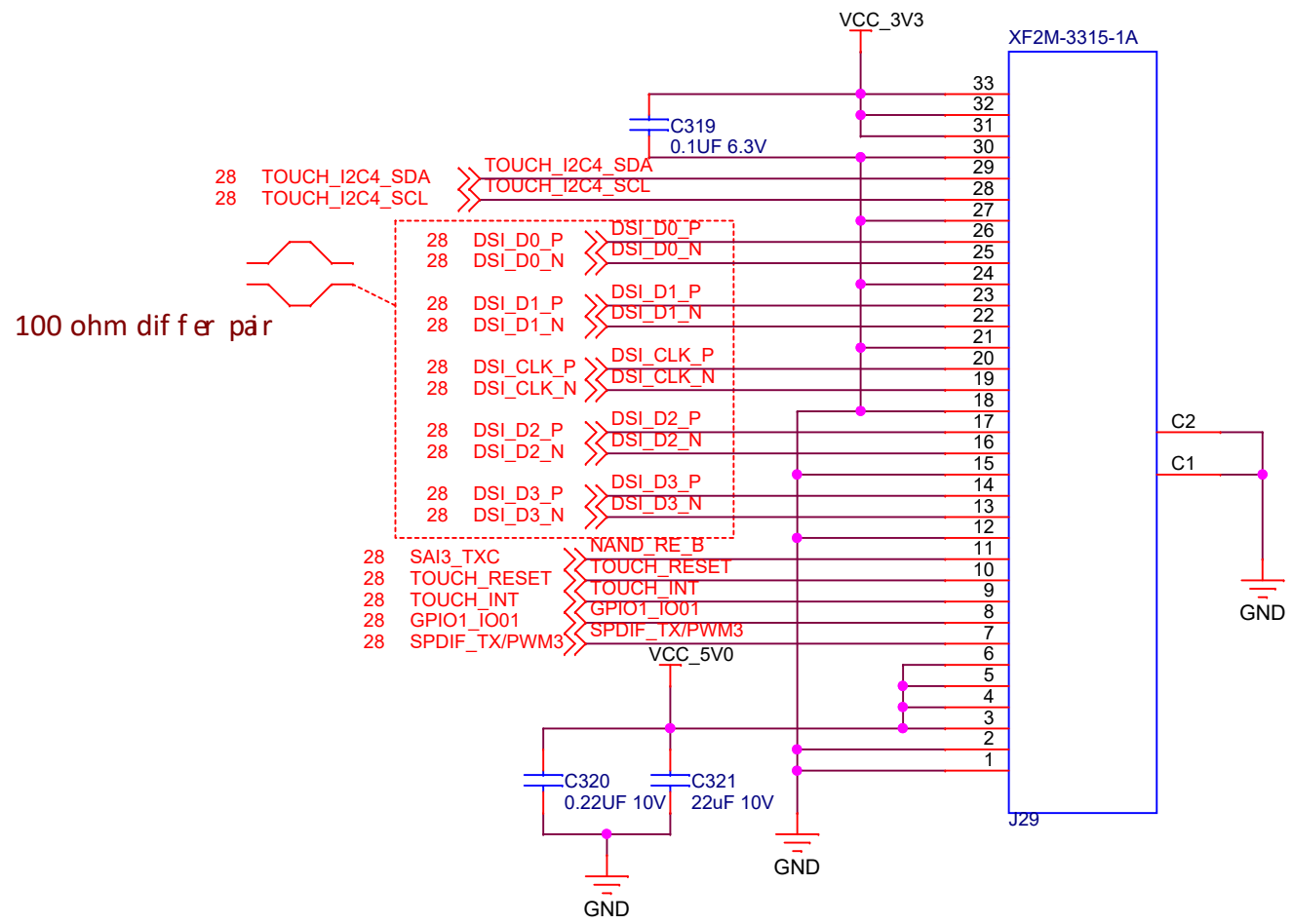


J5 is a flip of J4



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