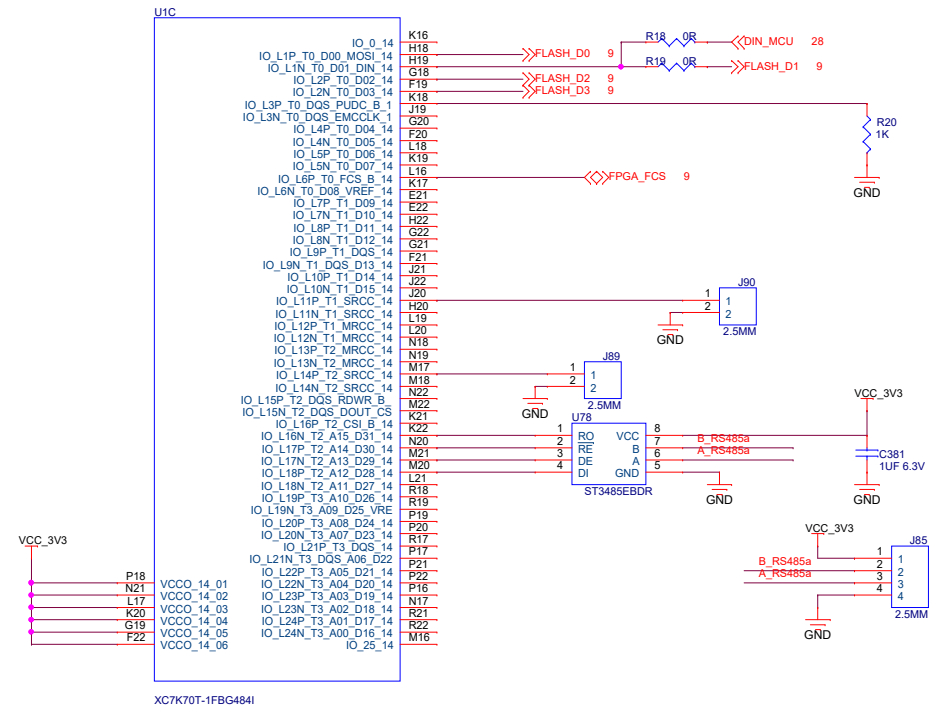
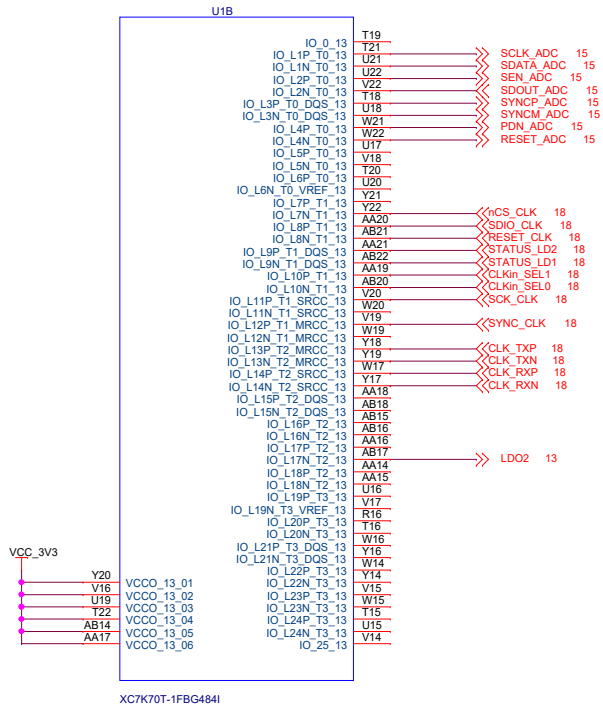
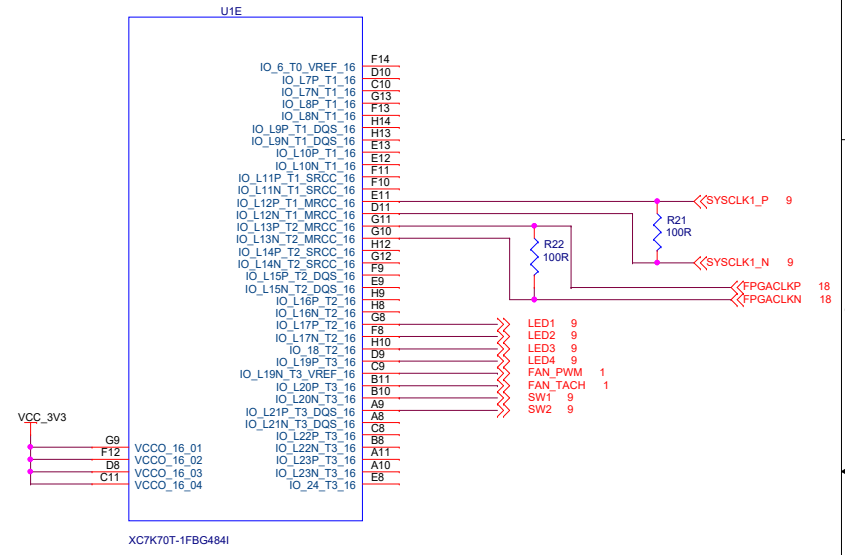
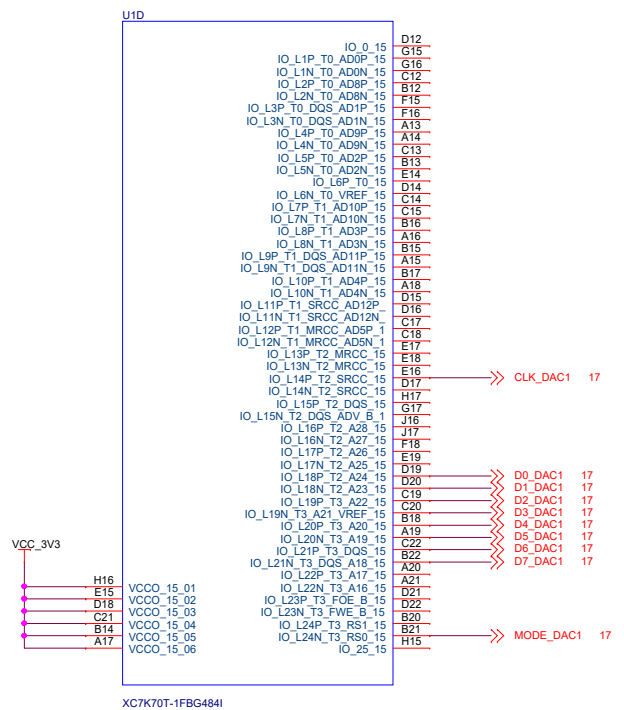


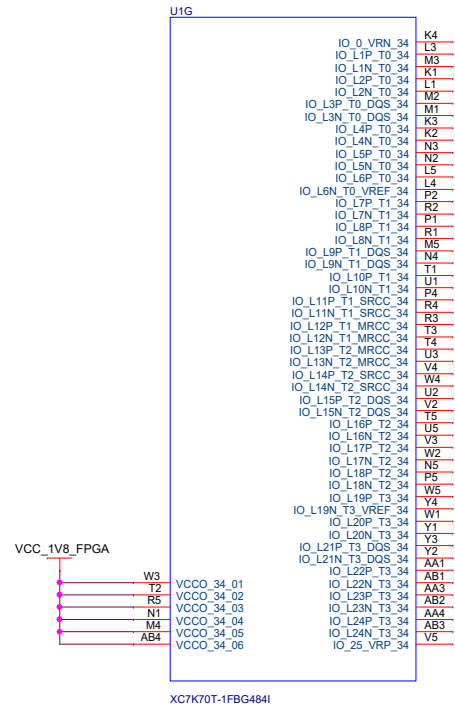
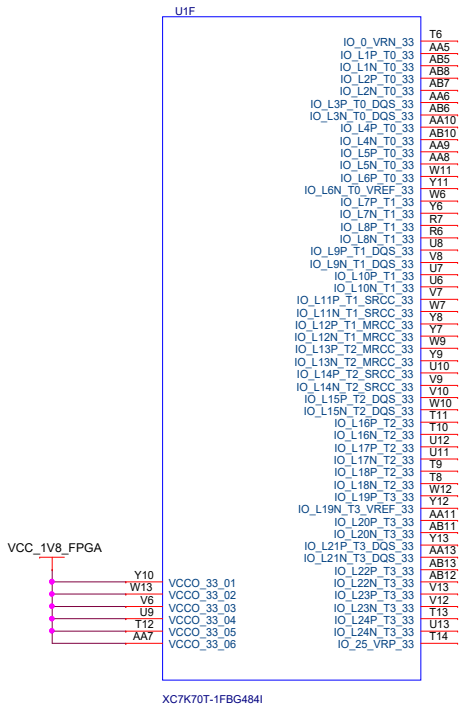
Title		
Fiber Sensing		
Size	Document Number	Rev
B	SCH001-2022	A
Date:	Thursday, August 25, 2022	Sheet 1 of 29



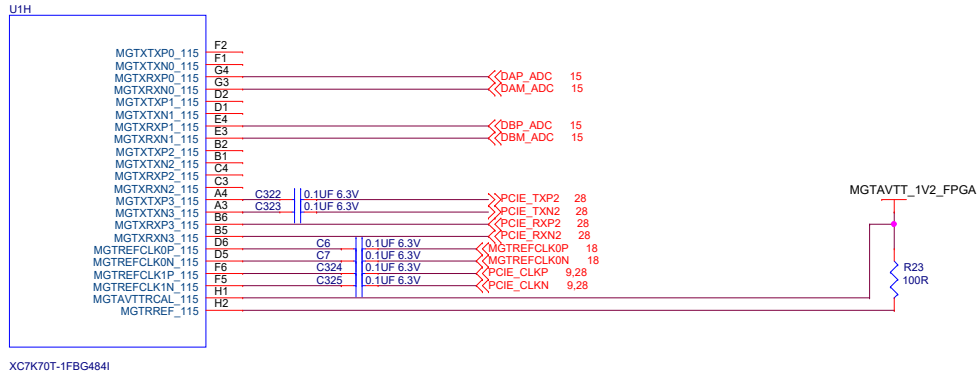
Title		
Fiber Sensing		
Size	Document Number	Rev
B	SCH001-2022	A
Date:	Thursday, August 25, 2022	Sheet 2 of 29



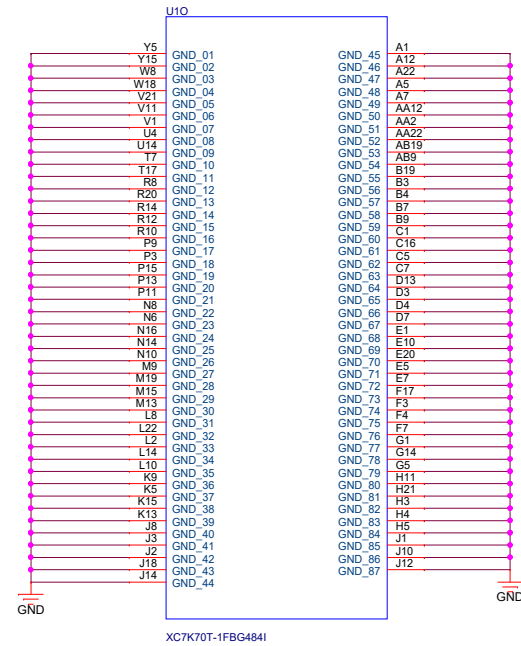
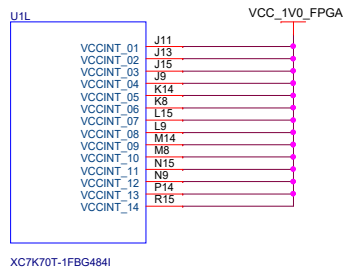
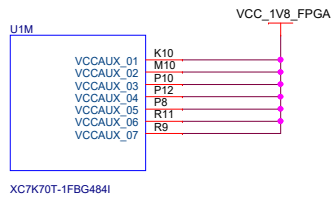
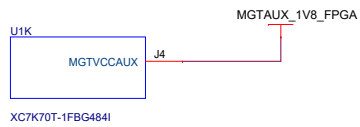
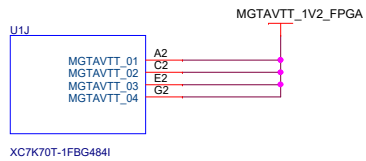
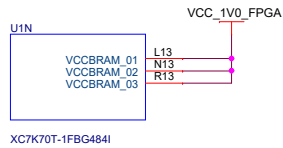
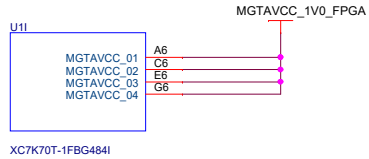
Title		
Fiber Sensing		
Size B	Document Number SCH001-2022	Rev A
Date:	Thursday, August 25, 2022	Sheet 3 of 29



Title		
Fiber Sensing		
Size B	Document Number SCH001-2022	Rev A
Date:	Thursday, August 25, 2022	Sheet 4 of 29



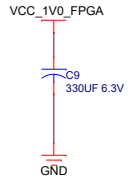
Title		
Fiber Sensing		
Size	Document Number	Rev
B	SCH001-2022	A
Date:	Thursday, August 25, 2022	Sheet 5 of 29



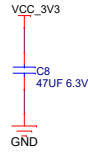
Title		
Fiber Sensing		
Size	Document Number	Rev
B	SCH001-2022	A
Date:	Thursday, August 25, 2022	Sheet 6 of 29

# BYPASS CAPACITORS

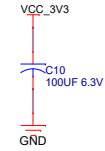
## VCCINT 330uF (2)



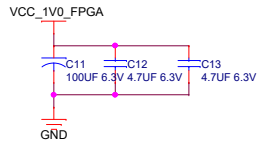
## Bank 0 1.5V VCCO



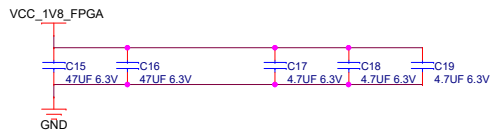
## Bank 13/14/15 1.5V VCCO



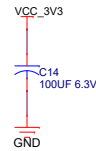
## VCCBRAM 100uF (1), 4.7uF (3) 0402



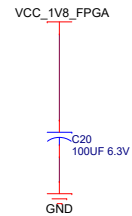
## VCCAUX 47uF



## Banks 16 3.3V VCCO



## Banks 33, 34 1.5V VCCO

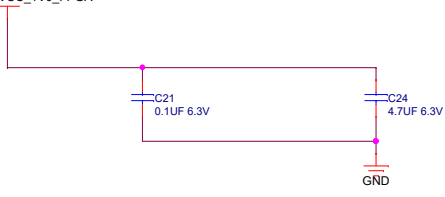


## FPGA Bypass Capacitors

Title		Fiber Sensing	
Size	Document Number	Rev	
Custom	SCH001-2022	A	
Date:	Thursday, August 25, 2022	Sheet	7 of 29

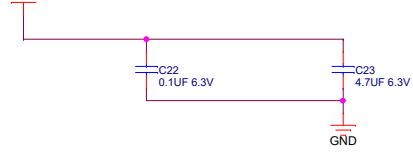
### MGTAVCC

MGTAVCC\_1V0\_FPGA



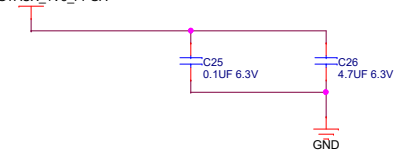
### MGTAVTT

MGTAVTT\_1V2\_FPGA



### MGTAUX

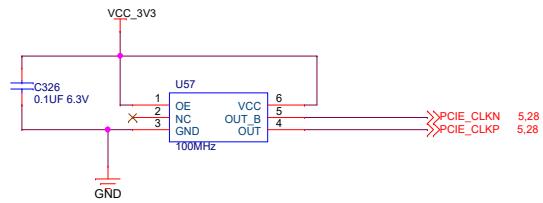
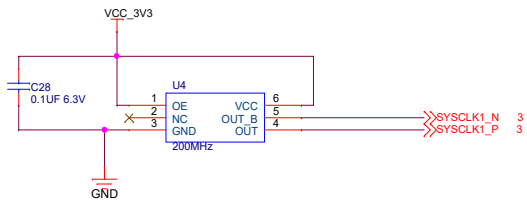
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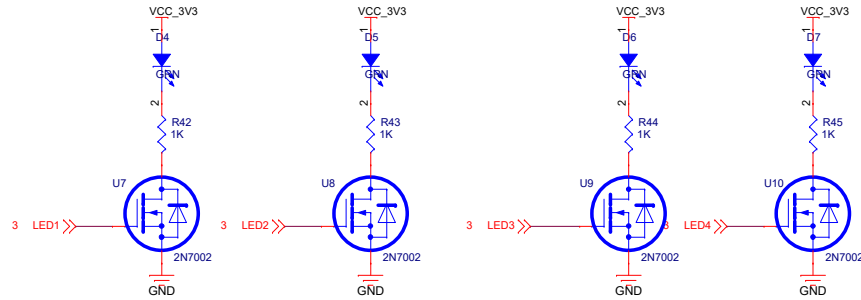
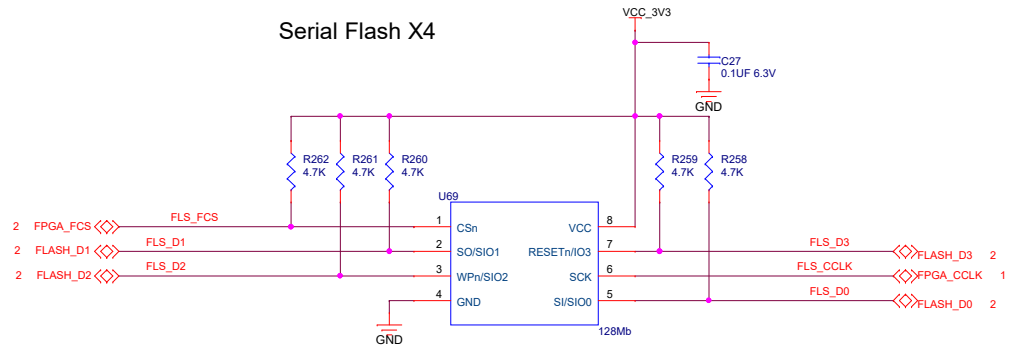
### FPGA MGT Bypass Capacitors

Title			Fiber Sensing
Size	Document Number	Rev	
Custom	SCH001-2022	A	
Date:	Thursday, August 25, 2022	Sheet	8 of 29





### Serial Flash X4



### FPGA JTAG, Clock, Flash, Buttons

Title Fiber Sensing

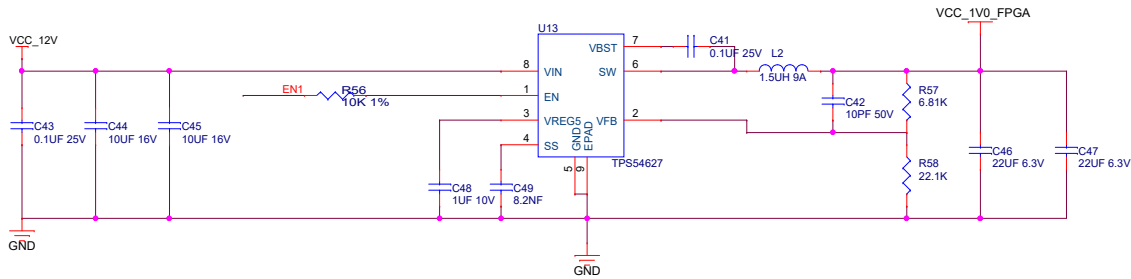
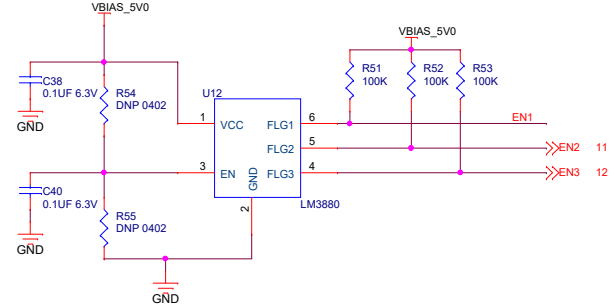
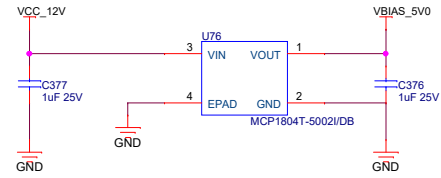
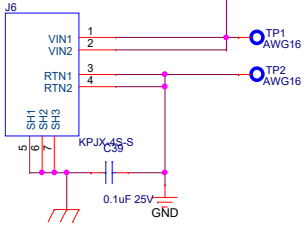
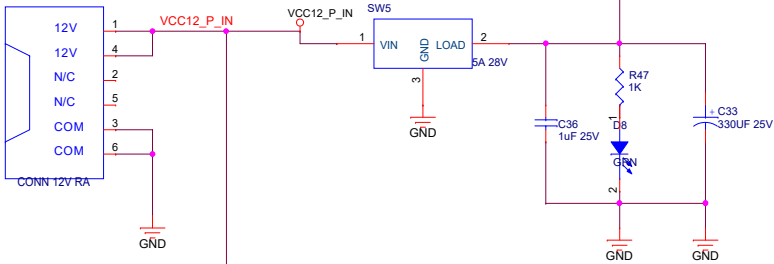
Document Number SCH001-2022

Rev  
A

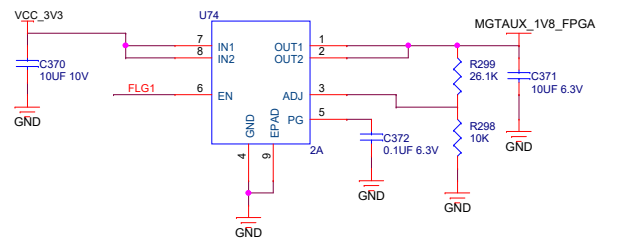
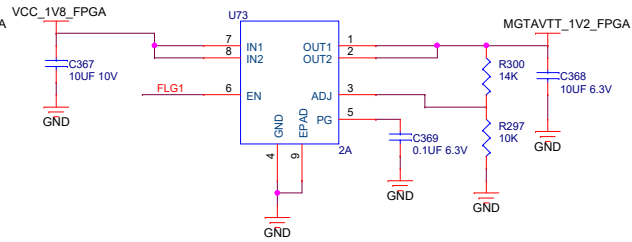
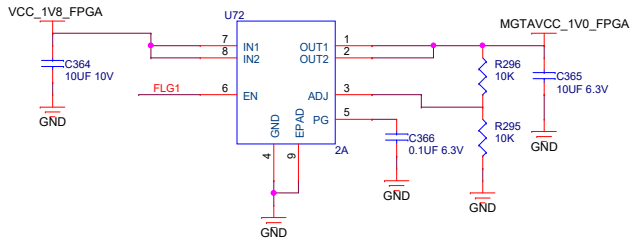
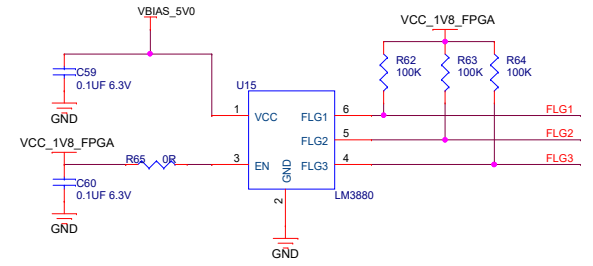
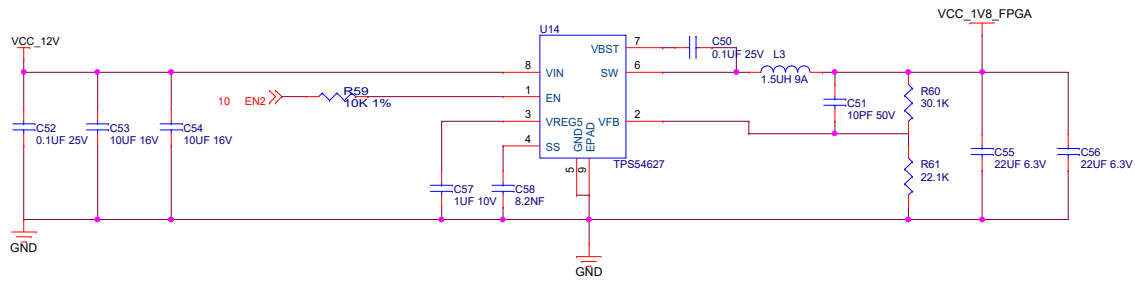
Date: Thursday, August 25, 2022

Sheet 9 of 29

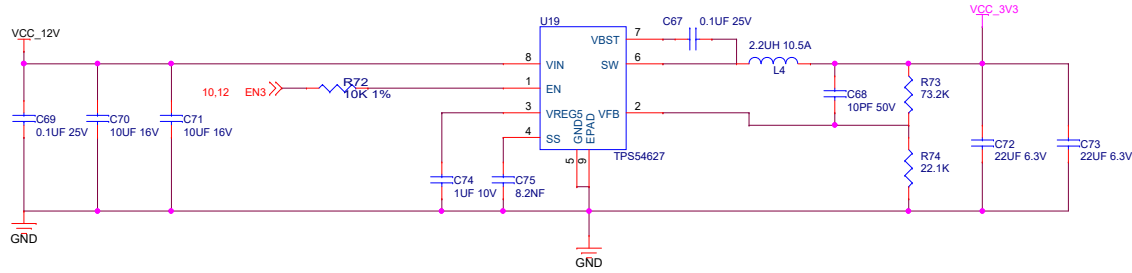
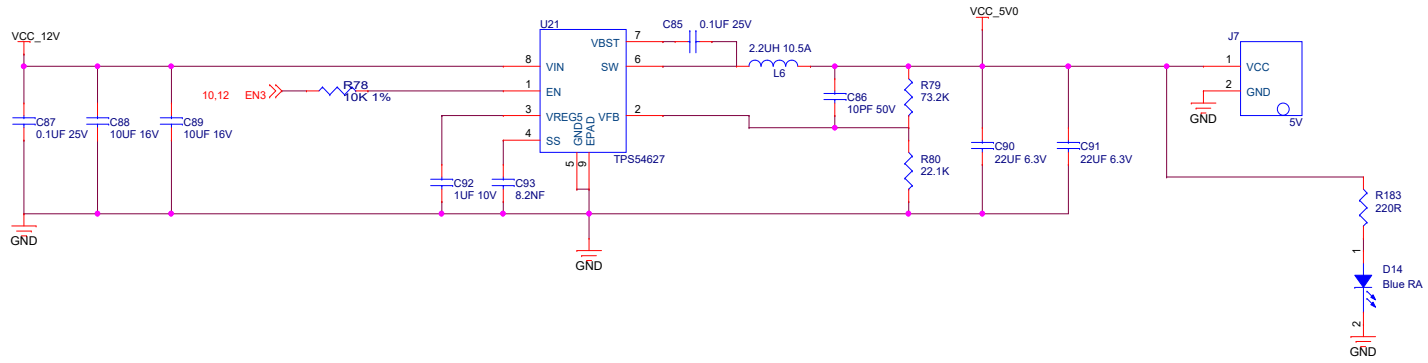
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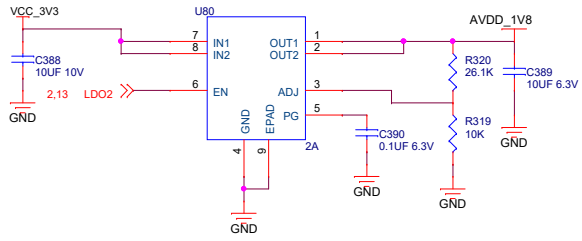
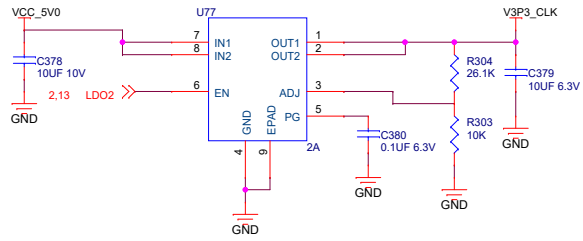
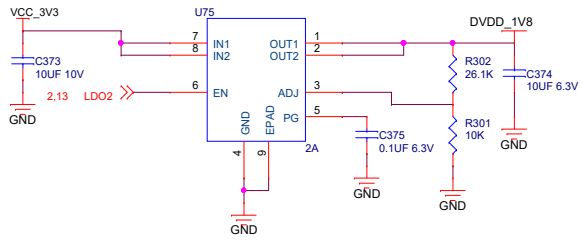
Title		
Fiber Sensing		
Size	Document Number	Rev
B	SCH001-2022	A
Date:	Thursday, August 25, 2022	Sheet 10 of 29



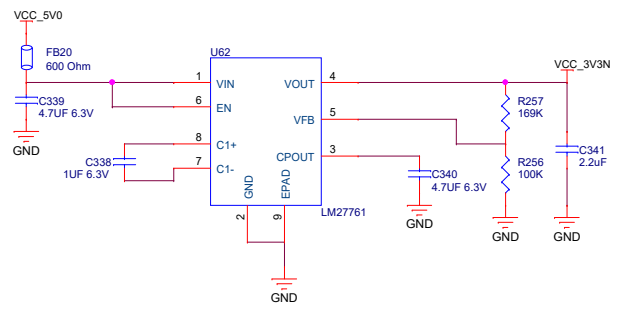
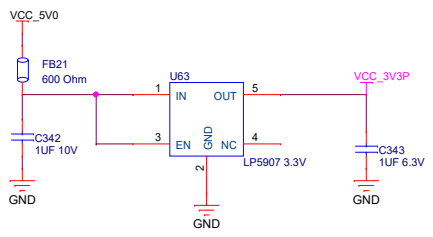
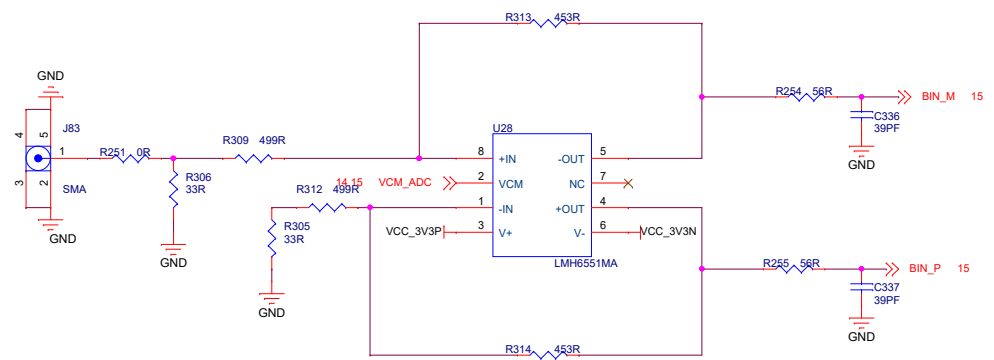
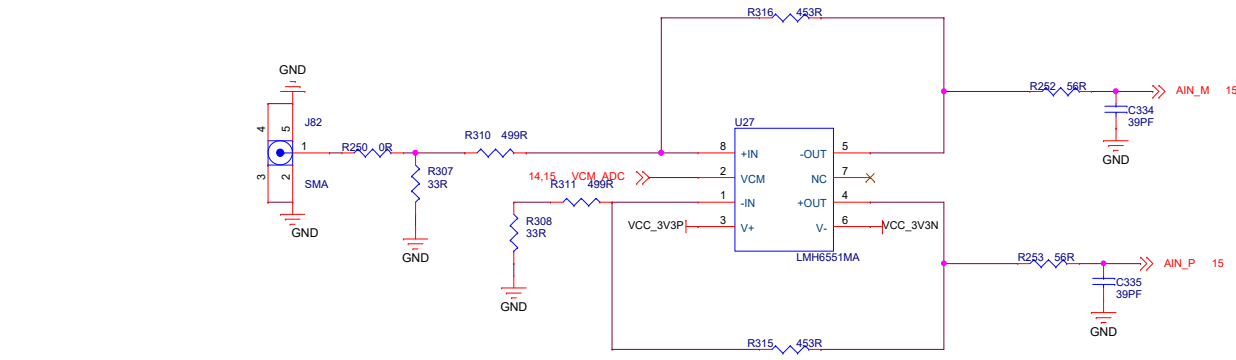
Title		
Fiber Sensing		
Size	Document Number	Rev
B	SCH001-2022	A
Date:	Thursday, August 25, 2022	Sheet 11 of 29



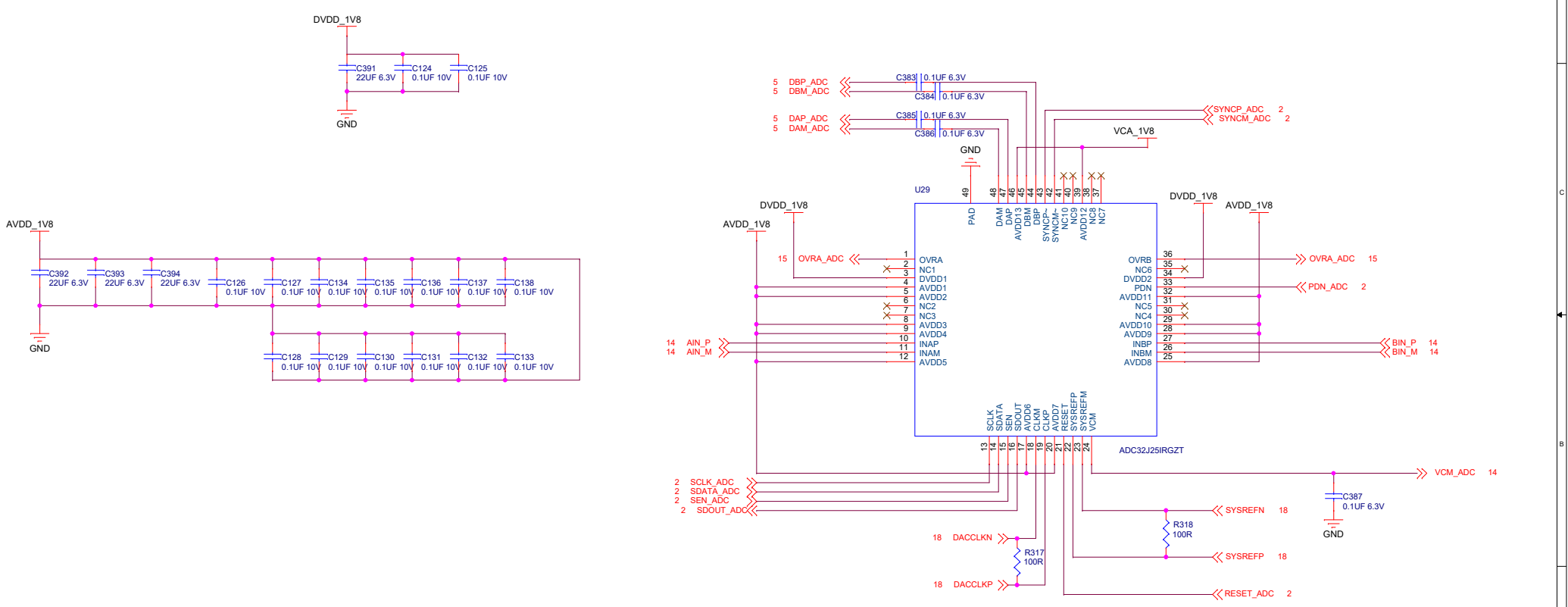
Title		
Fiber Sensing		
Size	Document Number	Rev
B	SCH001-2022	A
Date:	Thursday, August 25, 2022	Sheet 12 of 29



Title		
Fiber Sensing		
Size	Document Number	Rev
B	SCH001-2022	A
Date:	Tuesday, November 01, 2022	Sheet 13 of 29



Title		
Fiber Sensing		
Size	Document Number	Rev
CustomSCH001-2022		A
Date:	Thursday, August 25, 2022	Sheet 14 of 29



Title		
Fiber Sensing		
Size	Document Number	Rev
	CustomSCH001-2022	A
Date:	Tuesday, November 01, 2022	Sheet 15 of 29

5

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3

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C

B

B

A

A

Title Fiber Sensing		
Size A	Document Number SCH001-2022	Rev <Rev Co
Date: Saturday, August 13, 2022	Sheet 16	of 29

5

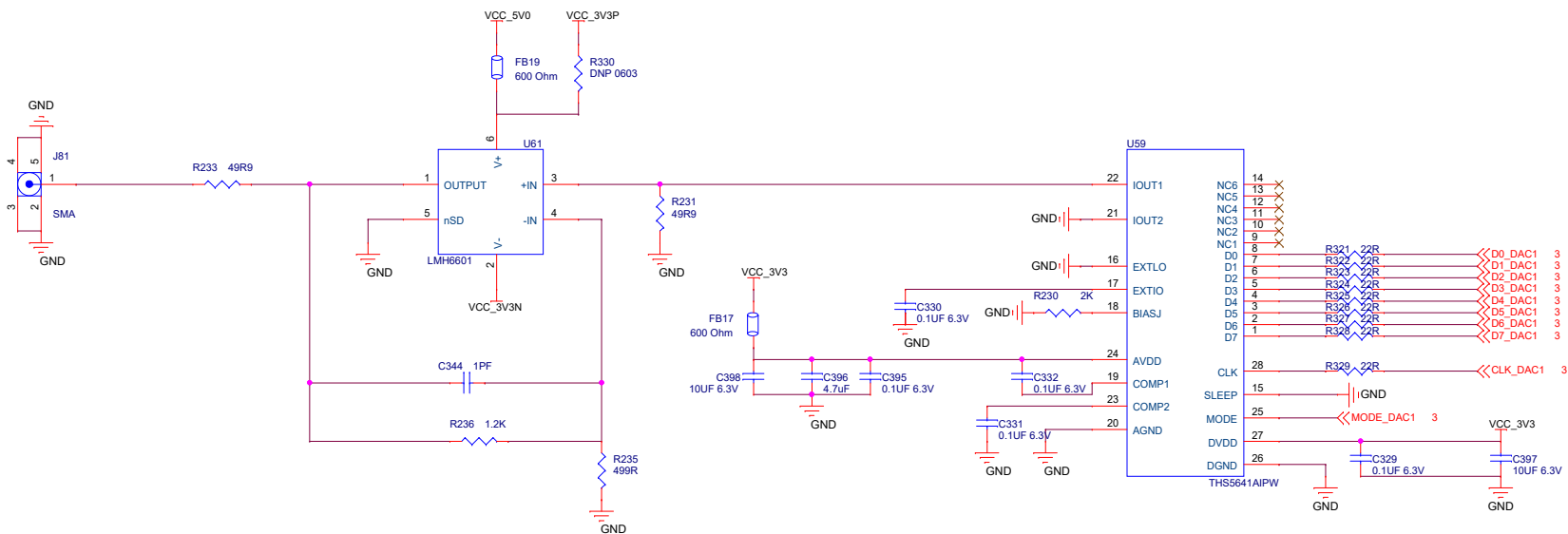
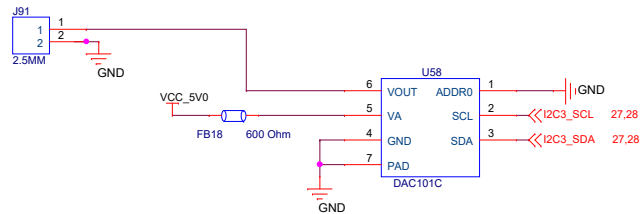
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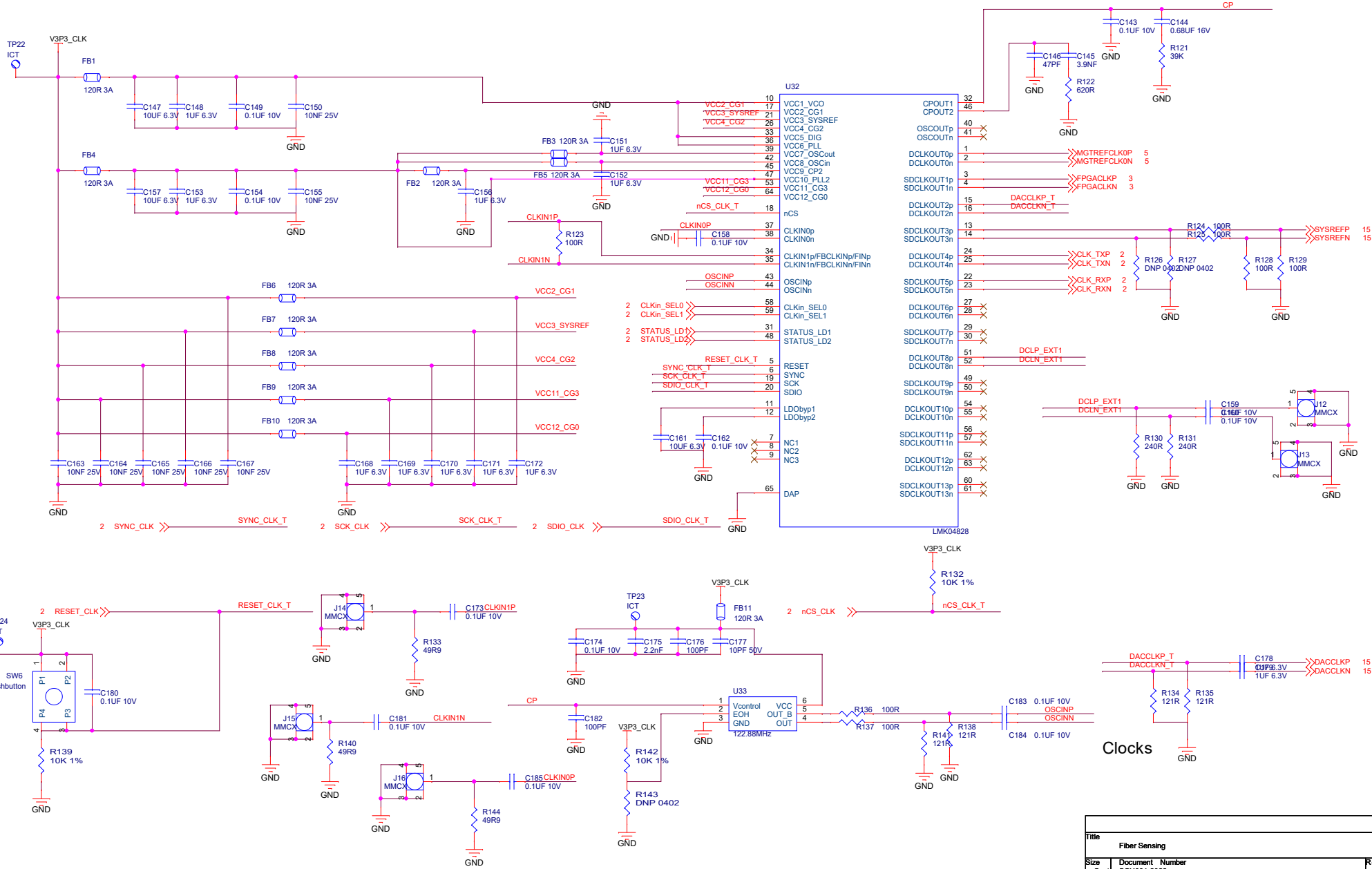
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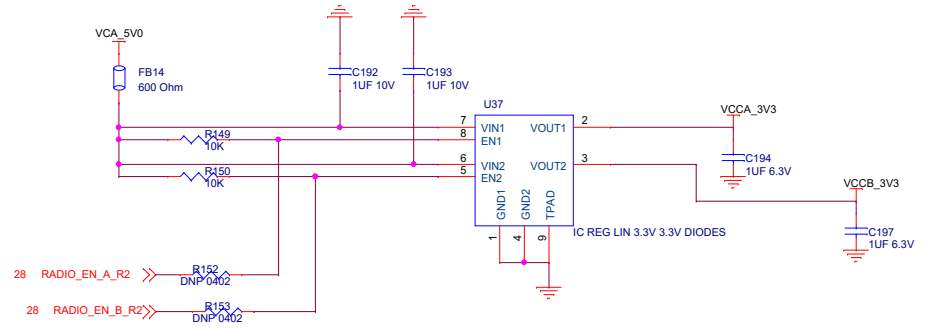
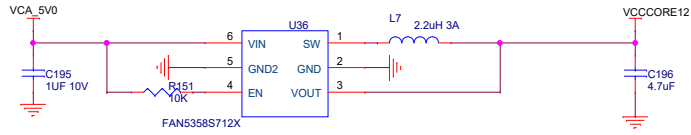
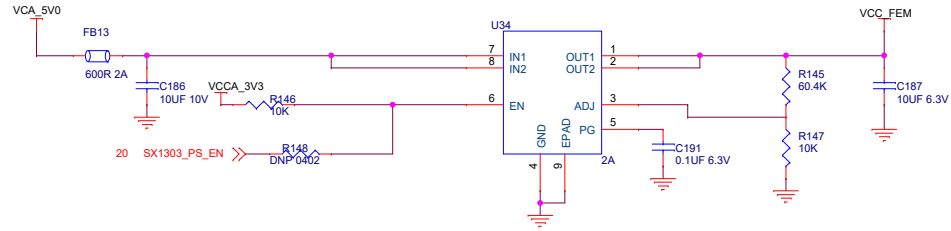
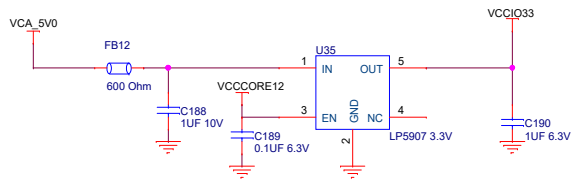


Title		
Fiber Sensing		
Size	Document Number	Rev
Custom	SCH001-2022	A
Date:	Thursday, November 03, 2022	Sheet 17 of 29

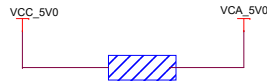


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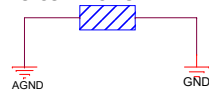
Title			
Fiber Sensing			
Size	Document Number	Rev A	
	CustomSCH001-2022		
Date:	Thursday, August 25, 2022	Sheet	18 of 29



**HOW TO CONNECT gnd TO AGND2?  
VIA STICING?  
CONNECT POWER PLANE?**

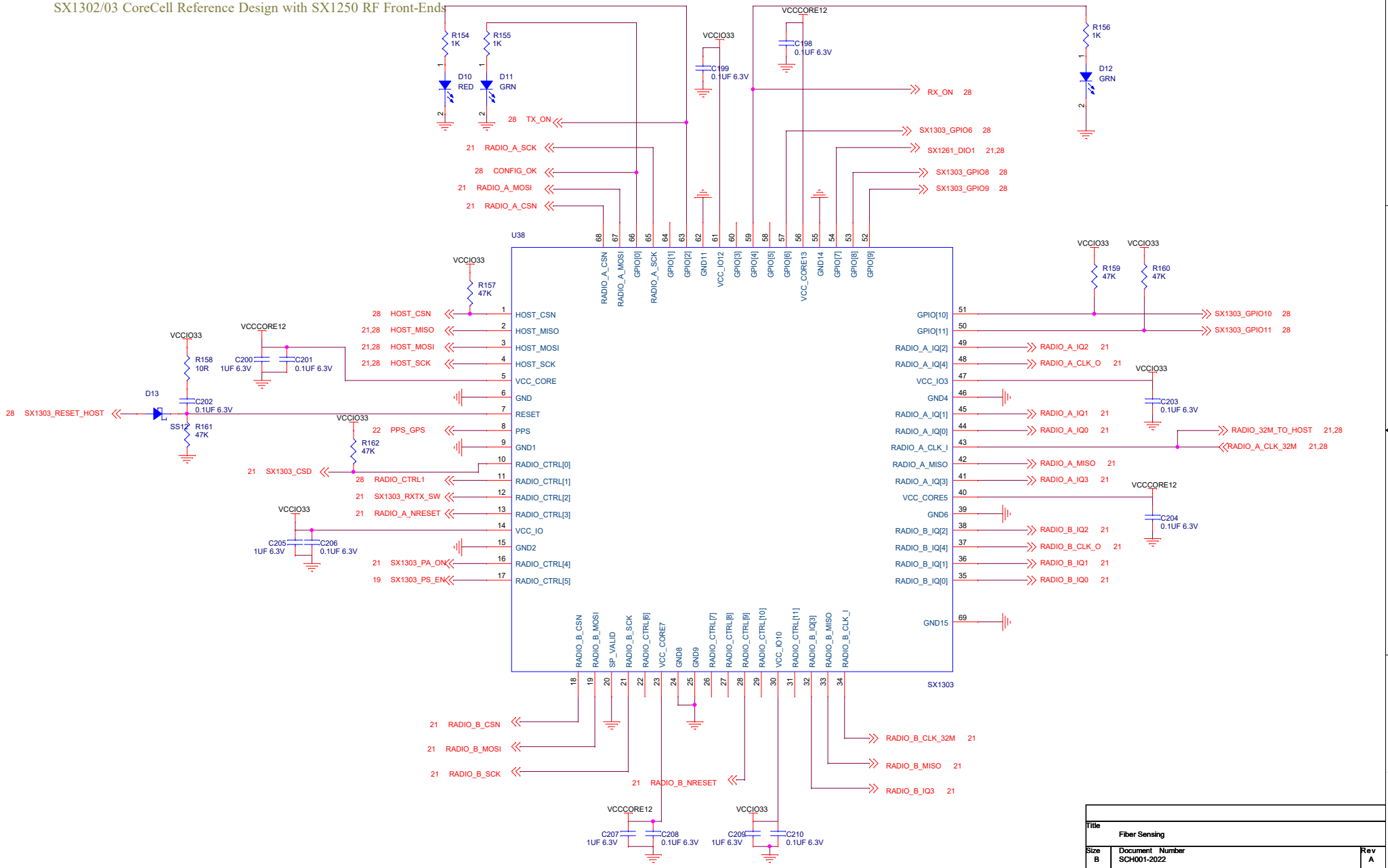


**FORCE TO CONNECT GND AND AGND2**



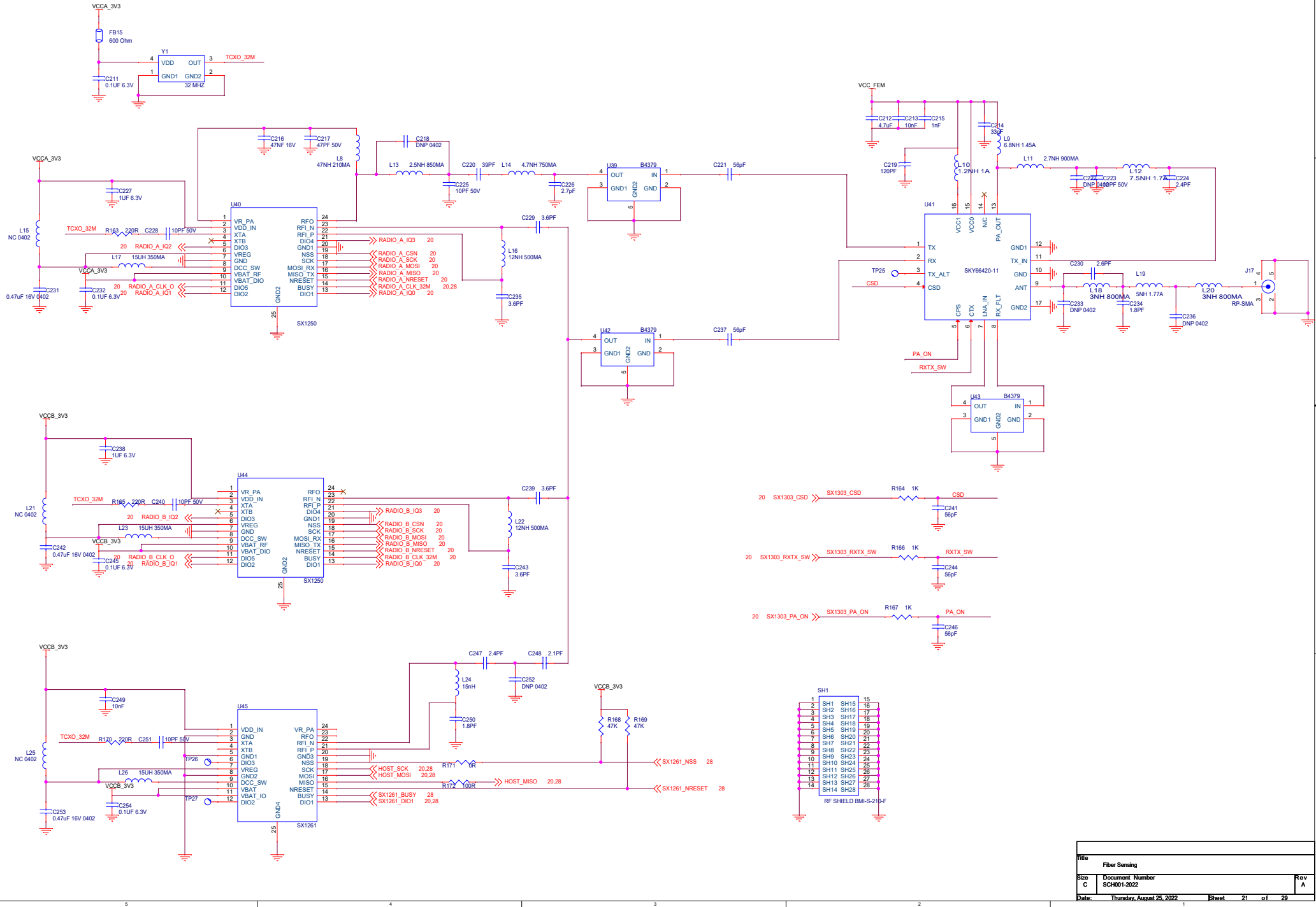
Title		
Fiber Sensing		
Size	Document Number	Rev
B	SCH001-2022	A
Date:	Thursday, August 25, 2022	Sheet 19 of 29

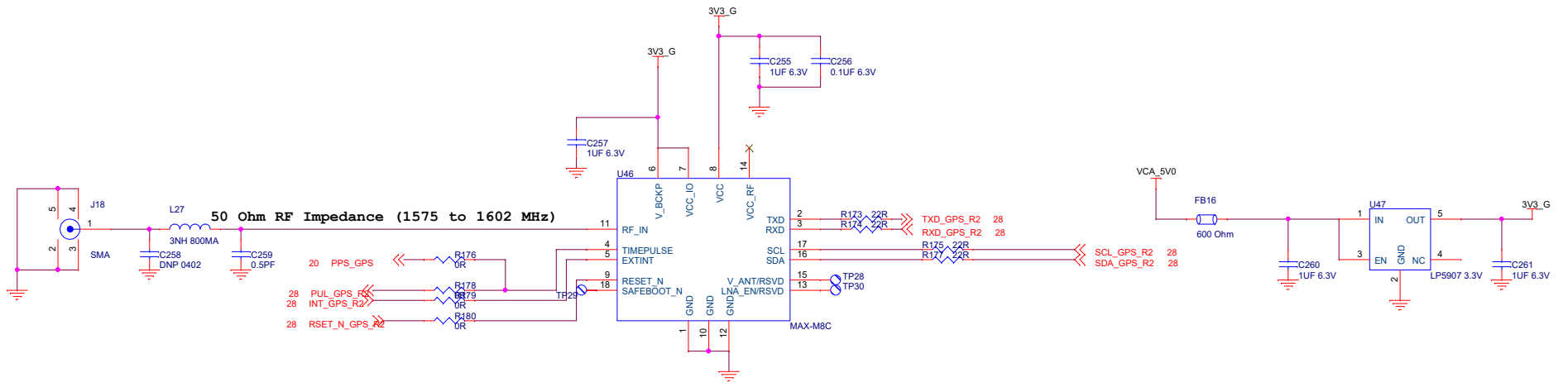
SX1302/03 CoreCell Reference Design with SX1250 RF Front-Ends



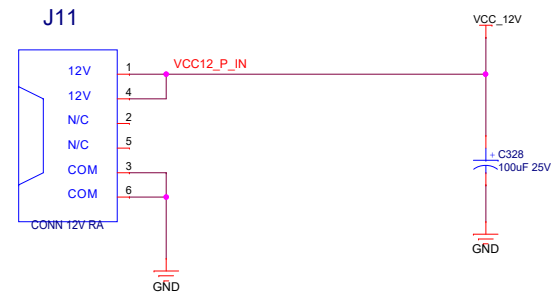
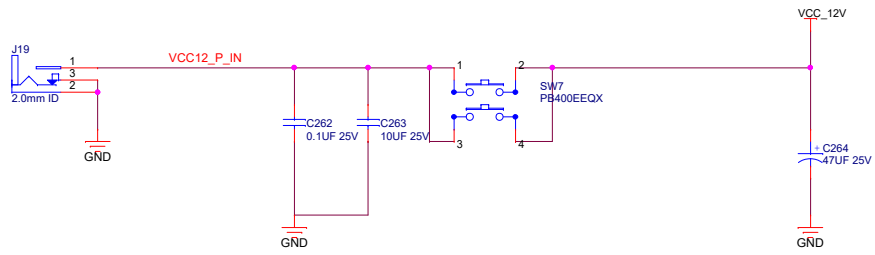
Title		
Fiber Sensing		
Size	Document Number	Rev
B	SCH001-2022	A
Date:	Thursday, August 25, 2022	Sheet 20 of 29

# SX130x CoreCell Reference Design - RF Part with 2x SX1250 RF Front-Ends:

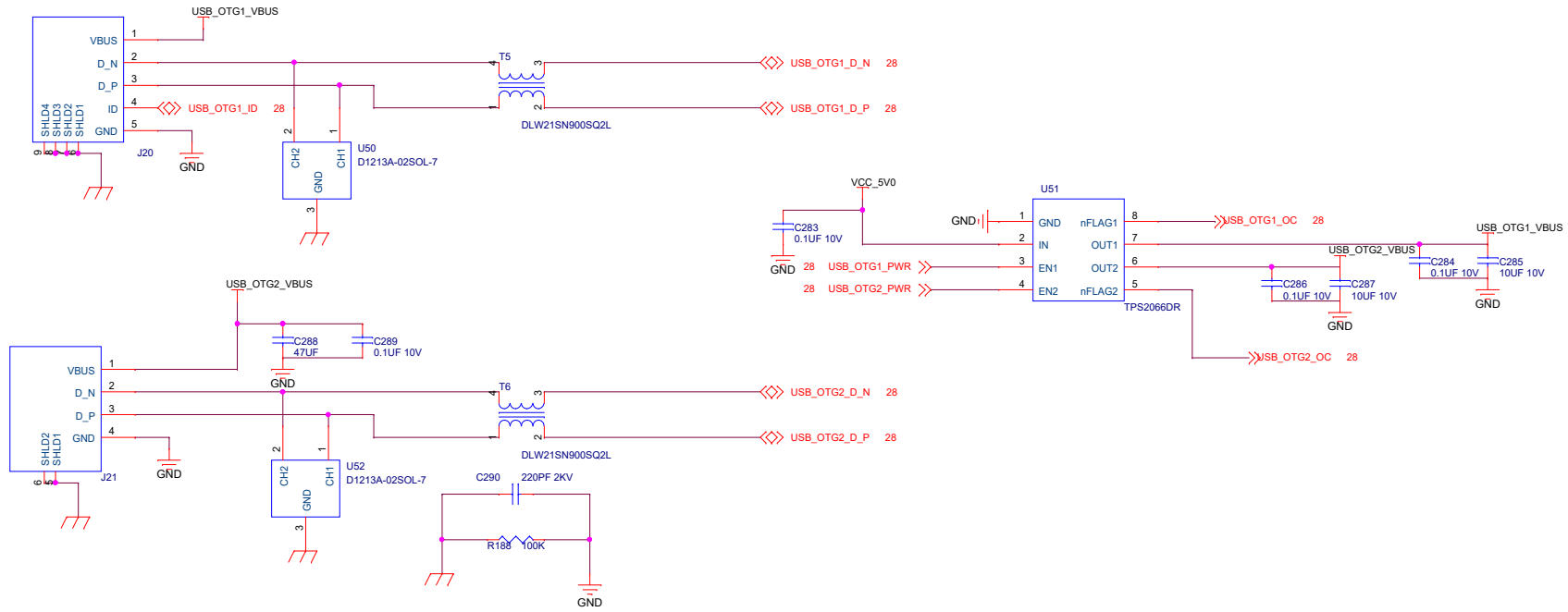




Title			
Fiber Sensing			
Size	Document	Number	Rev
	CustomSCH001-2022		<RevCode>
Date:	Thursday, August 25, 2022	Sheet	22 of 29

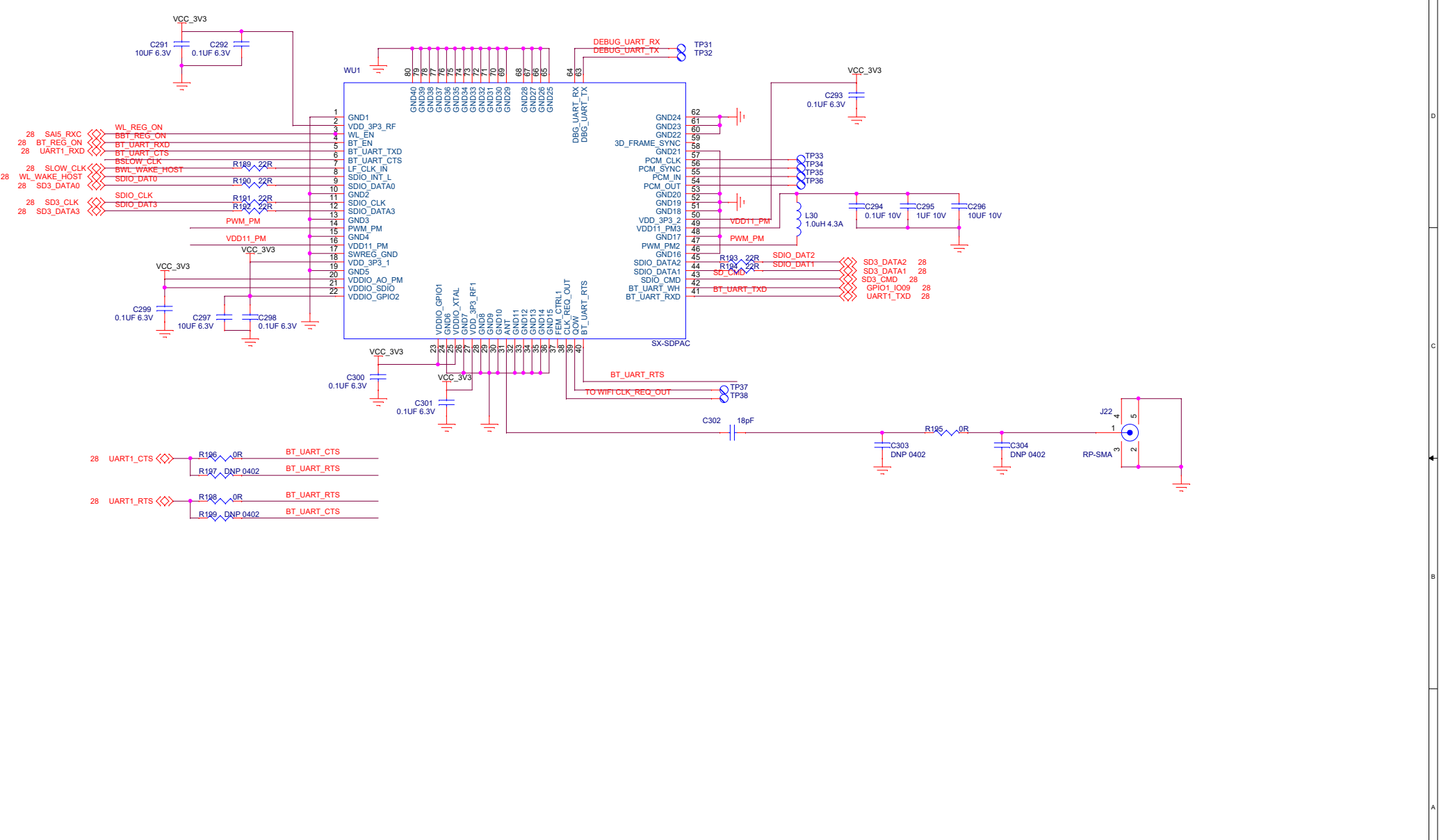


Title			
Fiber Sensing			
Size	Document Number	Rev	
	CustomSCH001-2022	<Rev Code>	
Date:	Thursday, August 25, 2022	Sheet 23 of 29	

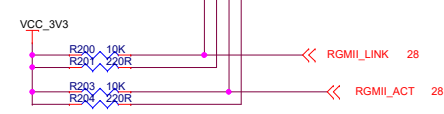
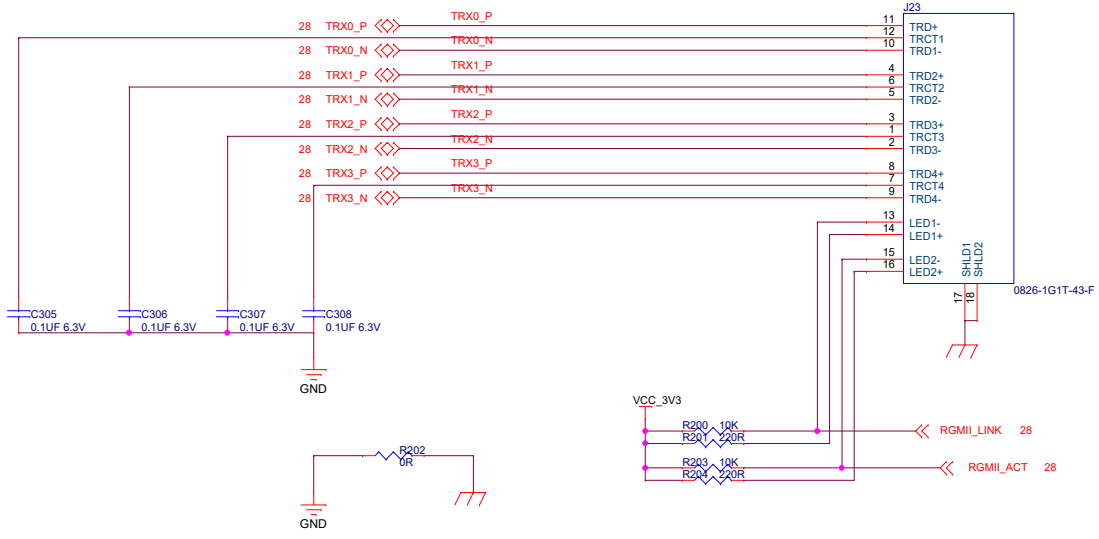
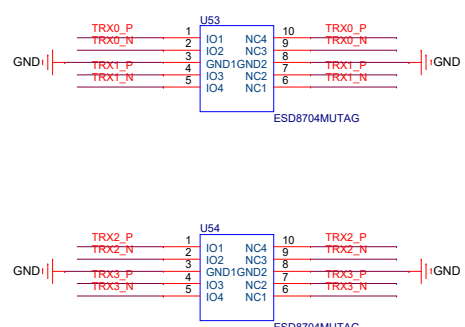


Title			
Fiber Sensing			
Size	Document Number	Rev	
	CustomSCH001-2022	<RevCode>	
Date:	Thursday, August 25, 2022	Sheet	24 of 29

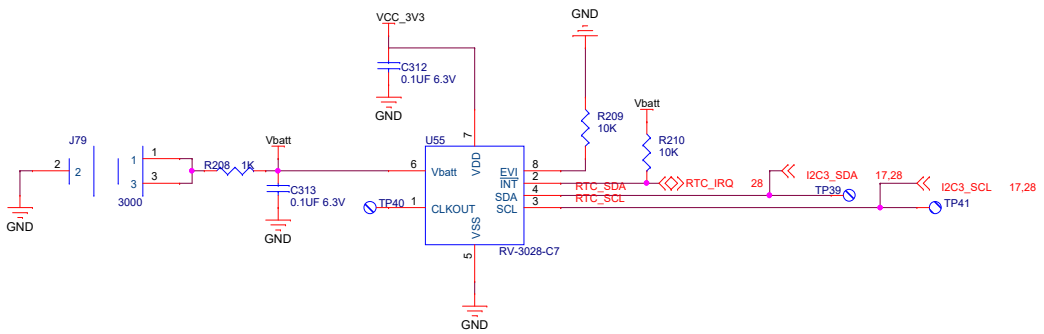
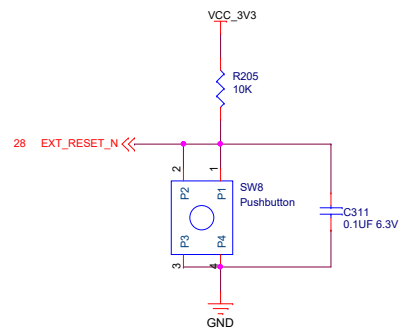
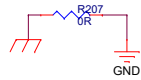
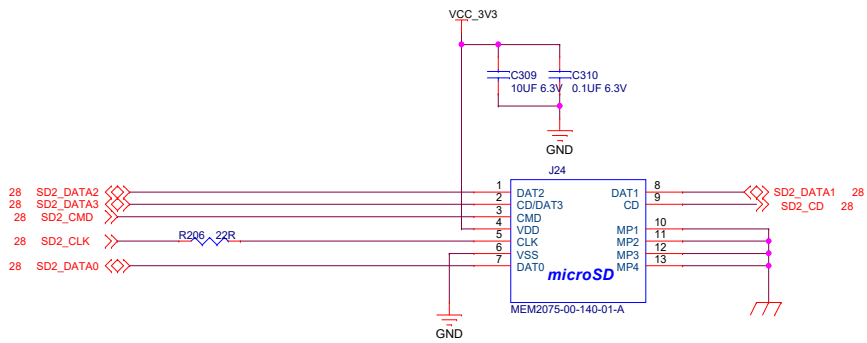




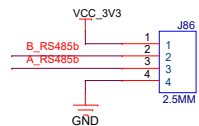
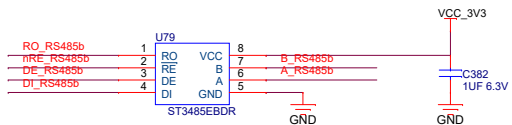
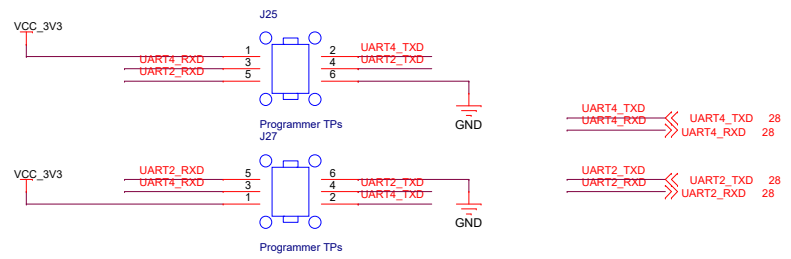
Title		
Fiber Sensing		
Size	Document Number	Rev
	CustomSCH001-2022	<Rev Code>
Date:	Thursday, August 25, 2022	Sheet 25 of 29



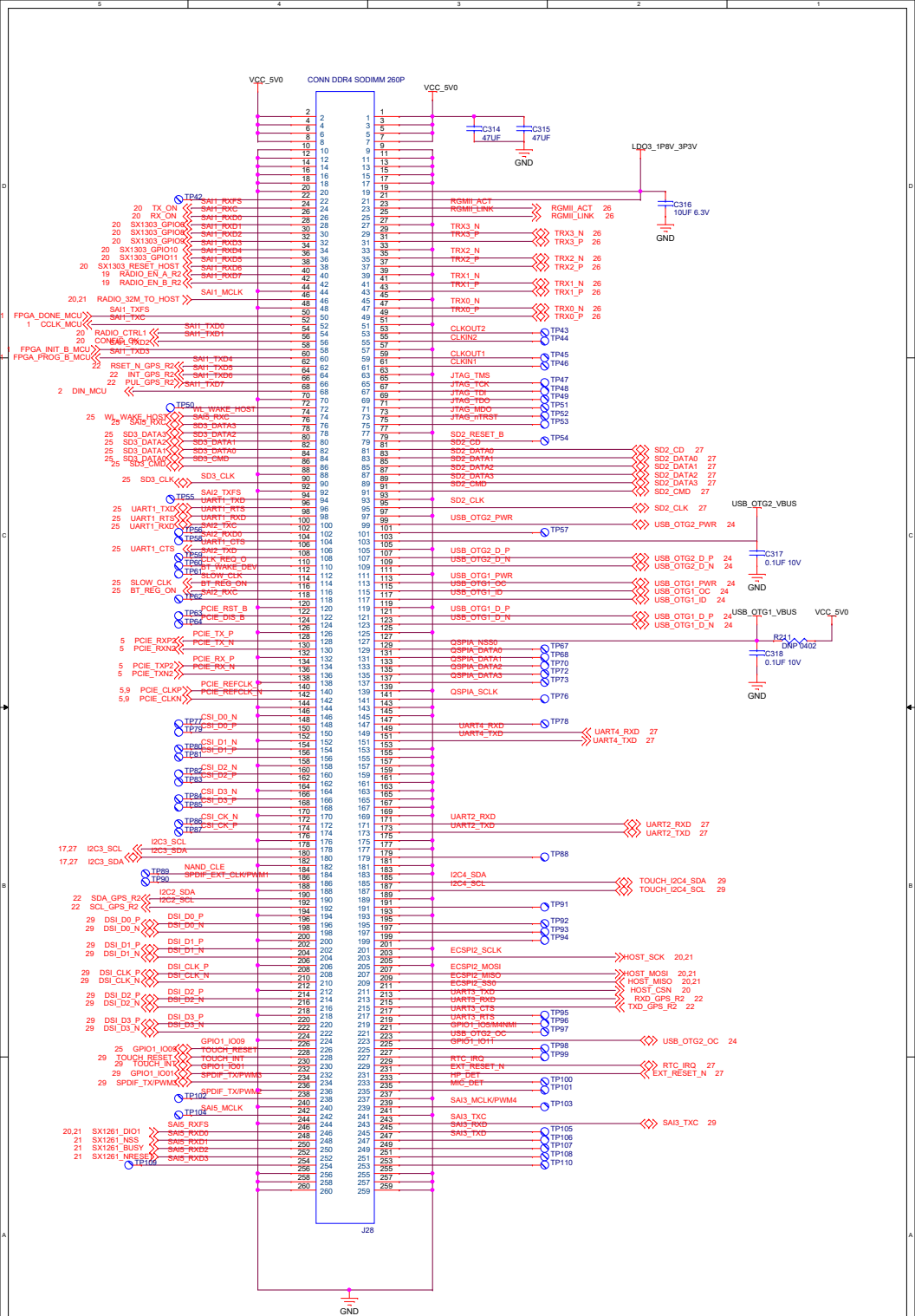
Title			
Fiber Sensing			
Size	Document Number	Rev	
	CustomSCH001-2022	<RevCode>	
Date:	Thursday, August 25, 2022	Sheet	26 of 29

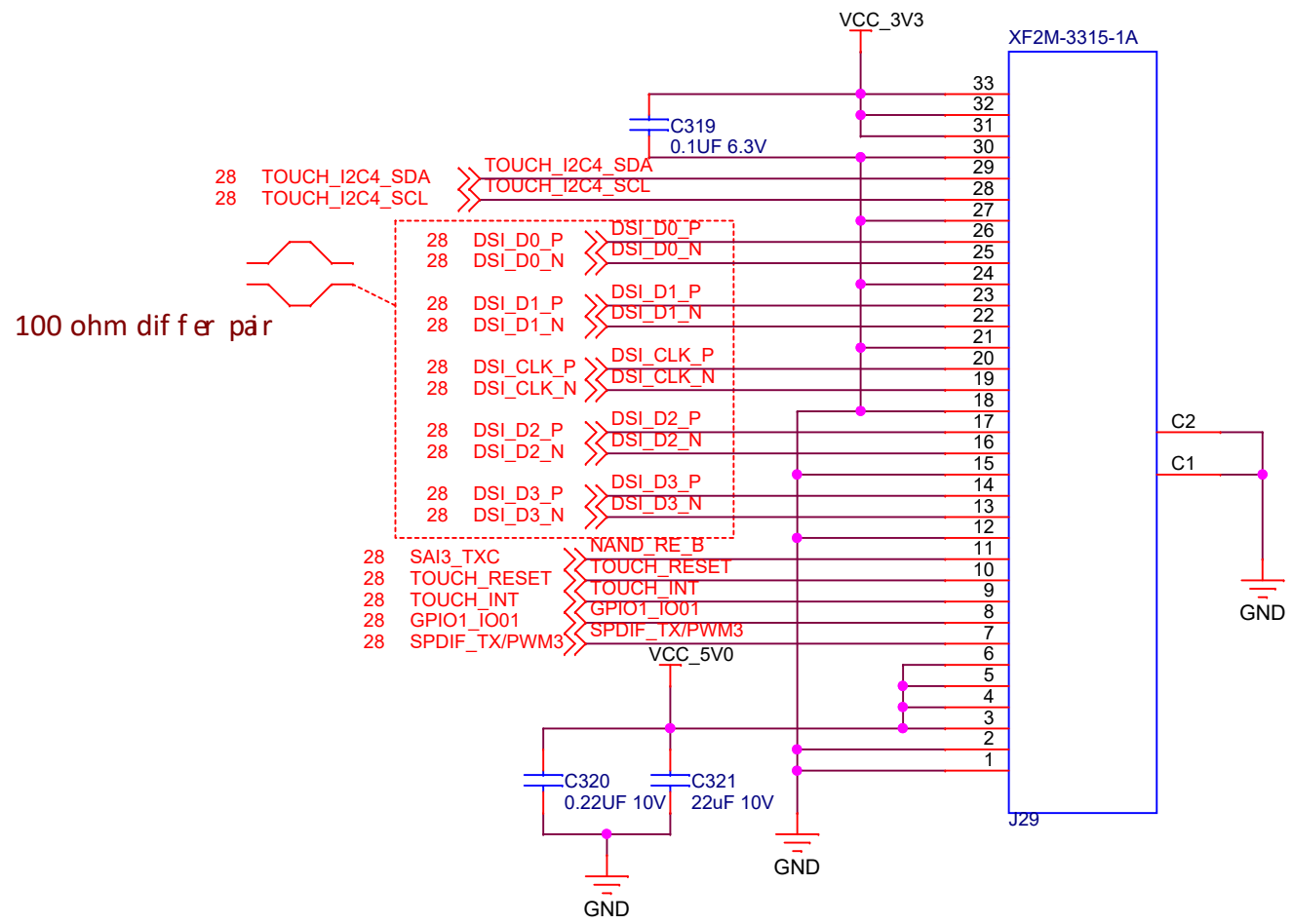


J5 is a flip of J4



Title			Fiber Sensing
Size	Document Number	Rev	
	CustomSCH001-2022	<RevCode>	
Date:	Thursday, August 25, 2022	Sheet	27 of 29





100 ohm differential pair

Title		
Fiber Sensing		
Size	Document Number	Rev
A	SCH001-2022	<Rev Co
Date:	Thursday, August 25, 2022	Sheet 29 of 29