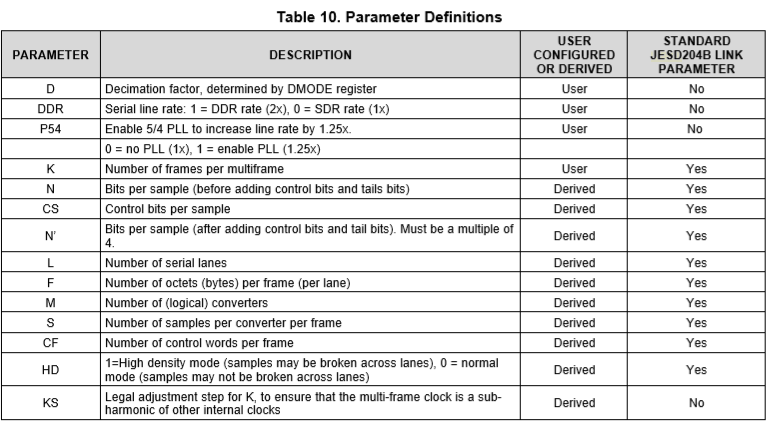
Hardware:

ADC12J1600 + TSW14J10 + KC705

Configuration of ADC12J1600:



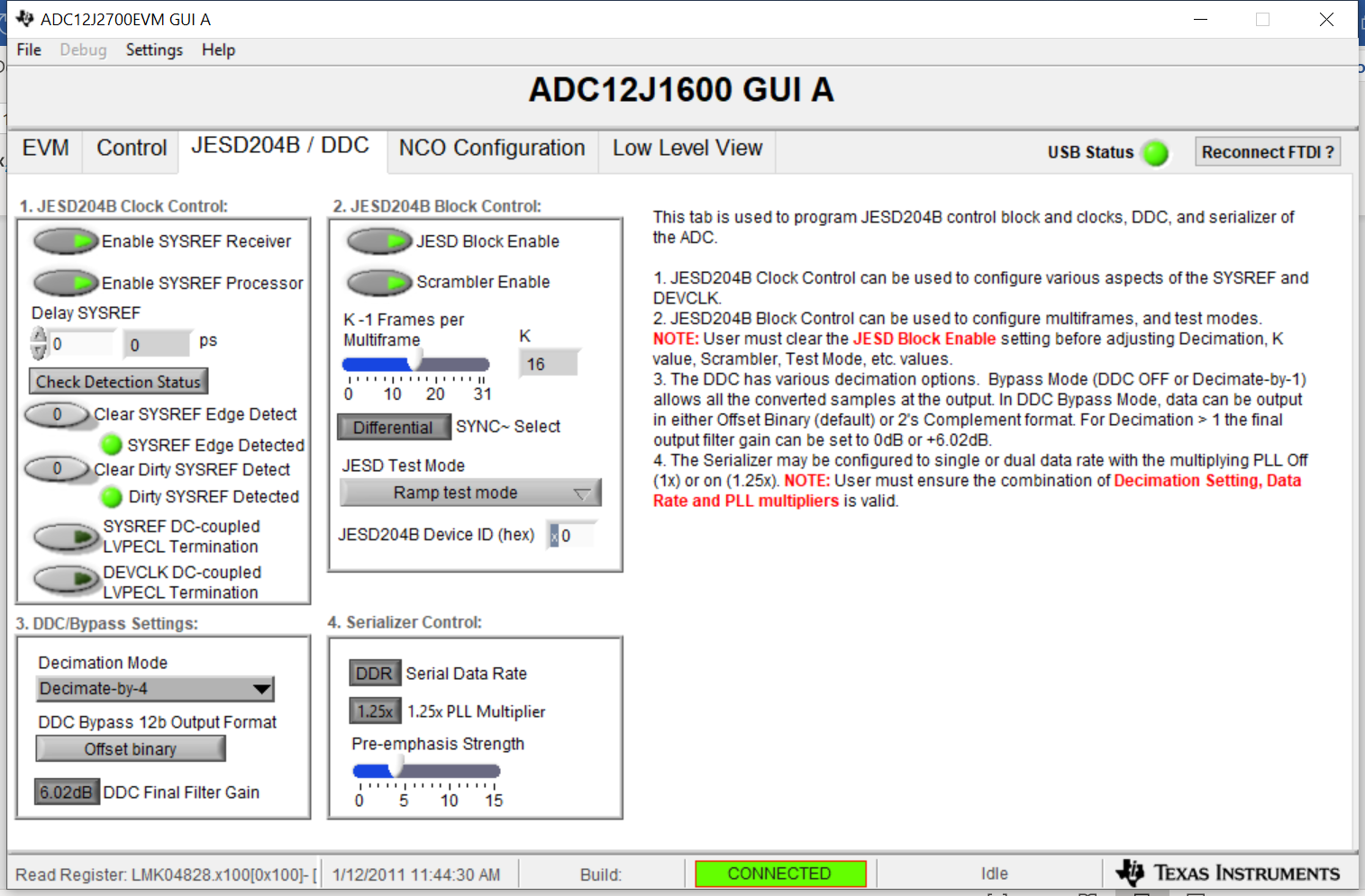
|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Decimation factor(D) | DDR | P54 | N | CS |  | L | F | M | S | K |
| 4 | 1 | 1 | 15 | 1 | 16 | 4 | 2 | 2 | 2 | 16 |

Lane rate = 4GbPS;

Ref Clock = Lane rate/20 = 200MHz;

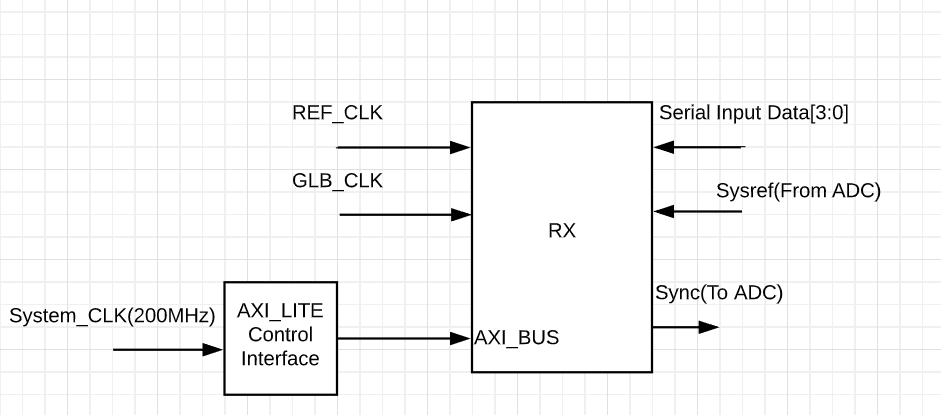
Core Clock(named as global clock in FPGA design) = Lane rate/40 = 100MHz;

Configuration of ADC’s JESD204B for Ramp Test:



In the ramp test mode, the JESD204B link layer operates normally, but the transport layer is disabled and the input from the formatter is ignored. After the ILA sequence, each lane transmits an identical octet stream that increments from 0x00 to 0xFF and repeats.

JESD204B Receiver on FPGA:



AXI Control Register Configuration:

0 => x"8008", -- Addr x008

1 => x"0000", -- Data x0000\_0001 Enable Lane Alignment

2 => x"0001",

3 => x"800C", -- Addr x00C

4 => x"0000", -- Data x0000\_0001 [0] Enable Scrambling

5 => x"0001",

6 => x"8020", -- Addr x020

7 => x"0000", -- Data x0000\_0001 F (octets per frame) = 2

8 => x"0001",

9 => x"8024", -- Addr x024

10 => x"0000", -- Data x0000\_000F K (Frames per multi) = 16

11 => x"000F",

12 => x"8014", -- Addr x014 Tx Only

13 => x"0000", -- Data x0000\_0003 [7:0] ILA multiframes = 4

14 => x"0003",

15 => x"880C", -- Addr x80C Tx Only

16 => x"0000", -- Data x000\_0ABC [15:12] BID = xA [7:0] DID = xBC

17 => x"0ABC", --

21 => x"8818", -- Addr x818 Tx Only

22 => x"0000", -- Data x0000\_1234 [7:0] RES1 [15:8] RES2 [28:24] CF

23 => x"1234",

24 => x"0000",

The writing and reading process of AXI Controller has been checked, the results of Subclass(=01), F(octets per frame), and K(frame per multiframe) are correct.

Debug of interface signals:

The status of several interface signals have been checked by using GPIO LEDS

LED[4] is blinking, showing the FPGA can receive the reference clock and global clock;

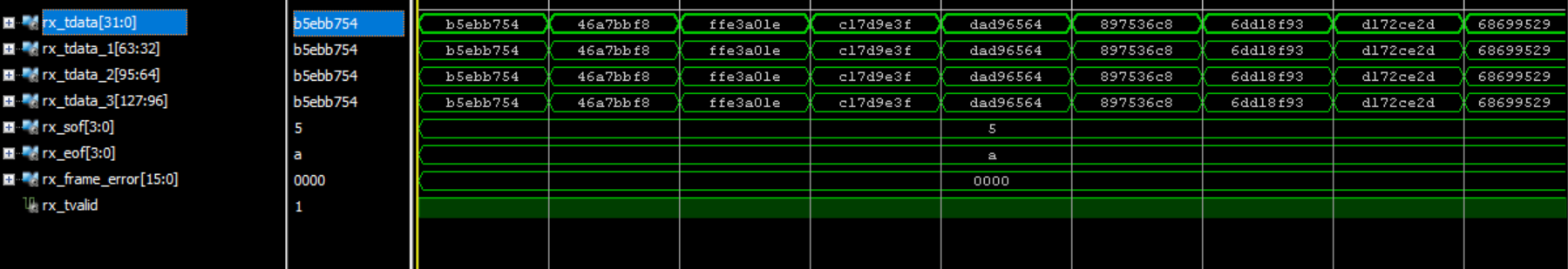
LED[3] is on, showing the system clock is locked, and generating 200MHz clock for AXI Controller;

LED[2] is on, showing the JESD204B receiver can generate RX\_aresetn signal, which serves as the reset signal for data demapping block;

LED[1] is on, showing the tx\_resync is asserted, which is sent out to ADC;

LED[0] is on, showing the rx\_resync is asserted, which is the synchronizing signal generated by the receiver;

Captured data from ILA:



The data from 4 lanes are exactly same, which is reasonable since the ADC are sending identical octet stream to each lane. However the value of the captured data is incorrect for now.

The configuration of JESD204B Receiver on FPGA:



