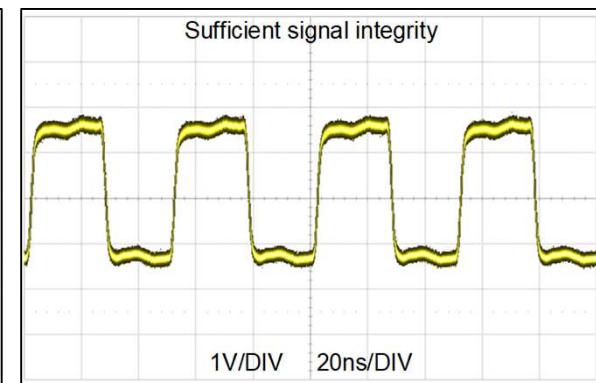
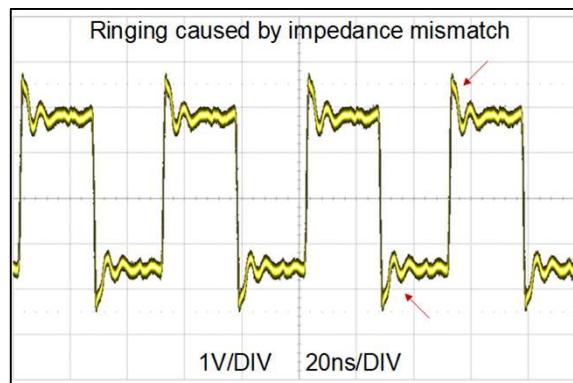
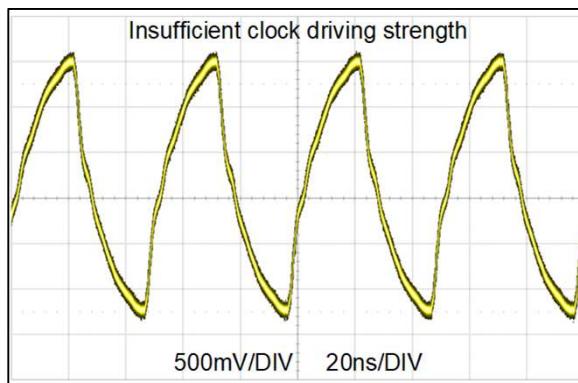
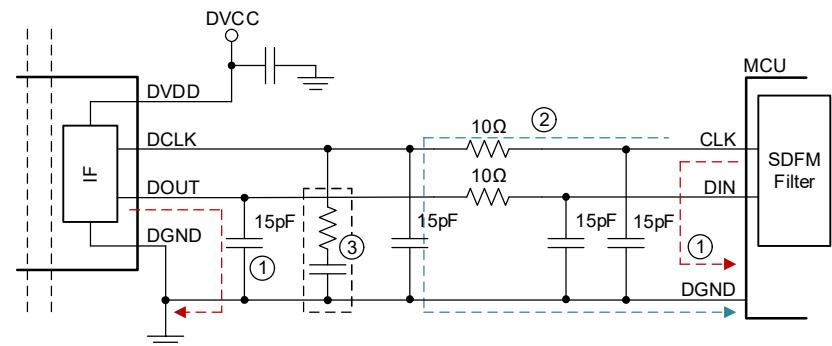


Delta-sigma filter – clock & data signal integrity

- Capacitor (1) reduces slew-rate on the logic gate level
- RC-Filter (2) further reduces slew-rate and HF EMI content
- AC-termination (3) might be necessary



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