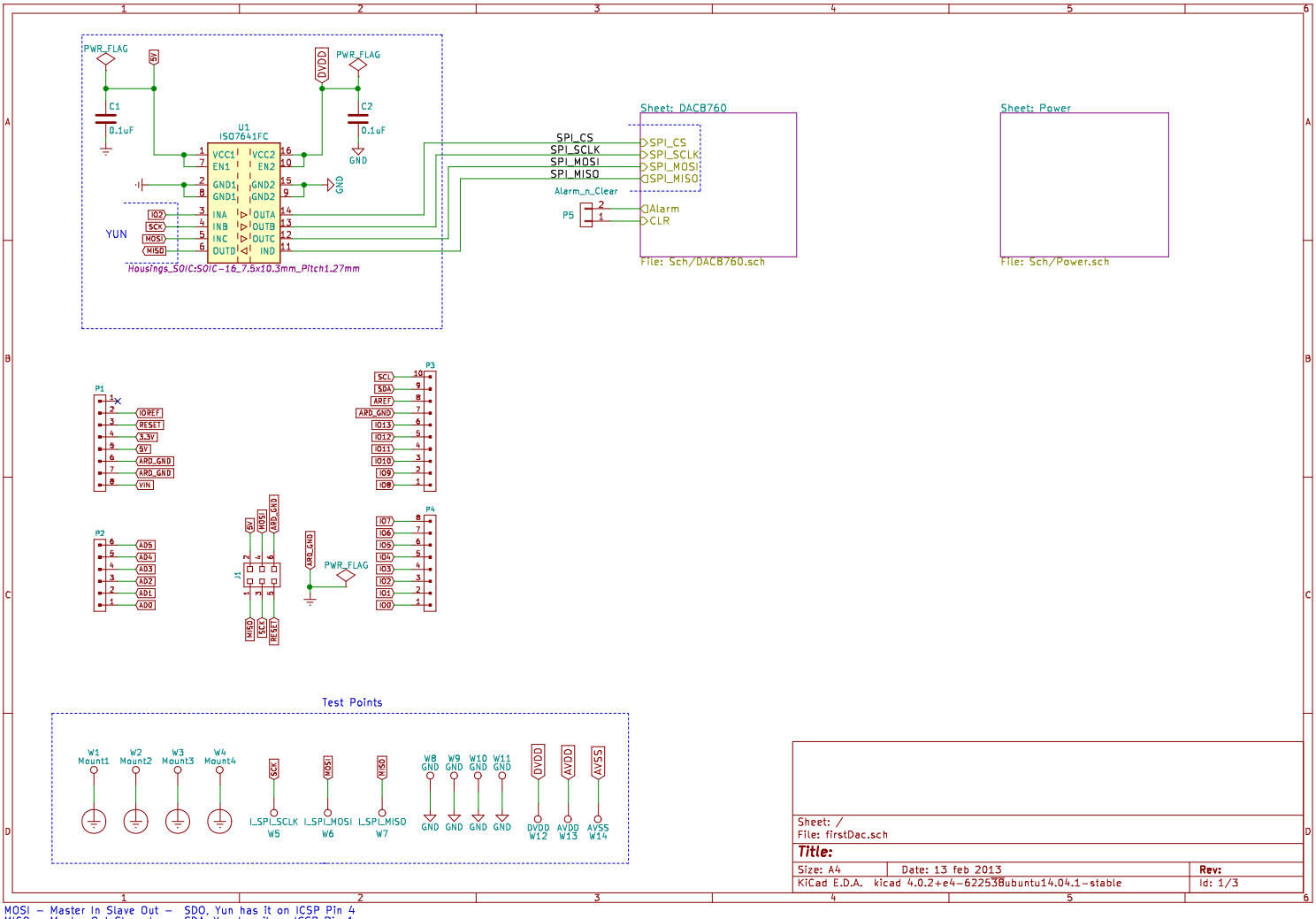
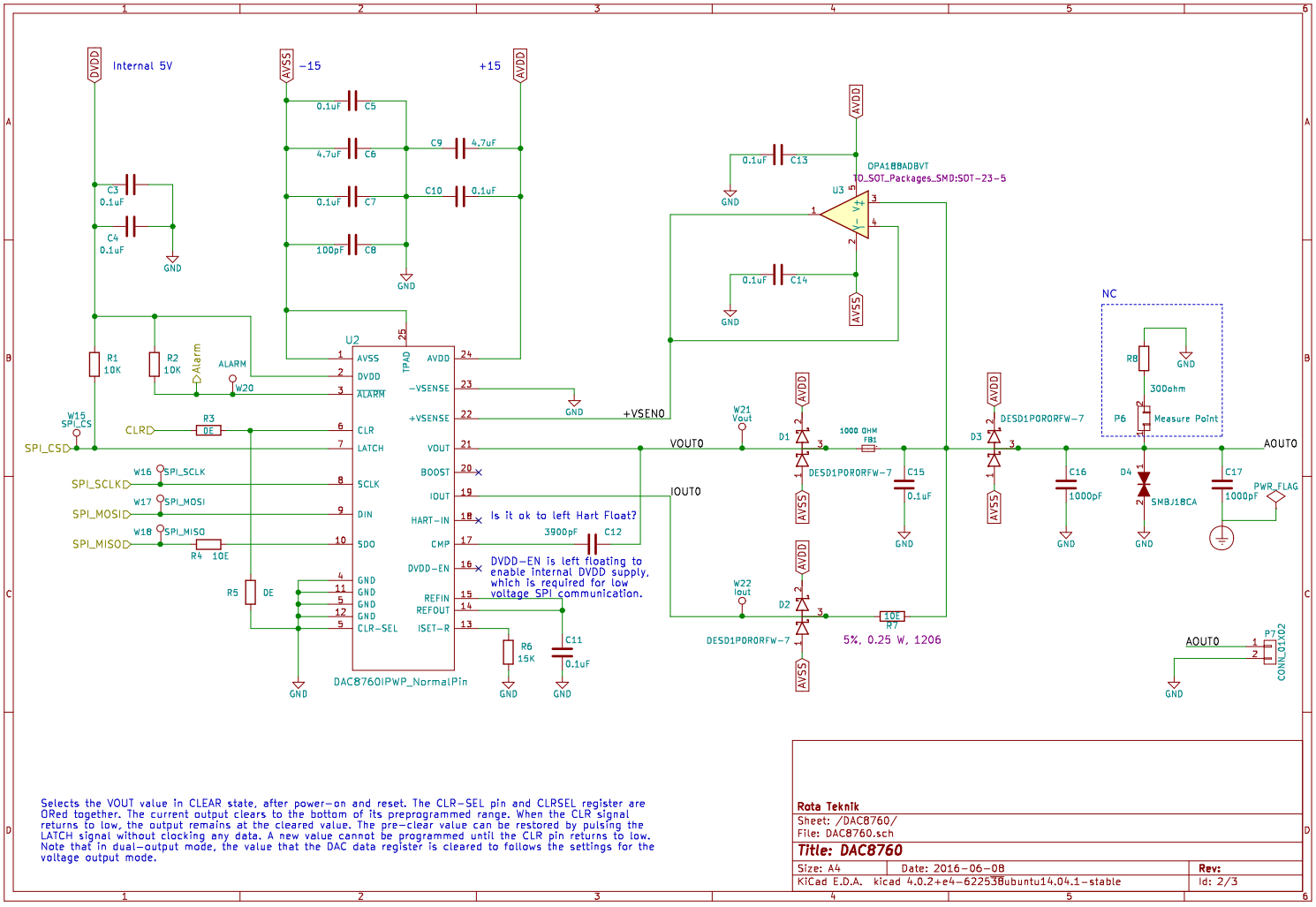



MOSI – Master In Slave Out – SDO, Yun has it on ICSP Pin 4
MISO – Master Out Slave In – SDA, Yun has it on ICSP Pin 1
SCK – Serial ClocK – SCL, Yun has it on ICSP pin 3
SS – Slave Select – CS (Chip Select), Yun has no dedicated pin, use any digital data pin




Selects the VOUT value in CLEAR state, after power-on and reset. The CLR-SEL pin and CLRSEL register are ORed together. The current output clears to the bottom of its preprogrammed range. When the CLR signal returns to low, the output remains at the cleared value. The pre-clear value can be restored by pulsing the LATCH signal without clocking any data. A new value cannot be programmed until the CLR pin returns to low. Note that in dual-output mode, the value that the DAC data register is cleared to follows the settings for the voltage output mode.

| | | |
|---|---|---|
| **Rota Teknik** | | |
| Sheet: /DAC8760/ | | |
| File: DAC8760.sch | | |
| ***Title: DAC8760*** | | |
| Size: A4 | Date: 2016-06-08 | **Rev:** |
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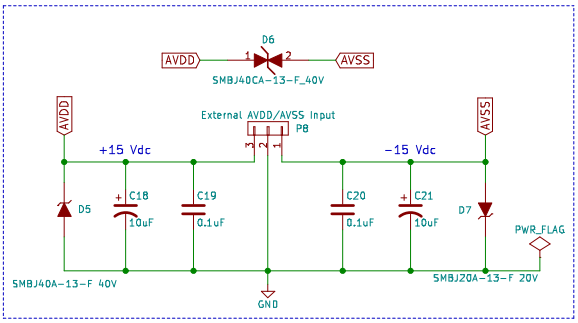


Rota Teknik

Sheet: /Power/

File: Power.sch

**Title: DAC8760**

| Size: A4 | Date: | Rev: |
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