Application Report
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Passive Terminations for Current Output DACs

Ken Chan *Wireless Infrastructure*

ABSTRACT

The correct implementation of the high-speed DAC output termination is critical to achieving the best possible performance. The typical application involves choosing the correct network to create the necessary dc bias levels and correct effective impedance load to keep the output voltage within the compliance levels. This ensures that the maximum output signal amplitude and optimum ac performance characteristics are achieved. The passive resistive termination to a modulator with equal and unequal bias levels are explored with various examples looking at the requirements for current source and current sink outputs.

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1 Introduction

For current output digital-to-analog converters (DAC), the amplitude of the output voltage depends on the output load impedance with a V=IR relationship. A larger amplitude voltage can be generated if a larger resistor is used. Considerations must be made, however, not to exceed the maximum voltage on the output current pins to ensure that the part is operating within the specified operating conditions and maximum compliance voltages.

The output stage of a current-steering DAC is not ideal for interfacing directly to other 50-Ω interfaces and usually requires some interface circuitry. This type of DAC output can either be a current sink or source architecture. Figure 1 and Figure 2 illustrate a current source and current sink output. The S(n) are the control signals generated from the DAC bits.

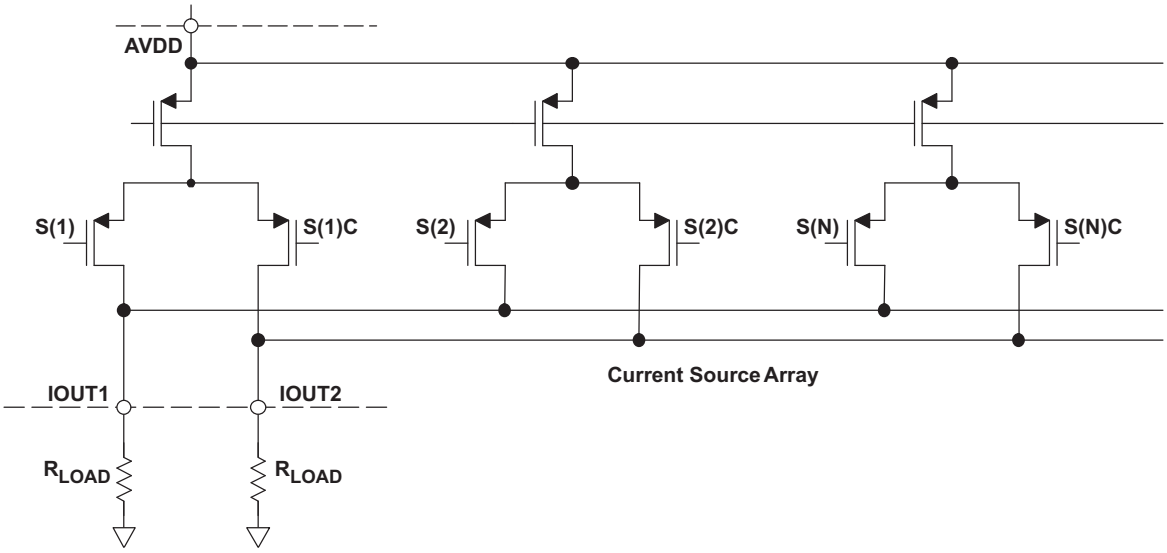

Figure 1. Current Source Output DAC56x2/DAC5674

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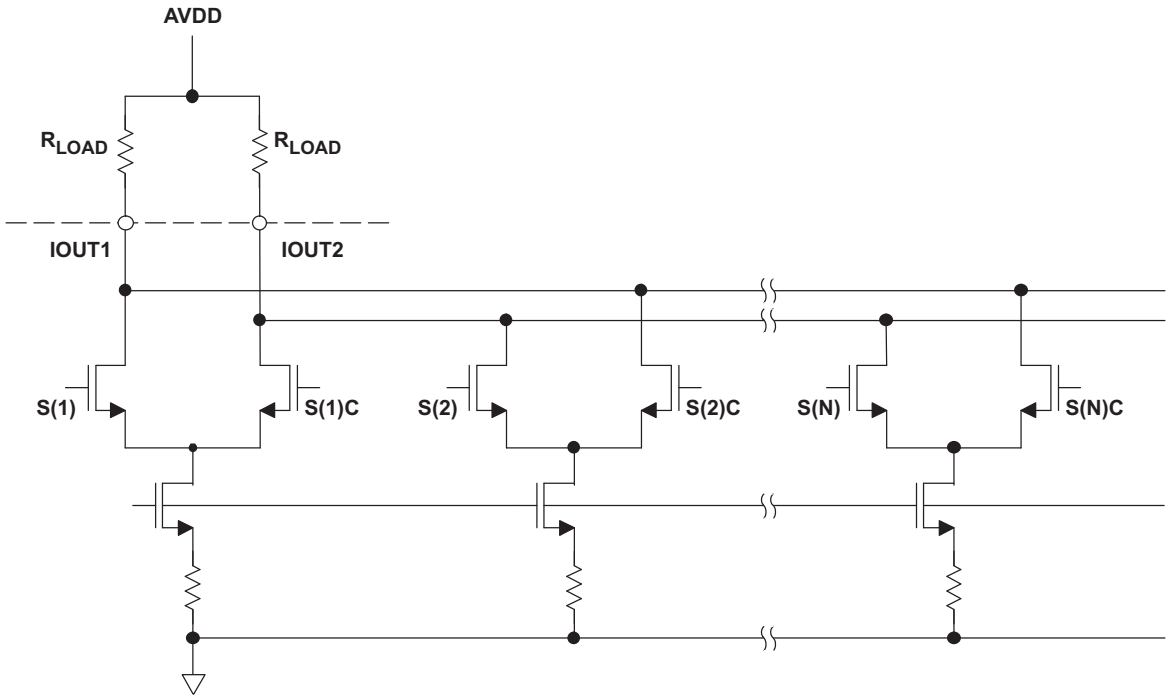

Figure 2. Current Sink Output
DAC5675A/5686/5687/5688/5682Z/5681Z/5681

Normally, some external termination/network is required for a proper interface to a 50-Ω system while providing the necessary bias voltages. This external network can consist of a resistive termination resulting in two single-ended signals that then can be buffered and impedance-matched through a single-ended or differential amplifier. The network also can consist of a resistive termination, followed by an impedance ratio transformer to perform the differential-ended (DE) to single-ended (SE) conversion. This application report covers the passive interface to a resistive or transformer termination and the passive interface to an IQ modulator.

The use of the passive transformer and output termination resistor allows the user to choose the appropriate combination to meet signal amplitude, biasing, and impedance-matching requirements.

2 Current Source Architectures

The equivalent circuit of this output can be represented as a current source controlled by the bits of the DAC. Each bit causes the current source to switch out a fixed amount of current. This kind of output requires that the output termination on IOUTA and IOUTB offers a path to ground.

2.1 Single-Ended Unbuffered Output, No Transformer Required

Singled-ended output can be used to drive a 50-Ω, doubly terminated cable through one of the differential outputs. In this case, one side of the complementary output is terminated by 50 Ω and then connected to a cable and a 50-Ω load. The other complementary output is connected to 25 Ω to create a balanced system. In this way, the differential voltage between IOUT and its complement is 1 Vpp for 20-mA, full-scale current output. However, only the single-ended voltage of 0.5 Vpp appears on the cable and load. This architecture is not recommended for applications where the third harmonics are of concern. The differential outputs are necessary for suppression of the third harmonics created by the current switches. It is generally recommended that the DAC outputs always be used in a differential manner until they have gone through a conversion from DE to SE.

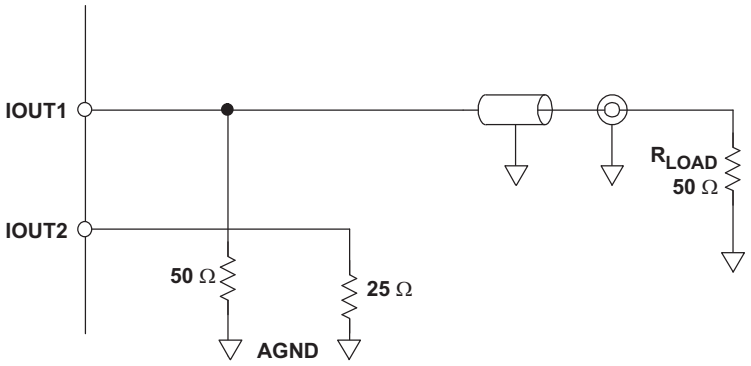

Figure 3. Single-Ended Termination in for Current Source Output Driving 50 Ω, DAC5672/DAC5674

2.2 Driving Doubly Terminated, 50-Ω Cable Using 1:1 Impedance Ratio Transformer

This configuration can be used to create a SE signal from the DE output and connect to a 50-Ω load such as a spectrum analyzer. The middle of the primary turn of the transformer must be grounded to allow a path for the dc current to flow. By analyzing the equivalent impedance at the IOUT complementary terminals, it is possible to determine the output voltage level of the ac signal.

The 50-Ω load is transformed to the primary side by the impedance ratio to be 50 Ω across the primary. However, the primary is grounded in the middle and splits the 50 Ω into 25 Ω to ground on each side.

The 100 Ω between the IOUT complementary terminals also appears to have a virtual ground point in the middle for ac signals, and can be thought of as having 50 Ω to ground from each IOUT complementary terminal for ac signals. This is important in determining the ac load and the resulting ac amplitude.

Considering all these ac equivalent impedances, the effective impedance is 50//50//25 or 12.5 Ω.

With a 20-mA, full-scale current, this results in 0 to 250 mVp on the IOUT terminals. This is well within the compliance voltage of the DAC5672 (–1 V to 1.2 V) and the DAC5674 (–1 V to 1.25 V). This results in a differential voltage on the primary and secondary side of the transformer of 500 mVpp. Keep in mind that the impedance ratio (Zp/Zs) is the square of the turns ratio (Np/Ns) or voltage ratio. For a 1:1 impedance ratio transformer, the voltage ratio is also 1:1.

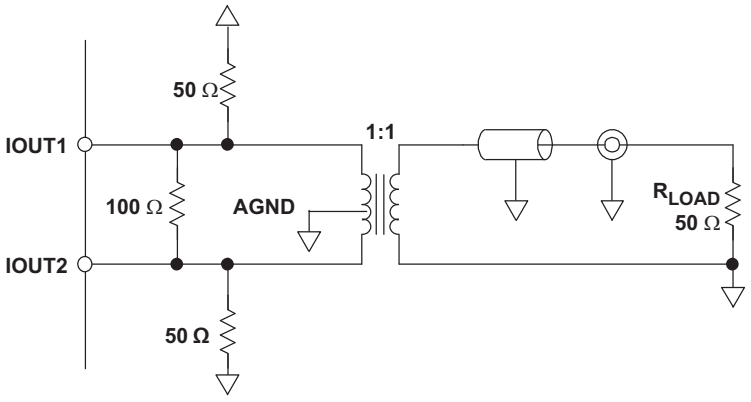

Figure 4. Driving Doubly Terminated 50-Ω Cable Using 1:1 Impedance Ratio Transformer, DAC5672/DAC5674

2.3 Driving a Doubly Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer, 2:1 Voltage Ratio

This configuration also can be used to connect the differential outputs to a single-ended, 50-Ω terminated cable. The middle of the primary coil is grounded to provide a path for the dc current to flow. In this case, the 50 Ω on the secondary looks like 200 Ω on the primary, and with the ground point in the middle of the coil, effectively looks like 100 Ω to ground.

This 100 Ω in parallel with the IOUT termination of 100 Ω results in an equivalent of 50 Ω connected to each of the complementary IOUT terminals. With a 20-mA, full-scale current output, this results in 0 to 1 Vp which is within the compliance voltages of the DAC5672/74. This corresponds to 2 Vpp across the complementary IOUT terminals. Taking into account the 4:1 impedance ratio transformer (2:1 voltage ratio), the output on the secondary side of the transformer and on the output 50-Ω load is 1 Vpp.

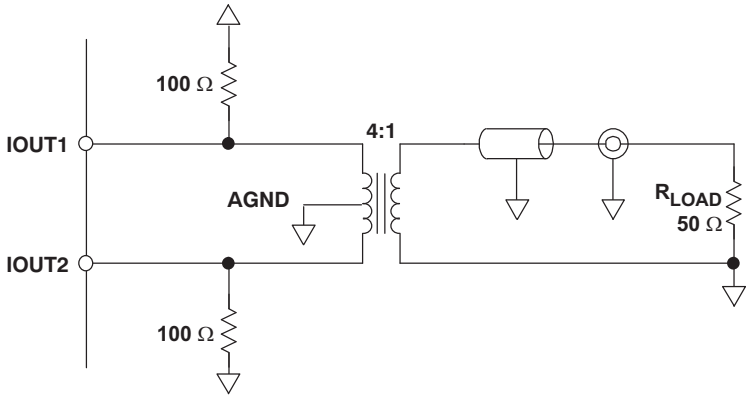

Figure 5. Driving Doubly Terminated 50-Ω Cable Using 4:1 Impedance Ratio Transformer DAC5672/DAC5674

Although the 4:1 impedance transformer gives a 2x or 6-dB larger signal, the 1:1 impedance transformer generally results in slightly better distortion.

3 Current Sink Architecture

This architecture has an equivalent circuit that looks like a current sink with the DAC bits as control switches. This kind of output requires that the IOUT terminations have a path to AVDD to provide the current for the current sinks.

3.1 Single-Ended Output, No Transformer Required

The outputs of the current sink DAC can be terminated in a resistive network as long as the compliance voltages of the DAC output are maintained. For the DAC5686/5687, which has a compliance voltage of AVDD ±0.5 V, the following network can be used to interface to a high-impedance circuit. This network has an equivalent ac impedance of 50 Ω. Some care must be taken when determining the resistor network required to provide the correct dc bias as well as providing the desired ac impedance and resulting ac signal level. The average dc current sink into the device must be considered (in this case, 10-mA average current) in determining the value of the two resistors. An Excel™ spreadsheet is available which solves the necessary network equations to determine the correct resistor network to meet load and bias requirements for a given current setting.

If the network is just considered as a voltage divider, it will be incorrect, resulting in incorrect biasing, which will give poor results at the least, and damage the device at the worst.

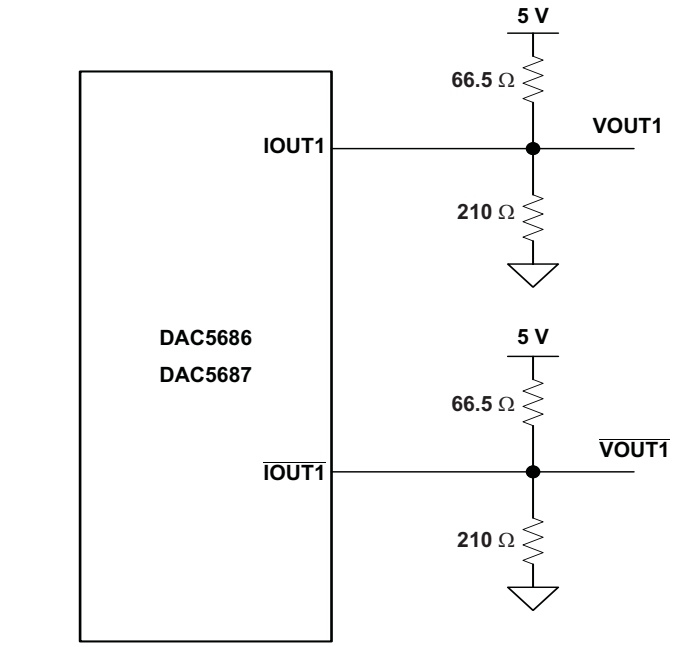

Figure 6. Single-Ended Termination Output to Meet Compliance Voltage of DAC5686/87/88/82/81

This results in a 1-Vpp signal centered on 3.3 V or 3.3 V ±0.5 V which is the compliance voltage of the DAC5686/87/88/82 IOUT terminals.

The DAC5675A has compliance voltages AVDD -1 V to AVDD +0.3 V and requires a different termination network to take advantage of the full-scale, 20-mA current. A resistor combination of 70 Ω and 175 Ω yields minimum and maximum swings of 2.57 V and 3.57 V. This is within the compliance voltage of the DAC5675A. Operational amplifiers or buffer circuits can be used after the resistor network to drive a load.

3.2 Driving a Doubly Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer

Current sink outputs can be easily configured to drive a 50-Ω system using a transformer. This configuration is similar to the current source configuration, except that all the grounds on the interface network are replaced by AVDD. The same logic applies for the resistors and transformers and results in an equivalent 50//50//25=12.5 Ω from AVDD to the current sink terminals. This results in 250 mVp on each terminal and 500 mVpp on the primary side of the transformer. Again, the 1:1 impedance and corresponding 1:1 voltage ratio produces a 500-mVpp, single-ended signal on the primary side of the transformer.

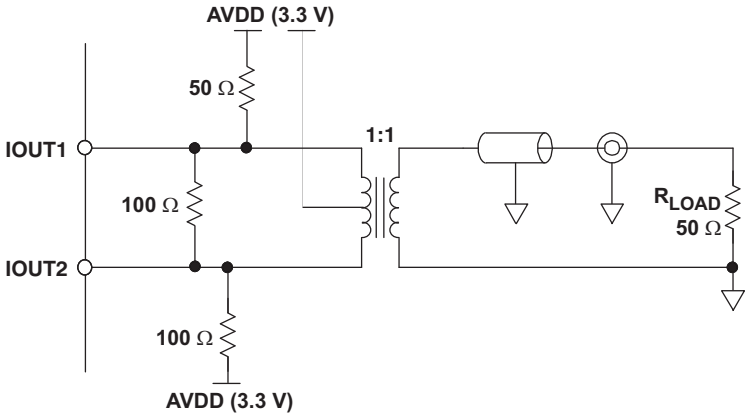

Figure 7. Driving a Doubly Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer, DAC5686/87/88/82, and DAC5675A

This configuration can be used for the DAC5686/87 because the compliance voltages for these parts are AVDD ±0.5 V. The DAC5675A also can use this 1:1 configuration as its voltage compliance limits are AVDD -1 V to AVDD +0.3 V.

3.3 Driving a Doubly Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer

This configuration is similar to the 4:1 impedance ratio configuration for the current source outputs. The ground terminations on the resistor and transformer network are instead connected to AVDD. The effective impedance on each IOUT terminal is 50 Ω to AVDD. This results in a 1-V drop at the IOUT terminals causing a differential voltage on the primary side of the transformer of 2 Vpp. The 4:1 impedance ratio transformer has a voltage ratio of 2:1 and results in a 1-Vpp signal on the secondary side of the transformer, driving the load.

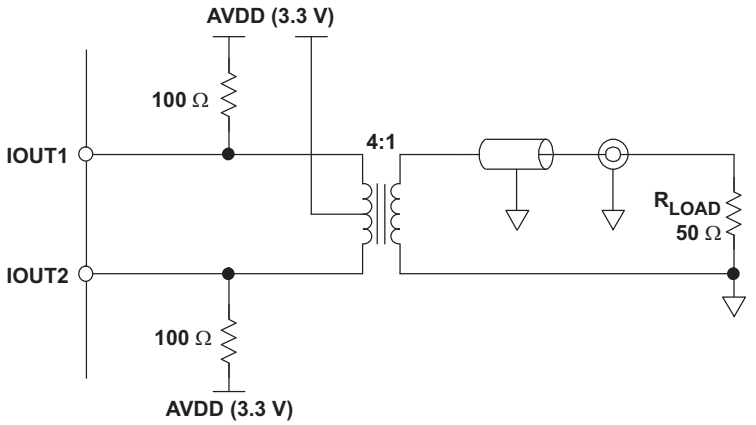

Figure 8. Driving a Doubly Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer, DAC5686/87/88/82

This configuration works well for the DAC5686, DAC5687, DAC5688, DAC5682Z, DAC5681Z, and DAC5681. The 3.3-V center tap keeps the dc common mode of the IOUT terminals at 3.3 V with the ac deviation of 1 Vpp centered on 3.3 V. This allows the primary differential voltage to be 2 Vpp and produces a 1-Vpp voltage on the secondary side of the 4:1 impedance ratio or 2:1 voltage ratio transformer.

However, this configuration is not suited for the DAC5675A due to its voltage compliance limitation of AVDD -1 V to AVDD +0.3 V. The AVDD ±0.5 V exceeds the upper compliance limit. In this case, a resistor can be placed inline with the center tap voltage. For the DAC5675A, a 15-Ω resistor on the center tap causes the center tap voltage to drop down to 3 V. This ensures that 3 V ±0.5 V does not exceed the DAC5675A compliance limits of AVDD -1 V to AVDD +0.3 V.

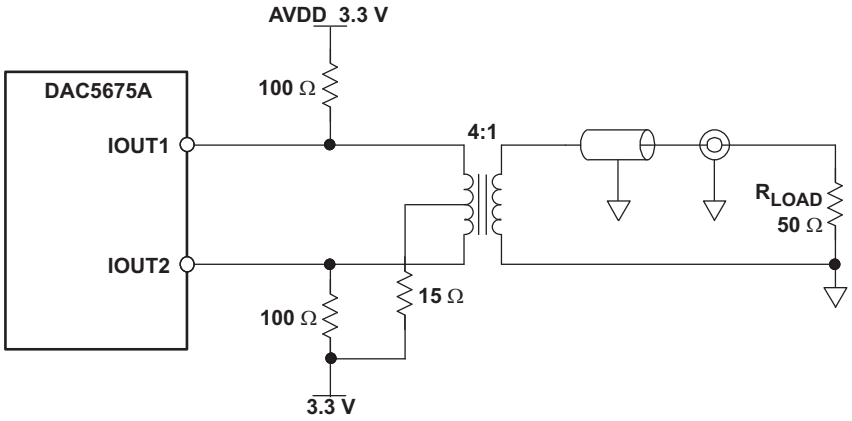

Figure 9. Driving a Doubly Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer, DAC5675A

4 Interfacing a Current Output DAC to an IQ Modulator

4.1 Current Sink DAC5686/5687/5688/5682Z/5681Z/5681 Passive interface to an IQ Modulator

A common application for the DAC5686, DAC5687, DAC5688, DAC5682, and DAC5681 is to interface them to an IQ modulator like the TRF3703 family of modulators from Texas Instruments. The input of the modulator is generally of high impedance compared to the 50-Ω load. A specific common-mode voltage is generally required. A resistive network can be used to maintain a 50-Ω load impedance for the DAC, keep the IOUT signal level within the DAC output compliance voltages, and also provide the necessary common-mode voltage for the DAC and modulator.

In all the following examples, IQ amplitude, phase, and dc correction are not affected and allow for correction of the sideband and LO feedthrough, phase, and dc offset between the IQ signal paths. Also, the examples typically use a low-pass filter to attenuate DAC output images before they go into the IQ modulator. For band-pass filters, a pullup network on the modulator side is needed to replace the filter termination and provide the modulator with its required common-mode voltage.

4.1.1 Interfacing the TRF3703-17 to the Current Sink DAC

The TRF3703 IQ modulator family can be operated at three common-mode voltages: 1.5 V, 1.7 V, and 3.3 V. The common-mode voltages of the modulators must be reconciled with the common-mode voltage of the DAC that is driving the modulator. A typical application involves connecting the 3.3-V, common-mode DAC like the DAC5687/88/82 to the TRF3703-17. Figure 15 shows a passive network that can be used to develop the 3.3 Vdc required at the DAC output and 1.7 V at the modulator input, while still maintaining 50-Ω load for the DAC. An Excel spreadsheet calculator is available that can help with the resistive network calculation. An application report is also available to help with the design of differential LC filters (SLWA053).

If the V1 is set to 5 V and V2 is set to -5 V, then the network looks like R1=57 Ω, R2=80 Ω, and R3=336 Ω. The loss developed through R2 is about -1.86 dB. In most applications, the –5 V is not available, V2=0. In this situation, the resistor network looks like R1=66 Ω, R2=101 Ω, and R3=107 Ω, and the loss through R2 results in –5.76 dB.

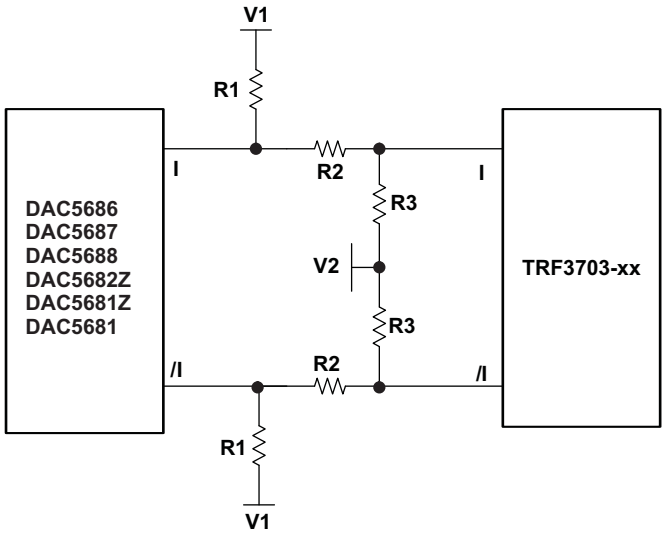

Figure 10. Termination Requirements for Interfacing Current Sink DAC to TRF3703-17

If the system is insensitive to frequencies near dc, a simple capacitor can be placed in parallel to R2. This allows the dc levels to be set up correctly with the resistor network and provides a path to bypass R2 for the ac signals. A high-pass corner is set up by the values of R3 and C. Typically, with values of C in the 1-µF range, the high-pass corner is approximately 100 Hz to 1 kHz. This works best for IF signals as well as wideband baseband signals which are not affected by the attenuation of some low-frequency components. In this situation, R1=77 Ω, R2=132 Ω, and R3=140 Ω. This sets up the correct dc bias voltages at 3.3 V and 1.7 V and for the ac load the DAC sees R1//R3=50 Ω.

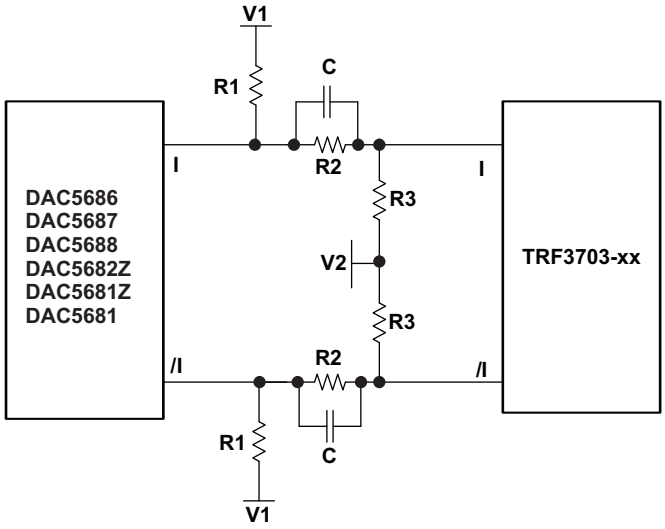

Figure 11. Termination for Current Sink DAC to TRF3703-17 With Capacitor to Mitigate ac Signal Loss

4.1.2 Adding a Filter to the TRF3703 Current Sink Interface

A filter also can be placed after the common-mode biasing network. For the dc coupled network (no parallel capacitor), R2 and the filter load R4 needs to be considered in the DAC impedance. The filter has to be designed for the source impedance created by the resistor combination of R3//(R2+R1). The effective impedance seen by the DAC is affected by the filter termination resistor resulting in R1//(R2+R3//(R4/2)).

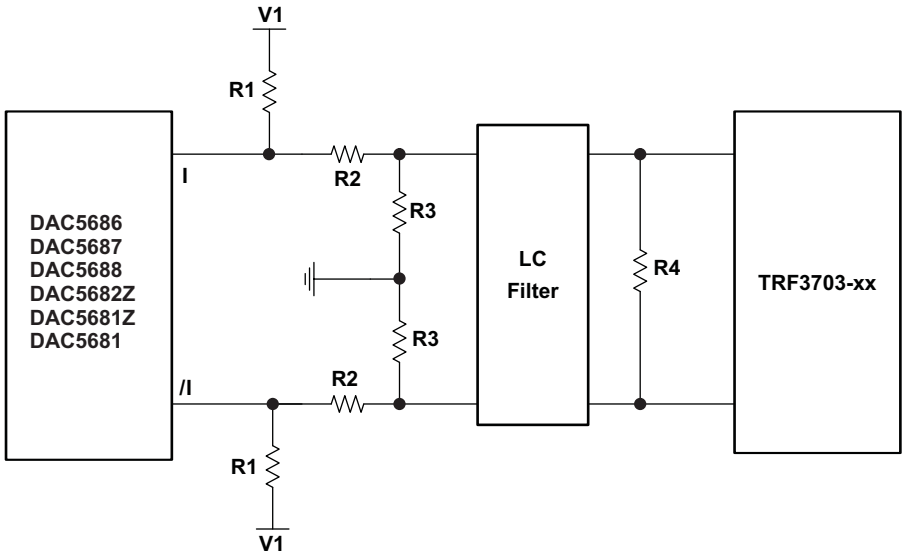

Figure 12. Termination Requirements for Interfacing Current Sink DAC to TRF3703-17 With LC Filter

Factoring in R4 into the DAC load, a typical application results in the following values: R1=72 Ω, R2=116 Ω, R3=124 Ω, R4=150 Ω. This implies that the filter needs to be designed for 75-Ω input and output impedance (single-ended impedance). The dc levels are maintained at 3.3 V and 1.7 V and the DAC load is 50 Ω. The added load of the filter termination causes the signal to be attenuated by –10.8 dB.

The filter can be designed to have unequal terminations such that the R4 load is significantly larger than R3. This still has a minimum loss as determined by the ratio of R3 and R2, in this case closer to –5.76 dB as opposed to –10.8 dB. This requires the bias network to be recalculated to account for the unequal terminations. This is not covered in this document, but the same design methodology can be extended to that application as well.

For the partially ac coupled case (with parallel capacitor C), the R2 resistor is not considered in the ac DAC termination or the filter load. R2 only has an effect on the dc biasing. The network values for this are: R1=127 Ω, R2=434 Ω, R3=462 Ω, and R4=200 Ω. The ac impedance seen by the filter is R1//R3=100 Ω. The DAC impedance seen by the DAC is R1//R3//(R4/2)=50 Ω. The dc biasing is maintained at 3.3 V and 1.7 V. The ac signal is not attenuated due to the bypass path offered by C.

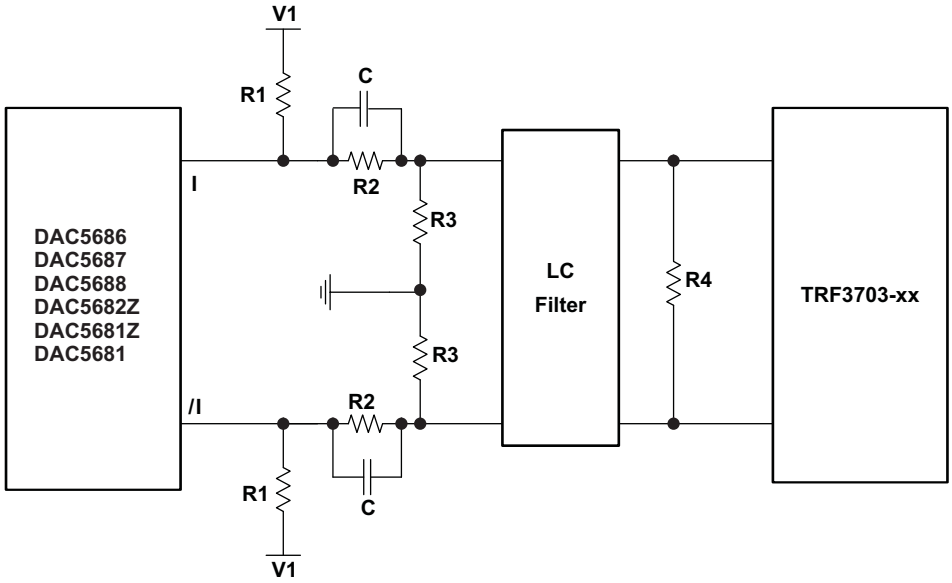

Figure 13. Termination for Current Sink DAC to TRF3703-17 With Capacitor to Mitigate ac Signal Loss With LC Filter

The following graph shows a typical frequency response including the LC response and the high-pass corner created by the parallel C. The high-pass corner frequency is dictated by the value of C. The dc response levels off at the attenuation level created by R2 and R3//(R4/2).

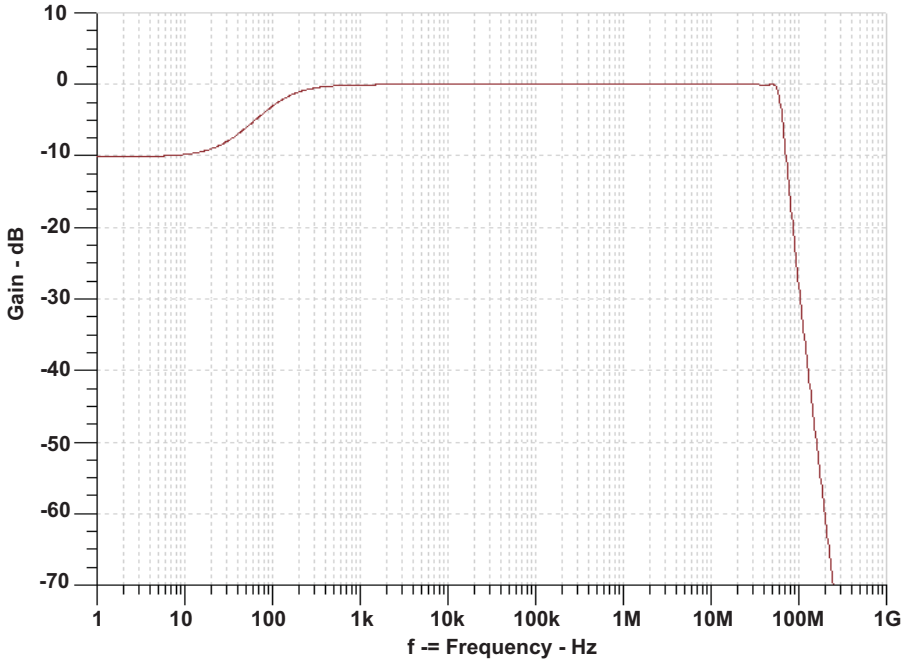

Figure 14. Typical Response of TRF3703 Termination With Capacitor to Mitigate Loss

4.1.3 Interfacing TRF3703-33 to a Current Sink DAC

For modulators requiring a 3.3-VCM interface, a more versatile network can be used as shown in Figure 15. Because a voltage shift is unnecessary, R2 can be set to 0, V1=5 V, V2=0. The 3.3 VCM on the DAC output is determined by the resistor ratio of R1 to R3 and with 1/2 the full-scale current (10 mA) sinking into the DAC output. The load seen by the DAC is R1//R3.

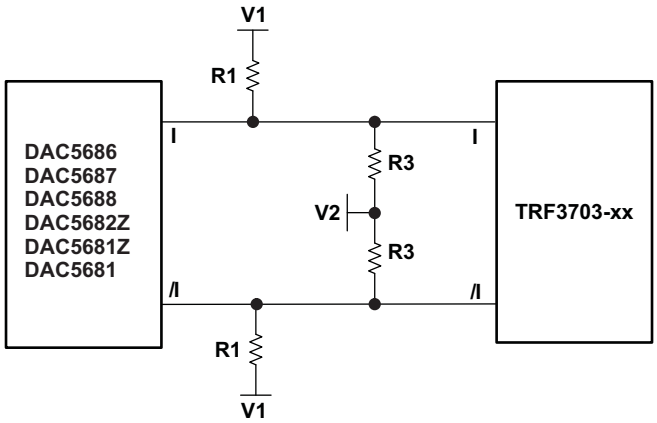

Figure 15. Passive Network for 3.3-VCM Modulator

A filter also can be implemented in a similar manner as in the previous section. However, it is much simpler to balance the loads and dc biasing without R2 (consequently no loss). The network can be designed such that R1=115 Ω, R3=681 Ω, and R4=200 Ω. The results in filter impedance of R1//R2=100 Ω, and a DAC load of R1//R3//(R4/2)=50 Ω. R4 is a differential resistor and does not affect the dc biasing created by R1 and R3. The common-mode voltage is set at 3.3 V for a full-scale current of 20 mA.

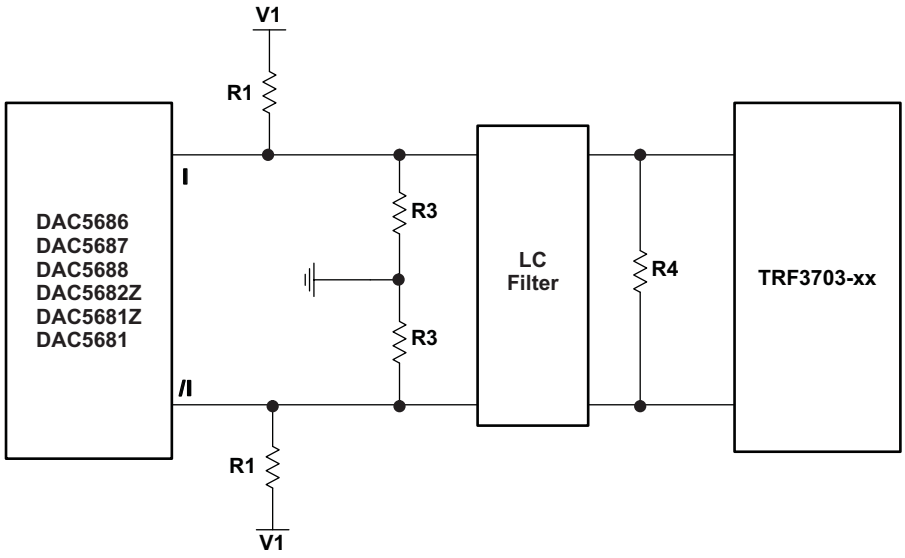

Figure 16. Passive Network for 3.3-V Modulator With LC Filter

4.2 Current Source DAC56x2/DAC5674 Passive Interface to an IQ Modulator

A similar application to interface a current source DAC to an IQ modulator can be achieved using a resistor network as well. The same concepts used in the current sink interface to the IQ modulator covered in the previous section can be applied. The only difference being that the common-mode voltages as well as the compliance voltages are different. In this case, the DAC output compliance voltage varies from –1 V to about +1.25 V. The TRF3703-33 3.3-V, common-mode modulator is not used in this application. The large level shift for the common-mode voltage creates an unnecessarily large attenuation of the ac signal. Instead, the TRF3703-17 with a 1.7-V common mode is used. These ideas can also be applied to the TRF3703-15 modulator with a 1.5-V common mode.

Although the DAC5674 is included in this application, it is not typically used for IQ modulator applications because it is a single DAC and requires two DACs for the IQ interface. It is shown mainly to include it in an application that requires a fixed, common-mode voltage.

4.2.1 Interfacing the TRF3703-17 to a Current Source DAC

It is desirable to have the DAC common-mode voltage set as close as possible to the modulator common-mode voltage to reduce the dc voltage level shift and corresponding ac attenuation. This requires the DAC common voltage to be set at 0.7 Vdc, with the understanding that a +0.5-V deviation is still within the upper compliance voltage of 1.2 V.

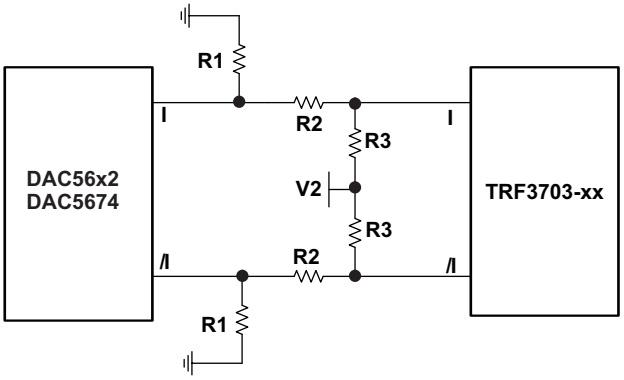

Figure 17. Interface Modulator to Current Source DAC

By requiring the DAC termination to be 50 Ω with the DAC current of 20 mA, a DAC common voltage of 0.7 V and a modulator common-mode voltage of 1.7 V, the values for the resistors need to be R1=52 Ω, R2=290 Ω, and R3=959 Ω, with V1=0 V and V2=5 V. This results in a –2.3-dB loss of the ac signal through the series resistor R2 that is needed to level-shift the common-mode voltage. Unlike the current sink case, having a bipolar ±5-V supply for this network does not affect the attenuation of the network.

The –2.3 dB of loss can be mitigated by using a parallel capacitor C with R2. This slightly changes the ac impedance seen by the DAC. Keeping the same set of values: R1=52 Ω, R2=290 Ω, and R3=959 Ω, the dc levels are maintained at 0.7 V on the DAC output and 1.7 V on the modulator input. The capacitor C provides a path for the ac signal to bypass R2 and not suffer the attenuation created by R2 and R3. The ac impedance seen by the DAC is R1//R3=49 Ω. Slight adjustments to the R values can be made such that the ac impedance is 50 Ω. All baseband corrections for dc offset, amplitude, and phase are still possible with this configuration.

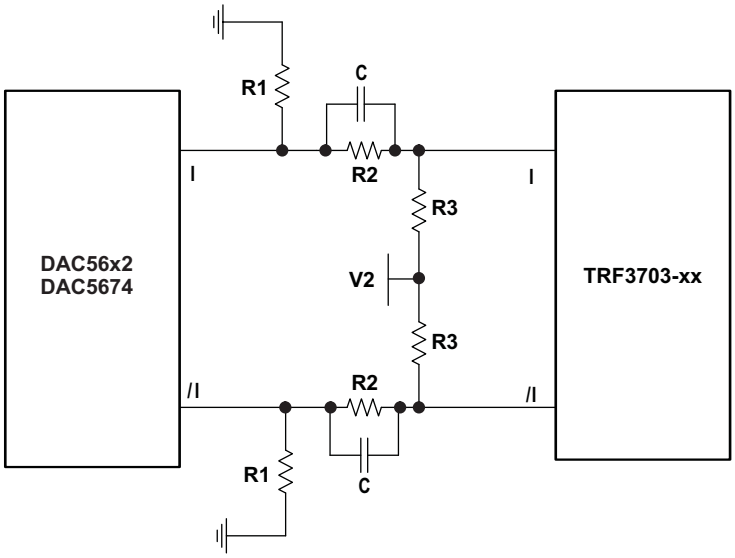

Figure 18. Interface Modulator to Current Source DAC With Capacitor to Mitigate Loss

4.2.2 Adding a Filter to the TRF3703-17 Current Source Interface

A filter can be added after the bias network. Similar considerations must be made here, as in the current sink configuration, with regard to the DAC and filter loads and the compliance and common-mode voltages. However, the requirements for this configuration are more challenging due to the current source interface.

For the case when only a +5-V supply is available for the network, the network design has some limitations. The maximum network impedance that can be designed is related to the DAC output common-mode voltage. For the 0.7-V, common-mode case and maximum output current of 20 mA, the maximum value for R1 approaches 70 Ω (assuming 10 mA is the dc current). For this condition, R2 and especially R3 approach very large values as R1 approaches 70 Ω. For the case when the DAC load is 50 Ω, and the capacitor is not used, the filter input termination is comprised of R3//(R2+R1) = 959//(290+52) = 252 Ω. The filter termination R4 also affects the ac load seen by the DAC. With R4=500 Ω, the DAC load is R1//(R2+R3//R4/2) = 47 Ω. The biasing network and the filter termination can be adjusted slightly to provide the maximum load and resulting output swing. The filter load also causes the ac response to be attenuated more than the original 2.3 dB caused by R2 and R3. The ac attenuation is now a factor of R2 and R3//(R4/2). For the preceding given example, the attenuation becomes about –8 dB.

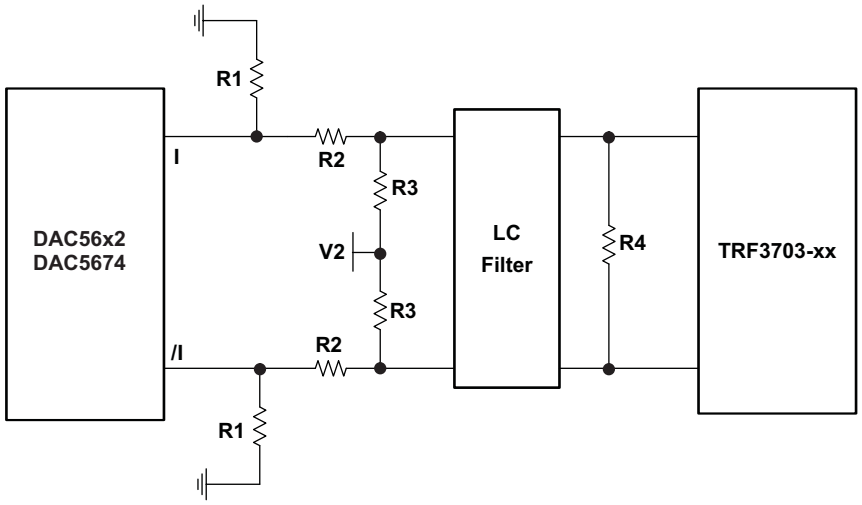

Figure 19. Interface Modulator to Current Source DAC With LC Filter

A filter with unequal termination can be designed such that R4 is much larger than the source impedance. This results in attenuation being closer to the –2.3 dB created by R3 and R2 because R4 has minimal impact on the value of R3. The bias network needs to be recalculated to account for the unequal terminations of the new filter.

A similar treatment can be done for the case with the parallel capacitor. For a single 5-V supply, the maximum load that can be designed for is up to 70 Ω. A target of 65 Ω for the ac DAC load results in more realistic values for R1=66 Ω, R2=1512 Ω, and R3=4988 Ω. The capacitor shorts out for the ac response so that the ac load for the termination of the filter is R1//R3=65 Ω, resulting in R4=130 Ω. The DAC ac load is R1//R3//(R4/2)=32 Ω which is less than optimal for the maximum DAC ac swing. An unequal termination filter can be designed such that R4 does not have much of an impact on R1 and R3. This is not covered in this application report.

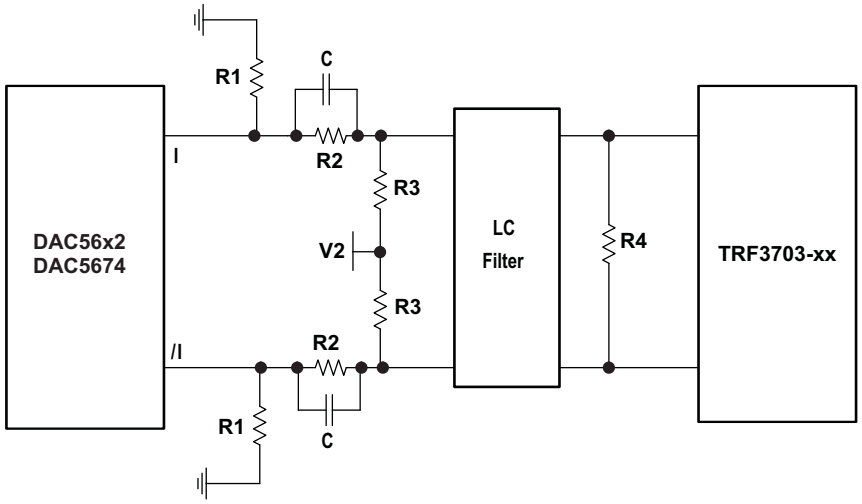

Figure 20. Interface Modulator to Current Source DAC With Capacitor to Mitigate Loss With LC Filter

For larger ac impedances (with the capacitor), a -5-V supply is necessary. To achieve the maximum ac swing requires the ac load to be 50 Ω. This necessitates the filter terminations to be designed for 100 Ω, which requires R1//R3=100 Ω, and R4=200 Ω. The result is V1=-5 V, V2=5 V, R1=211 Ω, R2=59 Ω, R3=194 Ω, and R4=200 Ω. The frequency response looks similar to the current sink case, but the dc attenuation is determined by R2 and R3 which results in about –2.3 dB. Because R4 is differential, it has no effect on the dc signal.

5 Summary

Current output DACs can either come with a current source output or a current sink output. Both cases can use unbuffered resistive terminations or can be used in a differential to single-ended application through a transformer. In all these cases, the most important consideration is to ensure that the DAC output compliance voltages are met for the entire output current range. A few examples have been outlined in this document for the DAC5672, DAC5674, DAC5675A, DAC5686, DAC5687, DAC5688, DAC5682, and DAC5681. These examples along with the Excel spreadsheet calculator tools, and TINA™ spice models available from Texas Instruments simplify the network design to meet all biasing and load requirements to achieve the best possible performance from each type of DAC.

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