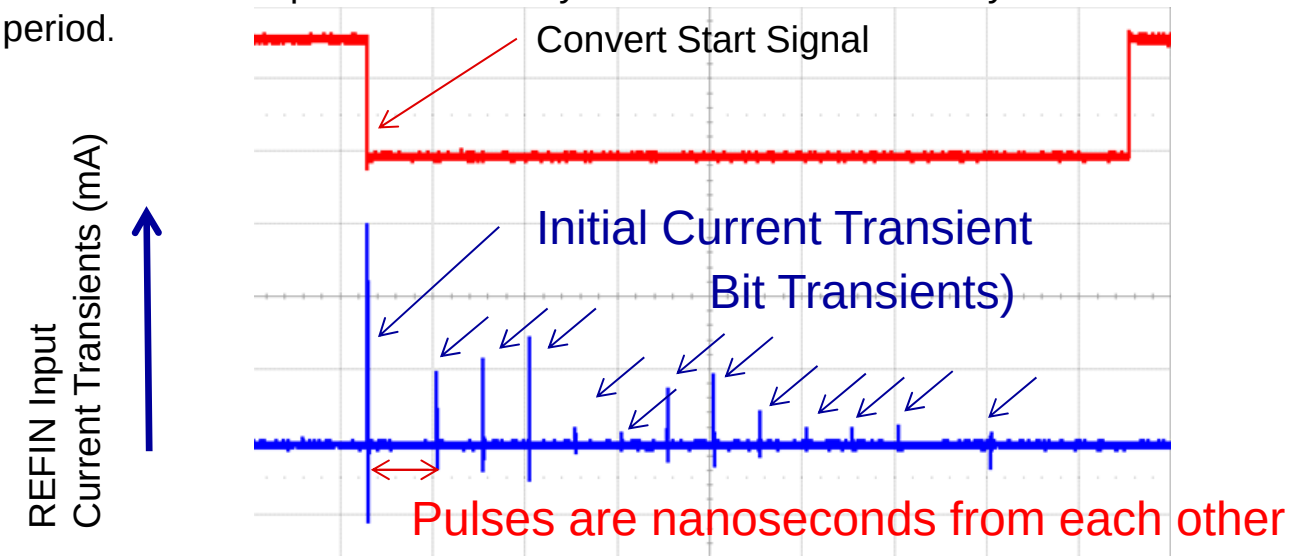
Optimal Voltage Reference Design for SAR ADCs

Luis Chioye – Precision Data Converters

SAR ADC Architecture

- The Reference is sampled several times during each conversion
- High-current transients (~10's mA range) are present in this REF input where the ADC's internal capacitor array is switched and charged as the bit decisions are made as binary weighted bit conversions are made.
- Current transient pulses occur only a few nanoseconds away of each other during the conversion period.



ADS8881 Reference Bypass capacitor

- 10uF to 22µF range
- Ceramic X7R-grade, 0805-size, > 10-V rating
- Place right at the REFIN pin, use wide, low inductance connections
- **Follow datasheet recommendations**

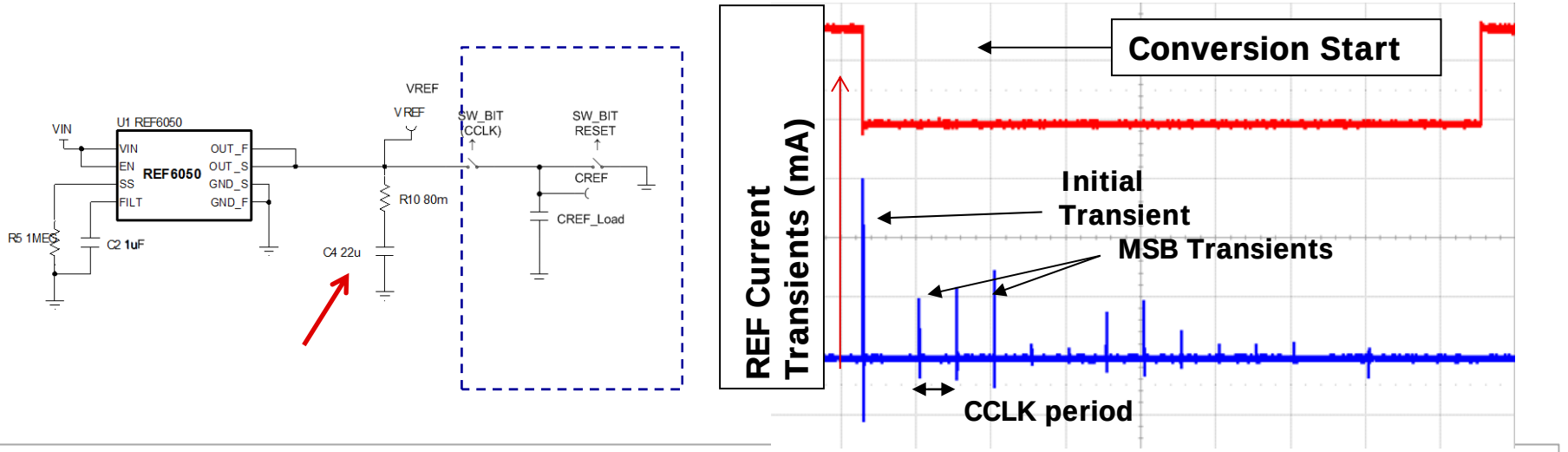
ADS8881:18-Bit, 1-MSPS, SAR ADC:

EXTERNAL REFERENCE INPUT					
V_{REF}	Input range	ADS8881C	3	5	V
		ADS8881I	2.5	5	
	Reference input current	During conversion, 1-MHz sample rate, mid-code		300	µA
	Reference leakage current			250	nA
C_{REF}	Decoupling capacitor at the REF input		10	22	µF
	Input leakage current	During acquisition for dc input		5	nA

High-performance (16-Bit) often require $C_{REF} \geq 10\mu F$

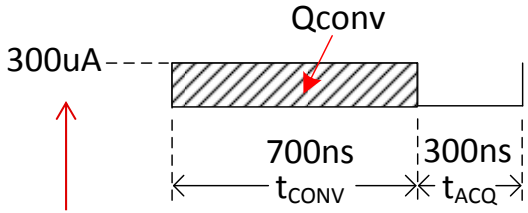
Reference Bypass capacitor

- Why is the large reference bypass capacitor required?
  - Works as large charge bucket
  - Provides instantaneous charge at MSBs decisions
  - Fast Transients are separated by CCLK period (10's ns)
  - Reference droop must be less < ½ LSB between CCLKs



Reference Bypass capacitor

- Why is the large reference bypass capacitor required?
  - For example, ADS8881, 18-B, 1-MSPS, SAR ADC:



Datasheet
Average REFIN Current

$$Q = I * t$$
$$Iconv = 300\mu A$$
$$tconv = 700ns$$
$$Qconv = 300uA * 700ns = 210\,pC$$

REFIN charge during each conversion

Charge/current during MSB bit decision

$$Qconv = Q_{MSB} + Q_{LSBs}$$
$$Q_{MSB} = \frac{1}{2}Qconv = \frac{210\,pC}{2} = 105\,pC$$
$$t_{CCLK} = \frac{700ns}{18_{CCLKs}} \simeq 40ns \rightarrow$$ Conversion Clock
$$I = \frac{Q}{t_{CCLK}} = \frac{105\,pC}{40ns} = 2.63mA$$

Reference Bypass capacitor

- Why is the large reference bypass capacitor required?
  - For example, ADS8881, 18-B, 1-MSPS, SAR ADC:

For this approximate calculation,
Assume most charge from bypass Capacitor and
keep VREF voltage droop <1/4 LSB

$$I_C = C\frac{dV}{dt}$$

$$LSB = 38.14uV$$ → 18-B ADC Full-Scale=±5V

$$dV = \frac{1}{4}LSB = 9.53uV$$

$$dt = t_{CCLK} = 40ns$$ → Conversion Clock

$$C = I_C\frac{dt}{dV} = 2.63mA \cdot \frac{40ns}{9.53uV} = \sim 11.04uF$$

Datasheet recommends 10uF - 22uF

ADS8881

Build TINA REF Input Model for a SAR

Important Datasheet Parameters

Example: ADS8881 18-B, 1-MSPS, Fully-Differential Input ADC

Sampling Rate = 1-MSPS
Throughput Period: t_{cycle}=1µs
Conversion Time: t_{conv}=710ns (max)

Input Equivalent Circuit: R_{SH} / C_{SH}

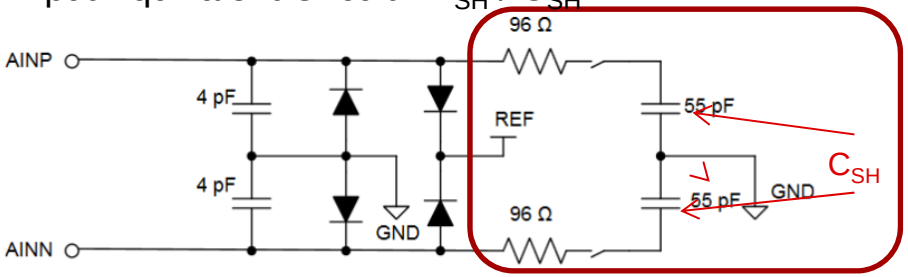


Figure 47. Input Sampling Stage Equivalent Circuit

VREF = 5V
Fully-Differential Input ADC
Full-scale Range: ±VREF = ±10V
ADC Resolution / Least Significant Bit (LSB):

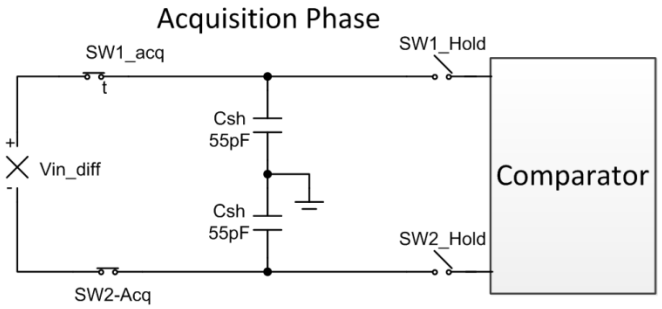
$$LSB = \frac{\pm VREF}{2^N} = \frac{2 \cdot VREF}{2^{18}} = 38.14uV$$

$$\frac{1}{2} LSB = 19.07uV$$

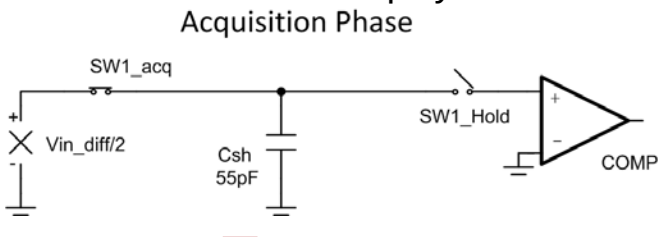
'Average' Reference Input Current
At Full throughput

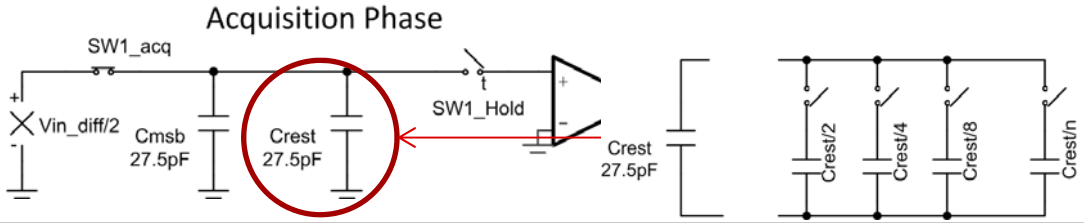
EXTERNAL REFERENCE INPUT					
V_{REF}	Input range	ADS8881C	3	5	V
		ADS8881I	2.5	5	
	Reference input current	During conversion, 1-MHz sample rate, mid-code		300	µA
	Reference leakage current			250	nA
C_{REF}	Decoupling capacitor at the REF input		10	22	µF

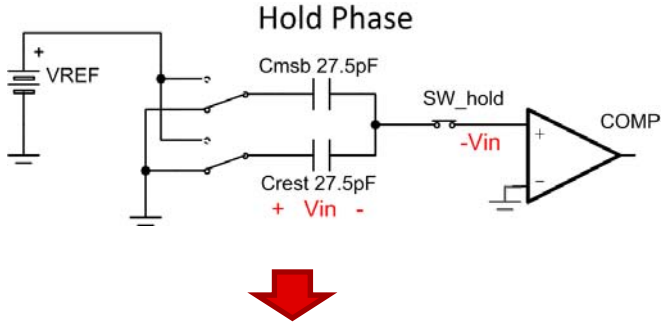
Estimate REFIN Capacitive Load:

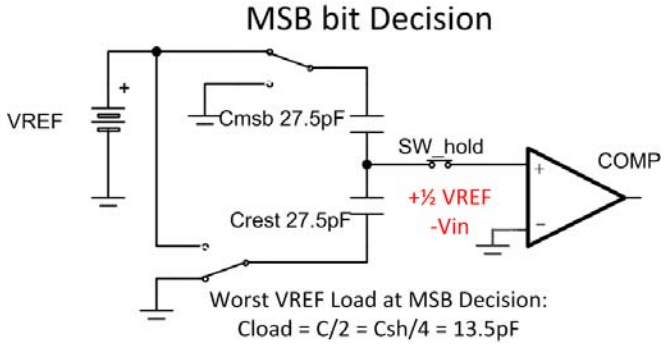


Simplify/Redraw as SE circuit









NOTE: REFIN Cmsb not always ¼ Csh; depends on device Architecture!!
This is a first order estimate.

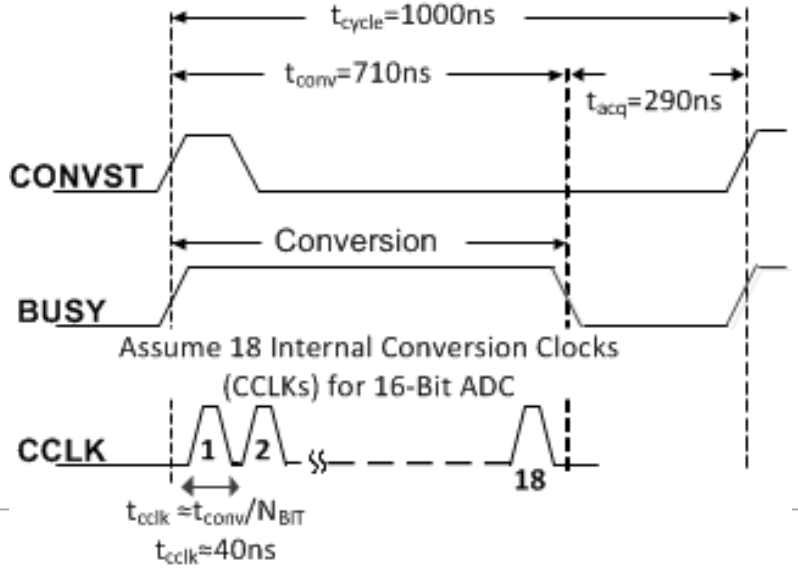
Conversion Period and Conversion Clock Timing

ADS8881 uses an internal conversion clock (CCLK)

Datasheet Specifies t_{conv} max

SAMPLING DYNAMICS					
t_{conv}	Conversion time		500	710	ns
t_{ACQ}	Acquisition time		290		ns
	Maximum throughput rate with or without latency			1000	kHz

Estimate internal Conversion Clock period



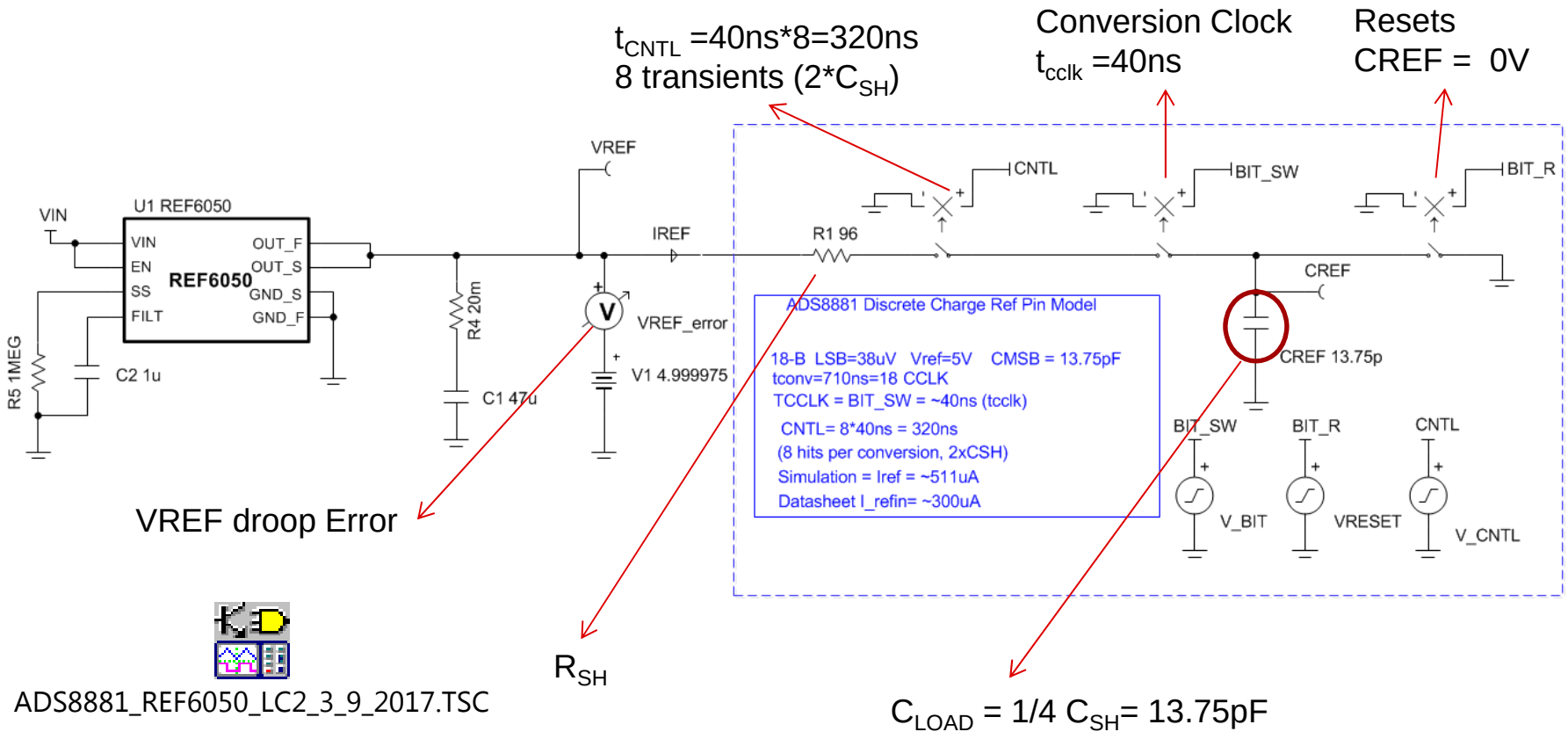
$$Fsample = 1000kHz$$

$$tcycle = \frac{1}{1000kHz} = 1us$$

$$t_{conv} = 710ns$$

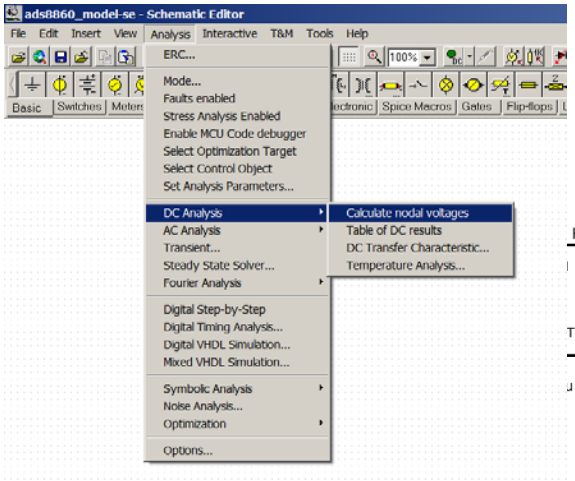
$$t_{cclk} \simeq \frac{t_{conv}}{N_{BIT}} = \frac{710ns}{18} \simeq 40ns$$

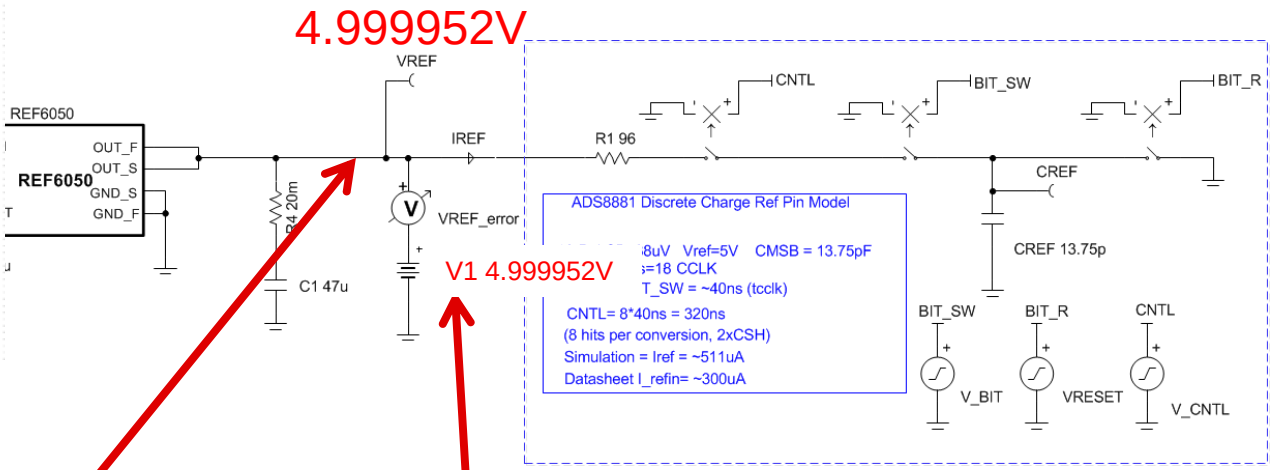
TINA SPICE Equivalent Model



ADS8881_REF6050_LC2_3_9_2017.TSC

Steady state Simulation Results

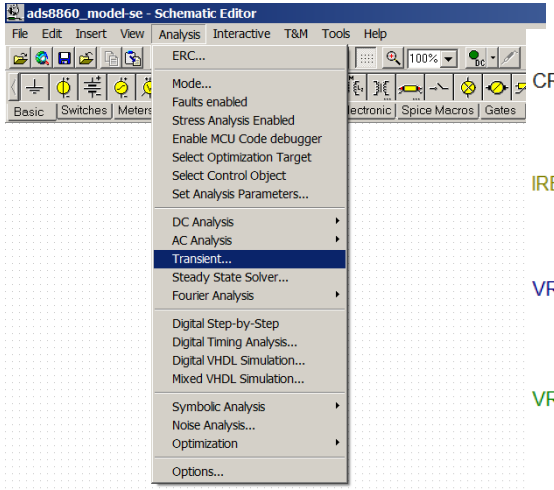


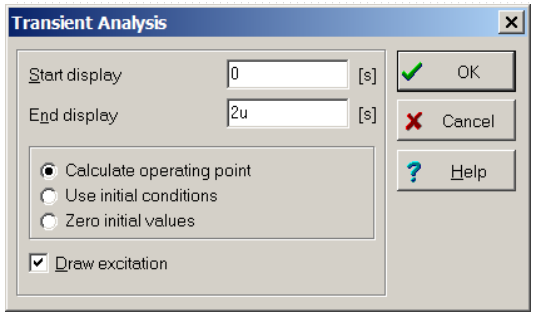


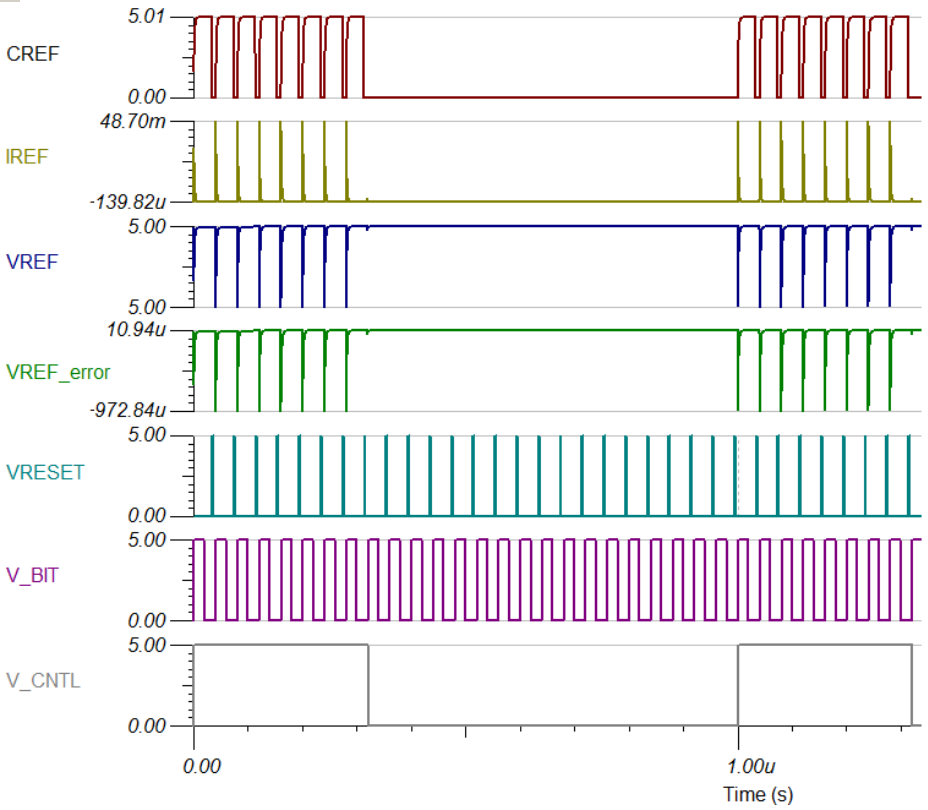
The steady state Reference input to the includes external reference initial accuracy error.

Set the Reference input source to match the steady state Reference input.

Example simulation: transient results







Voltage across CREF Load Cap

Transient Current into REFIN Pin

REFIN Pin voltage

REFIN error Voltage

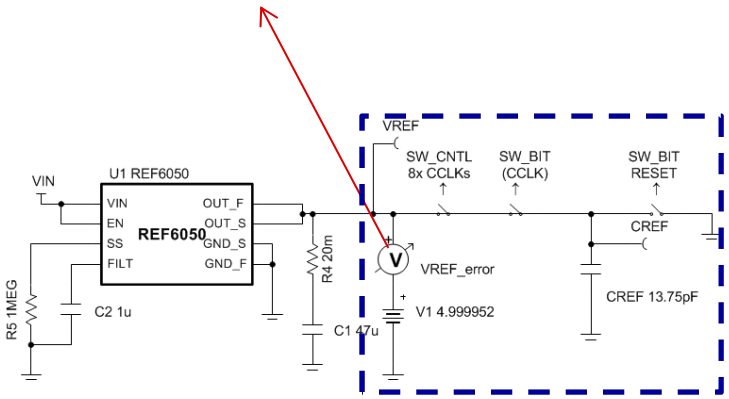
Switch control signal RESETs C_{REF} voltage

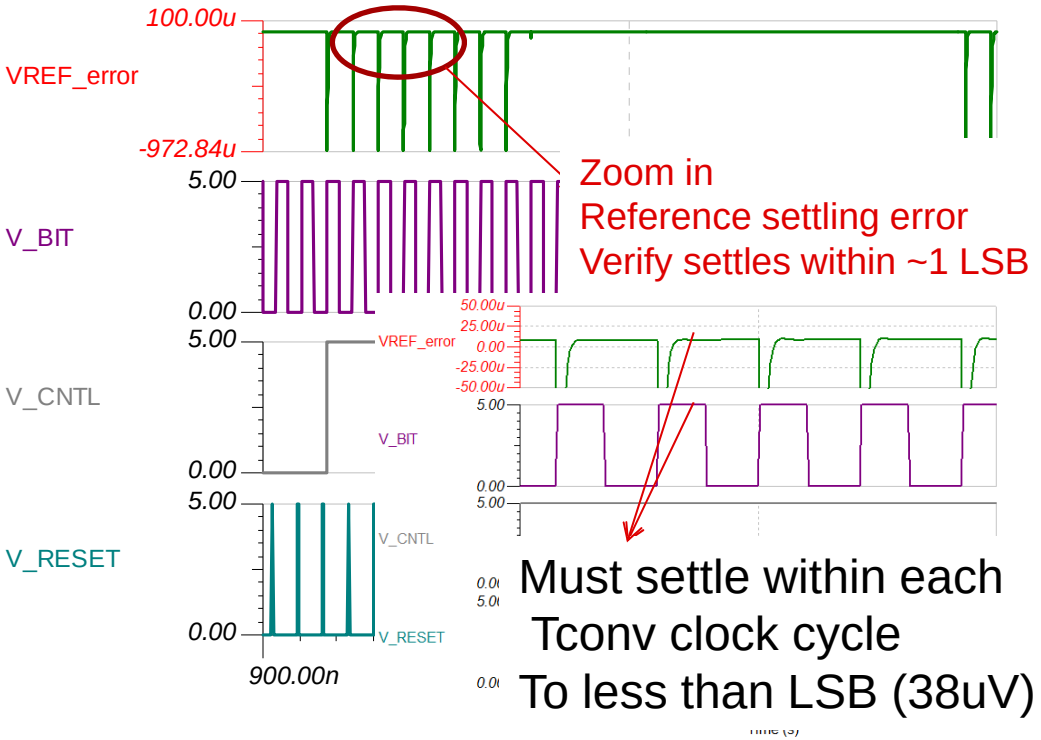
Switch control signal Conv Clock (CCLK)

CNTL switch signal ($8xC_{REF}$ Loads per Conv)

Key Result: Error Signal

Check Settling



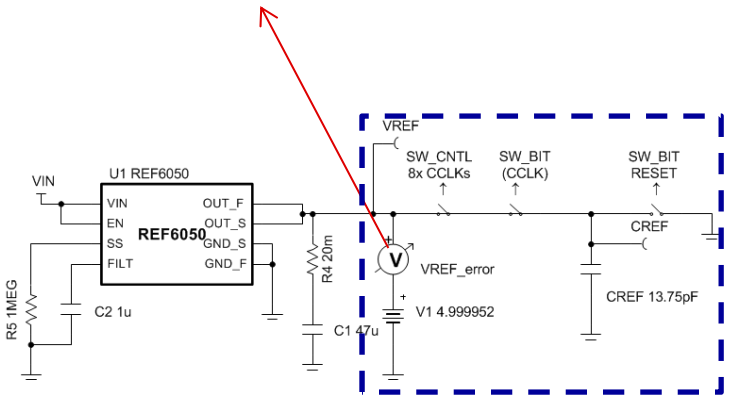


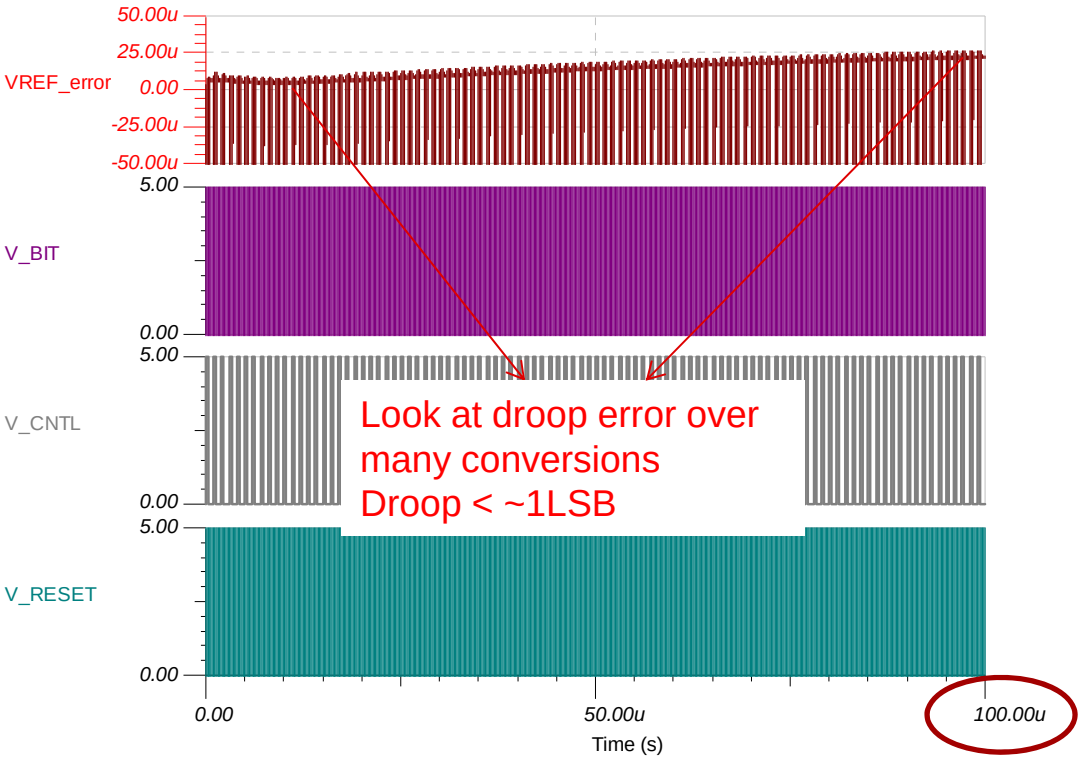
Zoom in
Reference settling error
Verify settles within ~1 LSB

Must settle within each Tconv clock cycle To less than LSB (38uV)

Key Result: Error Signal

Check Settling





Average Current in Simulation

Average Current over the conversion cycle is 529µA in approximate TINA simulation model (conservative)

Datasheet spec is 300µA