PROGRAMMING THE MSC1210

By Russell Anderson

SERIAL FLASH PROGRAMMING

AUTOBAUD AND SETUP

The BootROM start address is $F800_H$ for User Application Mode (UAM), and 0000_H for Flash Programming Mode (FPM). Since the 2kB BootROM code is using only an 11-bit address (e.g., ACALL, AJMP), all commands run both at $F800_H$ and 0000_H (for UAM and FPM). Autobaud measures the host asynchronous serial port 0 baud rate. Autobaud is expecting a carriage-return ($0D_H$) from the host.

When Autobaud completes, a greeting message with the version number is sent to the host via serial port 0.

The monitor serial transmit and receive has no specific flow control with the host machine. Turning off echo during Intel Hex transfer will yield the highest possible throughput.

Timers Setup

Flash programming requires accurate timing. This is controlled through related SFRs. For example, at 1MHz crystal clock, the following SFRs are initialized before any flash write, mass erase, or page erase:

USEC = 00_H

MSECL = $0E7_H$

MSECH = 03_H

FTCON = $0A5_H$

SFR modification is done through the 'RW' command (see Table I).

Flash Erase Before Load

To load new data into flash memory, the flash memory must be erased before write. In FPM, the Mass Erase command ('Mnnnn') or the Code Page Erase command ('CPnnnn') must be used before the Load command.

Input Format and Responses

Load command recognizes Intel Hex format, as shown in Figure 1.

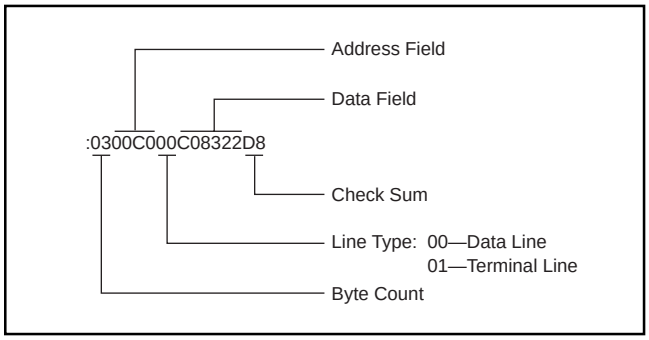

FIGURE 1. Intel Hex Format.

Intel Hex Addressing

During Serial and Parallel Flash Programming, the Hardware Configuration bytes are mapped into the memory address starting at 8000_H, as shown in Figure 2. The address translation is done in the embedded ROM.

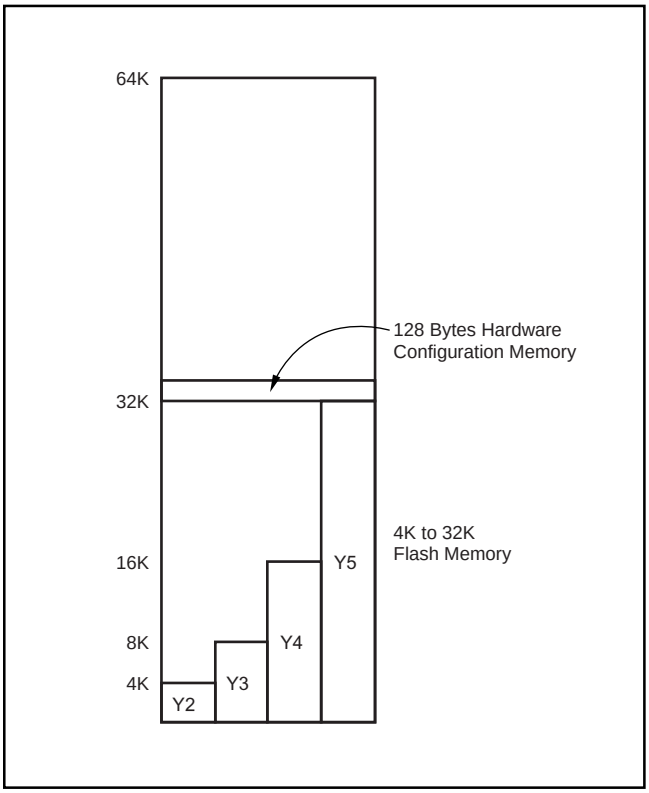

FIGURE 2. Flash Programming Mode Memory Orginization.

All of the flash memory is fully accessible when in FPM, assuming the security bit is disabled. This address map allows program flash setup, data flash setup, and configuration/info flash setup all in one Intel Hex file download. Note that the data flash starting address (e.g., 4000_H for 16kB data flash and 16kB program flash) will map to 0400_H when in UAM. All serial commands are enabled if the security bit, SBn bit of HCR0, is 1. If the security bit is cleared to 0, Flash Write, Flash Read for 0000_H~$7FFF_H$ (as shown in Figure 2), and Flash Page Erase commands are disabled (after reset) for code security.

SERIAL PROGRAMMING AND UAM MONITOR COMMANDS

COMMAND	COMMAND NAME	RESPONSE	PARAMETERS
XRnnnn	External Data Read	Display: None	Read 16 bytes from nnnn (External Data Memory).
XWnnnnyy	External Data Write	Display: None	Write to nnnn (External Data Memory) with yy.
XFnnnnyy	Data Flash Write	Display: 'ok' or 'x' for failing	Write to nnnn (flash byte data flash memory) with yy.
XPnnnn	Data Flash Page Erase	Display: 'ok' or 'x' for failing	Erase a 128-byte data flash page.
CRnnnn	Code Memory Read	Display 16-byte code memory starting from nnnn	Read 16 bytes from nnnn (code memory).
CWnnnnyy	Code Flash Write	Display: 'ok' or 'x' for failing	Write to nnnn (32kB code memory) with yy.
CPnnnn	Code Flash Page Erase	Display: 'ok' or 'x' for failing	Erase a 128-byte code flash page at nnnn, lower 7 bits are ignored.
RRnn	Register (SFR) Read	Display 1-byte SFR at nn	Read from nn (128-byte SFR).
RWnnyy	Register (SFR) Write	Display: None	Write to nn (128-byte SFR) with yy.
Fnn	PS1 Flash Memory Read	Display 16-byte PS1 flash memory starting from nn	Read 16 bytes of config/info flash (128-byte PS1 Flash Memory).
Mnnnn	Mass Erase	Display: 'ok' or 'x' for failing	0~7FFFF$_H$ for PS0 program memory mass erase, 8000$_H$~807F$_H$ for PS1 flash memory.
Q	Continue Execution from Break	Display: None	
S	Single Step	Display: None	
E	Toggle Echo	Display: None	
L	Load Intel Hex	Display: '.' — data line write passes 'X' — line write error 'E' — line checksum error 'T' — termination of transfer	Command is disabled when HCR0.EPMA = 0.
IRnn	Internal RAM Read	Display: 16-byte IRAM starting from nn (256 bytes RAM)	Read 16 bytes from nn (256 bytes of internal RAM).
IWnnyy	Internal RAM Write	Display: None	Write to nn (internal RAM) with yy.
B0nnnnxx	Set Breakpoint 0 and Status in BPCON	Display: None	Write address nnnn to BP0 and status xx to BPCON.
B1nnnnxx	Set Breakpoint 1 and Status in BPCON	Display: None	Write address nnnn to BP1 and status xx to BPCON.
Gnnnn	Goto Address	Display: None	Go to address nnnn.

NOTE: nnn, nn, and yy are hex digits.

TABLE I. Serial Programming Command List.

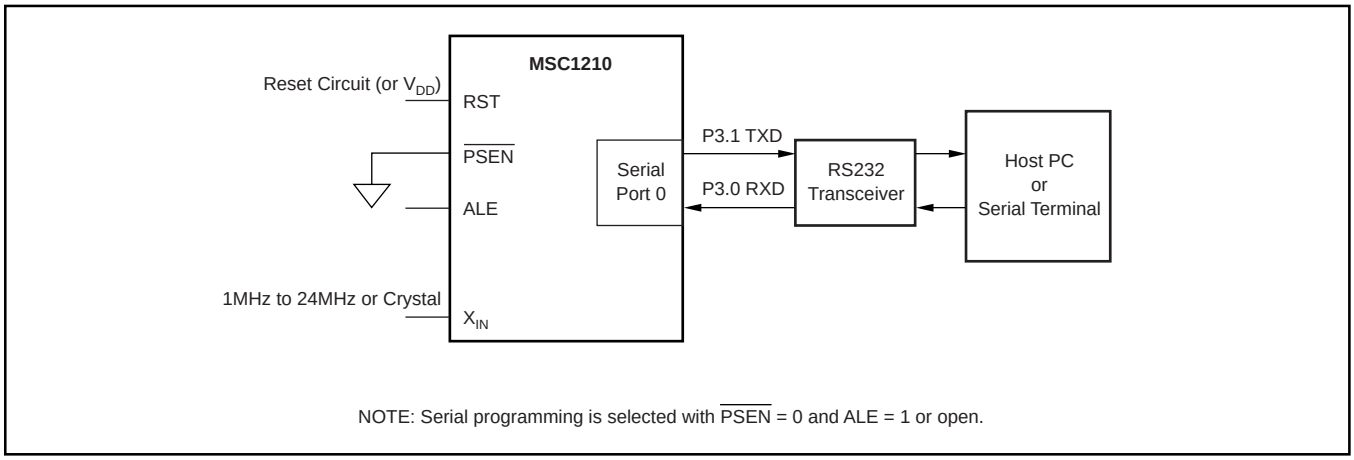

FIGURE 3. Serial Programming and Monitor Configuration.

PARALLEL FLASH PROGRAMMING

Configuration

When the MSC1210 is configured to parallel programming mode by pulling $\overline{\text{PSEN}}$ HIGH (or NC) and pulling ALE LOW while RST is asserted, the device ports will be configured for parallel interface with the Host Flash Programming, as shown in Figure 4. Table III shows the port definitions. The host will provide Addr/Cmd/Req/RST/Clk signals, and the MSC1210 will respond with Ack/Pass/Data. The command address Addr[14:0] is divided into two parts, AddrHi[6:0] and AddrLo[7:0], i.e. Addr[14:0] = (AddrHi[6:0], AddrLo[7:0]). P3[1:0] are reserved. and must not be connected (NC).

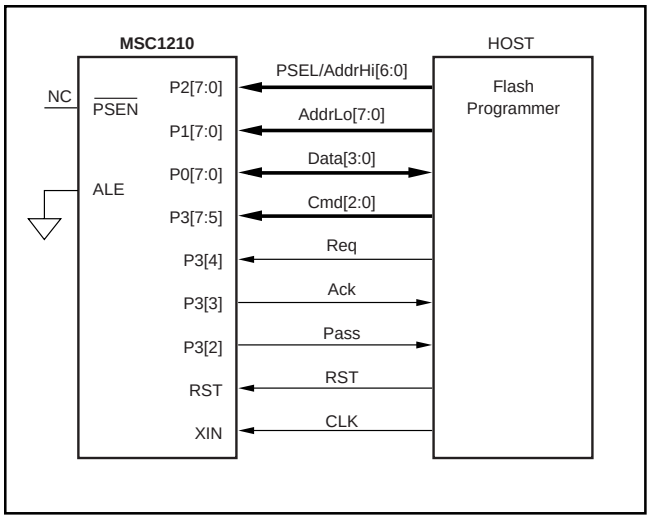

FIGURE 4. Parallel Programming Configuration.

Command Handshaking

Figure 5 shows the parallel programming sequence starting from power-on reset. After power-on with $\overline{\text{PSEN}}$ HIGH and ALE LOW, the MSC1210 is setup for parallel programming; reference the numbers in Figure 5.

(1) Power-On—Ack and Pass signals have internal pull-ups. Ack and Pass will change to zero when the MSC1210 is ready to accept new or first commands.

(2) Command Request—After the Host detects a LOW on Ack, the host should setup Addr/Dara/Cmd, and raise the Req flag. For Host read commands (SFR Read, Flash Read), the host must drive Data with hi-z. For Host write commands, the host must drive Data with command data.

(3) Command Done—After the MSC1210 detects Req, it executes the command, and sets the Pass line if the command is successful or clears the Pass line if the command fails (e.g. Flash Write Value Check Error). If the command is a read command, it will drive the read result on the Data bus. Ack is driven HIGH to acknowledge a command or signal that the command is finished.

(4) Host Acknowledge—The host should detect the Ack signal, drive hi-z to Data for write commands or fetch Data for read commands, and release the Req line to signal the MSC1210 to acknowledge command complete. Setting up a new Addr and Cmd is optional.

(5) MSC1210 Acknowledge—After the MSC1210 detects Req release, Data is driven with hi-z for read commands to avoid bus conflict, and Ack/Pass is released to prepare for a new command.

(6) New Command—Procedure repeats from (2) to (5).

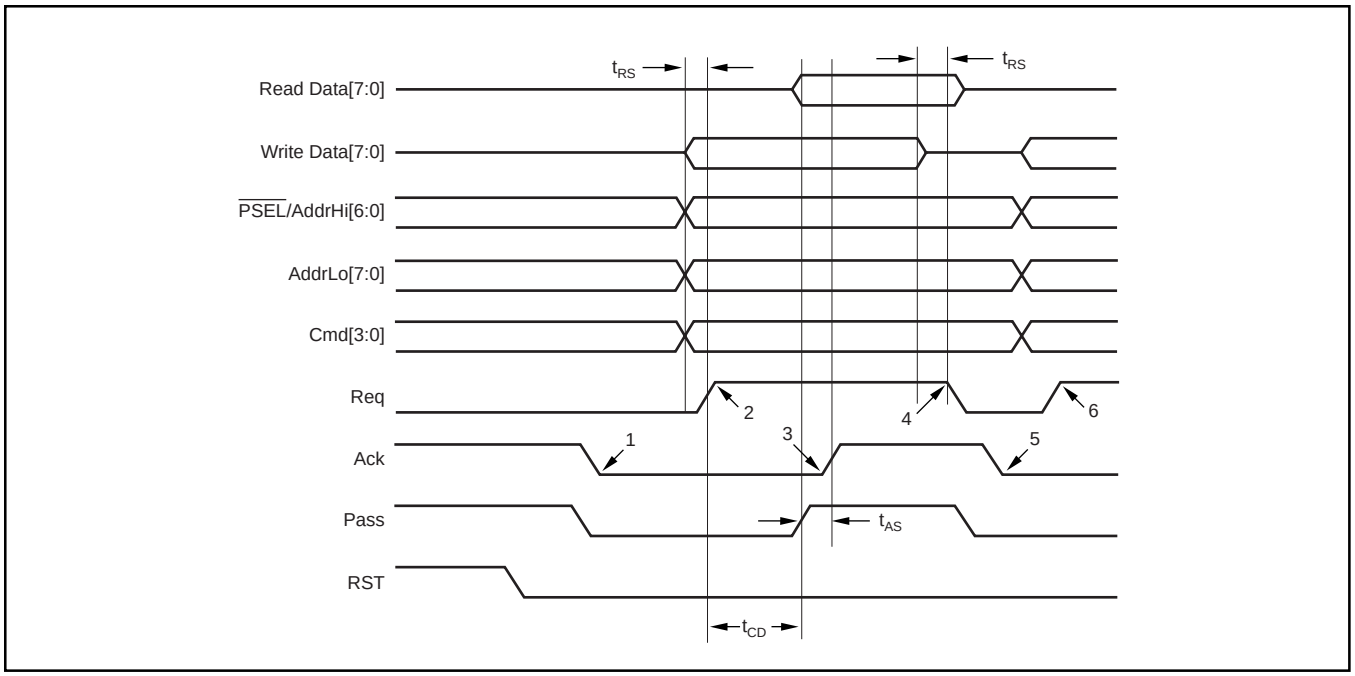

FIGURE 5. Parallel Programming Handshaking and Timing.

PORT NUMBER	PORT NAME	DIRECTION		DESCRIPTION
		FROM	TO	
P2[7]	PSEL	Host	MSC1210	Host Flash Memory PS0/PS1 Select
P2[6:0]	AddrHi[6:0]	Host	MSC1210	Host Command Address 14 to 0
P1[7:0]	AddrLo[7:0]	Host	MSC1210	
P0[7:0]	Data[7:0]	Host	MSC1210	Host Data for Write Commands
		MSC1210	Host	MSC1210 Data for Read Commands
P3[7:5]	Cmd[2:0]	Host	MSC1210	Host Programming Command
P3[4]	Req	Host	MSC1210	Host Command Request Handshake Line
P3[3]	Ack	MSC1210	Host	MSC1210 Command Acknowledge Handshake Line
P3[2]	Pass	MSC1210	Host	MSC1210 Command Pass/Fail Line

TABLE III. Parallel Programming Port Definitions.

Cmd[2:0]	COMMAND NAME	DATA BUS DRIVER	DESCRIPTION
000	Flash Read	MSC1210	PSEL = 0 for PS0, PSEL = 1 for PS1, Addr[14:0] is the Read Address
001	Flash Write	Host	PSEL = 0 for PS0, PSEL = 1 for PS1, Addr[14:0] is the Write Address
010	Flash Mass Erase	None	PSEL = 0 for PS0, PSEL = 1 for PS1, Addr[14:0] is Ignored
011	Flash Page Erase	None	PSEL = 0 for PS0, PSEL = 1 for PS1, Addr[14:7] is the Page Address, Addr[6:0] is Ignored (Page Size is 128 Byte)
100	Reserved	None	
101	Reserved	None	
110	SFR Read	MSC1210	PSEL and Addr[14:8] are Ignored, Addr[7:0] is the SFR Read Address
111	SFR Write	Host	PSEL and Addr[14:8] are Ignored, Addr[7:0] is the SFR Write Address

TABLE IV. Parallel Programming Commands.

PARAMETER	DESCRIPTION	DIRECTION		DESCRIPTION
		MIN	MAX	
t_{RS}	Req Setup	0µs	—	Data/Addr/PSEL/Cmd Setup Before Req
t_{AS}	Ack Setup	1µs	—	Data/Pass Setup Before Ack
t_{CD}(1)	Command Delay	—	11ms	Command Delay for Mass Erase and Page Erase Commands
		—	0.5ms	Command Delay for Flash Write Commands
		—	0.1ms	Command Delay for Flash Read/SFR Read/SFR Write Commands
CLK	Clock Frequency	1MHz	24MHz	System Clock Input.

NOTE: (1) t_{CD} is limited by Flash programming timing, higher CLK will not reduce timing significantly.

TABLE V. Parallel Programming Timing.

Command Timing

Programming Setup

Flash programming requires accurate timing. This is controlled through related SFRs. For example, at 1MHz crystal clock, the following SFRs must be initialized before any Flash Write, Mass Erase, and Page Erase:

$USEC = 00_H$

$MSECL = 0e7_H$

$MSECH = 03_H$

$FTCON = 0a5_H$

SFR modification is done through the 'SFR Write' command (see the Command Section).

Code Security

All parallel commands, as shown in Table IV, are enabled if the security bit, SBn bit of HCR0, is 1. If the security bit is cleared to 0, Flash Write, Flash Read for 0000_H~$7FFF_H$ (see Figure 2), and Flash Page Erase commands are disabled (after reset) for code security. Flash Read for addresses 8000_H~$807F_H$ for PS1 areas are always enabled, such that the manufacturer's information and device Flash configuration (HCR0/1) are accessible. SFR Read and SFR Write are not affected by the security bit.

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