Monitoring NTC thermistor circuit with single-ended ADC

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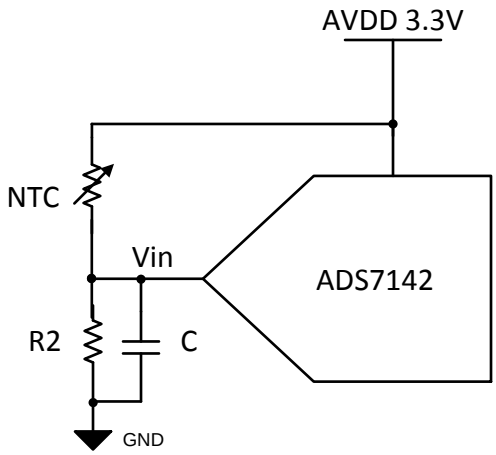
Input	ADC Input	Digital Output ADS7042
VinMIn	785mV	0x3CE
VinMax	2.51V	0xC2B

Power Supplies
AVDD
3.3V

Design Description

This cookbook describes how to design a circuit to directly monitor a thermistor with a SAR ADC. This temperature-sensing circuit uses a negative temperature coefficient (NTC) thermistor in series with a resistor to form a voltage-divider. This voltage divider has the effect of producing an output voltage that is directly related to the monitored temperature. The input voltage of the resister divider is also the analog power supply (AVDD) to the analog-to-digital converter, ADS7142, which for this device is also used as the reference. By connecting the sensor to the reference input, AVDD, the measurement will be ratiometric which will ensure that variations in the reference voltage will not impact the overall accuracy. The capacitor in parallel with the input resistor is used to filter intrinsic noise as well as noise pick-up.

Thermistors are used to monitor temperature in applications such as appliances, wireless environmental sensors, and smoke and heat detectors. In these applications, the thermistor voltage changes slowly thus it is not necessary to sample at high sampling rates. This means that there is no need for a driving input amplifier to condition the input voltage. A similar cookbook design, *Driving SAR directly without a front-end buffer circuit*, explains how to measure introduced drift from external components which can prove to be helpful in these applications.



Specifications

Specification	Calculated	Simulated
Temperature range	50ºC to 150ºC	50ºC to 150ºC
ADC input range	Within full scale range (< 3.3V)	785mV to 2.51V

Design Notes

1. Create resistor divider topology with NTC thermistor as the top component of the voltage divider. Using this configuration causes the ADC input voltage to increase with temperature. The input voltage decreases or increases as the temperature decreases or increases, respectively.
2. The bottom resistor (R2) in the voltage divider is designed based on the temperature range monitored. The equation used for this component is given later when selecting components. Look at the thermistor resistance tolerance as a guideline for choosing the tolerance on R2. Typically a 1% tolerance resistor is sufficient to match the thermistor tolerance. Normally, thermistors are used for low-cost, lower-accuracy applications.
3. The capacitor in parallel with R2 creates a filter for the ADC input signal, most commonly used to filter power supply noise. The capacitor also affects the start-up time of the system as it will take longer to charge larger capacitors.

Component Selection

1. Select a thermistor to best fit the application measurement needed. When selecting the thermistor, take into consideration the Beta value (or B), a common parameter found in the device data sheet and the accuracy need of your application. For a thermistor, the B value is specified across a given temperature range and represents the change of the resistance of the thermistor across that temperature range. The higher the B value the higher the rate of change of the resistance of the thermistor across the temperature range. Although, with a higher B value, the overall resistance of the thermistor tends to be higher. This document focus is monitoring a temperature range of 50°C to 125°C with a desired output within 0V to 3.3V. Thus, the NTC selected is a 100kΩ at 25°C, with B(25/85) value of 3977K, and an operating temperature range of 50°C to 150°C (223.15K to 423.15K).
2. The expected NTC resistances of the temperature range monitored are needed to select R2. The R2 value will be used to create a more linear voltage versus temperature relation. The following equation for NTC resistance uses the B value and temperature of the thermistor. Calculations require temperature to be in Kelvin.

$$R_{NTC} = R_{@\,298.15K} \cdot e^{B\left(\frac{1}{T} - \frac{1}{298.15K}\right)}$$

where

- R_{NTC} is the thermistor resistance (Ω) at temperature T
- $R_{@298.15K}$ is the thermistor resistance (Ω) measured at 25°C given in the data sheet
- B is the thermistor B value from data sheet in Kelvin (K)
- T is the temperature in Kelvin (K) that the thermistor is at (0°C + 273.15 = K).

- Temperature range in Kelvin:

$$T_{max} = 125°C + 273.15 = 398.15K$$

$$T_{min} = 50°C + 273.15 = 323.15K$$

- Thermistor resistance values:

$$R_{min} = R_{@\,398.15K} = 100k\Omega \cdot e^{3977K\left(\frac{1}{398.15K} - \frac{1}{298.15K}\right)} = 3.507k\Omega$$

$$R_{max} = R_{@\,323.15K} = 100k\Omega \cdot e^{3977K\left(\frac{1}{323.15K} - \frac{1}{298.15K}\right)} = 35.631k\Omega$$

3. Calculate the value of R2, using the minimum and maximum expected NTC resistances. The closest resister value is 11.1kΩ

$$R_2 = \sqrt{R_{@398.15K} \cdot R_{@323.15K}} = \sqrt{3.507k\Omega \cdot 35.631k\Omega} = 11.18k\Omega$$

4. Select the capacitor value. The capacitor value is selected to optimize ADC settling using the TINA SPICE simulation. The simulation steps and results are found in the simulation section, which results in a 1-nF capacitor.
5. The cutoff frequency of the RC filter can be calculated using the equation by implementing the parallel combination of the thermistor resistance value and R2. Note that increasing the capacitor value decreases the cutoff frequency of the filter. A large capacitor though can increase the system start up time because it takes longer to charge, and also increases the ADC input settling time. The following calculation shows the change in cutoff frequency across the temperature range for the thermistor:

$$f_c = \frac{1}{2\pi \cdot R_{NTC} \,||\, R2 \cdot C}$$

where

$$R_{eq\_1} = \frac{3.507k\Omega \cdot 11.1k\Omega}{3.507k\Omega + 11.1k\Omega} = 2.665k\Omega$$

$$R_{eq\_2} = \frac{35.631k\Omega \cdot 11.1k\Omega}{35.631k\Omega + 11.1k\Omega} = 8.463k\Omega$$

For the full range of the filter, apply the parallel equivalents:

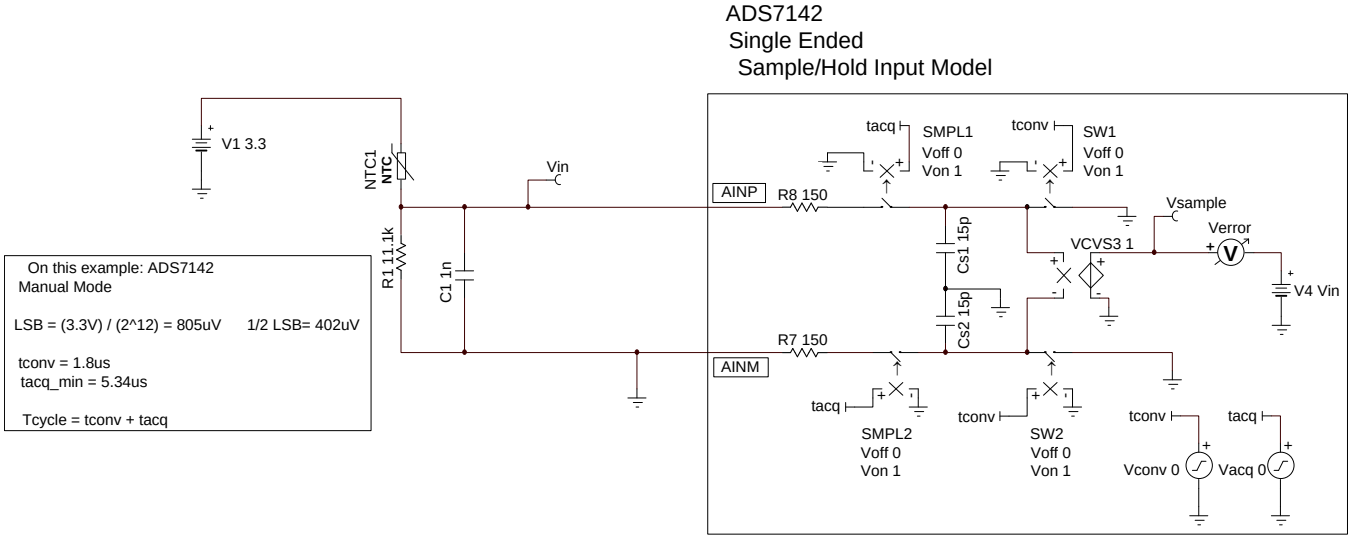
$$f_{c\_max} = \frac{1}{2\pi \cdot R_{eq\_1} \cdot C} = \frac{1}{2\pi \cdot 2.665k\Omega \cdot 1nF} = 59.72kHz$$

$$f_{c\_min} = \frac{1}{2\pi \cdot R_{eq\_2} \cdot C} = \frac{1}{2\pi \cdot 8.463k\Omega \cdot 1nF} = 18.805kHz$$

6. Running transient simulations highlights the settling of the internal sample and hold circuit and helps verify the input is settling within the acquisition time. The acquisition time can be increased by decreasing the sampling rate.

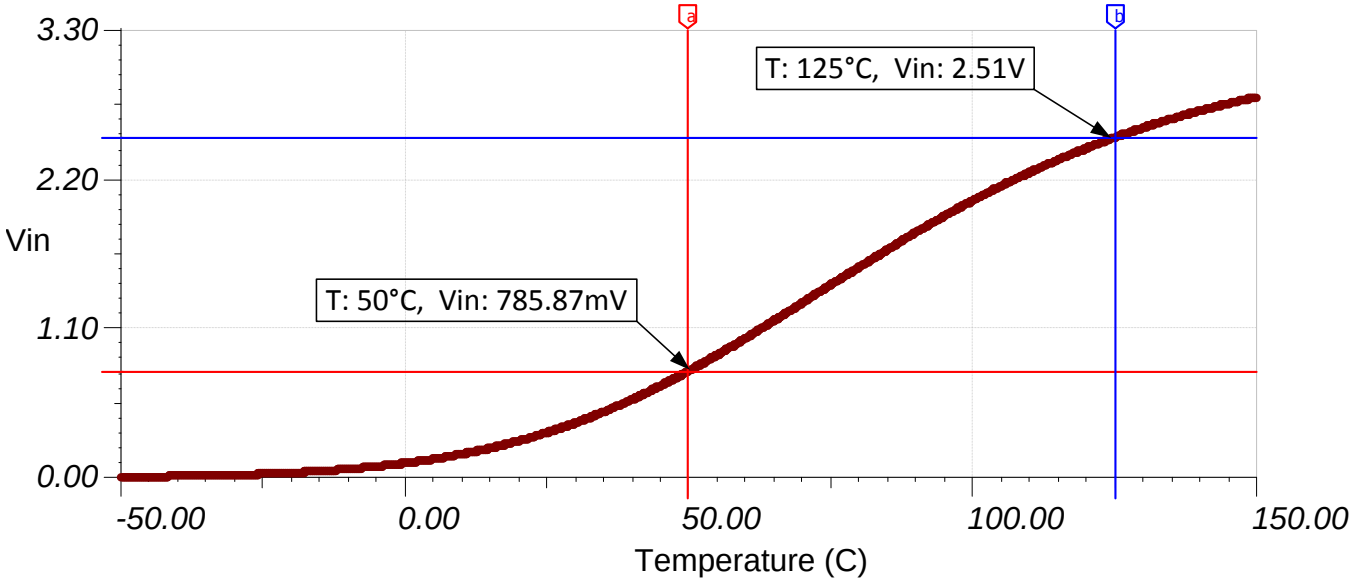
Design Simulation Model

The following schematic of the first order model of ADS7142 was built using the steps explained in Building the SAR ADC Model in TINA spice. The ADC sampling rate is set at 10kHz.



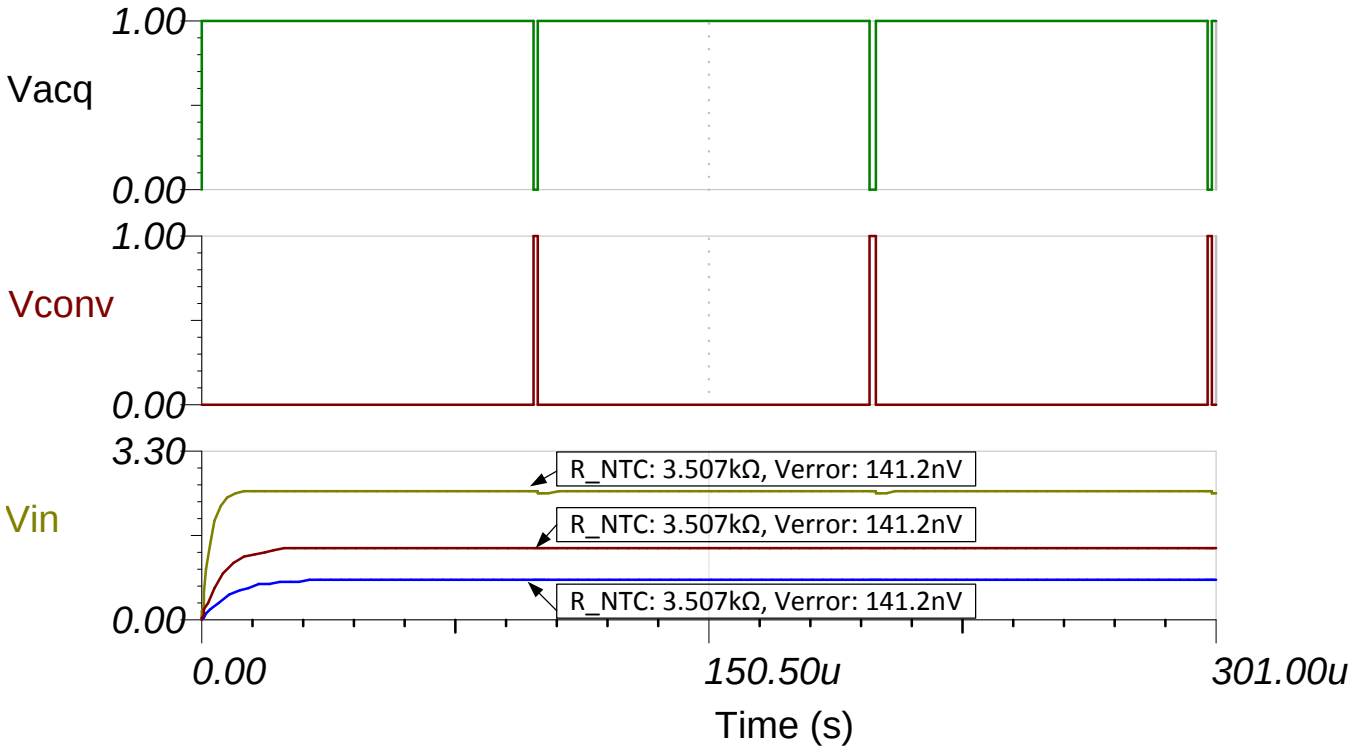
Temperature Transfer Characteristics

The linear NTC output voltage range within the desired temperature range of 50°C to 125°C is within the ADC input range and is set by step 3 of *component selection*.



Transient ADC Input Settling Simulation

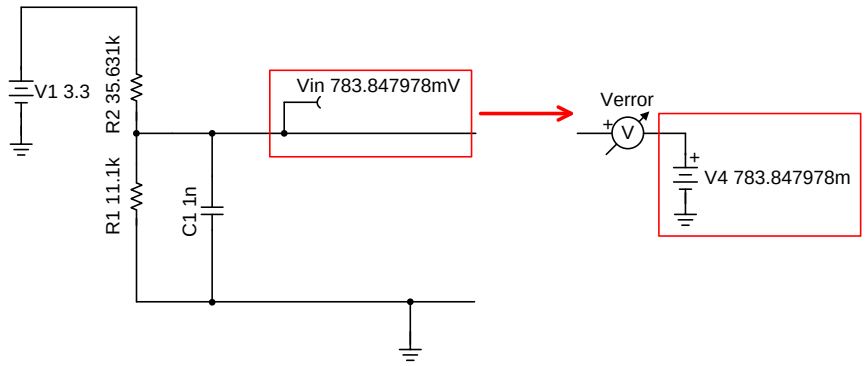
Expected start-up time varies by the current NTC resistance state. The following graph is tested at three different resistor values, for maxima 50°C, 125°C and a midpoint. The settling is verified to be less than ½ LSB at the end of the acquisition period. For an explanation of ADC settling, see *Refine the Rfilt and Cfilt Values*.



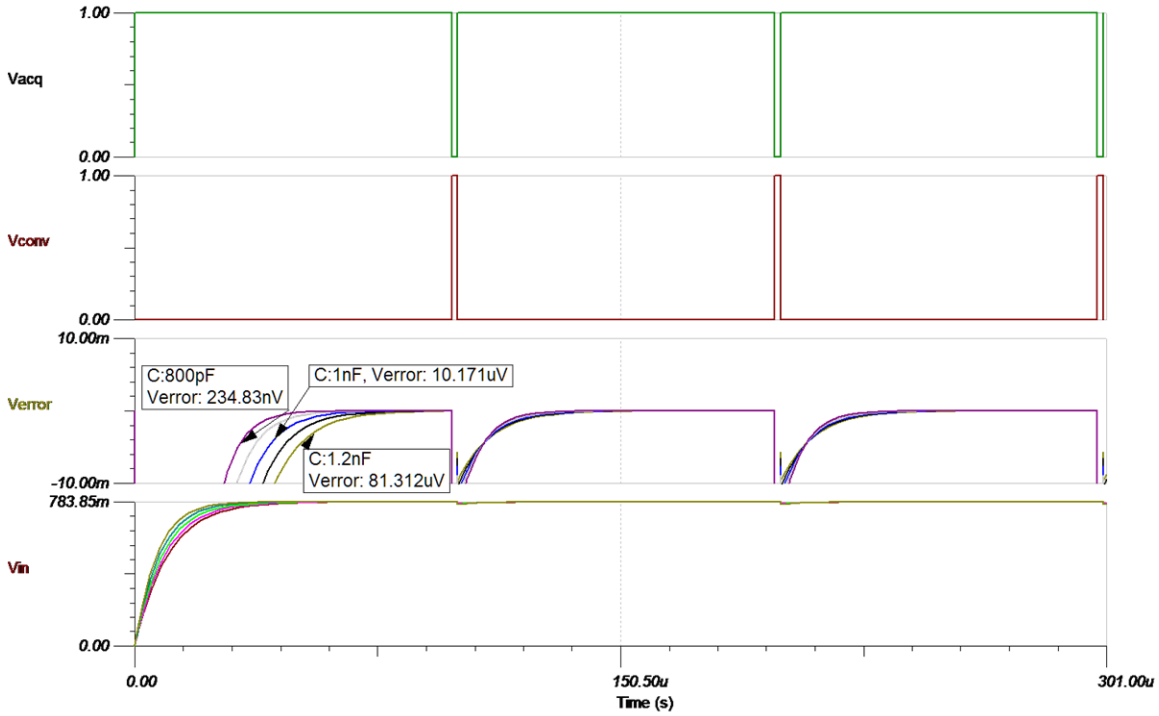
Selecting the capacitor value with simulation

This section uses the model shown in the “Design simulations model” section to choose a capacitor to optimize settling.

1. In the model, change the NTC to the maximum equivalent resistance value of 35.631kΩ as this will be the worst-case settling scenario. Run a DC nodal voltage simulation to find the expected ADC input. Using this measurement set V4. The voltage at V4 will be compared to the input through the V error voltmeter and demonstrate if the input is settling to less than ½ LSB, of 402µV.

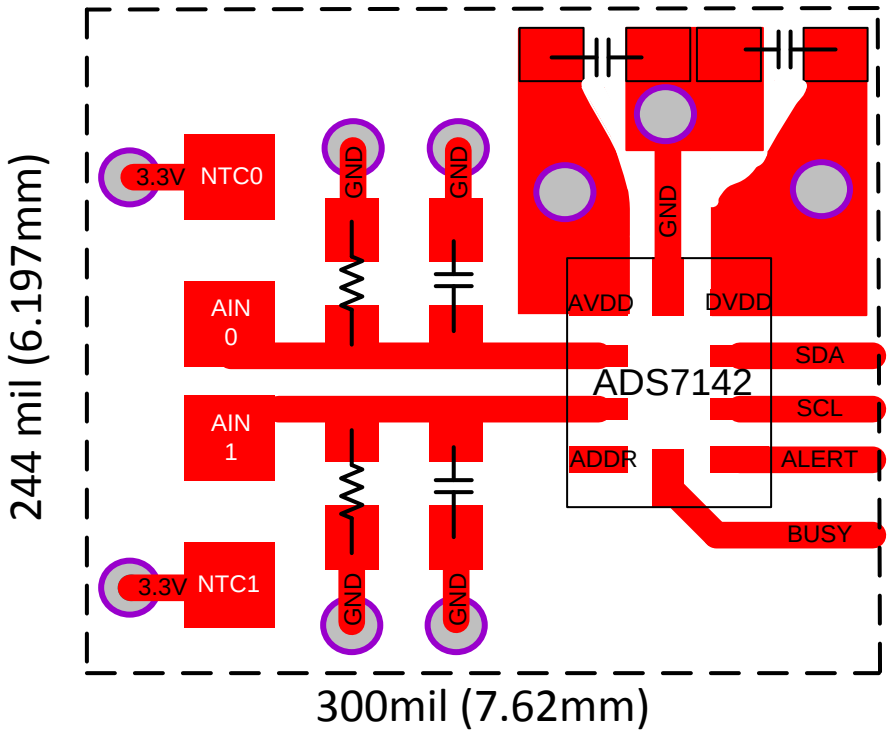


2. Run a parametric sweep of the capacitor value. Simulation results will dictate where to narrow the capacitor value range based on the final settling error. The following images shows an acceptable range of capacitor values of 800pF to 1.2nF, based on settling error. A 1-nF capacitor was chosen because it was the largest capacitor value to show best settling. For details on simulating ADC settling see *Refine the Rfilt and Cfilt Values*.



Small Layout

The ADS7142 is a dual-channel I2C analog-to-digital converter in a small X2QFN package size of 1.5mm × 2mm. The following image is a system-level solution using the ADS7142 with two NTCs connected at each analog input, though each input can monitor different types of sensors.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS7142[1]	12-bit resolution, I2C, autonomous monitor, dual-channel single-ended input, small package size: 1.5mm × 2mm	http://www.ti.com/product/ADS7142	http://www.ti.com/adcs
ADS7042[1]	12-bit resolution, SPI, 1MSPS sample rate, single-ended input, AVDD, Vref input range 1.6V to 3.6V	http://www.ti.com/product/ADS7042	http://www.ti.com/adcs

(1) The ADS7142 and ADS7042 use AVDD as the reference input. A high-PSRR LDO, such as the TPS7A47, should be used as the power supply.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Simulation Files

http://www.ti.com/lit/zip/sbac283

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