

TI Designs HSP: Verified Design

Analog Interfacing Networks for DAC348x and Modulators



TI Designs HSP

TI Designs HSP designs are analog solutions created by TI's analog experts. Verified Designs offer the theory, part selection, simulation, complete PCB schematic & layout, bill of materials, and measured performance of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

Design Resources

TINA Spice	SPICE Models (Referenced)
TINA Spice	SPICE Simulator
DAC3482	Product Folder
DAC3484	Product Folder
DAC34H84	Product Folder
DAC34SH84	Product Folder
TRF370315	Product Folder
TRF370317	Product Folder
TRF370417	Product Folder
TRF3705	Product Folder
TRF372017	Product Folder
TSW3085EVM	Tools Folder
TSW3085 Design Package	Schematic, PCB Layout, BOM
TSW3084EVM	Tools Folder
TSW3084 Design Package	Schematic, PCB Layout, BOM
TSW30H84	Tools Folder
TSW30SH84	Tools Folder
TSW30H84 and TSW30SH84 Design Package	Schematic, PCB Layout, BOM

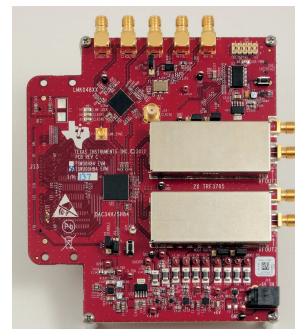
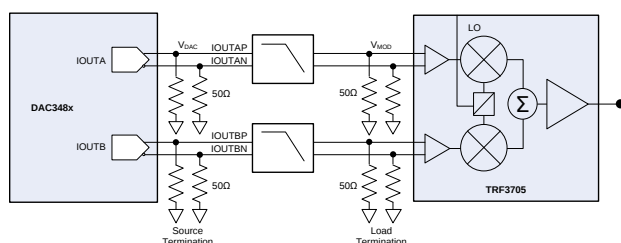
Circuit Description

The analog interface circuits in this design note are often used between current-source based digital-to-analog converters (DAC) and quadrature modulators. While the DAC348x is used as an example of a TI high-speed DAC, the circuits can be applied to other current-source based converters with slight modifications.

The DAC348x and TRF3705 analog interface are populated by default on the TSW308xEVMs. Both the DAC348x and TRF3705 are designed with the same DC bias and AC swing specification to provide seamless interface. Other circuit topologies are described to account for other DC bias and AC swing specifications. By accounting the correct DC bias and proper AC swing, system designers can apply these circuits based on their application needs in order to achieve optimal performance.



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1 Introduction

The DAC348x family provides high-performance digital-to-analog conversion (DAC) for many applications. The DAC is often part of the signal chain in the system with many down-stream analog components such as amplifiers, I/Q modulators, or mixers attached. While some are custom fit by design, typically, these down-stream analog components have different biasing, AC swing, and impedance requirements that are different than the DAC348x family. Therefore, achieving optimal performance requires proper design of the interfacing network. This reference design covers various interface-network options and design considerations for the TI modulators. These examples serve as guidelines in the design of interface networks for various down-stream analog components.

2 Definitions

IOUTFS: the full-scale output current of the DAC348x. Nominally set to 20 mA in this document.

V_{DAC} : any DAC output nodes: IOUTAp, IOUTAn, etc.

V_{MOD} : any modulator input nodes: BBIP, BBIN, etc.

I_{DAC_DC} : the average DAC output current. For 20-mA FS, $I_{DAC_DC} = 10$ mA.

R_{EQ_MOD} : the equivalent DC resistance of the modulator input.

V_{CC} : positive bias supply for the dual-supplies bias interface-network.

V_{EE} : negative bias supply for the dual-supplies bias interface-network.

V_{BIAS} : bias supply for the single-supply bias interface-network

3 DAC348x Output Operation

The DAC348x is a CMOS current output digital-to-analog converter (DAC). Therefore, the amplitude of the output voltage depends on the output load impedance with a $V = IR$ relationship. The DAC consists of a segmented array of PMOS current sources which are capable of sourcing a full-scale output current up to 30 mA.

The equivalent circuit of this output is represented as a current source controlled by the DAC input digital code, as shown in [Figure 1](#). Each bit causes the current source to switch out a fixed amount of current. The output architecture requires that both the complementary output nodes, IOUTP and IOUTN, terminate to ground. Differential current switches direct the current to either one of the complementary output nodes. Complementary output currents enable differential operations, thus canceling output common-mode noise sources (digital feed-through, and both on-chip and PCB noise), DC offsets, even-order distortion components, and increasing signal-output power by a factor of four.

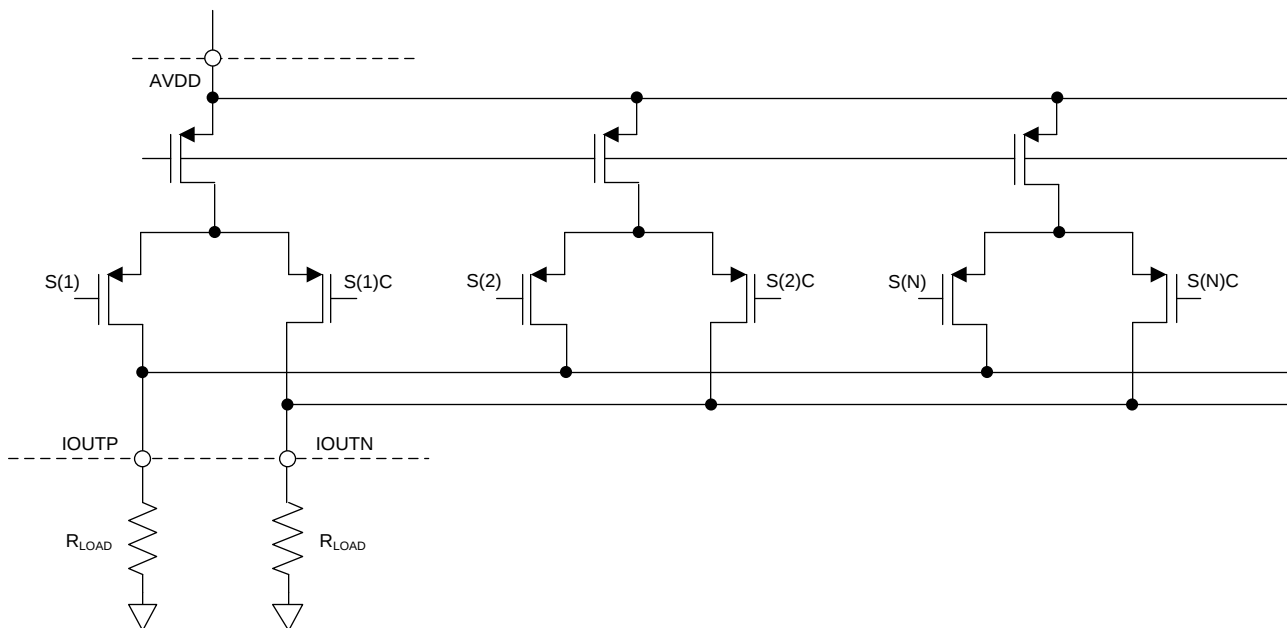


Figure 1. Current Source Array

The full-scale output current is set using an external resistor, R_{BIAS} , in combination with an on-chip bandgap voltage reference-source (+1.2 V) and control amplifier. Current (I_{BIAS}) through resistor (R_{BIAS}) is mirrored internally to provide a maximum full-scale output current equal to $64 \times I_{BIAS}$.

The relation between IOUTP and IOUTN is expressed as:

$$IOUTFS = IOUTP + IOUTN$$

The TI data sheet (see [Section 9](#)) denotes current flowing into a node as negative current, and current flowing out of a node as positive current. Because the output stage is a current source, the current flows from the IOUTP and IOUTN pins. The output current flow in each pin driving a resistive load is expressed as:

$$IOUTP = IOUTFS \times \text{CODE} / 65536$$

$$IOUTN = IOUTFS \times (65535 - \text{CODE}) / 65536$$

where CODE is the 16-bit decimal representation of the DAC data input word, which ranges from 0 to 65535. For the case where IOUTP and IOUTN drive resistor loads R_{LOAD} directly, this translates into single ended voltages at IOUTP and IOUTN:

$$VOUTP = IOUTP \times R_{LOAD}$$

$$VOUTN = IOUTN \times R_{LOAD}$$

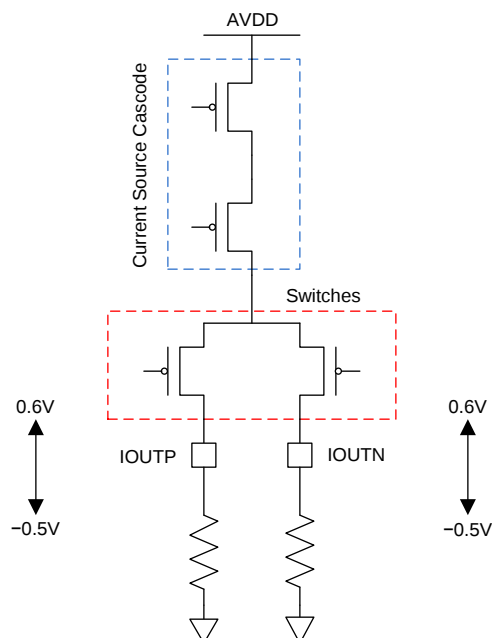
Assuming that the data is full scale (65535 in offset binary notation) and the R_{LOAD} is 25 Ω , the differential voltage between pins IOUTP and IOUTN is expressed as:

$$VOUTP = 20 \text{ mA} \times 25 \Omega = 0.5 \text{ V}$$

$$VOUTN = 0 \text{ mA} \times 25 \Omega = 0 \text{ V}$$

$$V_{DIFF} = VOUTP - VOUTN = 0.5 \text{ V}$$

An ideal current source generates larger amplitude voltage output if a larger load is attached. However, for practical current-source designs, the current source output should operate within the recommended compliance voltage limit. Each complementary output node of DAC348x, IOUTP or IOUTN, has a recommended output compliance voltage range of -0.5 to $+0.6$ V, as shown in [Figure 2](#). Exceeding the compliance voltage limit can result in reduced reliability of the device or adversely affect distortion performance.



ELECTRICAL CHARACTERISTICS – DC SPECIFICATIONS⁽¹⁾

over recommended operating free-air temperature range, nominal supplies, $I_{OUT_FS} = 20\text{mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT					
Course gain linearity			±0.04		LSB
Offset error	Mid code offset		±0.001		%FSR
Gain error	With external reference		±2		%FSR
	With internal reference		±2		%FSR
Gain mismatch	With internal reference		±2		%FSR
Full-scale output current		10	20	30	mA
Output compliance range		-0.5		0.6	V
Output resistance			300		kΩ
Output capacitance			5		pF

(1) Measured differentially across IOUTP/N with 25Ω each to GND.

Figure 2. DAC348x Compliance Voltage Range

Thorough DC and AC characterizations of the DAC348x over the recommended compliance voltage have been completed by TI. The specification and performance are found on the DAC348x datasheet (see [Section 9](#) for list of datasheets) on the TI web.

3.1 Current Source Array Simulation Model in TINA-TI™

The current source array can be modeled in any SPICE based simulation program. As shown in Figure 3, the full-scale current-source sine-wave output into R_{LOAD} of 25 Ω can decompose into both the DC component and AC component. The DC component is simply the time average of the IOUTP and IOUTN, while the AC component is the time-varying waveform of the IOUTP and IOUTN without the DC waveform.

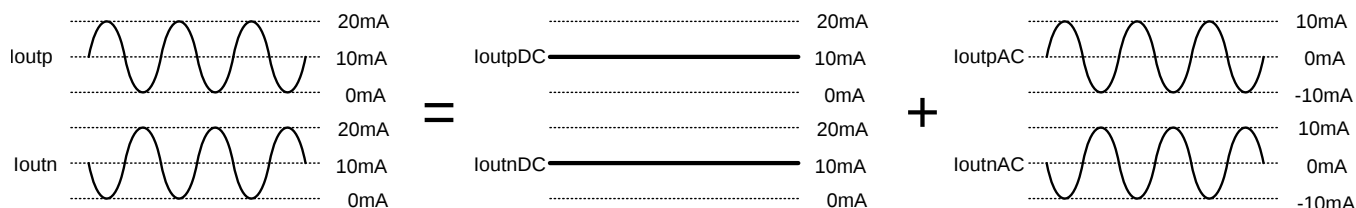


Figure 3. Decomposition of the 20-mA Full-Scale Output into the DC and AC Components

Assuming a 20-mA full-scale current, the DC component is equivalent to a 10-mA DC source while the AC component is equivalent to a 10-mA peak AC source. Based on the principle of superposition, the SPICE model can be generated. The current-source array model consists of DC current source and AC current source. These two current sources form the 20-mA full-scale current. The SPICE model components and an example TINA-TI SPICE model are shown in Figure 4.

SPICE Modeling of DAC Current Source Array

Equivalent TINA-TI SPICE Model

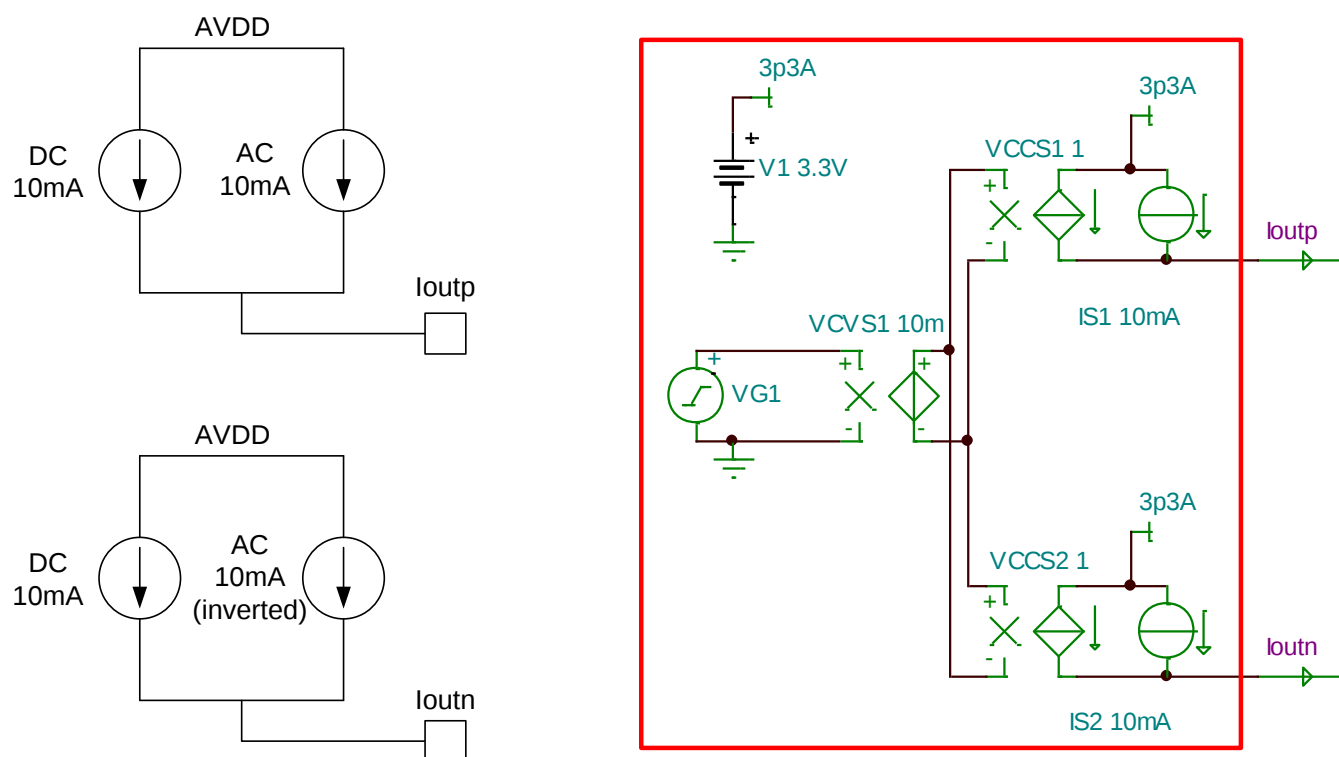


Figure 4. SPICE Modeling of DAC Current-Source Array and Equivalent TINA-TI Model

Before using the TINA-TI™ simulation, please see the Quick Start Guide, *Getting Started with TINA-TI: A Quick Start Guide*, [SBOU052](#).

4 DAC348x to TRF3705 Interface

The TRF3705 is ideally suited to interface with the DAC348x family because there is no translation network required and the common mode of the TRF3705 is typically set at 0.25 V. The interface network is shown in Figure 5.

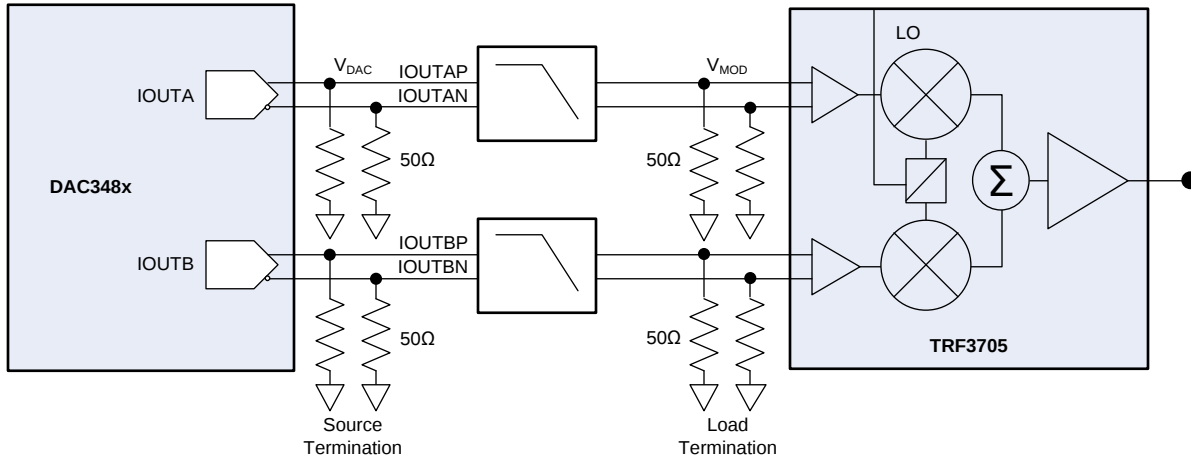


Figure 5. DAC348x to TRF3705 Interface

The goal of the interface design is to provide proper 0.25-V biasing for the TRF3705 while maximizing the AC swing of the DAC348x and keeping the output within the recommended compliance voltage range. Based on the characterization data, a 20-mA full-scale current has shown optimal AC performance, which is a factor to consider for interface design. With a 20-mA full-scale current, each complementary output node has an effective 10-mA DC current output, and the current setting with 25-Ω load creates the 0.25-V bias needed. Also, as previously mentioned, the 25-Ω load creates a 0.5-V peak differential-voltage output, or 1 V peak-to-peak.

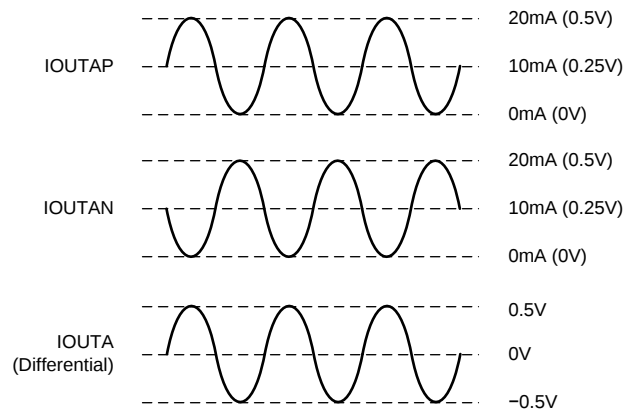


Figure 6. DAC348x and TRF3705 Interface Transient Response

Create balanced load and matching by splitting the 25-Ω load per output node into two parallel 50-Ω resistors. One 50-Ω resistor is placed at the source and another 50-Ω resistor is placed at the load. Therefore, the 100-Ω differential balanced termination filter is designed and placed in between the two parallel 50-Ω resistors. For best matching and gain flatness, place the first 50-Ω resistor as close to the DAC output as possible for source termination. Place the second 50-Ω resistor as close to the modulator input as possible for load termination. This interface design is also suitable for common PCB design with 100-Ω nominal differential-transmission line impedance, as other design constraints may raise PCB cost.

Simulate this interface circuit using the TINA-TI SPICE file: *DAC348x_TRF3705_Interface.TSC*. The circuit is shown in [Figure 7](#).

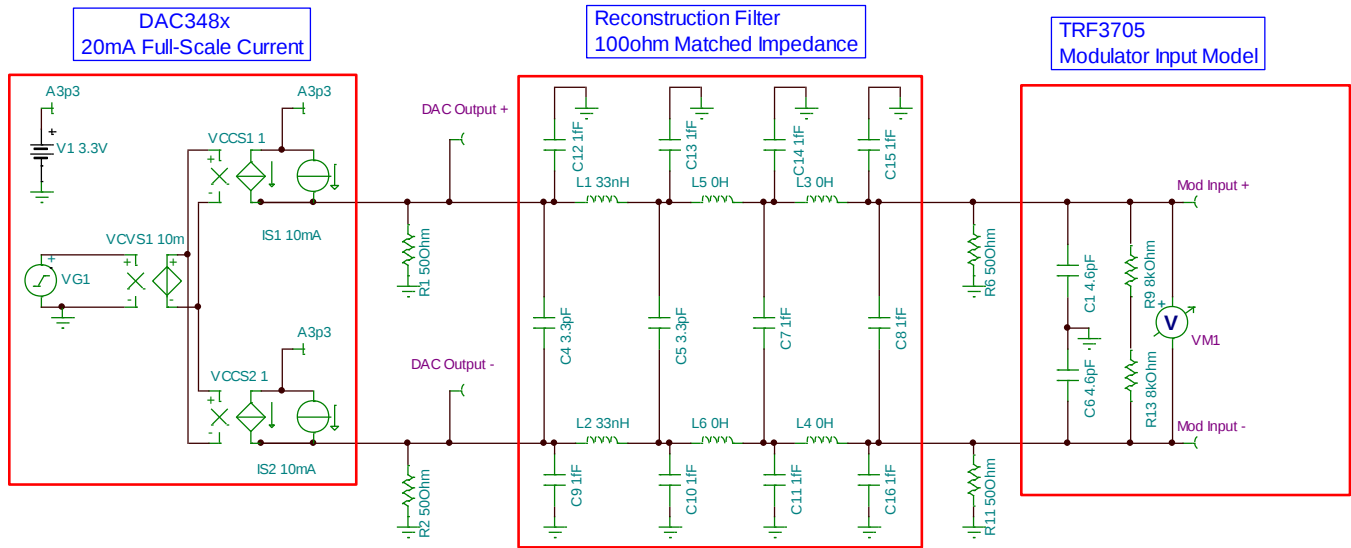


Figure 7. Typical DAC348x and TRF3705 Interface Network in TINA-TI (TSW308xEVM Default Network)

5 Single-Supply Level Translation

Interfacing the DAC348x to a higher common-mode voltage modulator requires a pullup voltage source and a resistor-divider network consisting of three resistors. The resistor-divider network of R4, R3, and a parallel combination of R1 and R2, can bias the DAC348x at lower common-mode voltage and bias the modulator at higher common-mode voltage. Place source-termination resistors, such as R1, immediately at the DAC output. Load-termination resistors, such as R2, terminate the transmission line. Place the R2, R3, and R4 network as close to the modulator input as possible. Refer to [Figure 8](#) for details.

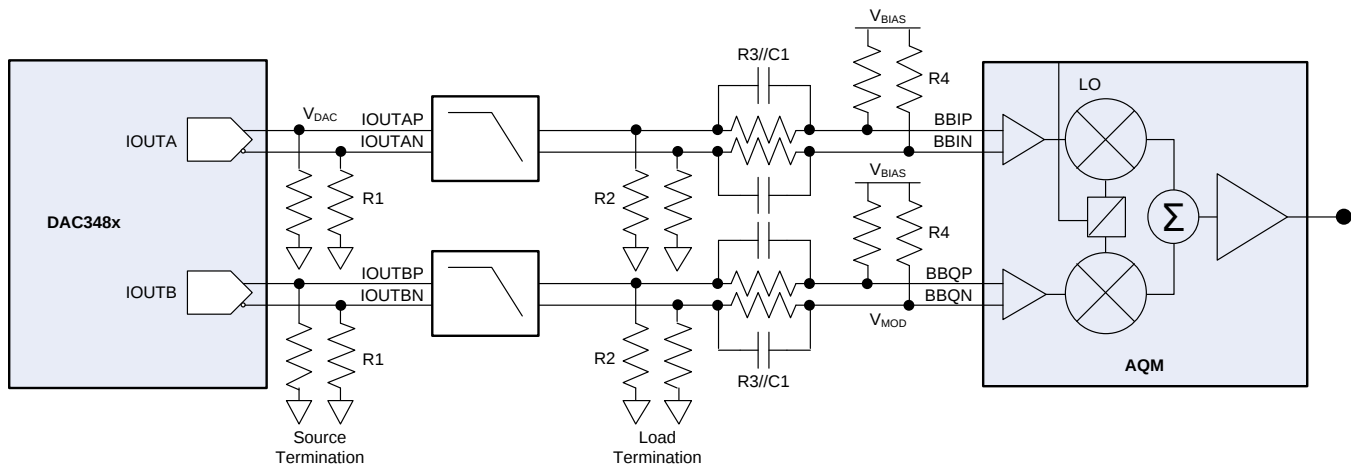


Figure 8. Single Supply Interface Network

Resistor values are calculated by writing Kirchhoff's Current Law (KCL) equations at node V_{DAC} and node V_{MOD} . DC analysis is applied to solve the resistor values required for the proper bias point.

$$\begin{aligned} \text{At node } V_{DAC}: I_{DAC_DC} + (-V_{DAC}) / (R1 // R2) + (V_{MOD} - V_{DAC}) / R3 &= 0 \\ \text{At node } V_{MOD}: (V_{BIAS} - V_{MOD}) / R4 + (-V_{MOD} / R_{EQ_MOD}) + (V_{DAC} - V_{MOD}) / R3 &= 0 \end{aligned}$$

Consider the following points for the interface network design:

1. R1 and R2 should have the same impedance for best source and load matching. Assume R3 and R4 are much larger than R1 and R2.
2. Maximize the AC swing by setting the DAC348x output bias (V_{DAC}) to approximately 0.25 V. The combination of output load and output current can create a 0.5-Vpp single-ended, or 1-Vpp differential swing.
3. Improve the modeling of the network by introducing the R_{EQ_MOD} variable. This variable is the equivalent DC input impedance of the modulator, and it has been verified empirically with the current recommended networks.
 - (a) For the TRF370315, TRF370317, and TRF370417, the R_{EQ_MOD} is approximately 20 k Ω .
 - (b) For the TRF372017, the R_{EQ_MOD} is 5 k Ω to ground with the internal 1.7-V reference disabled. The TRF372017 has the ability to generate the internal 1.7-V reference. Disable the internal reference for this network because the bias is externally generated.

Table 1. Interface-Network Component Values Using 5-V Bias, DAC output set at 20 mAFS

Modulator	V_{CM} (V)	R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	R_{EQ_MOD} (Ω)
TRF370315	1.5	47.5	47.5	1000	2740	20000
TRF370317	1.7	47.5	47.5	1150	2490	20000
TRF370417	1.7	47.5	47.5	1150	2490	20000
TRF372017	1.7	47.5	47.5	1200	2150	5000

The expected output swing of the DAC and the translated input swing of the modulator is shown in [Figure 9](#). Note that the common mode of the DAC output has been shifted up to the expected common mode (V_{CM_MOD}) of the modulator. The effective AC swing remains at 1Vpp.

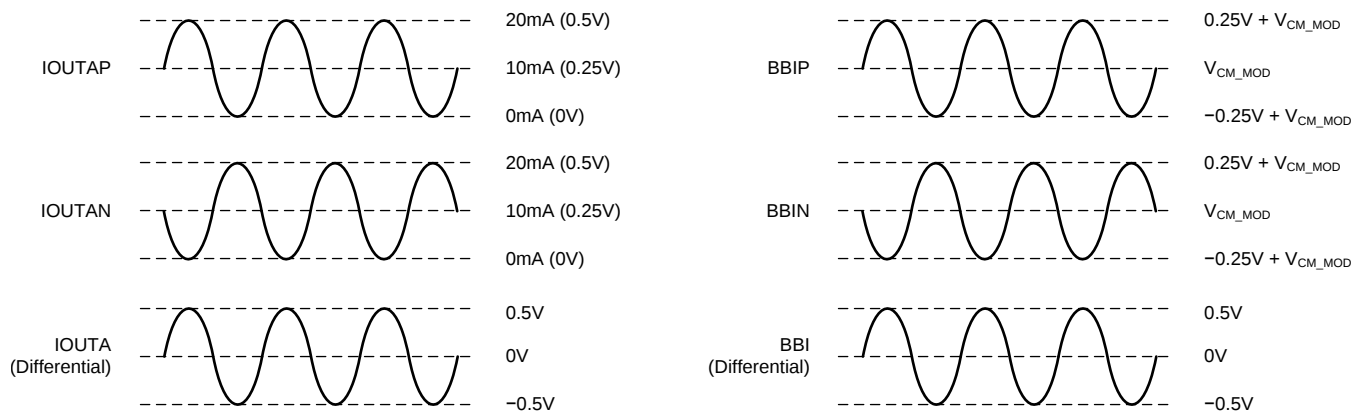


Figure 9. Single-Supply Interface Transient Response

Typically, in order to interface the DAC348x with some of the popular modulators such as TI's TRF370315 or TRF370417, series resistor R3 must be in the 1-k Ω range. This series resistance creates higher loss that limits the output power. R3 can also interact with the input capacitance of the modulator to create roll-off, which limits the signal bandwidth. Both outcomes may impact the overall system performance.

Overcome these limitations by placing pseudo-DC capacitors, such as C1, in parallel to series resistors R3. The intention is to create an AC short to eliminate the loss and roll-off effects created by R3. The effective 3-dB high-pass corner is estimated by [Equation 1](#).

$$nF_c = 1 / (2\pi R_3 C_1) \quad (1)$$

As shown in [Figure 10](#), with the C1 capacitor value set to 1 μ F, the 1-dB high-pass corner is less than 1 kHz. For zero-IF systems, this network can be acceptable depending on the modulation scheme being used. For example, some OFDM modulation schemes have symbol boundaries above 1 kHz and can adopt this type of interface network. System designers must consider this limitation prior to the circuit implementation.

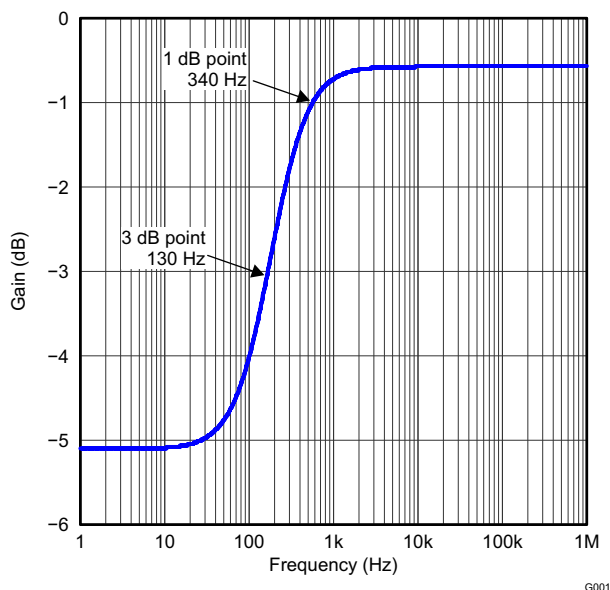


Figure 10. Frequency Response of the Pseudo-DC Network (Example Shown: DAC348x + TRF30417, 5-V Bias)

Simulate this interface circuit using the TINA-TI SPICE file: *DAC348x_TRF370417_Interface.TSC*. The circuit is shown in **Figure 11**.

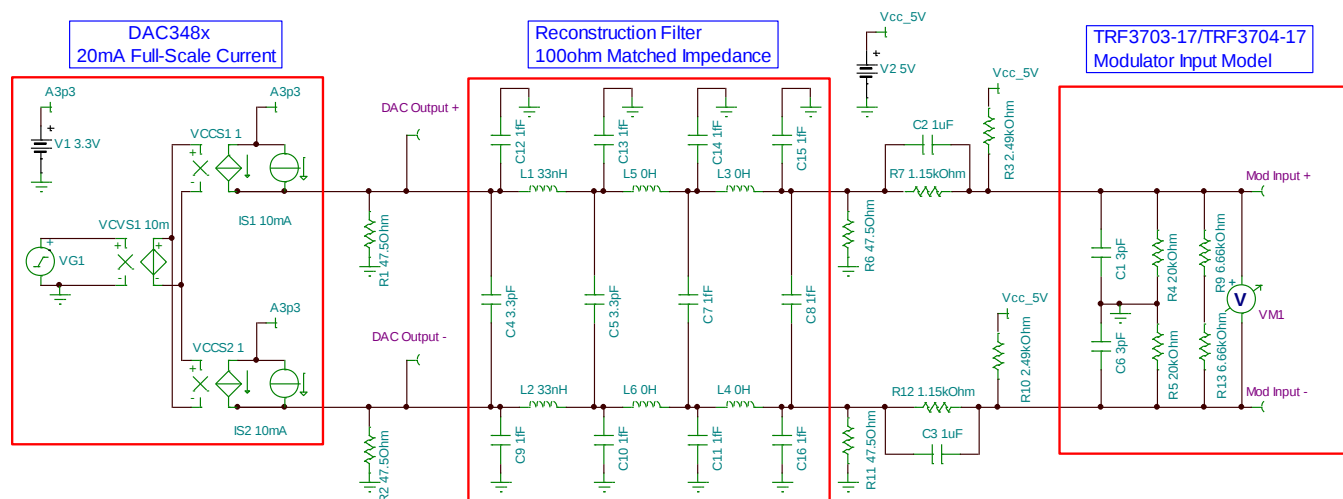


Figure 11. Typical DAC348x and TRF370417 Interface Network in TINA-TI (TSW308xEVM Optional Network)

6 Dual-Supplies Level Translation

Single-supply biasing limits the DAC348x output to positive swing only. If the DAC348x output is biased with the available negative supply rail, the negative-compliance voltage limit is achieved. Using this method, the DAC348x works in applications requiring higher output swing. Two types of dual-supplies networks are used: matched impedance and pseudo-DC matched impedance.

6.1 Dual-Supplies Matched-Impedance Network

Dual-supplies matched-impedance network, as shown in Figure 12, is useful for applications that require flat-frequency response near DC and can tolerate the attenuation from the translation network. R1, R2, and R3 bias the DAC output near 0 V while biasing the modulator input at the optimal common-mode voltage of the modulator input. The equivalent AC impedance of R1, R2, and R3 forms the DAC-output source impedance, while the differential R4 resistor forms the modulator input load impedance. R4 is set at differential in order to not affect the DC bias of the network and to simplify the design.

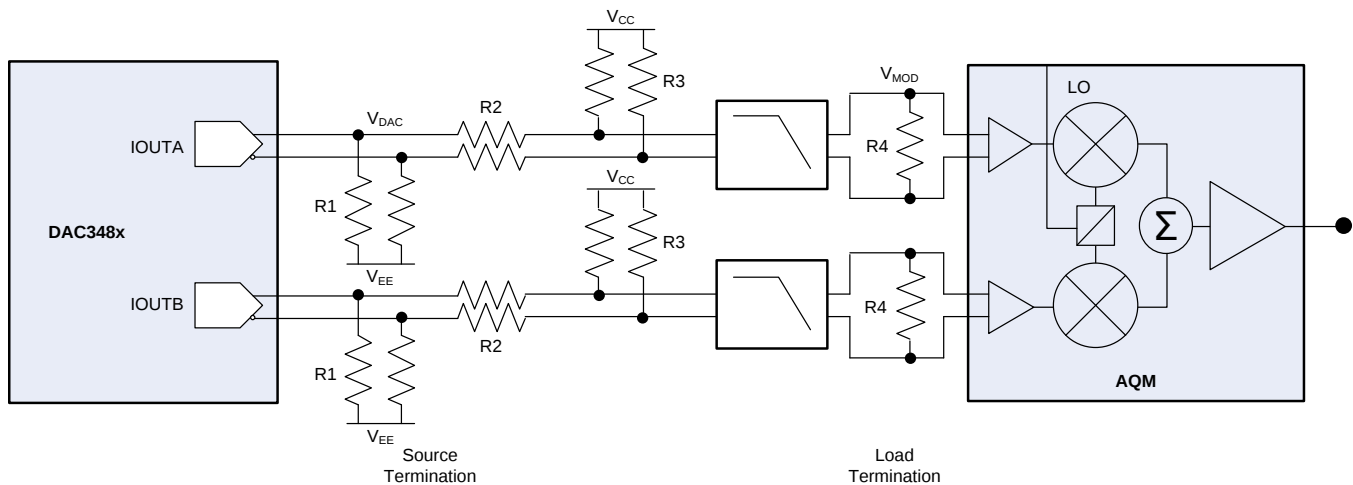


Figure 12. Dual-Supplies Matched-Impedance Interface Network

Resistor values are calculated by writing KCL equations at node V_{DAC} , and node V_{MOD} . DC analysis is applied to solve the resistor values required for the proper bias point.

$$\text{At node } V_{DAC}: I_{DAC_DC} + (V_{EE} - V_{DAC}) / (R1) + (V_{MOD} - V_{DAC}) / R2 = 0$$

$$\text{At node } V_{MOD}: (V_{CC} - V_{MOD}) / R3 + (V_{DAC} - V_{MOD}) / R2 = 0$$

Because the goal of the design is to provide matched impedance for the filter network, make the equivalent source impedance and load impedance equal.

$$R3 // (R2 + R1) = R4 / 2$$

Because the series resistance (R2) that is required for the bias-level translation, R2 interacts with the effective resistance of R3 and R4 and attenuate the signal. The attenuation is calculated by the effective resistor-divider network as shown in Equation 2.

$$\text{attenuation} = \frac{R3 // \frac{R4}{2}}{(R3 // \frac{R4}{2}) + R2} \quad (2)$$

With the availability of the negative supply network, the final output swing of the DAC output achieves the full compliance voltage range. The baseband input swing (V_p) of the modulator is the full DAC-output swing with the attenuation of the R2, R3, and R4 interaction. The transient response of this network is shown in Figure 13.

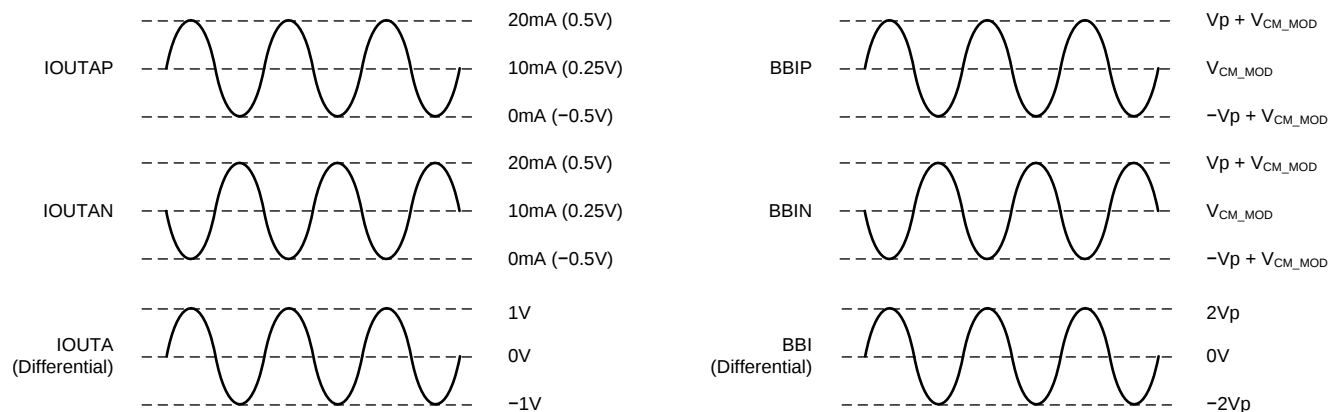


Figure 13. Dual Supplies Matched Impedance Interface Network Transient Response

Simulate this interface circuit using the TINA-TI SPICE file:

DAC348x_TRF370315_Dual_Supplies_DC.TSC. The circuit is shown in Figure 14.

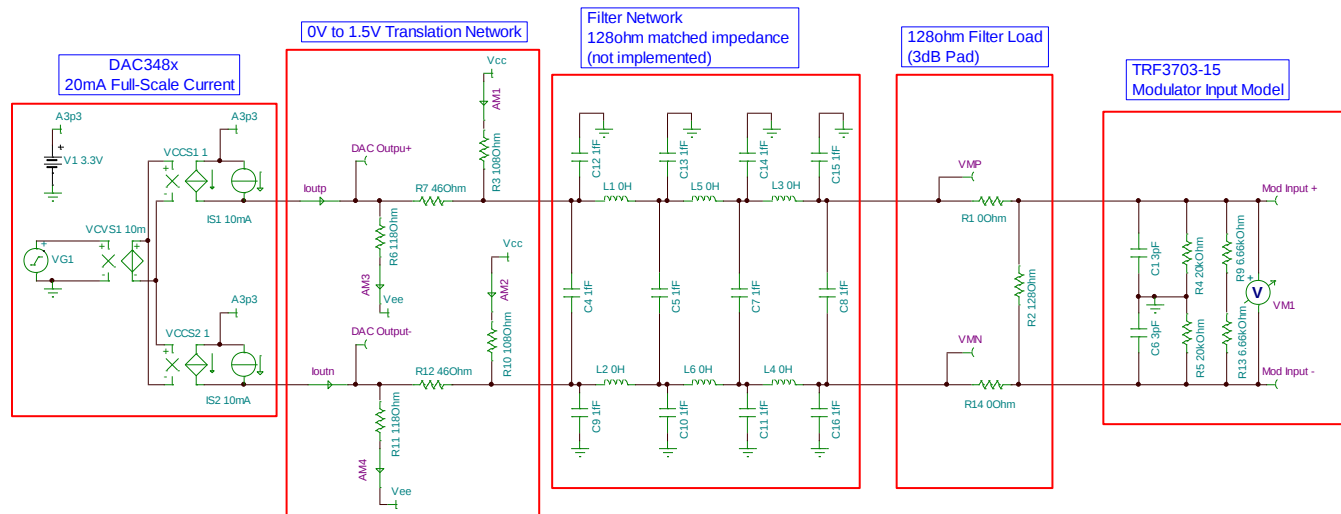


Figure 14. Typical DAC348x and TRF370315 Interface with Dual-Supplies DC Network in TINA-TI.

6.2 Dual-Supplies Matched Pseudo-DC Network

A dual-supplies matched pseudo-DC network, as shown in Figure 15, is useful for applications that require minimum translation loss of the interface network. R1, R2, and R3 bias the DAC output near 0 V while biasing the modulator input at its optimal common mode voltage. For the AC condition, the pseudo-DC capacitor shorts out the impedance of the series resistor, R2, to minimize translation loss. The equivalent AC impedance of R1 and R3 forms the DAC output source impedance, while the differential resistor, R4, forms the modulator input load impedance. Since the R4 resistor is differential between the positive and negative input of the modulator, this resistor does not affect the DC bias of the network.

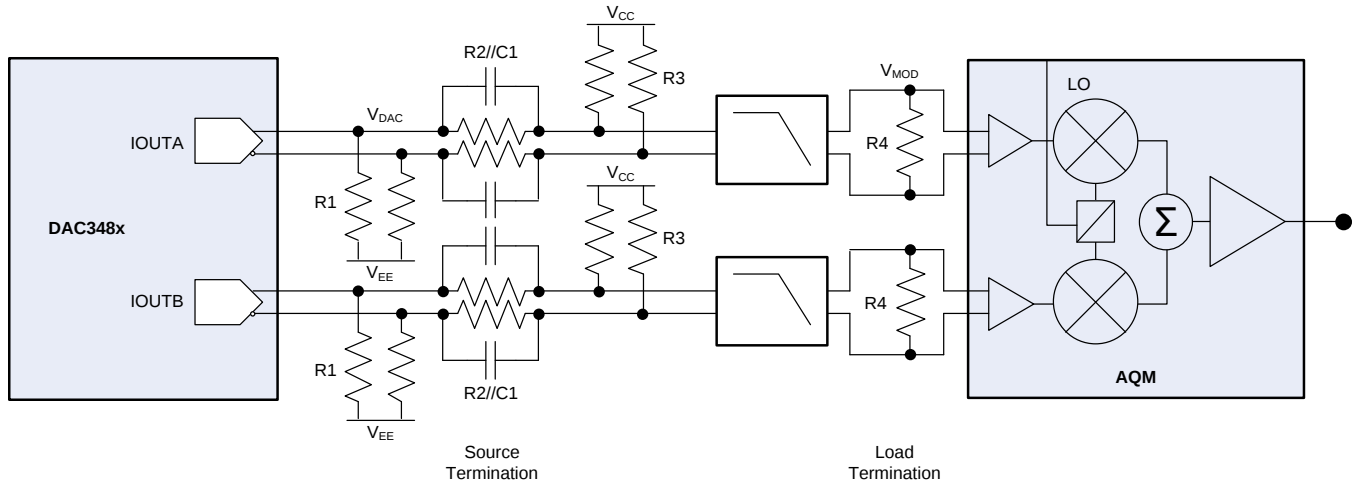


Figure 15. Dual-Supplies Pseudo-DC Interface Network

Resistor values are calculated by writing KCL equations at node V_{DAC} and node V_{MOD} . DC analysis is applied to solve the resistor values needed for the proper bias point.

$$\text{At node } V_{DAC}: I_{DAC_DC} + (V_{EE} - V_{DAC}) / (R1) + (V_{MOD} - V_{DAC}) / R2 = 0$$

$$\text{At node } V_{MOD}: (V_{CC} - V_{MOD}) / R3 + (V_{DAC} - V_{MOD}) / R2 = 0$$

Because the goal of the design is to provide matched impedance for the filter network, make the equivalent source impedance and load impedance equal.

$$R3 // (R1) = R4 / 2$$

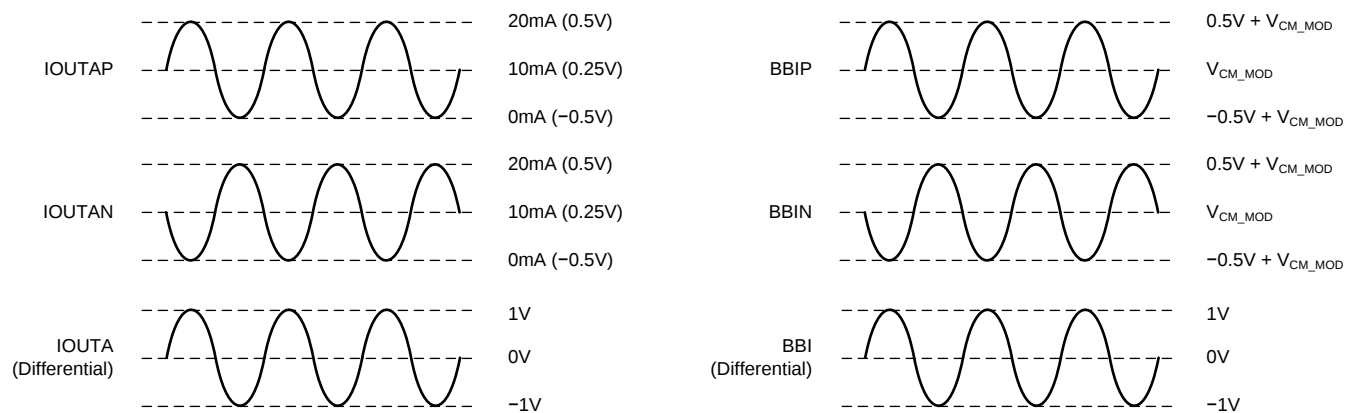


Figure 16. Transient Response of a Dual-Supplies Pseudo-DC Interface Network

The pseudo-DC capacitors, C1, are placed in parallel with the series resistor, R2, to create an AC short, which eliminates the attenuation created by the interaction of R2, R3, and R4 at low frequency. The effective 3-dB high-pass corner is estimated by Equation 3.

$$F_c = 1 / (2\pi R_2 C_1) \quad (3)$$

The exact cut-off frequency requires analysis of the equivalent resistance seen by the C1 capacitor. Use Equation 3 to approximate the cut-off frequency. Use TI's TINA SPICE model to simulate the exact cut-off frequency to speed-up design time.

Simulate this interface circuit using the TINA-TI SPICE file:

DAC348x_TRF370315_Dual_Supplies_Pseudo_DC.TSC. The circuit is shown in Figure 17.

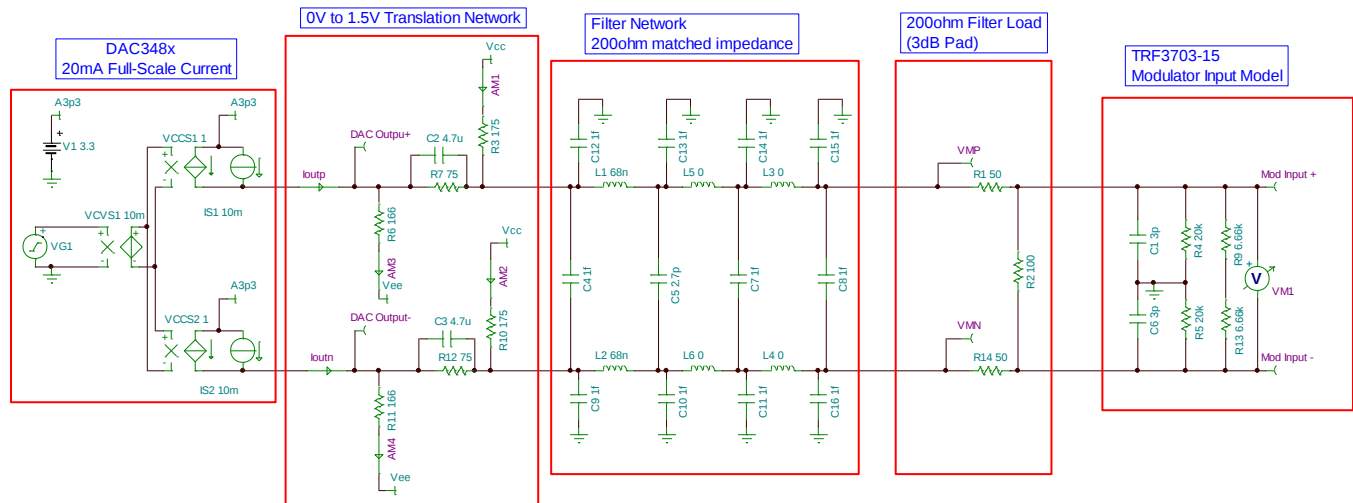
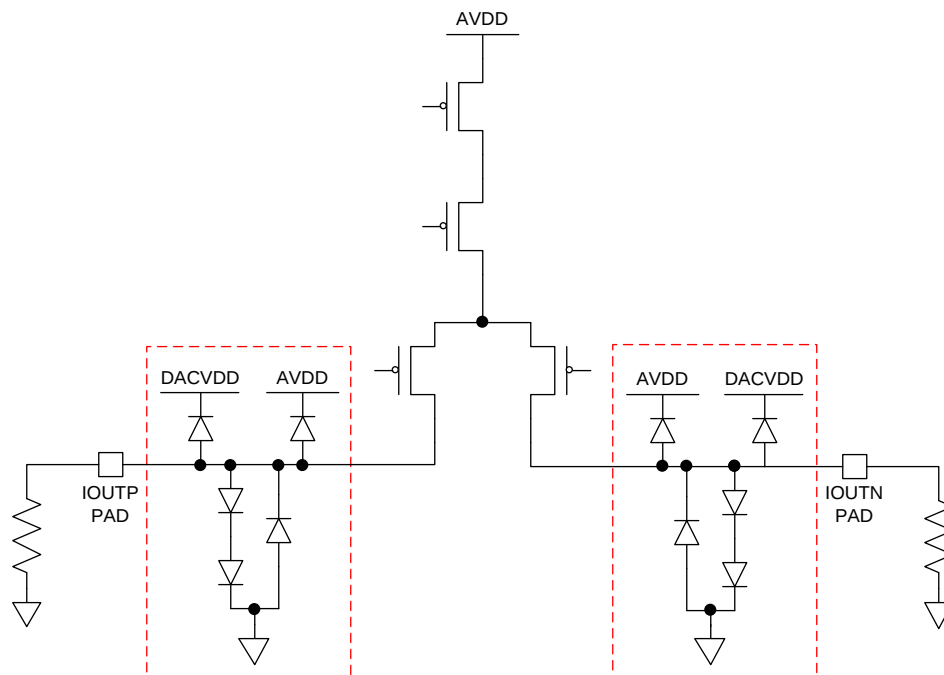


Figure 17. Typical DAC348x and TRF370315 Interface with Dual-Supplies (Pseudo-DC Network in TINA-TI)

6.3 Dual-Supplies Network Design Considerations

Consider the following points for the dual supplies interface network design:

1. Maximize the AC swing by keeping the DAC output common mode as close to 0 V as possible.
2. Depending on the available power supply rails and required bias common-mode voltage, the source impedance and load impedance may not be the common values of 50 Ω or 100 Ω. Adjust the AC swing and DAC output common mode for optimal impedance values.
3. Prevent permanent damage to the device by using the following design rules:
 - (a) TI recommends the DAC348x is always powered up before biasing the interface network rails.
 - (b) Consider the worst-case DAC output voltage when one of the biasing rails is on while the other one is off. This provides an estimate for the highest and lowest output biasing point when only one of the biasing rails is on. The DAC output is protected because the DAC348x output has internal ESD diodes that absorb the transient current and voltages. The ESD diodes can sink and source ±20 mA of current for hours without damaging the device permanently. However, as a conservative measure, keep the DAC output pins below 2 V and above –1 V at all times. Refer to Figure 18.



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		VALUE		UNIT
		MIN	MAX	
Pin voltage range ⁽²⁾	D[15..0]P/N, DATACLKP/N, FRAMEP/N, PARITYP/N, SYNCN/P	-0.5	IOVDD + 0.5	V
	DACCLKP/N, OSTRP/N	-0.5	CLKVDD + 0.5	V
	ALARM, SDO, SDIO, SCLK, SDENB, SLEEP, RESETB, TESTMODE, TXENABLE	-0.5	IOVDD + 0.5	V
	IOUTAP/N, IOUTBP/N, IOUTCP/N, IOUTDP/N	-1.0	AVDD + 0.5	V
	EXTIO, BIASJ	-0.5	AVDD + 0.5	V
	LPF	0.5	PLLAVDD + 0.5V	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Measured with respect to GND.

Figure 18. DAC348x Output ESD Cells

- (c) If the design requires the interface network bias supplies to start first, keep the DAC output pins below 2 V and above -1 V at all times. The DAC348x ESD diodes may turn on and conduct the supplies to the AVDD and DACVDD rails. The AVDD and DACVDD rails can be pre-biased at 1 V, and this pre-bias condition can damage the AVDD and DACVDD power supplies upon power-up. For example, some DC-DC power supplies do not have protections against pre-biased output and may damage the FET.

7 AC-Coupled Network

Some applications require the DAC output to achieve the full-compliance voltage range, but the system may not have the negative supply rail available to bias the DAC output for the negative swing. If the DAC output can be AC-coupled (no DC information needed), then the DAC interface can be either transformer coupled or inductor pulled-down.

7.1 1:1 Transformer-Coupled Network

Figure 19 shows the network for a 1:1 impedance ratio transformer-coupled network. The biasing between the DAC output and the down-stream device is isolated by a transformer. On the transformer primary side, the DAC output is biased through the transformer center tap to ground. On the transformer secondary side, the TRF372017 is shown as an example device with the option for internal biasing at 1.7 V. This feature simplifies the biasing circuit for an AC-coupled network. Other potential devices such as a mixer or an amplifier may require external biasing at the input.

Note the load termination at the TRF372017 is 100 Ω , which is required for the LO-feedthrough correction feature of the TRF372017. The internal DC-trim DAC requires the differential 100 Ω in order to trim the DC offset level at the modulator input. Other potential down-stream devices can also have internal 100- Ω termination. Because of the load termination requirement, the DAC output can provide higher swing, or the ability to swing to the negative rail, to meet the input power requirement. Also, with this network, the design can require a matched-impedance filter network with 100- Ω input and output design.

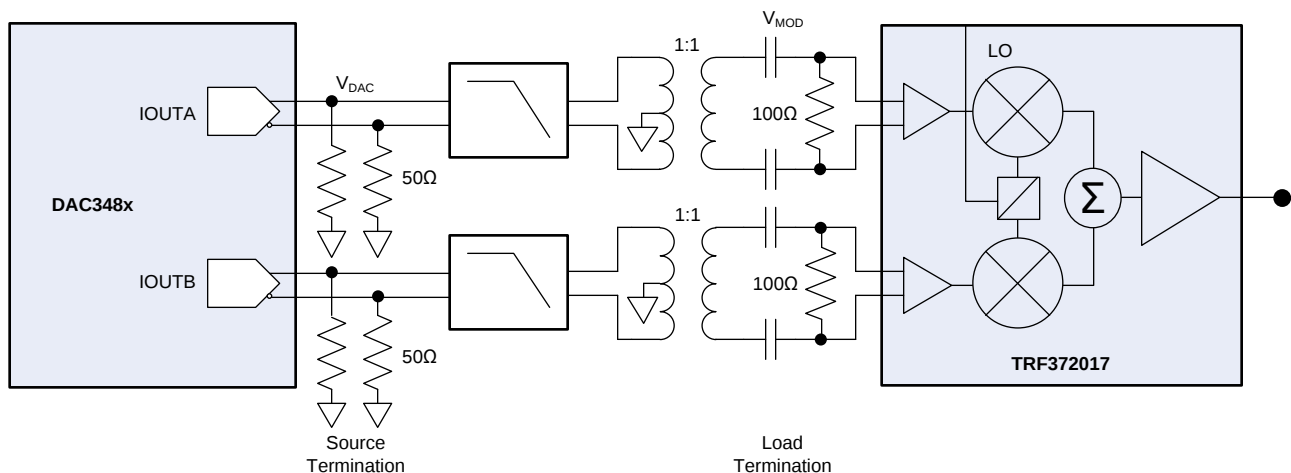


Figure 19. 1:1 Transformer-Coupled Network

With regard to AC-amplitude, both the source and load termination affect the output swing of the DAC. The total differential equivalent impedance as seen by the DAC is the two 50- Ω source resistance and the 100- Ω load resistance that is referred to the primary side. The parallel differential impedance is 50 Ω , and, with a 20-mA full-scale output-differential current, the DAC output can swing differentially from -0.5 to $+0.5$ V (1 Vpp). Because of the ability of the transformer to oppose changes in current through the transformer by developing a voltage that is proportional to the rate of change of the current, the DAC output can swing below ground. Figure 20 shows the transient response of the network. Note that if the 100- Ω load termination is not present, the DAC output can swing up to 2-Vpp differential because of the equivalent impedance of 100 Ω .

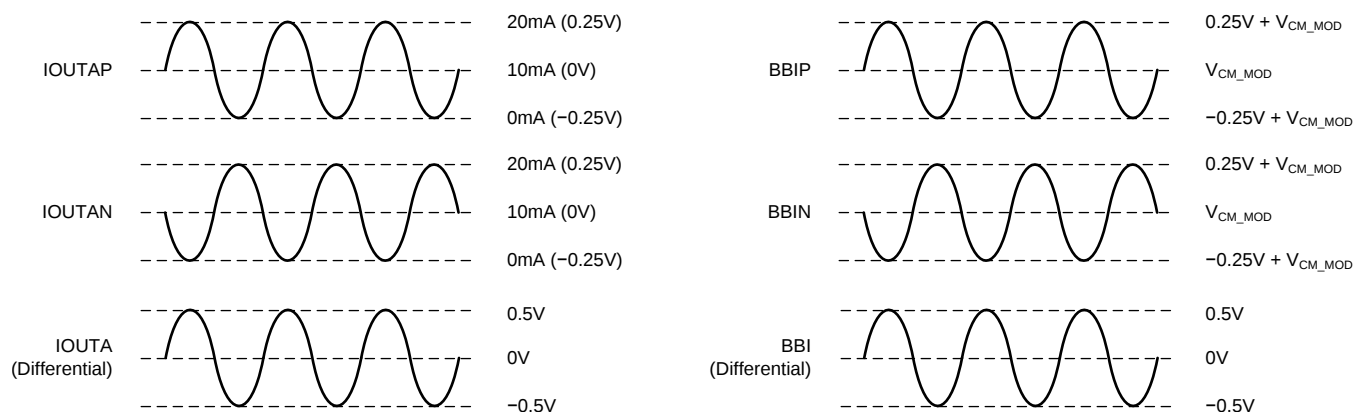


Figure 20. 1:1 Transformer-Coupled Network Transient Response

Simulate this interface circuit using the TINA-TI SPICE file: *DAC348x_1_1_XFRM_Coupled*. The circuit is shown in Figure 21.

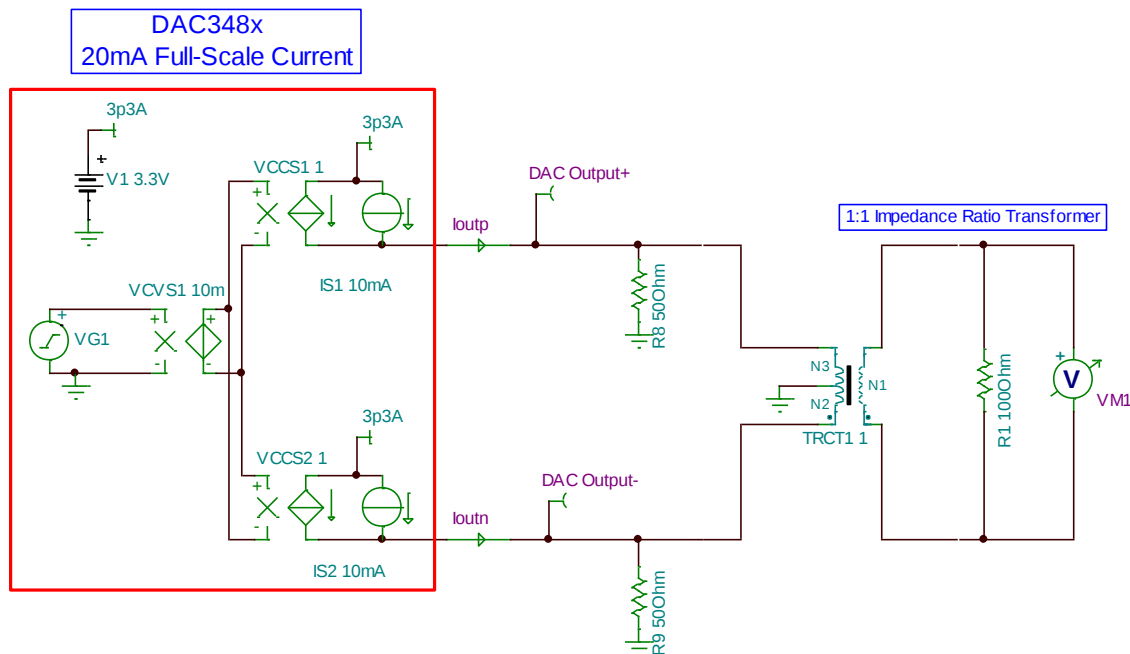


Figure 21. Typical DAC348x 1:1 Transformer Coupled Interface Network in TINA-TI

7.2 2:1 Transformer-Coupled Network

Figure 22 shows the network for a 2:1 impedance ratio transformer-coupled network. The total differential equivalent impedance as seen by the DAC is the two 100- Ω source resistance and the 200- Ω load resistance that is referred to the primary side. (The 100- Ω load termination is stepped up by 2:1 ratio from the secondary to the primary side). With this network, consider a matched impedance filter network with 200- Ω input and output design.

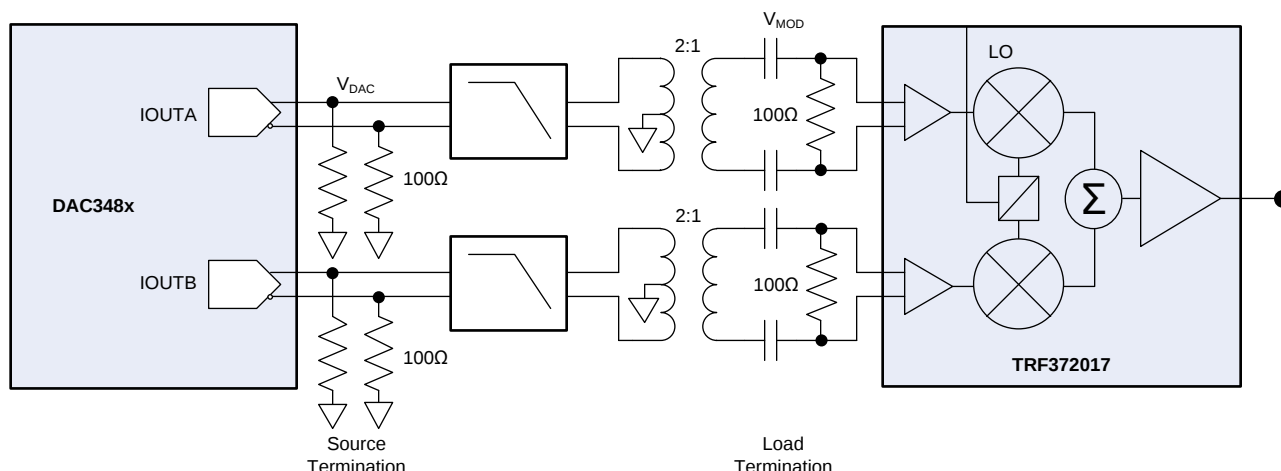


Figure 22. 2:1 Transformer-Coupled Network

When compared to the 1:1 impedance network, the parallel impedance is now 100 Ω , and with a 20-mA full-scale output differential current, the DAC output can swing from -1.0 V to +1.0 V (2Vpp) differentially. The swing at the input of the modulator is calculated by the voltage ratio of the transformer. The voltage ratio of the transformer is the square root of the impedance ratio, so a 2:1 impedance ratio transformer has a 1.414:1 voltage ratio. Therefore, the 2 Vpp differential output swing of the DAC is stepped down to 1.414 Vpp at the modulator input. Figure 23 shows the transient response of the network.

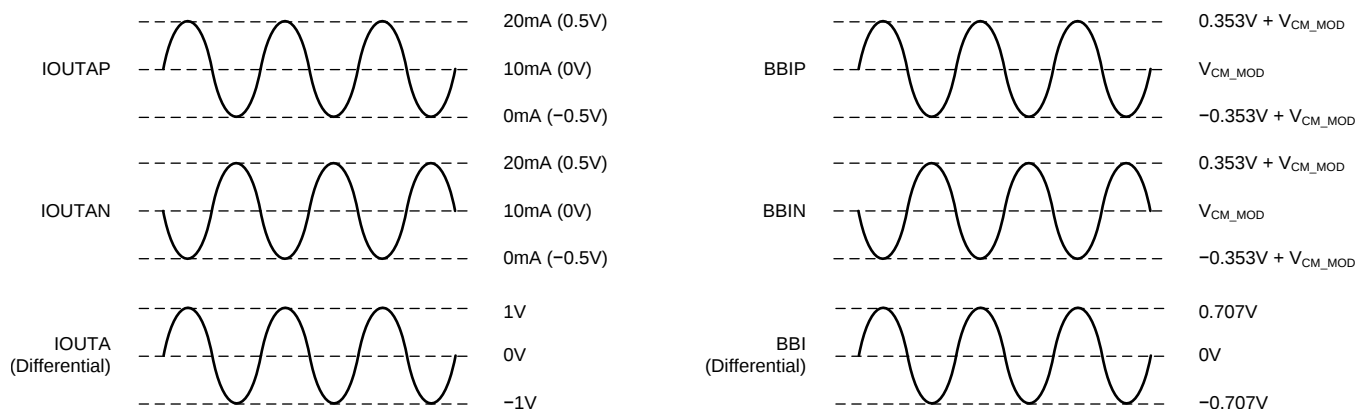


Figure 23. 2:1 Transformer-Coupled Network Transient Response

Simulate this interface circuit using the TINA-TI SPICE file: *DAC348x_2_1_XFRM_Coupled*. The circuit is shown in Figure 24.

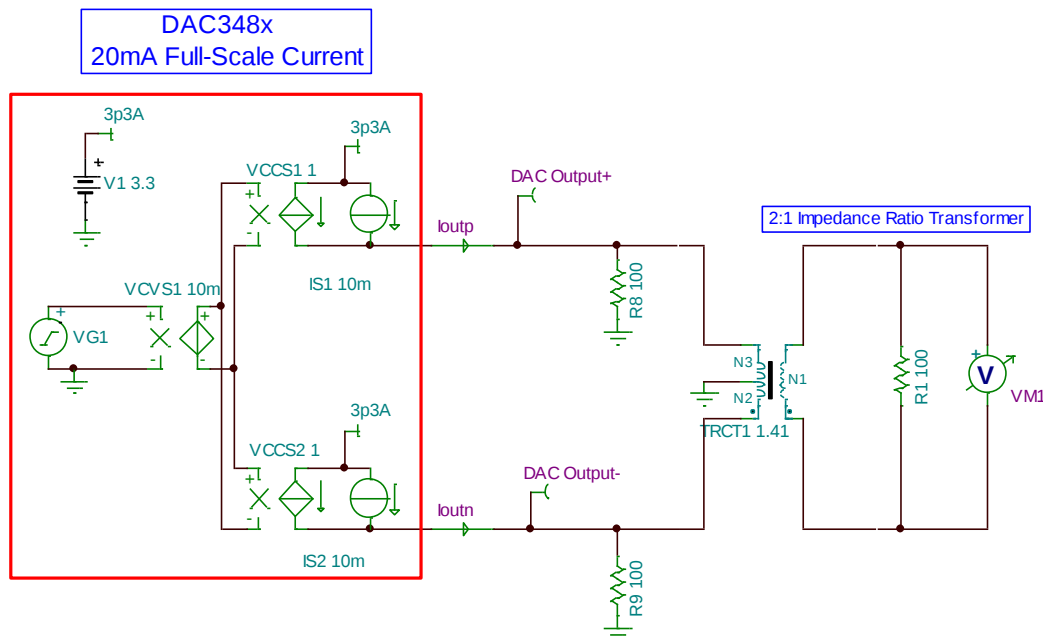


Figure 24. Typical DAC348x 2:1 Transformer-Coupled Interface Network in TINA-TI

7.3 Inductor Pulled-Down Network

Although the transformer-coupled network provides a seamless AC-coupled network interface with the ability of providing negative DAC output swing, design constraints such as cost may limit the feasibility of the implementation. A cost-effective technique, called inductor pulled-down network, may provide an alternative to the transformer-coupled network.

As shown in Figure 25, the inductor (L) can pull the DAC output to 0 V at DC. The AC-coupling capacitors provide DC isolation between the biasing of the DAC output and the modulator input. At a higher output frequency, the inductor (L) acts as a high-impedance load, and the effective load seen by the DAC are the 50-Ω pulldown resistors and the 100-Ω differential load. The frequency response is similar to a high pass response, with the inductor shorting out the DAC output at low frequency. The cut-off corner is approximated by Equation 4.

$$F_c = 1 / (2\pi L/R) \quad (4)$$

Because of this cut-off frequency, a large inductor value is necessary to push the cut-off corner as low as possible. When selecting components, the size and frequency range of the inductor may not be feasible for the design. Therefore, this type of network can be limited to high frequency output range applications. For instance, with the network shown in Figure 25, in order for a flat response from 150 MHz and above, the inductor is about 300 nH,

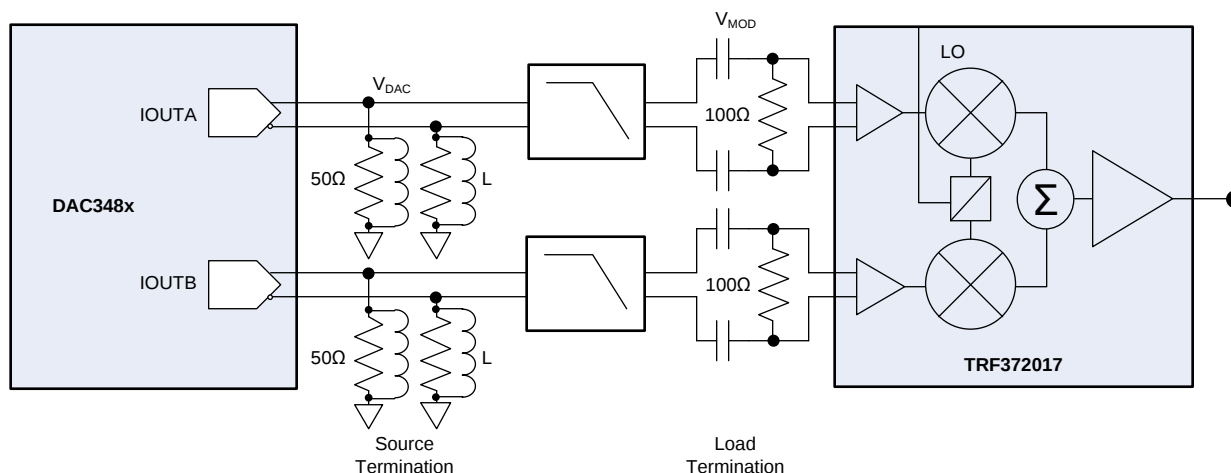


Figure 25. Inductor Pulled-Down Network

With regard to AC-amplitude, the total differential-equivalent impedance as seen by the DAC is the two 50-Ω source resistance and the 100-Ω load resistance. The parallel differential impedance is 50 Ω, and, with a 20-mA full-scale output-differential current, the DAC output can swing differentially from –0.5 to +0.5 V (1 V_{pp}). Similar to the transformer, the inductor acts as an energy storage element allowing the DAC to swing below ground. The transient response of the network is shown in [Figure 26](#).

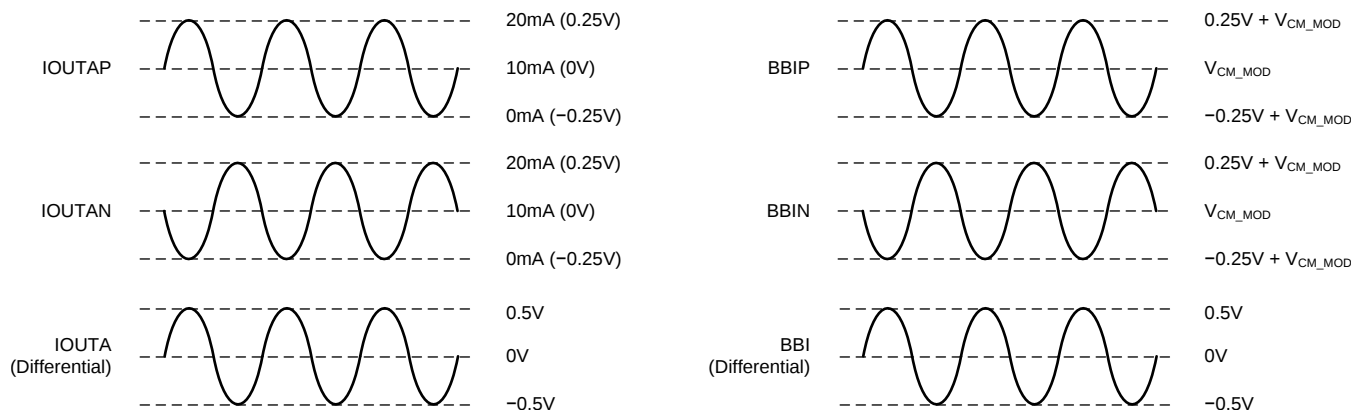


Figure 26. Inductor Pulled-Down Network Transient Response

Simulate this interface circuit using the TINA-TI SPICE file: *DAC348x_Inductive_Pull-Down_with_Filter*. The circuit is shown in [Figure 27](#).

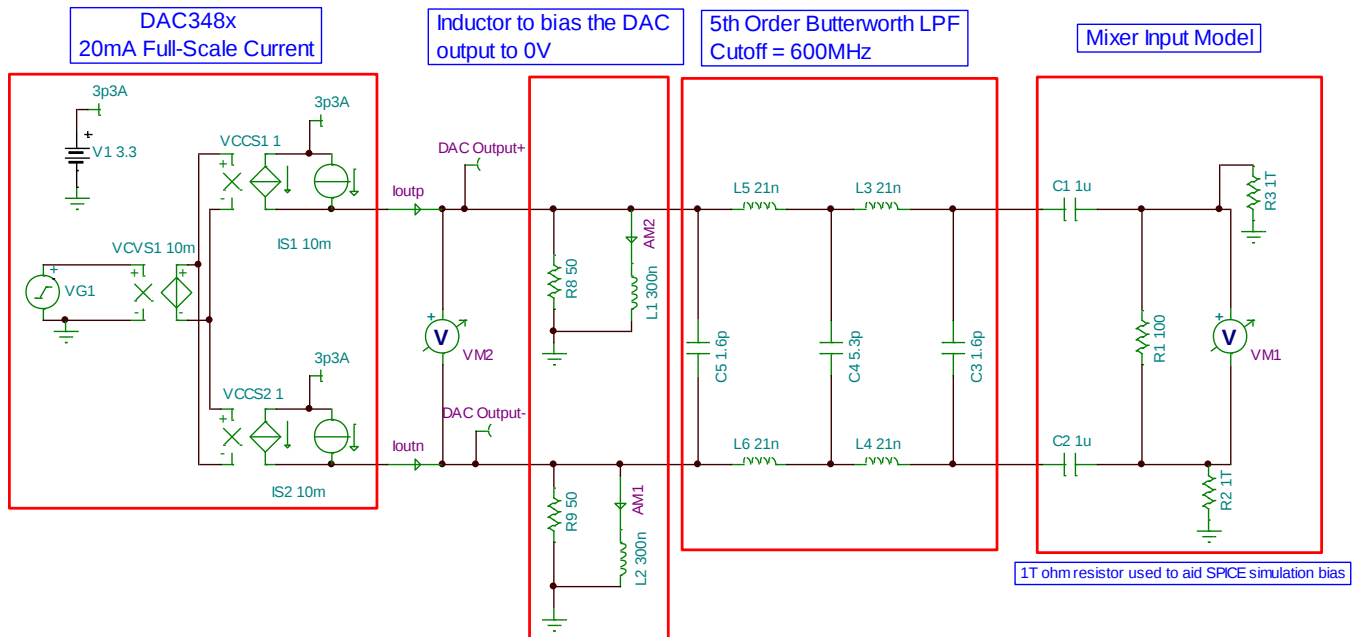


Figure 27. Typical DAC348x Inductive-PullDown Interface Network in TINA-TI

8 Conclusion

The interface networks discussed in this report provide options for interfacing the DAC348x device to down-stream devices such as I/Q modulators or mixers. As long as the DAC and the down-stream device are biased correctly and are set for the recommended signal levels, the overall system achieves the optimal performance.

Consider the following key points:

1. Both DC and AC swing must meet the DAC output compliance voltage requirement.
2. Load requirement and output full-scale current requirements must be considered.
3. Down-stream network and devices must be biased appropriately.
4. Impedance seen by the filter.

Refer to [Table 2](#) a brief overview of the interface networks:

Table 2. Summary of the Interface Networks

Interface Network	Common Mode	Translation Network Loss	DAC Output Swing	Advantages	Designer Considerations
TRF3705	0.25 V	0 dB	1 V _{pp}	The circuit provides same common-mode interface without loss between the DAC348x and TRF3705.	The circuit is optimized for 20-mA full-scale output and 100-Ω input and output filter impedance.
Single-Supply Biasing	Depends on modulator bias	Depends on modulator bias	1 V _{pp}	The circuit provides the appropriate common-mode bias for both the DAC348x and modulators.	Pseudo-DC capacitors in the circuit are required to minimize loss and maximize bandwidth. Optimize DAC output common mode to maximize AC swing.
Dual Supplies Biasing (DC Coupled)	Depends on modulator bias	Depends on modulator bias	2 V _{pp}	The circuit enables DC interface with the ability for the DAC output to swing to the negative rail for higher output power.	Consider DAC and interface network power-supply startup sequence. Adjust the bias level and power supply rails for some of the common 50- or 100-Ω impedance networks. The translation network can create loss and result in lower swing at the modulator input
Dual Supplies Biasing (Pseudo-DC Coupled)	Depends on modulator bias	Depends on modulator bias	2 V _{pp}	The circuit enables pseudo-DC interface that maximizes the DAC-to-modulator input-power transfer. It allows the DAC output to swing to the negative rail.	Consider DAC and interface network power-supply startup sequence.
Transformer Coupled	Centered tap biased to ground	Independent bias after AC coupling	Depends on the transformer ratio	Enables AC interface with the ability for the DAC output to swing to the negative rail	Consider the overall transformer cost and bandwidth. Transformer does not pass DC.
Inductor Pulled-Down	Inductor pulled-down to ground	Independent bias after AC coupling	Depends on the DAC total impedance	Enables AC interface with the ability for the DAC output to swing to the negative rail	Consider inductor size and frequency limitations. The inductor and resistor constant can affect the low frequency limit.

9 References

1. *Getting Started with TINA-TI*, [SBOU052](#)
2. TINA-TI Spice files, [SLUC481](#)
3. DAC3482 datasheet, *Dual-Channel, 16-Bit, 1.25 GSPS Digital-to-Analog Converter (DAC)*, [SLAS748](#)
4. DAC3484 datasheet, *Quad-Channel, 16-Bit, 1.25 GSPS Digital-to-Analog Converter (DAC)*, [SLAS749](#)
5. DAC34H84 datasheet, *Quad-Channel, 16-Bit, 1.25 GSPS Digital-to-Analog Converter (DAC)*, [SLAS751](#)
6. DAC34SH84 datasheet, *Quad-Channel, 16-Bit, 1.5 GSPS Digital-to-Analog Converter (DAC)*, [SLAS808](#)

10 About the Author

Kang Hsia is an Applications Engineer in the High Speed Data Converters group at Texas Instruments. He primarily provides customer support for TI's high-speed ADCs and DACs. Prior to joining TI in 2007, Kang earned his bachelor of science in electrical engineering from California Polytechnic State University (Cal Poly) in San Luis Obispo, California. Kang is an active member of the TI E2E™ Community, and can be reached through [e2e.ti.com](#) for support.

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