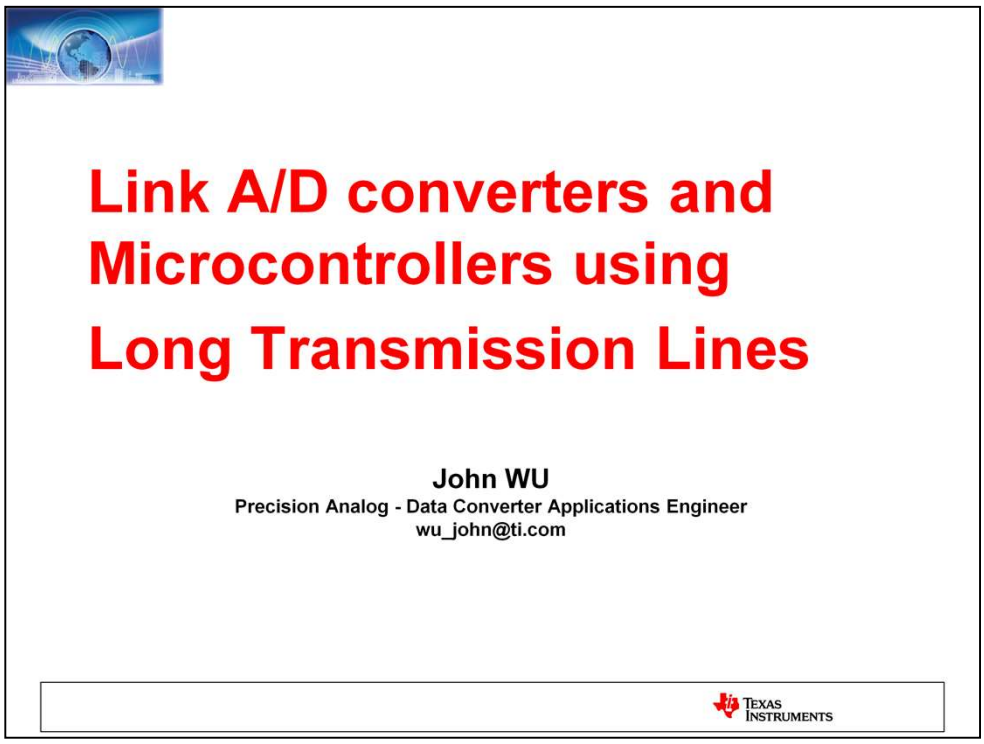

Precision devices are available so that you can build high performance systems. As you know, system layout and design is important, but if a system has multiple boards, a critical piece of the PCB design is board interconnection. A poor PCB interconnection design can easily ruin a great design using fabulous parts. This presentation will focus on the critical factors when achieving a high performance PCB interconnection system. The focus will be on long transmission line effects, such as reflection, termination and cross talk considerations in twisted pair cable and long PCB trace. You will leave this session armed with an interconnect strategy for your next design.

Transmission Line Effect Considerations

- Definition of the Highest Frequency Signal
- Transmission Line Model
- Reflection Concept
- Termination Topology
- Crosstalk Analysis

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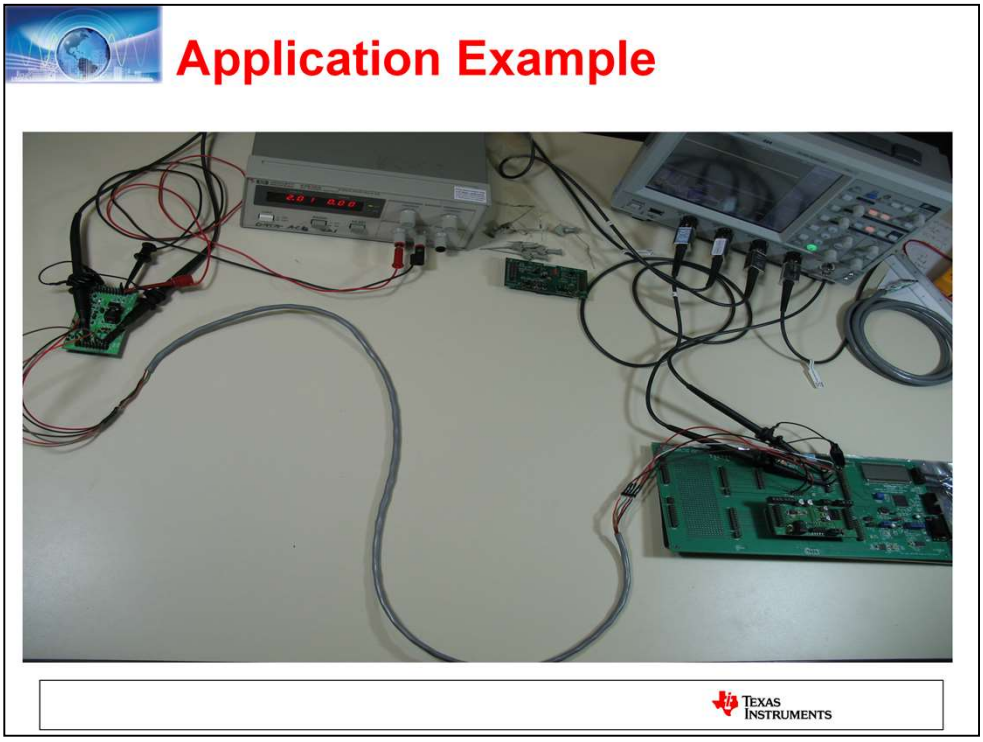


As we move through our termination discussion we are going to need an example circuit. This circuit will help us prove the theory that we will present in the beginning of this session.

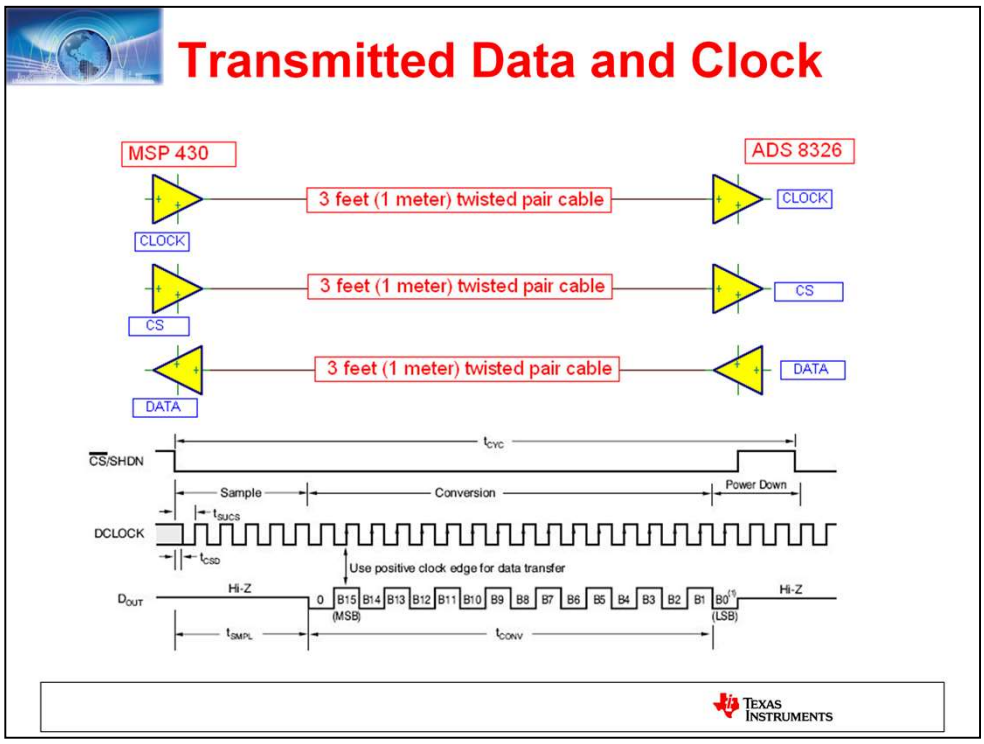
Our example circuit connects the ADS8326 analog-to-digital converter to a MSP430 micro-controller. Each device resides on their respective evaluation boards (or EVM). The boards are connected through a 1 meter (~3 feet) CAT-5 twisted pair cable.

The ADS8326 is a 16-Bit, High-Speed, 2.7V to 5.5V *micro*Power Sampling Analog-to-digital converter. Low power and small size make this device ideal for portable and battery-operated systems. It is also a perfect fit for remote data-acquisition modules, simultaneous multichannel systems, and isolated data acquisition.

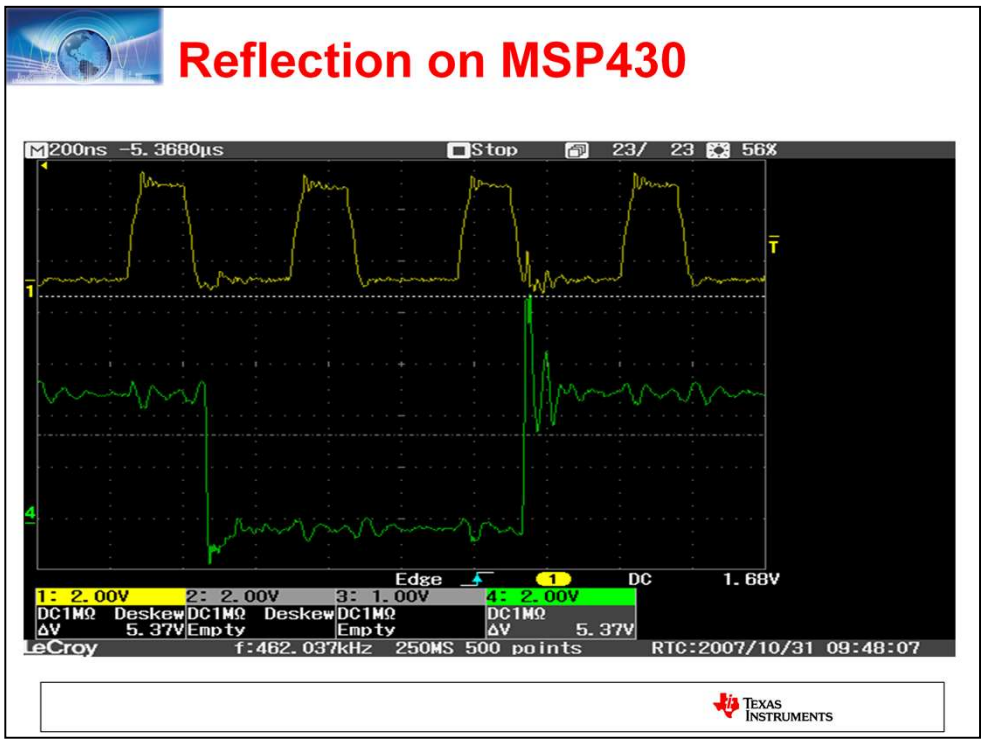
The MSP430 family of ultra-low-power 16-bit RISC mixed-signal processors provide the ultimate solution for battery-powered measurement applications. Using leadership in both mixed-signal and digital technologies, TI has created the MSP430 which enables system designers to simultaneously interface to analog signals, sensors and digital components while maintaining unmatched low power.

Initially, a designer may think that the speeds of these two devices will not cause termination problems. However, the transmission data between these boards and the mismatched characteristic impedance causes a significant reflection and crosstalk around the 3 feet long loop. These reflections distort the clock and data signals between the boards.

The picture in this slide shows the ADS8326 EVM and MSP430 evaluation boards are connected through 3 feet cable.



In our system, the MSP430 transmits a clock and chip select (CS) signals to the ADS8326. The ADS8326 responds by transmitting the conversion data back to the MSP430. All of these signals travel across the 3-foot CAT-6 cables.



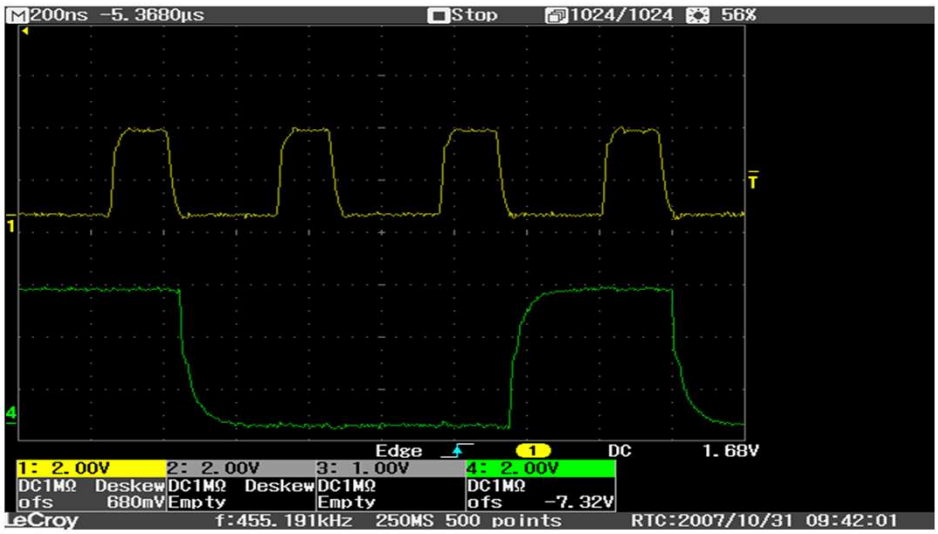
In the initial design, line impedances are ignored. This slides shows the mismatched impedances measured results at the MSP430. The mismatched impedances is a result of simply connecting the two boards together through the 3 foot wires.

Ch1 in this scope photo is a clock at 2.25MHz that is transmitted to the ADS8326. The ADS8326 uses this clock signal to synchronize the transmission of data back from the ADS8326 to the MSP430. The range of the clock rate to the ADS8326 is 24 kHz to 6.0 MHz. But, as we will see, the frequency of the clock is not the issue that we will need to address in our circuit. We will actually be concerned with the rise and fall time of this clock signal.

The data from the ADS8326 to the MSP430 is on Ch4.

The clock and data signal termination distortion creates signals that exceed specified high-level and low-level thresholds (overshoot and undershoot), signals that have false edges (ringing), and signals that have reduced operating margins (degraded eye diagram) caused by inter-symbol interference. You can see examples of these errors in this slide.

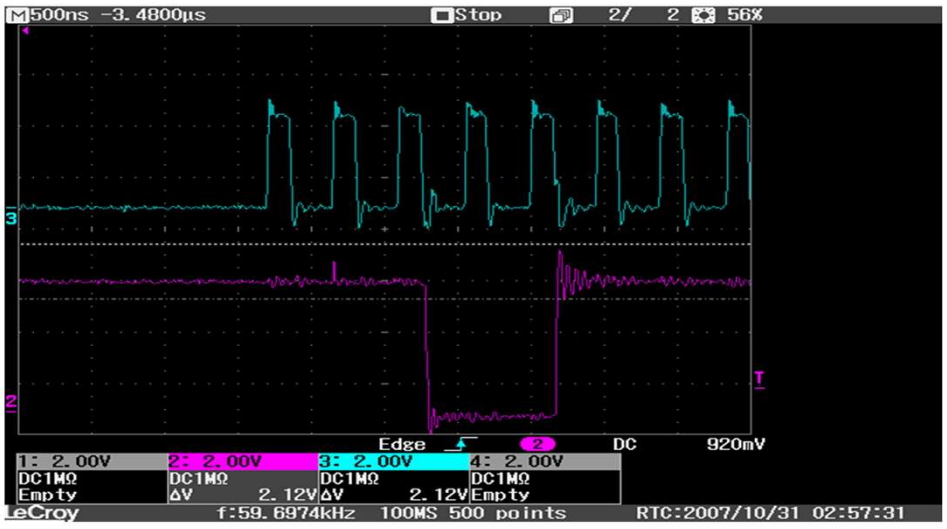
With Termination on MSP430



If we use the same fundamental circuit and pay attention to termination issues, you can correct the clock and data distortion issues at the MSP430. Again, in this scope capture, Ch1 is MSP430 output clock and Ch4 shows the ADS8326 received data.

The theory and description behind good termination will be discussed later in this presentation.

Reflection on ADS8326 EVM

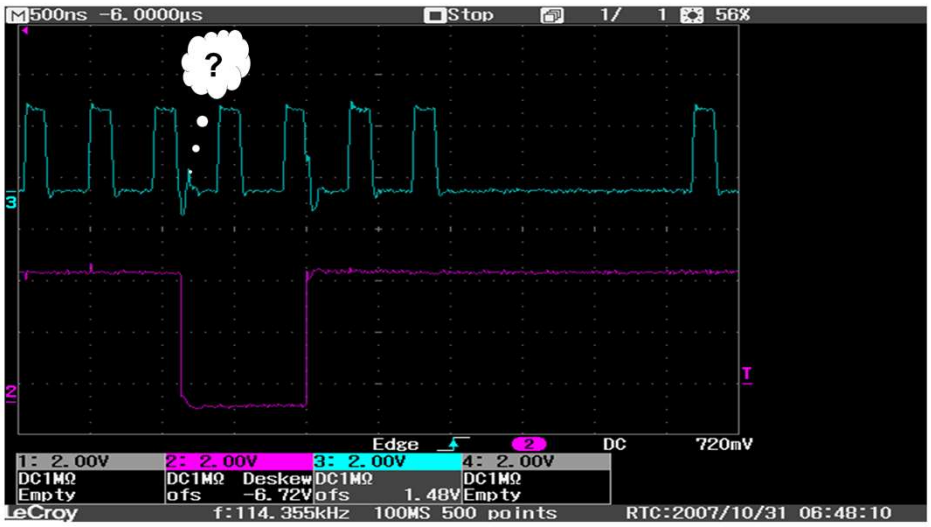


Texas Instruments

If we go through the same exercise by looking at the ADS8326 side of our wires, we can witness similar effects. In this slide, Ch3 is the received clock (from the MSP430) and Ch2 is the ADS8326 output data. Once again, the clock and data signal termination distortion creates signals that exceed specified high-level and low-level thresholds, signals that have false edges, and signals that have reduced operating margins caused by inter-symbol interference.

We are using the ADSMSOP8 board to take this data.

With Termination on ADS8326



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And once again, if we use the same fundamental circuit and pay attention to termination issues, you can correct most of the clock and data distortion issues at the ADS8326, with the exception of a small undershoot problem of the clock signal. Although good termination techniques are used in this circuit, there is still a interaction between the rising and falling edge of the data line (Ch 2) and the clock line (Ch 3). This is a cross-talk problem. Cross-talk will be covered at the end of this presentation.

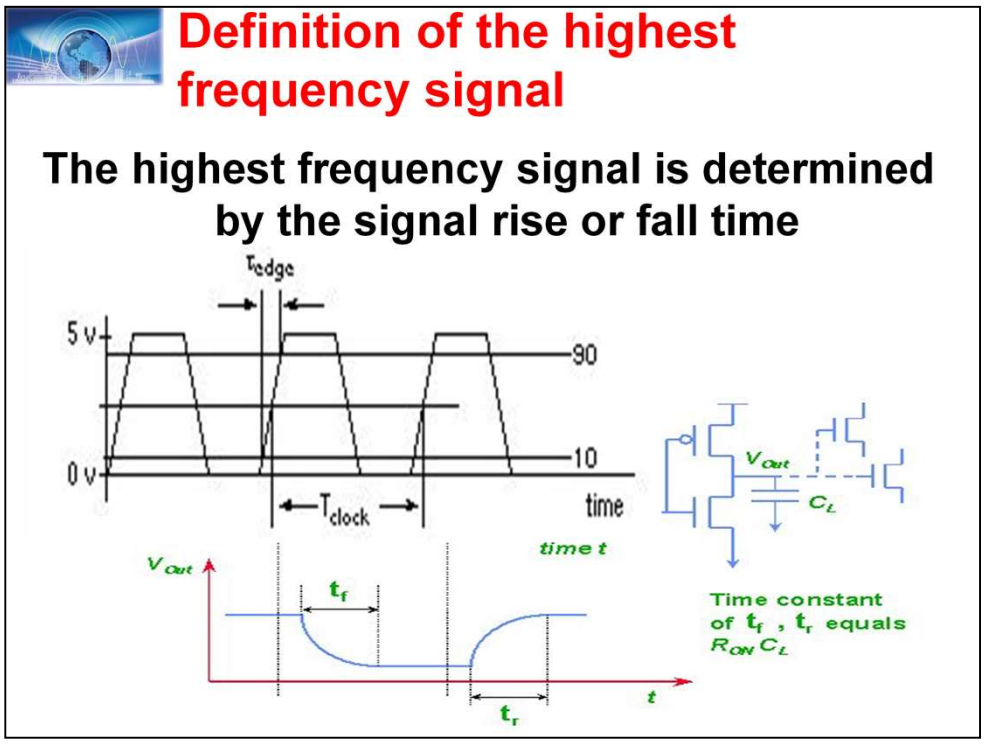
Again, in this scope capture, Ch3 is MSP430 clock at the ADS8326 and Ch2 shows the ADS8326 output data at the ADS8326.

Definition of the highest frequency signal

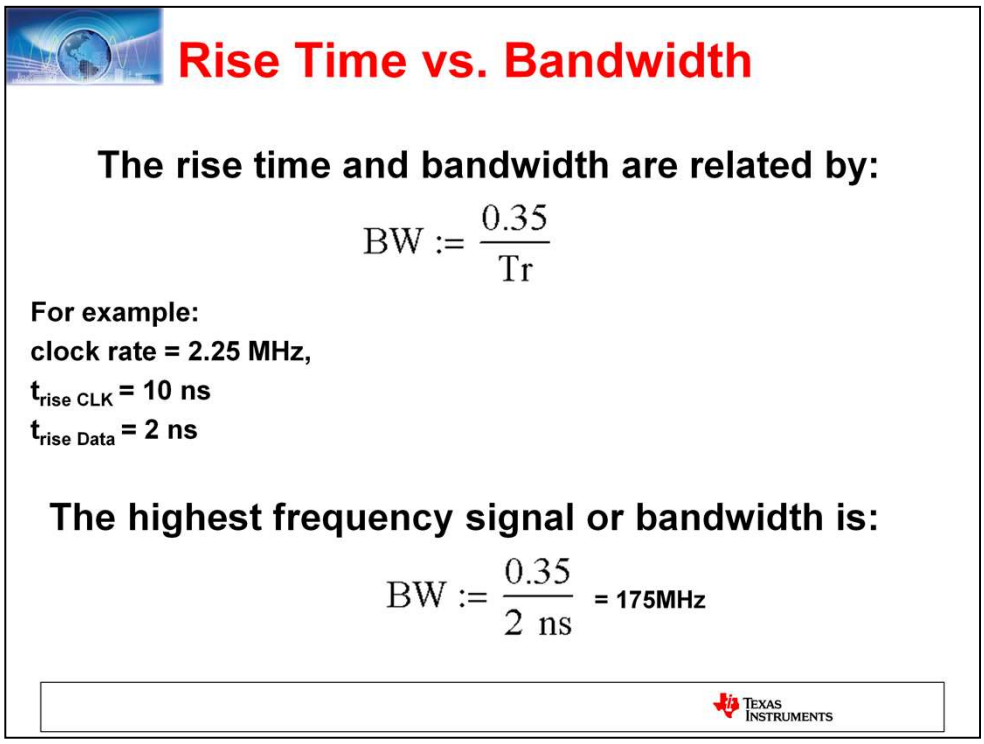
What is the highest frequency signal in a 2.25MHz sample clock rate ADC ?

An immediate response to the ringing in the previous slides it slow down the frequency of the clock. This may be a quick fix and you may or may not be successful, however, you have not really attacked the root of the problem.

Frequently, engineers are convinced that the clock rate dictates the type of PCB implementation and they ignore the clock or signal switching time. But if you are going to effectively understand the transmission line effects, you really need to define your highest frequency signal as rise and fall times and not frequencies.



The clock speed or T_{clock} is an indicator of high speed, but not the determining factor for transmission lines. A 2.25 MHz clock looks like a low frequency signal, however, it can have fast rise and fall times or t_{edge}. It is the rise and fall times that dictate when to use high speed PCB design techniques. With this in mind, the switching time determines the critical signal speed and not the signal clock frequency. The true challenge of high-speed PCB design is how to design your board with the fast switching time digital signals in mind.



There is a difference between the actual clock frequency and the effective operating frequency. The actual clock frequency describes the clock or data rate in the application. In our circuit this frequency is 2.25 MHz. The Effective Operating Frequency of a PCB circuit is defined as:

Bandwidth [GHz] = [0.35] / [Signal Transition Time {nSec}].

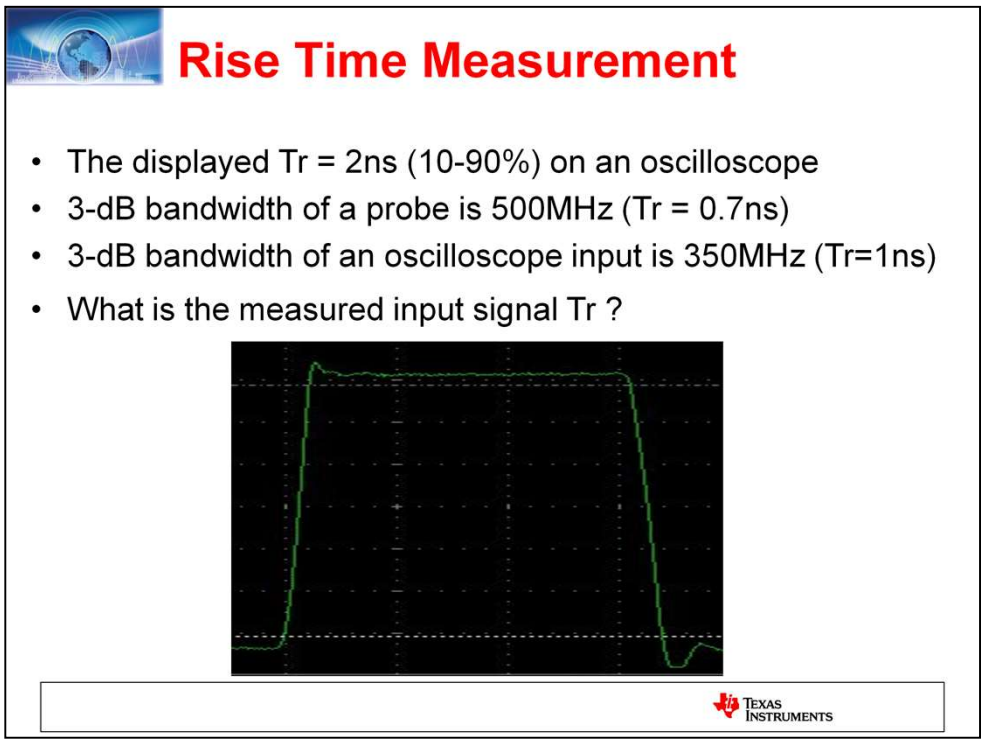
For a worst case calculation you should use the shorter value of t_{rise} [Rise Time] and t_{fall} [Fall Time].

BW = 1/(2π x RC)

$t_{rise} = t_{10\%-90\%} = 2.2\ RC$;

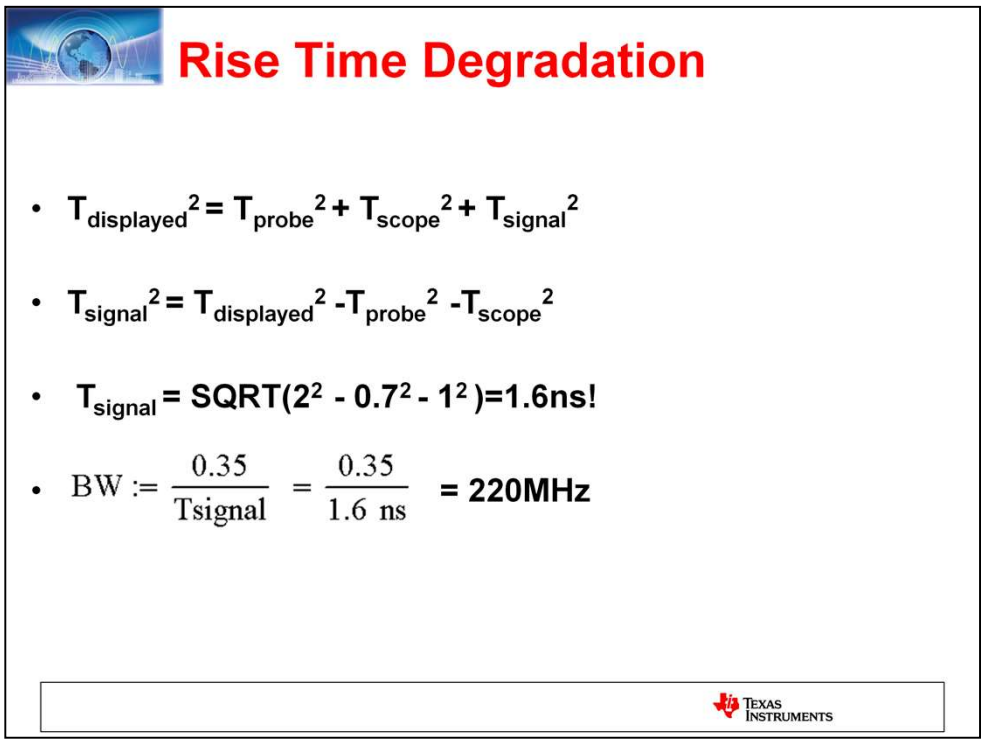
BW = 2.2/(2π x $t_{10\%-90\%}$)

BW = 0.35/t_{rise}



If you determine the rise time on the bench, be aware of your test equipment limitations. In this slide we have a scope photo of a clock signal. From this display you can calculate the rise and fall time of the signal. You will note that the rise time is faster than the fall time. If you use a rise time of 2 ns, the bandwidth or BW of this signal is 175 MHz.

Be careful during this measurement to insure that you are measuring the signal and not the equipment limitations on your signal. In this measurement the bandwidth of the probe is 500 MHz and the bandwidth of the oscilloscope in 350 MHz. These two equipment limitations can have an influence on your measurement of the signal.



These timing errors can be quantified with a formula the uses the square-root-of-the-sum-of-the-squares or root-sum-square (RSS). If you implement this formula, the measured 2 ns rise time of the signal is actually equal to 1.6 ns.

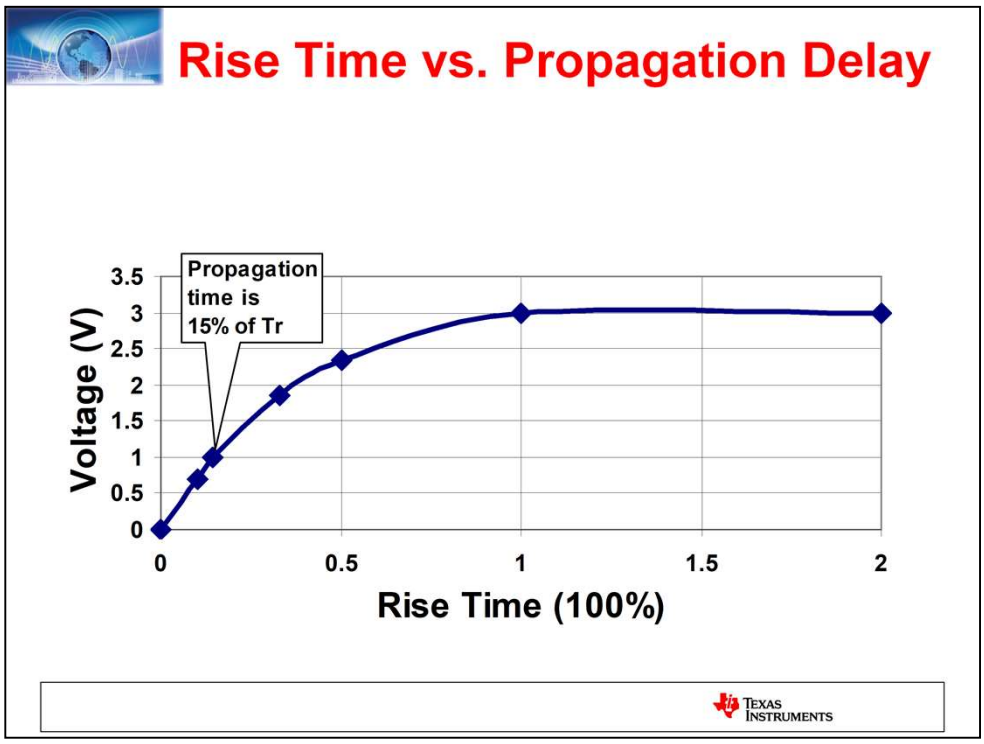
Now with this information, the data signal has an Effective Operating Frequency of 220MHz.

This is far above the actual operating clock frequency (2.25MHz) of the ADC and the previous calculated Effective Operating Frequency of 175 MHz.

Critical Microstrip Length

What is the critical length of a microstrip that must be considered as transmission line?

Now that we have determined the Effective Operating Frequency we will characterize the connections between the MSP430 and the ADS8326 by defining the critical length of our transmission line.

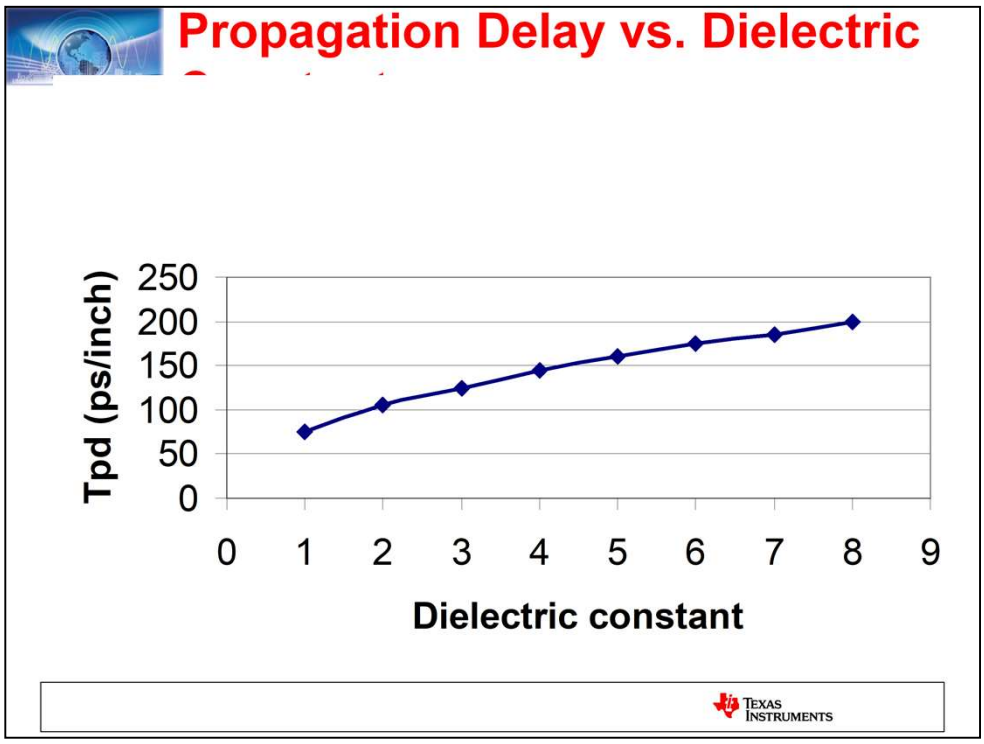


In our system, signal rise time, propagation delay and PCB trace length are related.

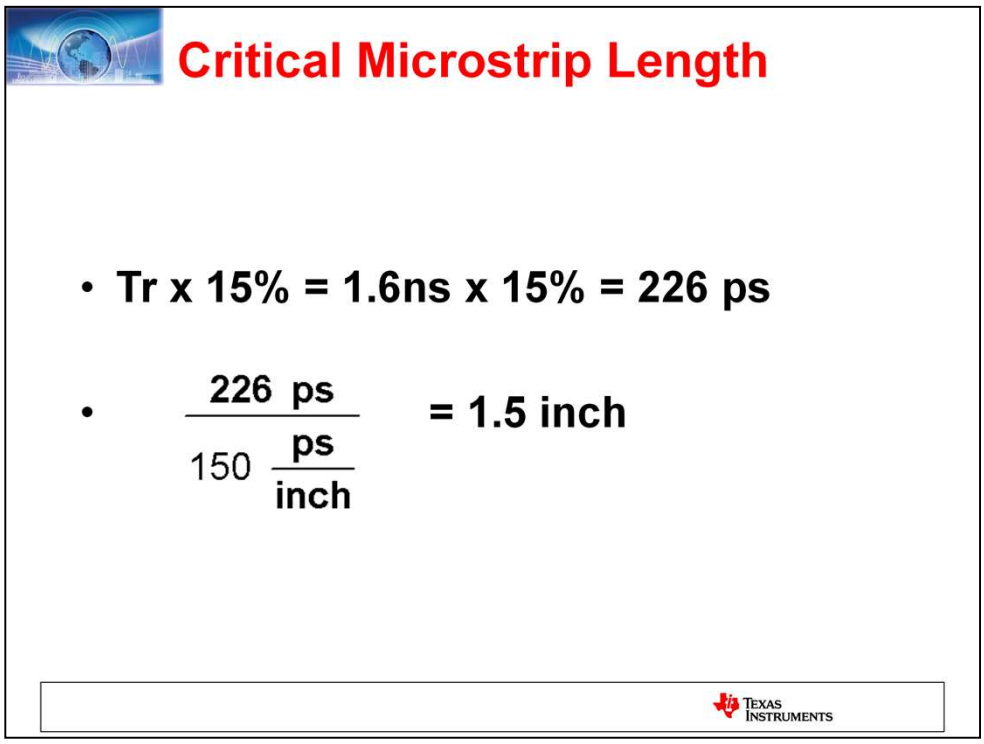
Propagation delay is the time required for a signal to travel from a driver to a receiver. One of the major high-speed PCB design challenges is to make sure this delay time is less than the rise time or fall time of the signal.

If the signal propagation delay time is less than 1/7 of t_{rise} (<15% x t_{rise}), we can model the microstrip as inductive-capacitive pi model (LC pi model). If t_{rise} is greater than the propagation delay time, we will use the microwave transmission line theory to model the PCB microstrip.

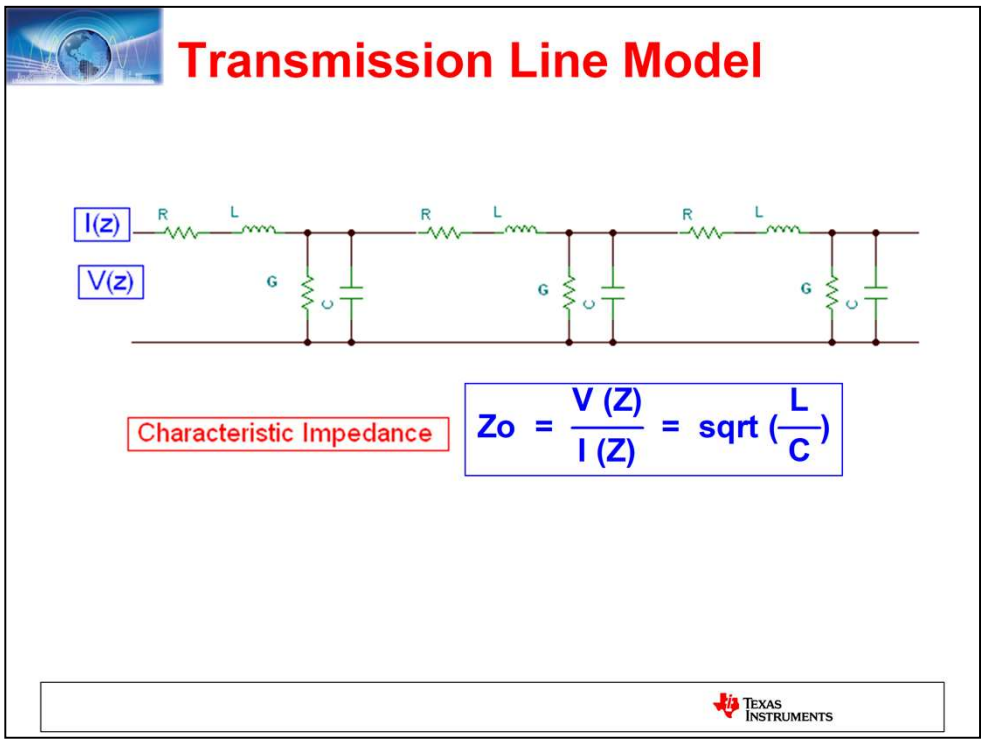
If the lines are sufficiently short, the signal will be rising during the propagation delay of the line, and the reflection will become a part of the rising edge. With longer lines, the propagation delay may be greater than the rise time of the signal, and reflections will appear as an overshoot or undershoot.



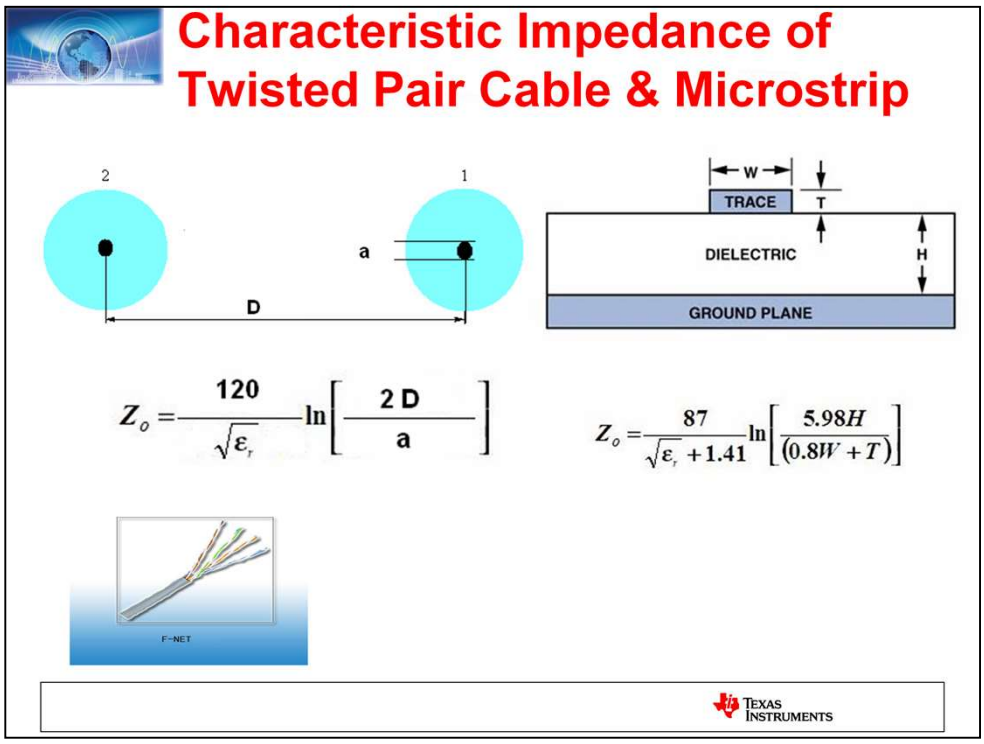
Propagation delay time (Tpd) is proportional to the dielectric constant of PCB. For FR4 boards, the typical Tpd is around 150 ps/inch.



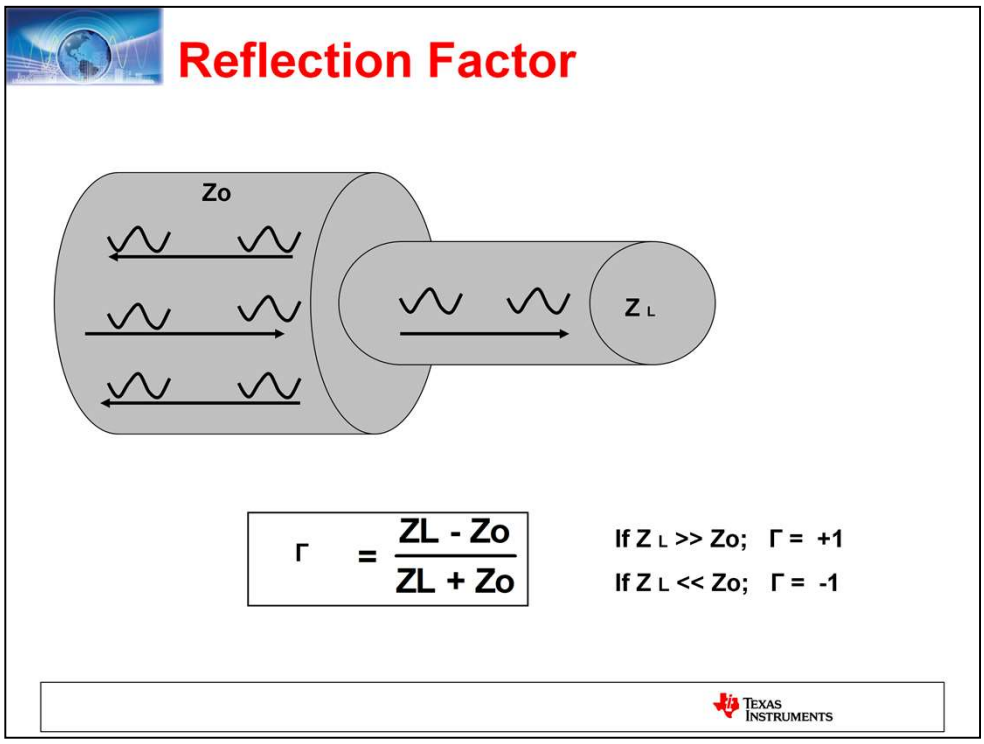
As long as a trace or a cable length is longer than 1.5 inches and a signal switching time is less than 1.6ns, the transmission line model is required to analyze the trace or cable.



In transmission-line theory, the voltage and current along a transmission line can vary in magnitude and phase as a function of position. Zo is the characteristic impedance of the transmission line when it is infinitely long or ideally terminated.

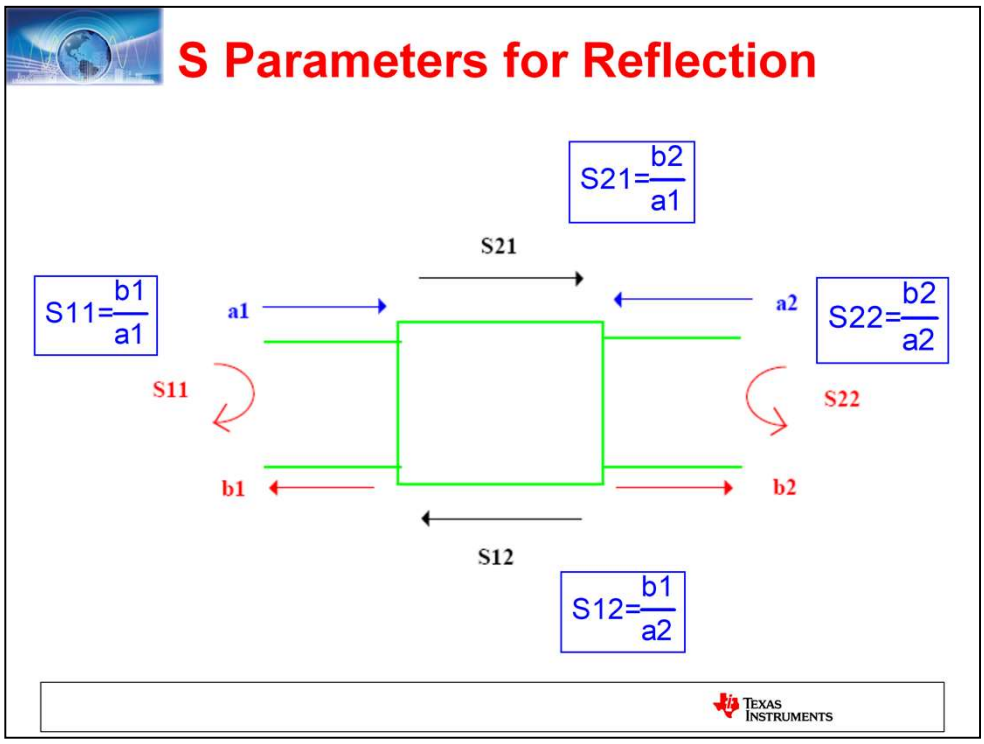


Both twisted pair cable and microstrip trace have similar formulas for their characteristic impedance. The characteristic impedance of a transmission line largely influences the transient response of a signal passing through it.

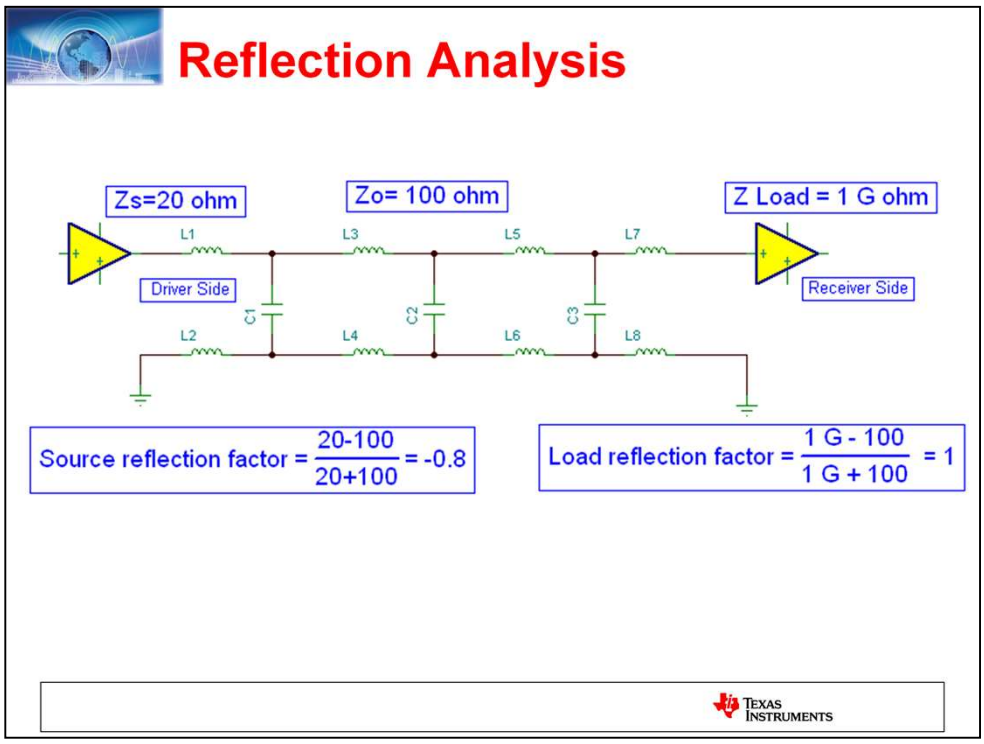


As a general microwave engineering concept, the voltage reflection coefficient refers to the ratio of amplitude of the reflected voltage wave to the incident voltage wave. ZL is the load impedance, and Zo is the characteristic impedance.

If the load is mismatched to the line, there will be a reflection of the incident wave at the interface of the line and load and the power delivered to the load will be reduced. This is also called return loss (RL).



With microwave theory, S11 is reflection coefficient at port 1, when a perfect matched load is at port 2, a2=0. S21 is voltage transfer ratio from port 1 to port 2, when a perfect matched load is at port 2, a2=0. S22 is reflection coefficient at port 2, when perfect matched load is at port 1, a1=0. S12 is voltage transfer ratio from port 2 to port 1, when perfect matched load is at port 1, a1=0

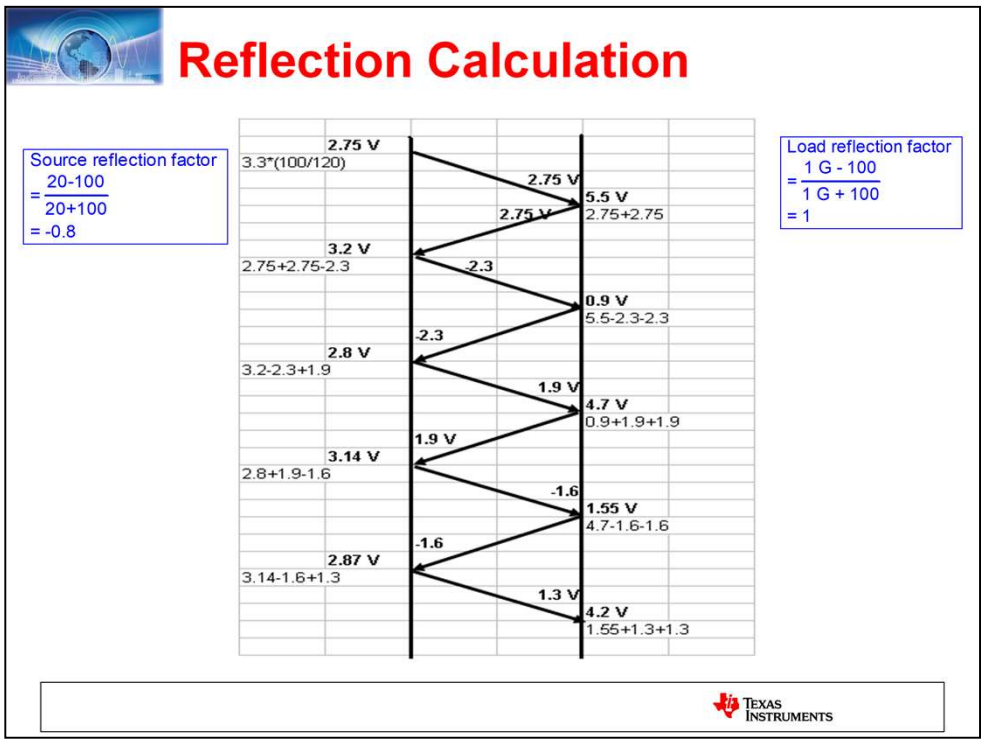


The figure in this slide shows a typical transmission line with one driver and one receiver.

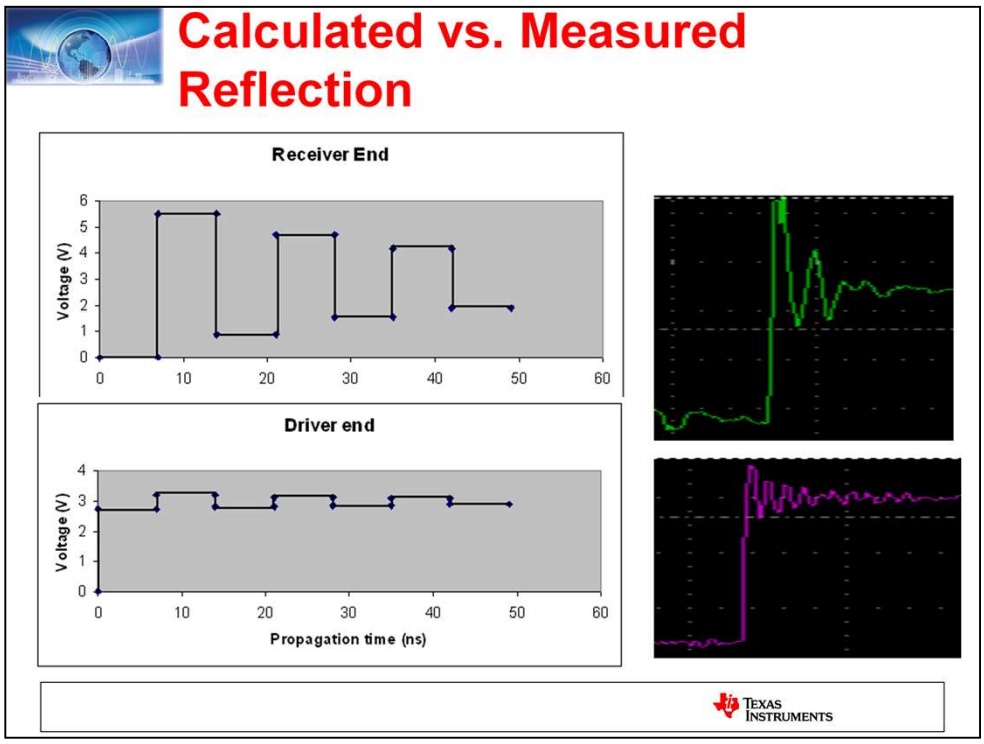
The driver has an internal source resistance of 20 Ω. The cable characteristic impedance is close to 100 Ω and the input impedance of the receiver is 1 GΩ. The output impedance of the driver Zs may change with current demand or it vary from device to device. The input impedance of the receiver [ZL] may be greater than 1 GΩ. For CMOS inputs, the infinite ZL resulting in a reflection coefficient of 1.

A digital rising edge acts as a pure AC signal. When this ac signal reaches the end of the path, and a mismatch between Zo and the termination ZL exists, some portions (up to 100% when reflection =1) of the wave are reflected.

When the wave reflects back along the transmission line, it will eventually reach the original source. If a mismatch exists between the Zo and Zs, some portions of the wave are re-reflected again. The superposition of these reflected waves can cause significant signal degradation.



With the reflection factor as 1 at the receiver end, and reflection factor as -0.8 at the driver end, we can calculate all the exact ringing amplitudes at any propagation time. The driver signal initial amplitude is 3.3V.



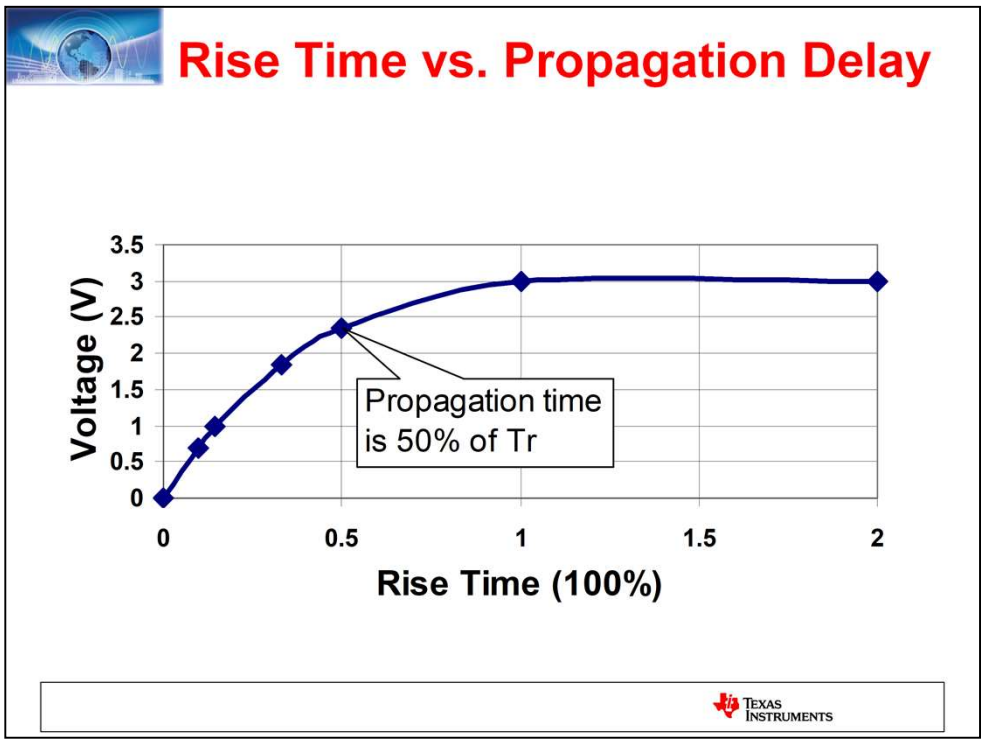
The figure in this slide compares our calculated ringing signal and measured results.

The ringing of the receiver end is much larger than the ringing of the driver end.

Critical Length of a Transmission Line

What is the critical length of a transmission line that must be terminated?

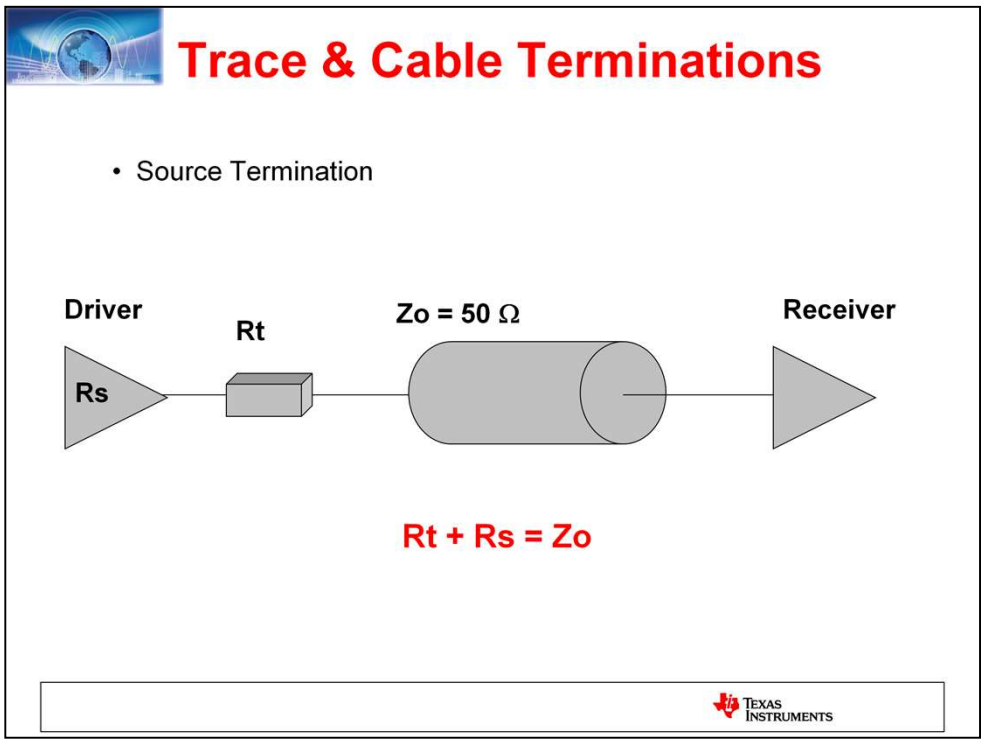
How do we know if we need a termination before we have simulation or measurement results?



Termination is required when the two-way total propagation delay is greater than or equal to the signal rise-time or 2 x Tpd >= tr. If the impedance is not matched, the signal at the load will be greatly distorted.

Therefore, PCB traces or cables should be terminated (using one of the schemes listed in the following slides) when the trace length propagation delay exceeds half of tr.

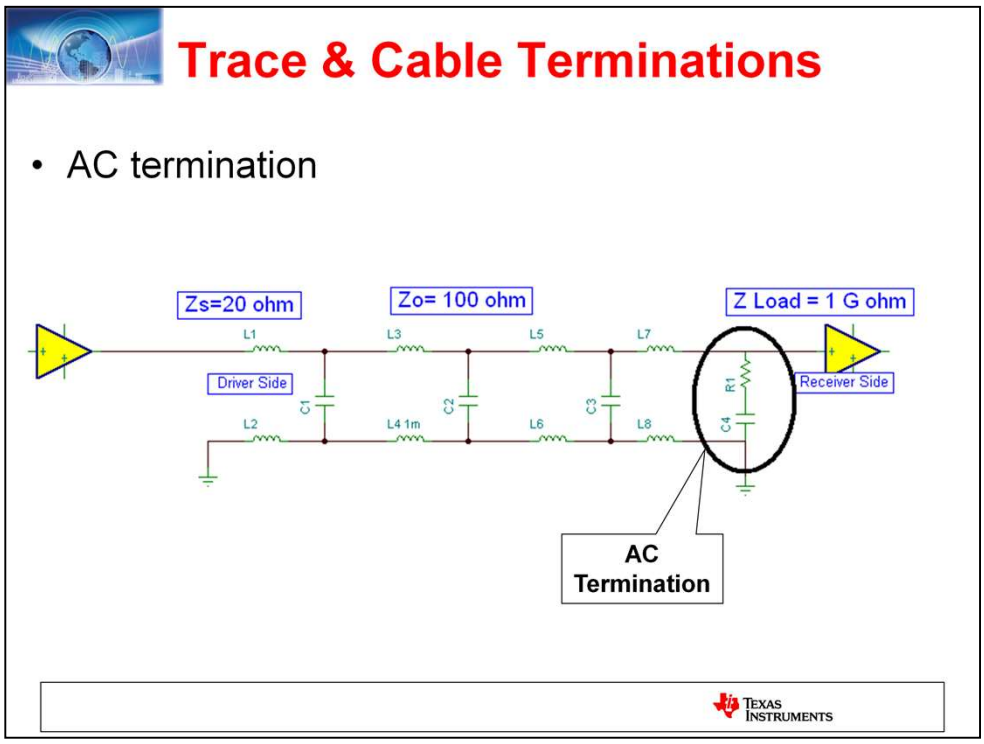
The target of a good termination is to make the characteristic impedance match the source and load impedance.



In a source series termination scheme, the resistor matches the impedance at the signal source instead of matching the impedance at load. Because driver output impedance is lower than 50 Ω, we should add a series resistor to the signal source impedance so that we match the line impedance Zo. The sum of Rt and the impedance of the output driver should be equal to the Zo.

The source termination is useful in point-to-point one-direction connection.

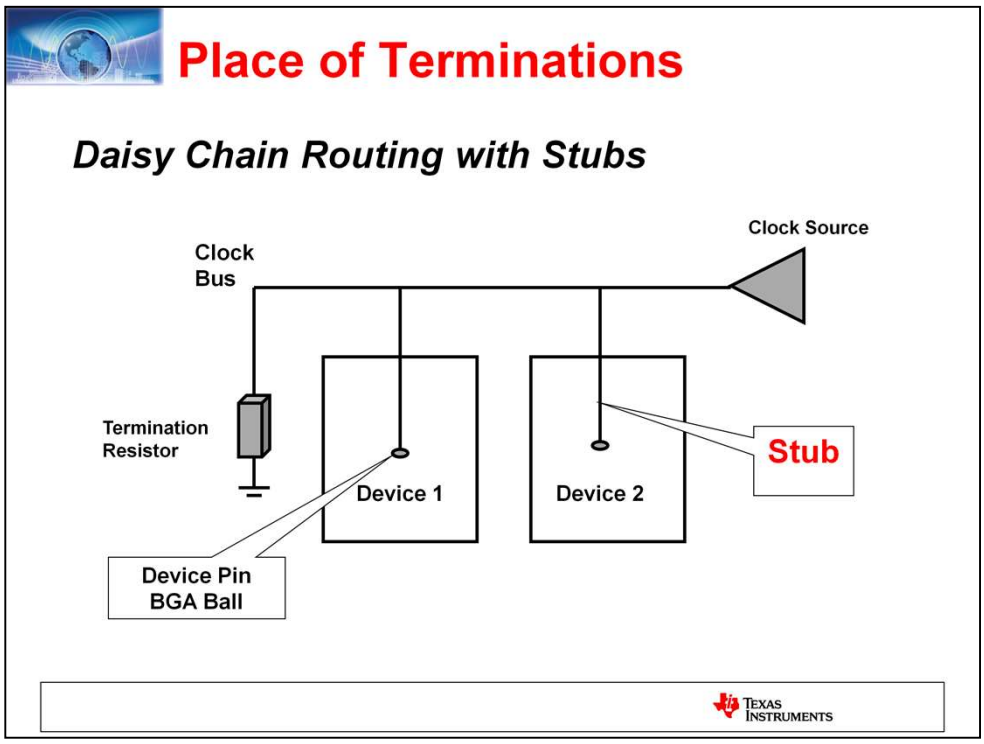
The disadvantage of this technique is that power consumption increases due to the Rt.



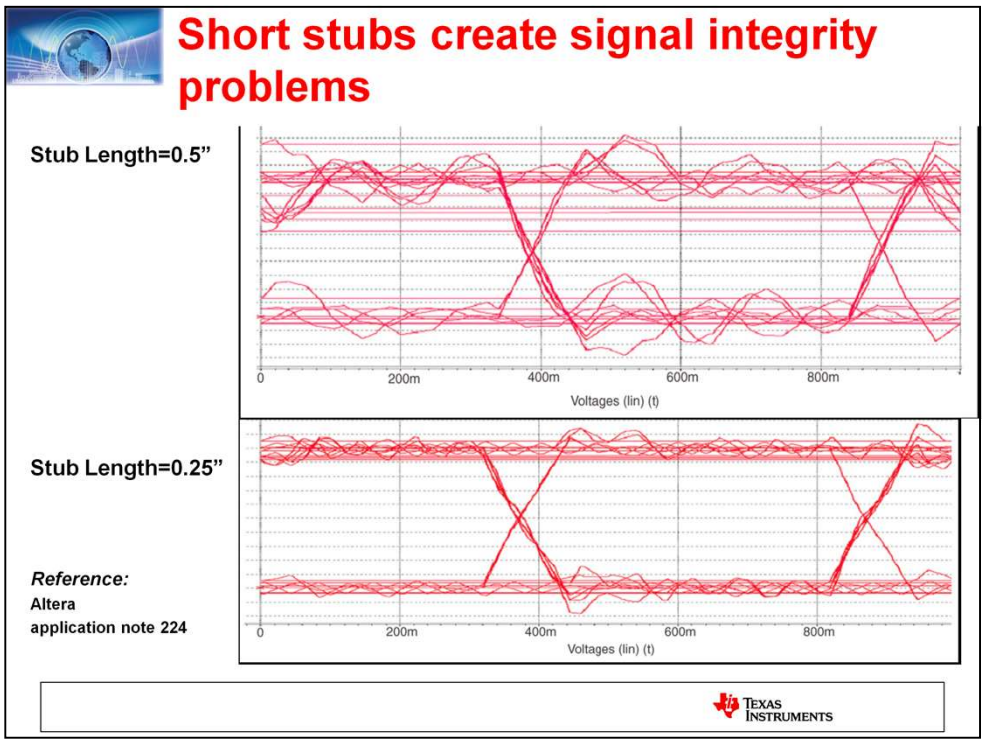
AC Termination has the lowest power drain because current only flows through the termination resistor while the capacitor is charging. The termination resistor [R] is selected to match the trace impedance [Zo], while the capacitor is selected using **Xc** = [3 x Tr] / Zo.

The capacitor value may be a lower value [below 200pF] which reduces power consumption. Higher values of capacitors produce a cleaner waveform but higher power consumption particularly at higher frequencies.

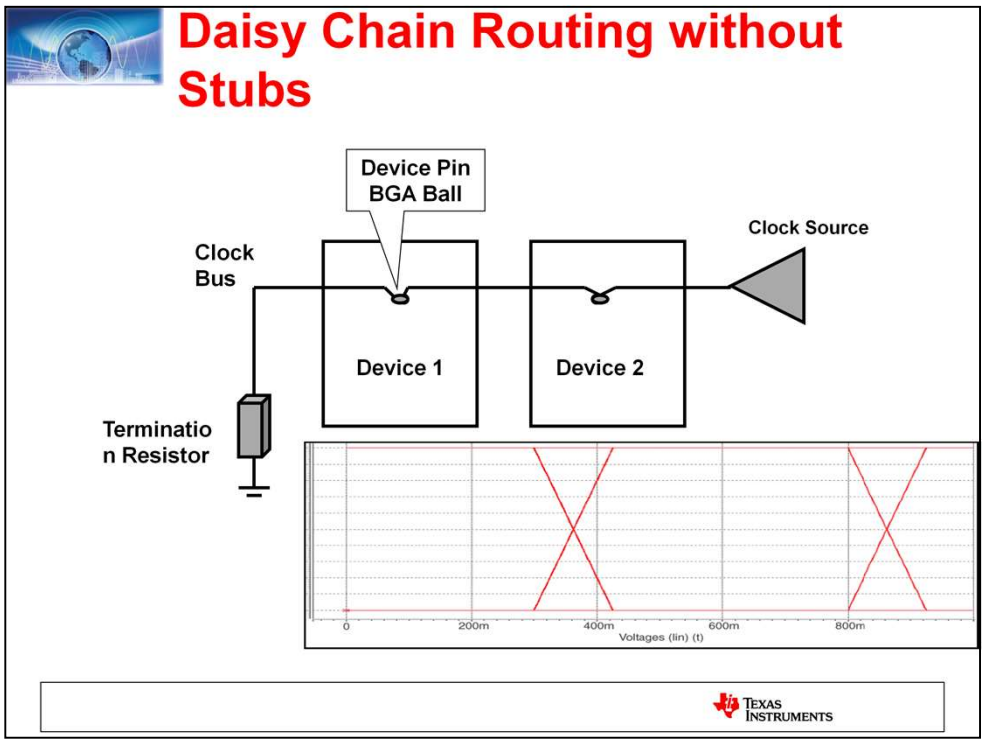
AC termination is useful in multipoint connection.



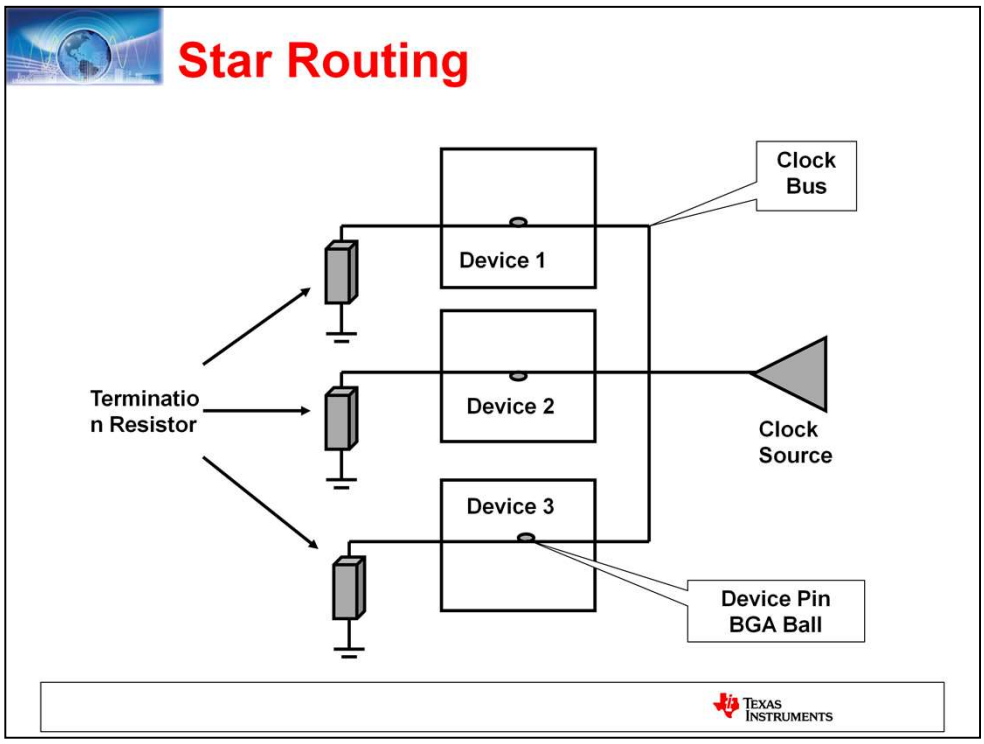
Short stubs can create signal integrity problems.



SPICE simulation shows results of different stub length. As the stub length decreases, there is less reflection noise, which causes the eye opening to increase.

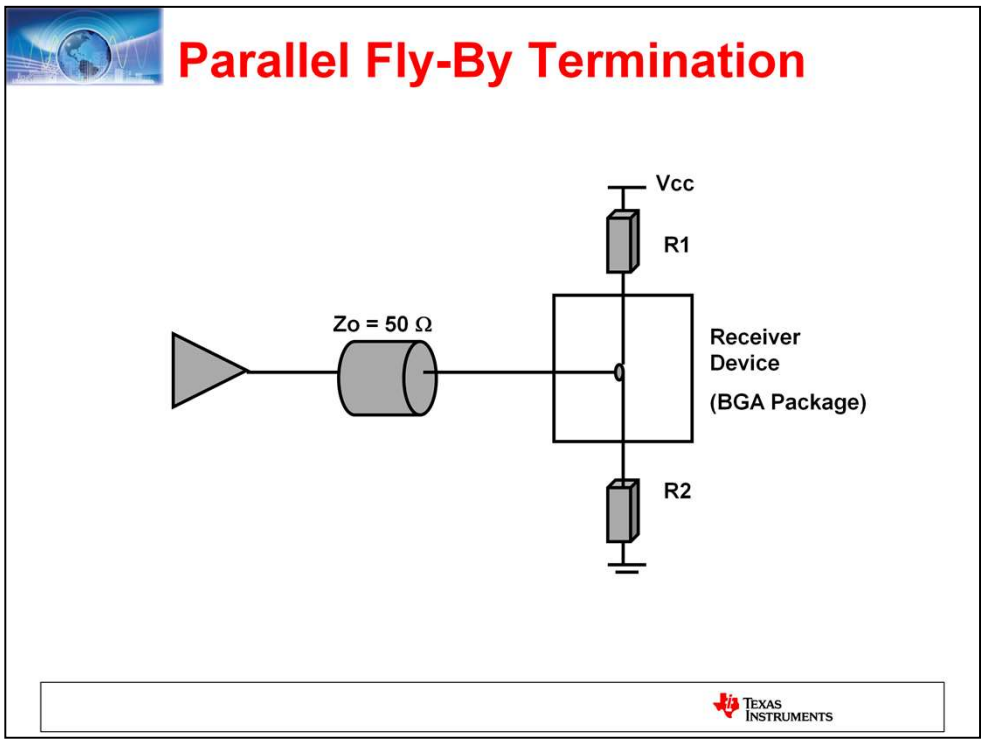


Daisy chain routing through the device pins can eliminate stubs. This layout minimizes signal integrity problems by removing the risk of impedance mismatch between the clock bus and the stubs.



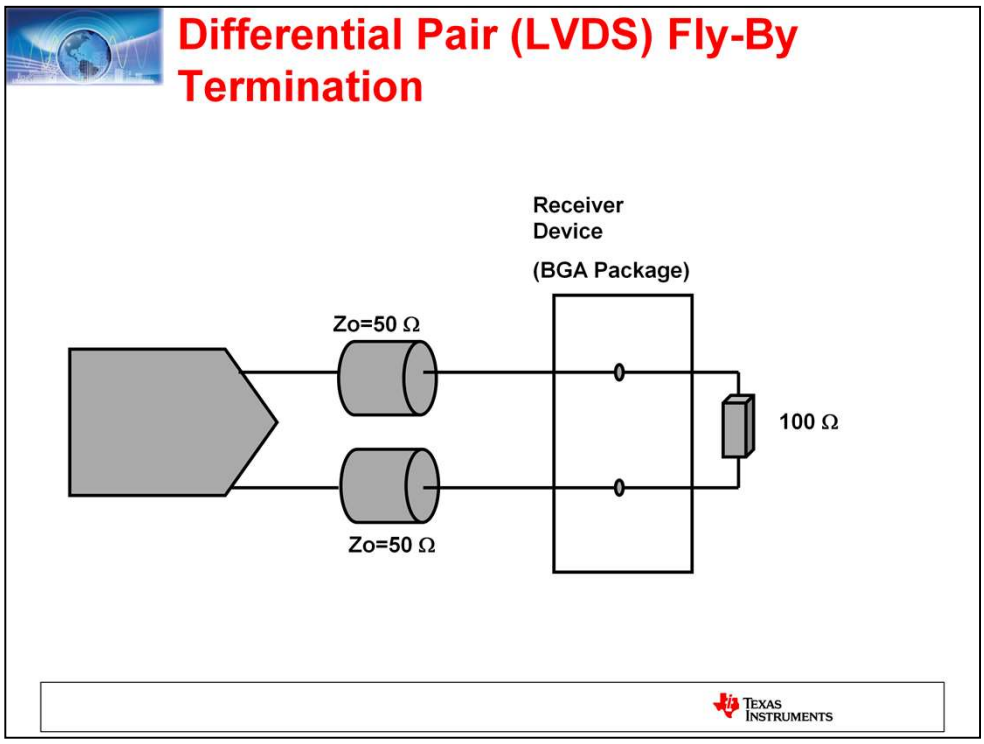
If you use star routing, each load and each branch length should be identical. This will minimize signal integrity problems. We must also match the impedance of the clock bus with each branch, which is connected to multiple devices.

To minimize the clock skew, all trace lengths between the clock source and devices must be matched so that the clock signal travels to all the devices at the same time.



With BGA package component, a PCB design requires a long termination line between a termination resistor and a pin of the device. Thus, the placement of the resistor is important.

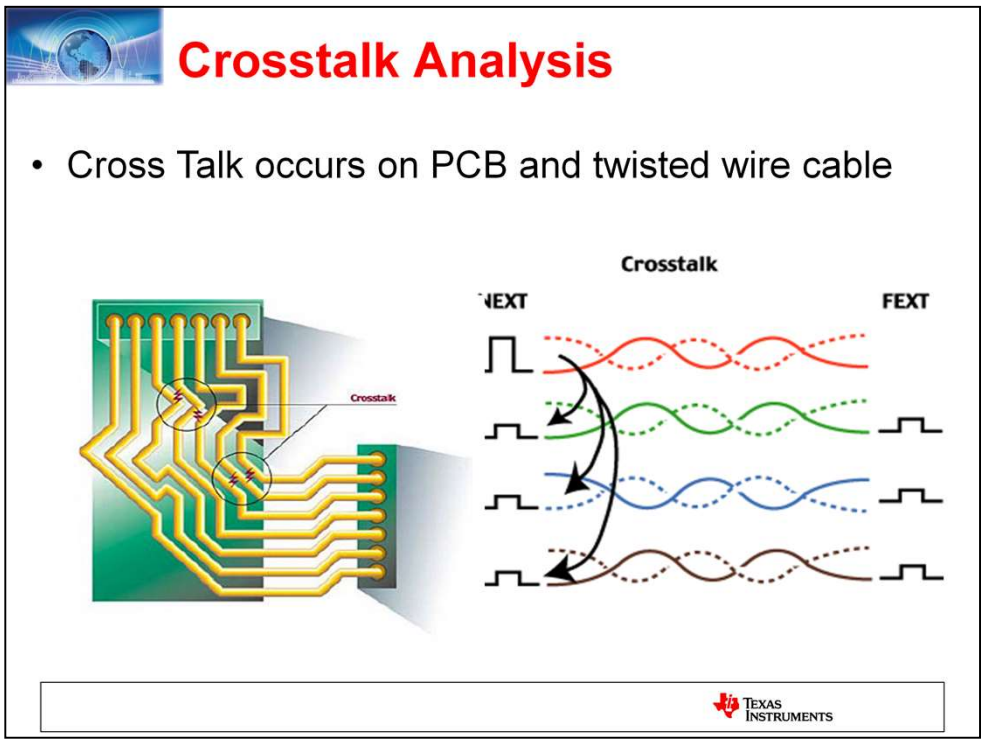
For this kind of long termination line, we should use fly-by termination. But the stub length should be less than 15% of the driver signal switching time. A longer stub length causes reflections from the receiver pads, which will result in signal degradation.



For the low-voltage differential signal (LVDS) and low-voltage positive emitter-coupled logic (LVPECL) standard, the RT should match the differential load impedance of the bus (typically 100 Ω).

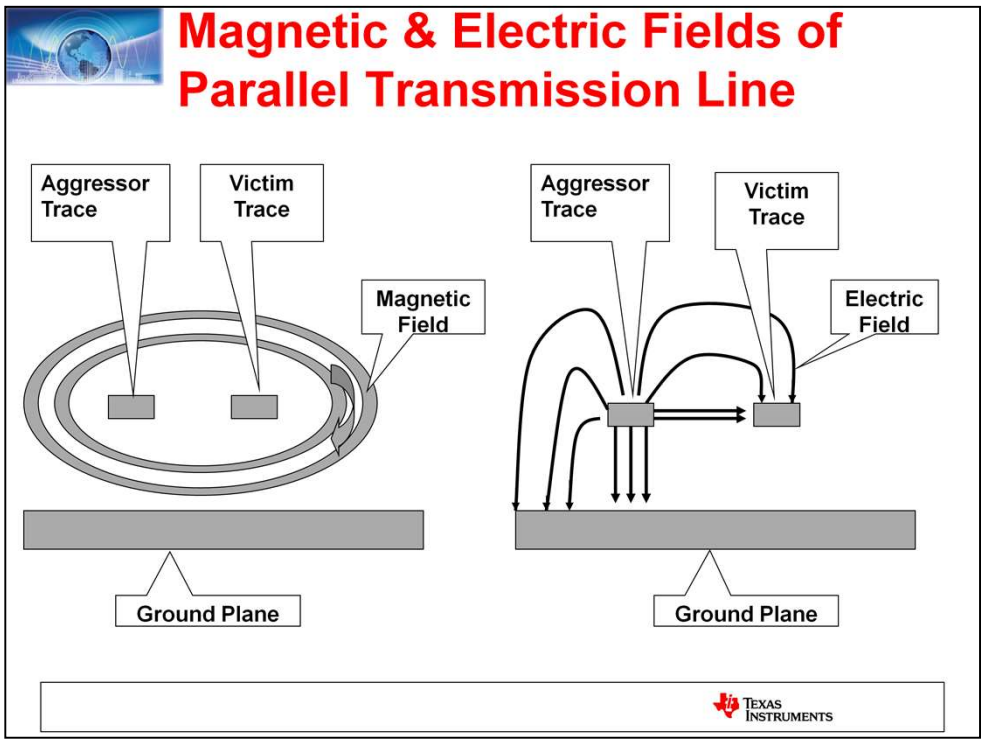
This type of configuration prevents a source reflection from an unterminated transmission line, plus it prevents reflections from the transmission line to the source at the input point (entry of the line).

Practically speaking, termination at only one end of the transmission line is often adequate and is more commonly used.



As a rule of thumb, noise at frequencies below 30 MHz will be transmitted by conduction and noise at frequencies above 30MHz will radiate.

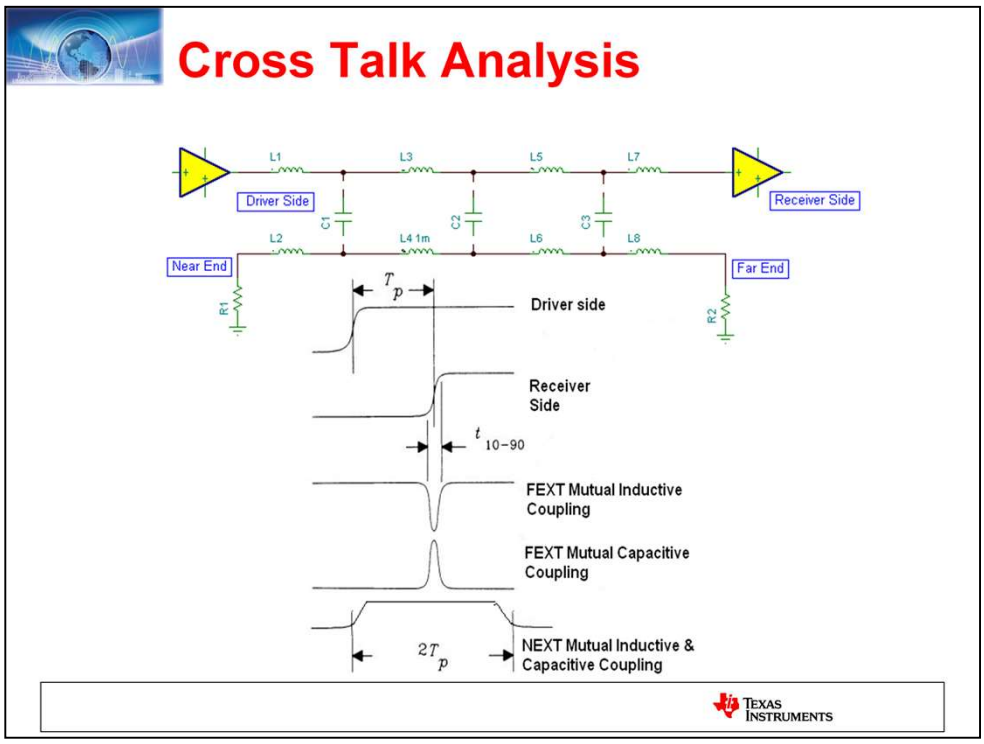
A 12 ns rise time will produce a Effective Operating Frequency around 30 MHz. Most logic drivers (such as CMOS, BiCMOS) will have a rise times less than 12ns.



Mutual inductance, Lm, will inject a voltage noise from a driven line onto any victim trace that is close enough to its magnetic field.

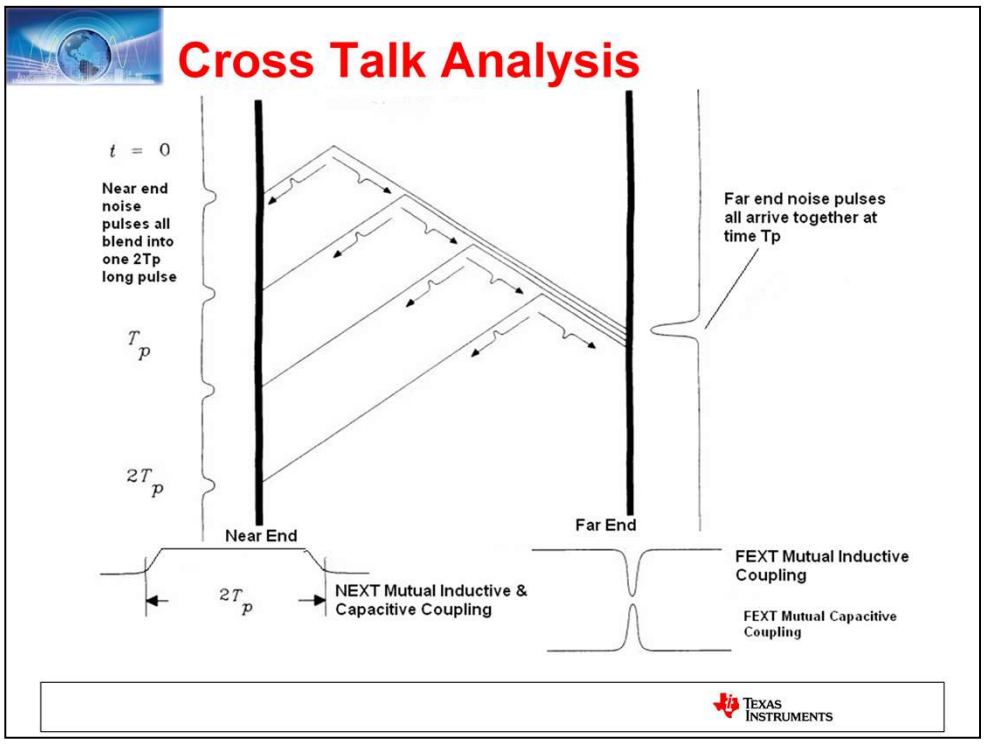
The coupled voltage is proportional to the changing rate of current, so the cross talk is worse in high-speed digital application.

In the twisted pair cable case, which is not shown in this slide, there is no reference plane nearby, so the current will distribute itself more uniformly around the conductor wires.



Let's look at the cross talk situation. As a voltage step moves from the driver to receiver end of a trace, the rising edge is coupled to its adjacent line as noise pulses by each section of the mutual inductances and capacitances.

Each noise pulse propagates to the near and far end on the neighboring transmission line.



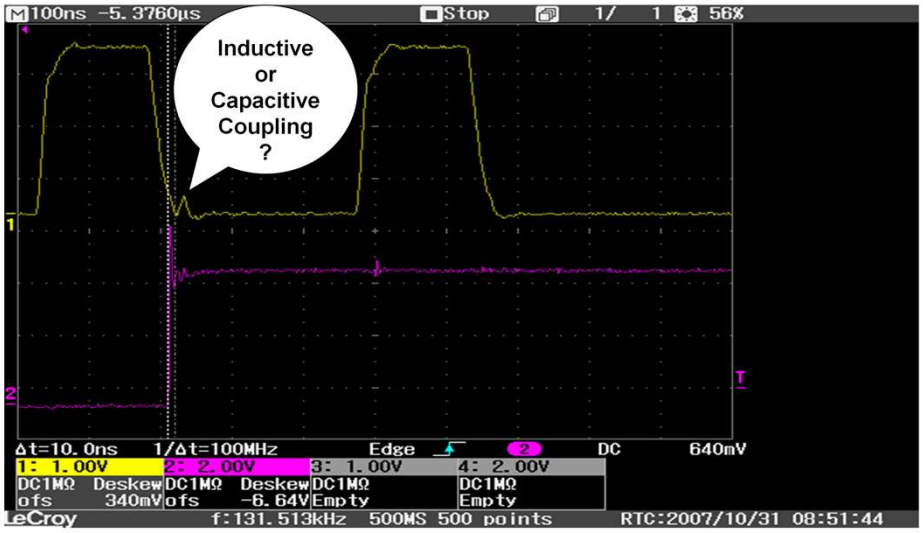
The rising edge will cause a negative short pulse at the far end by mutual inductive coupling. The rising edge will also cause a positive short pulse at the far end by mutual capacitive coupling.

If these two pulses are not equal, they can't be cancelled.

The rising edge will create a long pulse at the near end by both mutual inductive and capacitive coupling.

These two pulses are both appeared as positive ones at the near end.

FEXT Measurement



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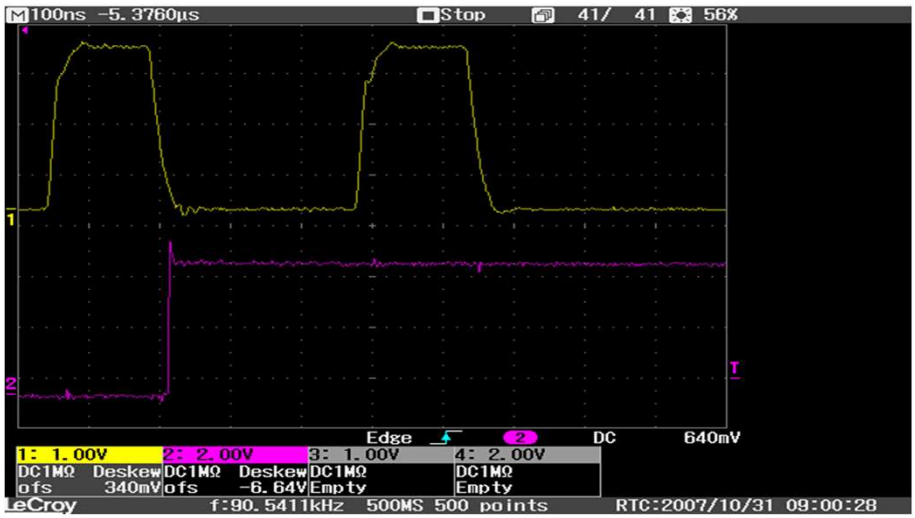
The measured FEXT result are shown in this slide.

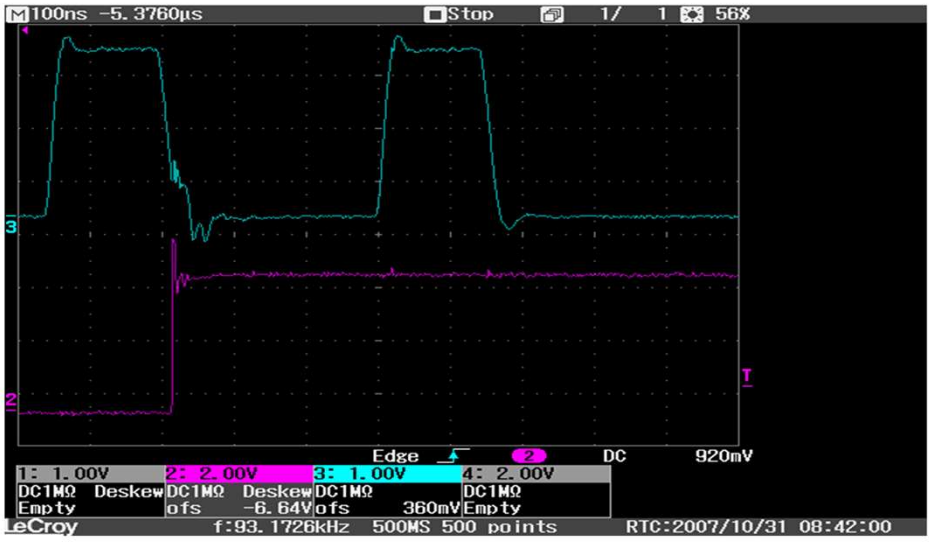
The combined two noise pulses still cause a short positive pulse at the far end, which means that the capacitive coupling is larger than inductive coupling in this cable since they are not 100% cancelled out.

Reduced FEXT Measurement



The data signal is transmitted in a separated wire, so the FEXT is greatly reduced.

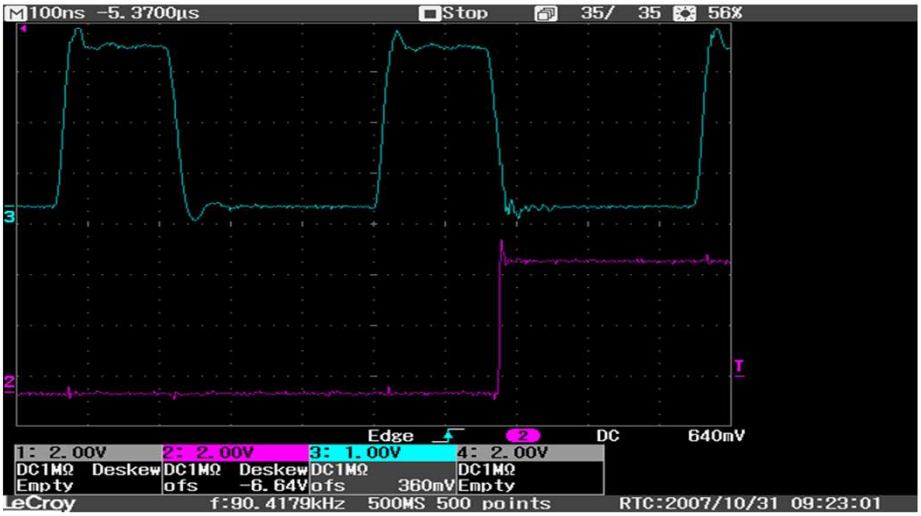
NEXT Measurement



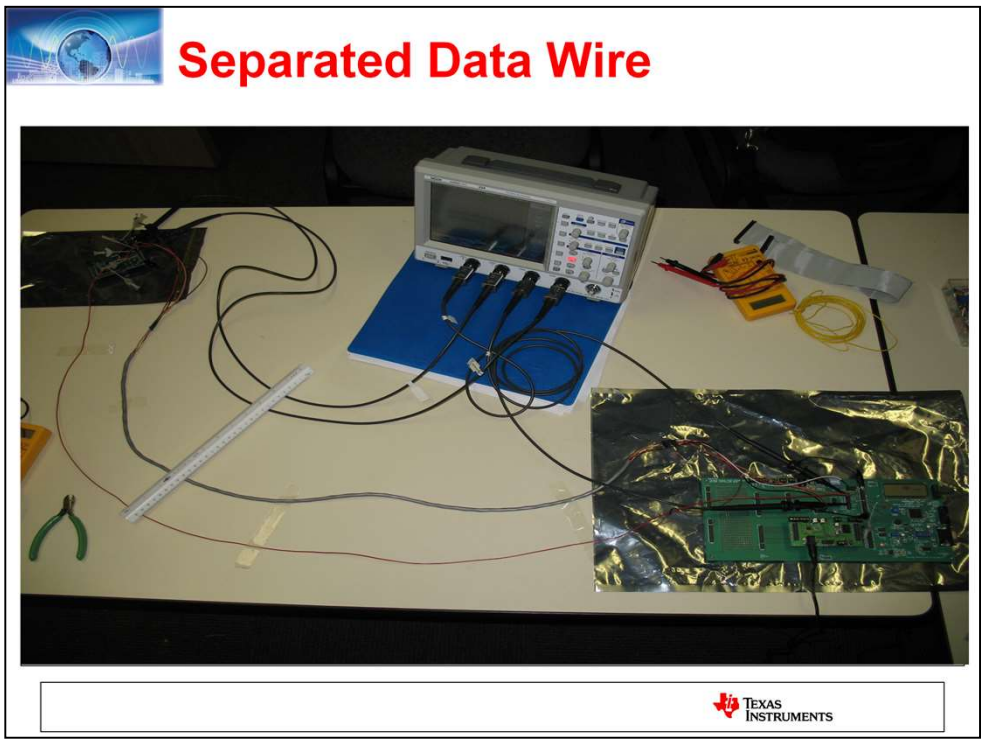
The noise pulse is measured at the near end.

The NEXT noise pulse area is larger than FEXT noise pulse area since the inductive and capacitive coupling is in phase (both are positive pulses). There is no cancellation at NEXT.

Reduced NEXT Measurement

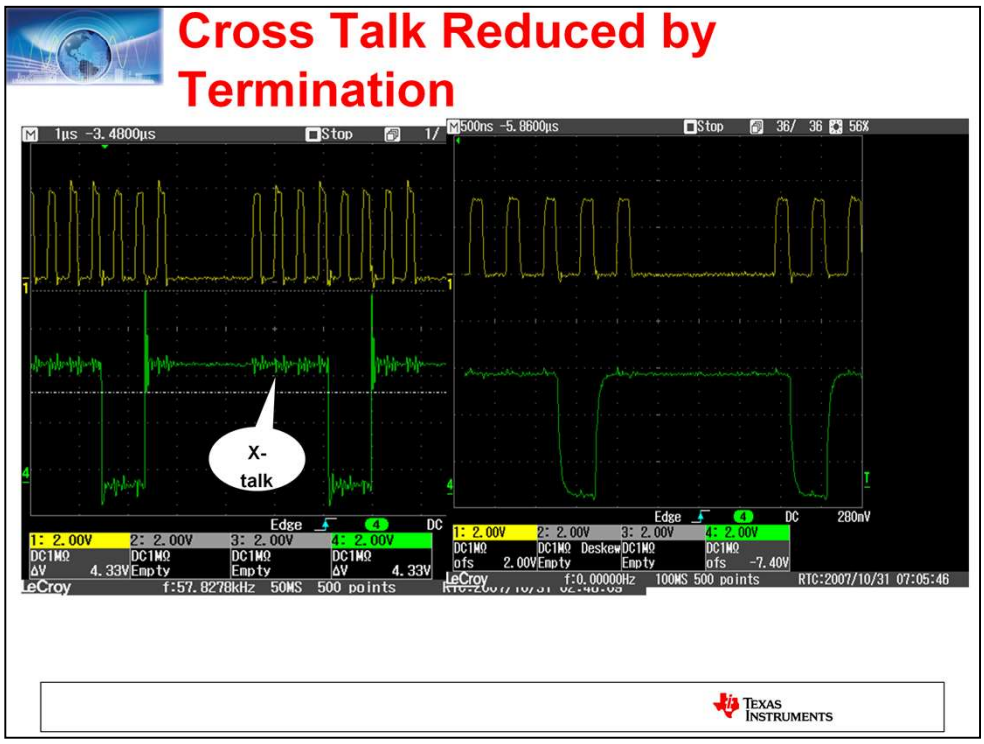


NEXT is measured at near end after the data and clock wires are separated.



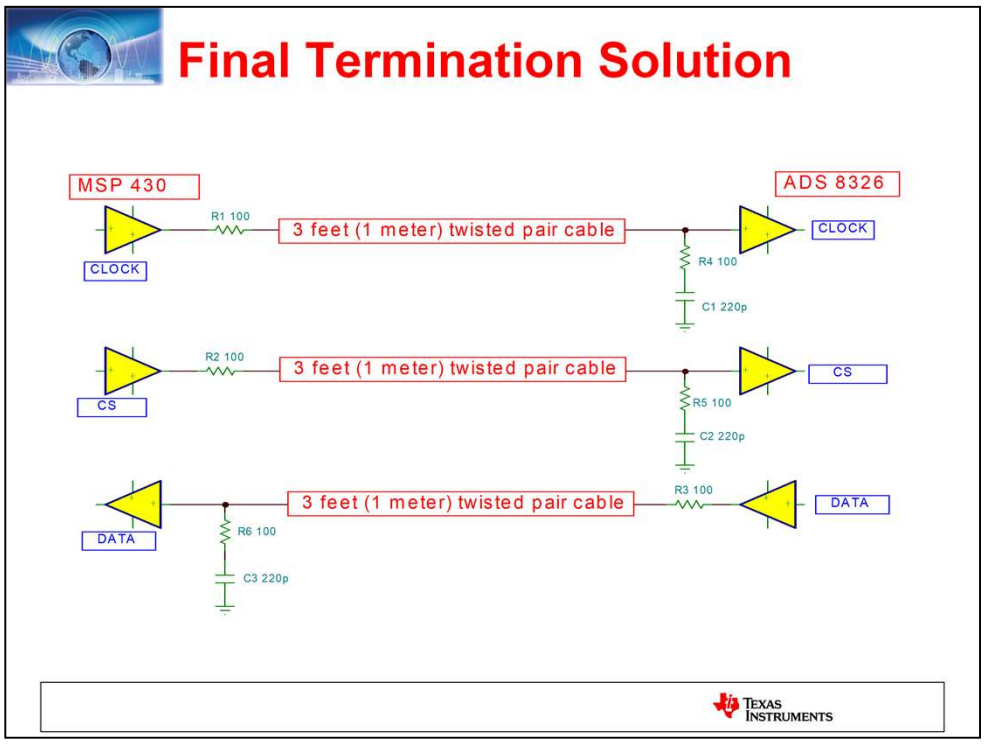
Here is the test setup where the data and clock wires are separated.

The ADS8326 EVM and MSP430 evaluation boards are connected through two 3 feet cables and are kept 3-inch distance as shown in this picture.



For clock and data share one CAT-5 cable case, an interesting point is that, the crosstalk can be dramatically reduced only by a proper termination technique.

The reason is that the mutual inductance and capacitance are proportional to either the voltage or the current changing rate. When ringing is reduced by termination, the signal slew rate becomes smaller. This results in less mutual coupling and cross talk. This has been proved by our measured results.



Here is our proposed termination solution to our application example, and all of our measured results are based on this termination scheme.

Note:

This technique uses an AC termination (a 100 Ω resistor in series with a 220pf capacitor) at receiver side, and series termination (100 Ω) at driver side.