```
U32 TiRocAFE77xxSetCtrlDb(U32 ulChipId,U32 ulBranchType,U32 ulchannel, U32 uldBValue_0p1db)
{
   U32 ulSemFlag = BSP_FALSE;
   U32 ulPageRegValue = 0;
   U32 ulPageAddr = 0;
   U32 uldBValue_1db = 0;
   U32 ulDsaReg = 0;

    __TRY
   {
      THROW_IF((ulChipId >= AFE77XX_MAX_NUM), M_common_PARAMETER_ERR);
      THROW_IF_PARA((ulchannel > EN_BRANCH_D), M_afe77xx_PARA_ERROR, ulchannel, NOT_CARE);
      CATCH_SEMTAKE(g_asemTIROCRWMutexsem[ulChipId], ulSemFlag);

      uldBValue_1db = uldBValue_0p1db/10;

      if(EN_BRANCH_TX == ulBranchType)
      {
         if ((0 == ulchannel)||(1 == ulchannel))
         {
            ulPageRegValue = 0x10;
         }
         else if((2 == ulchannel)||(3 == ulchannel))
         {
            ulPageRegValue = 0x20;
         }
         ulPageAddr = 0x0016;
         EXEC(AFE77xx_RegWrite(ulChipId,ulPageAddr,ulPageRegValue));
         if(0 == (ulchannel%2))

         {   /*Need two writes for u1dBValue_1db */
            EXEC(AFE77xx_RegWrite(ulChipId,0x0100,uldBValue_1db));
                                    EXEC(AFE77xx_RegWrite(ulChipId,0x0100,uldBValue_1db));
            EXEC(AFE77xx_RegWrite(ulChipId,0x0101,0x00));

         }
         else
         { /*Need two writes for u1dBValue_1db */
            EXEC(AFE77xx_RegWrite(ulChipId,0x0120,uldBValue_1db));
                                    EXEC(AFE77xx_RegWrite(ulChipId,0x0120,uldBValue_1db));
            EXEC(AFE77xx_RegWrite(ulChipId,0x0121,0x00));
```

```
    }
    EXEC(AFE77xx_RegWrite(ulChipId,ulPageAddr,0x00));
}
else if(EN_BRANCH_RX == ulBranchType)
{
    ulPageAddr = 0x0010;
    ulPageRegValue = 0x4<<(ulchannel>>1);
    EXEC(AFE77xx_RegWrite(ulChipId,ulPageAddr,ulPageRegValue));
    /* 设置mean */
    EXEC(AFE77xx_RegWrite(ulChipId,0x026d + (0x0400*(ulchannel&1)),uldBValue_1db));
    /* 设置defalt */
    EXEC(AFE77xx_RegWrite(ulChipId,0x0268 + (0x0400*(ulchannel&1)),uldBValue_1db));
    EXEC(AFE77xx_RegWrite(ulChipId,ulPageAddr,0x00));
}
else if(EN_BRANCH_FB == ulBranchType)
{
    ulPageAddr = 0x0016;
    EXEC(AFE77xx_RegWrite(ulChipId,ulPageAddr,0x10));
    EXEC(AFE77xx_RegWrite(ulChipId,0x0150,uldBValue_1db));
    EXEC(AFE77xx_RegWrite(ulChipId,ulPageAddr,0x00));
}
else if(EN_BRANCH_CAL_TX == ulBranchType)
{
    THROW_IF_PARA((uldBValue_1db > 39), M_afe77xx_PARA_ERROR, ulchannel, uldBValue_1db);

    ulPageAddr = 0x0013;
    EXEC(AFE77xx_RegWrite(ulChipId,ulPageAddr,0x10));
    EXEC(AFE77xx_RegWrite(ulChipId,0x00a0,0x13));
    EXEC(AFE77xx_RegWrite(ulChipId,0x00a1,0x04+((ulchannel&1)*0x20)));
    EXEC(AFE77xx_RegWrite(ulChipId,0x00a2,0x01));
    EXEC(AFE77xx_RegWrite(ulChipId,0x00a3,0x00));

    if ((ulchannel>>1)==0)
    {
      EXEC(AFE77xx_RegWrite(ulChipId,0x00a4,0xae));
    }
    else
    {
     EXEC(AFE77xx_RegWrite(ulChipId,0x00a4,0xaf));
    }
    EXEC(AFE77xx_RegWrite(ulChipId,0x00a5,uldBValue_1db));
```

```
    EXEC(AFE77xx_RegWrite(ulChipId,0x0193,0x02));
    EXEC(AFE77xx_RegWrite(ulChipId,ulPageAddr,0x00));
  }
  else if(EN_BRANCH_CAL_RX == ulBranchType)
  {
    THROW_IF_PARA((uldBValue_1db > 30), M_afe77xx_PARA_ERROR, ulchannel, uldBValue_1db);

    ulPageAddr = 0x0013;

    ulDsaReg=0x5C+(0x60*(ulchannel&1));
    EXEC(AFE77xx_RegWrite(ulChipId,ulPageAddr,0x10));
    EXEC(AFE77xx_RegWrite(ulChipId,0x00a0,0x13));
    EXEC(AFE77xx_RegWrite(ulChipId,0x00a1,ulDsaReg));
    EXEC(AFE77xx_RegWrite(ulChipId,0x00a2,0x00));
    EXEC(AFE77xx_RegWrite(ulChipId,0x00a3,0x00));
    if ((ulchannel>>1)==0)
    {
      EXEC(AFE77xx_RegWrite(ulChipId,0x00a4,0xae));
    }
    else
    {
       EXEC(AFE77xx_RegWrite(ulChipId,0x00a4,0xaf));
    }
    EXEC(AFE77xx_RegWrite(ulChipId,0x00a5,uldBValue_1db));
    EXEC(AFE77xx_RegWrite(ulChipId,0x0193,0x02));
    EXEC(AFE77xx_RegWrite(ulChipId,ulPageAddr,0x00));
  }

  CATCH_SEMGIVE(g_asemTIROCRWMutexsem[ulChipId], ulSemFlag);

  return M_afe77xx_OK;
}

 __CATCH
{
  if(0 != ulPageAddr)
  {
    (void)AFE77xx_RegWrite(ulChipId,ulPageAddr,0x00);
  }
  if((ulchannel <= EN_BRANCH_D)&&(ulChipId < AFE77XX_MAX_NUM))
  {
    CATCH_SEMGIVE(g_asemTIROCRWMutexsem[ulChipId], ulSemFlag);
```

```
      }
      CPBSP_DEBUGOUTPUT(IRF_IFLOGIC_CODEBASE, OUTPUT_RESERVED_MODULE_ID2,
OUTPUT_LEVEL_ERROR, \
         "[TiRocAFE77xxSetCtrlDb]Line %u, ErrNo 0x%x, para1 0x%x, para2 0x%x.\n\r", \
         ERR_LINE, ERR_CODE, ERR_PARA1, ERR_PARA2);
      return ERR_CODE;
   }

}
```