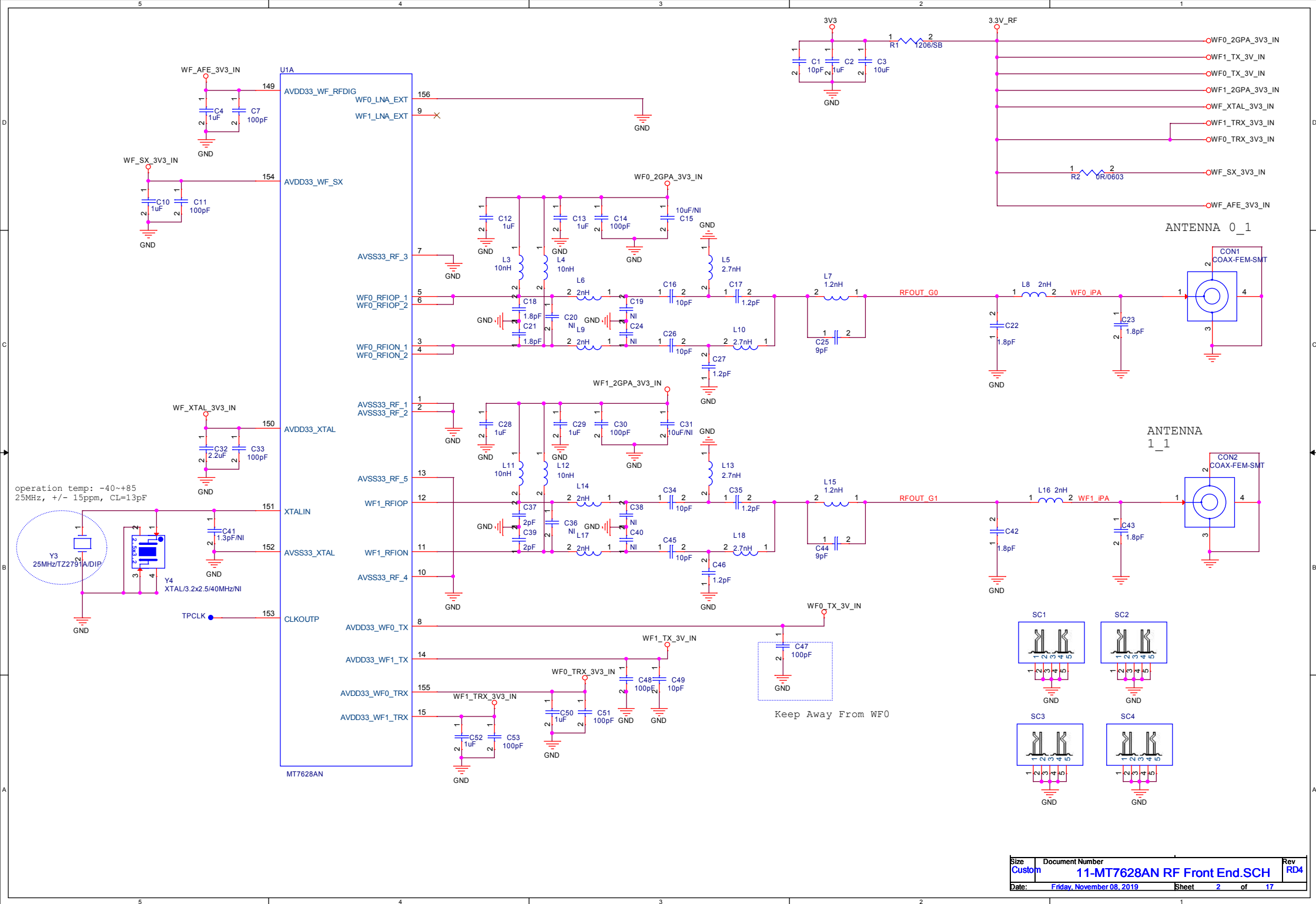
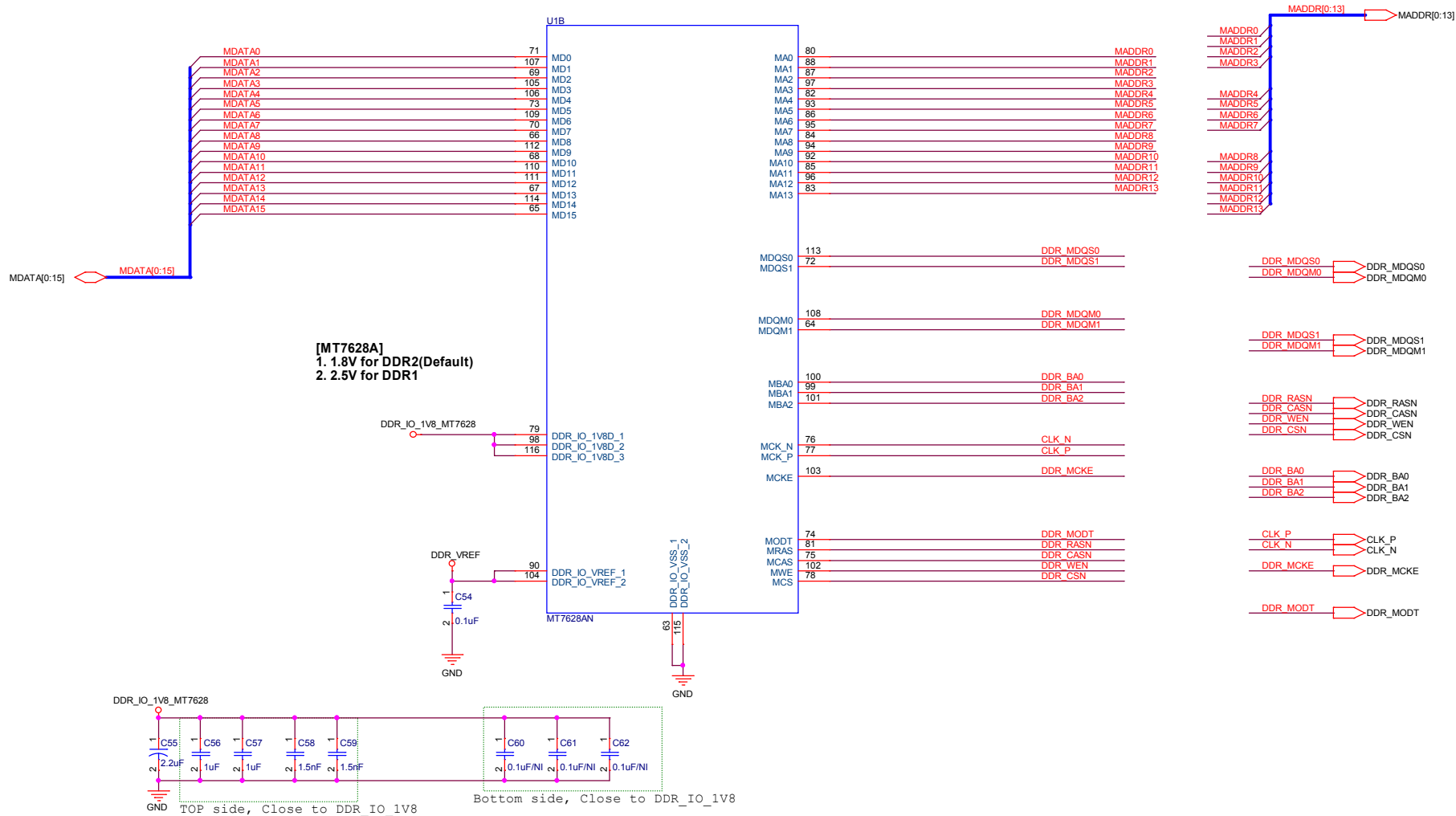


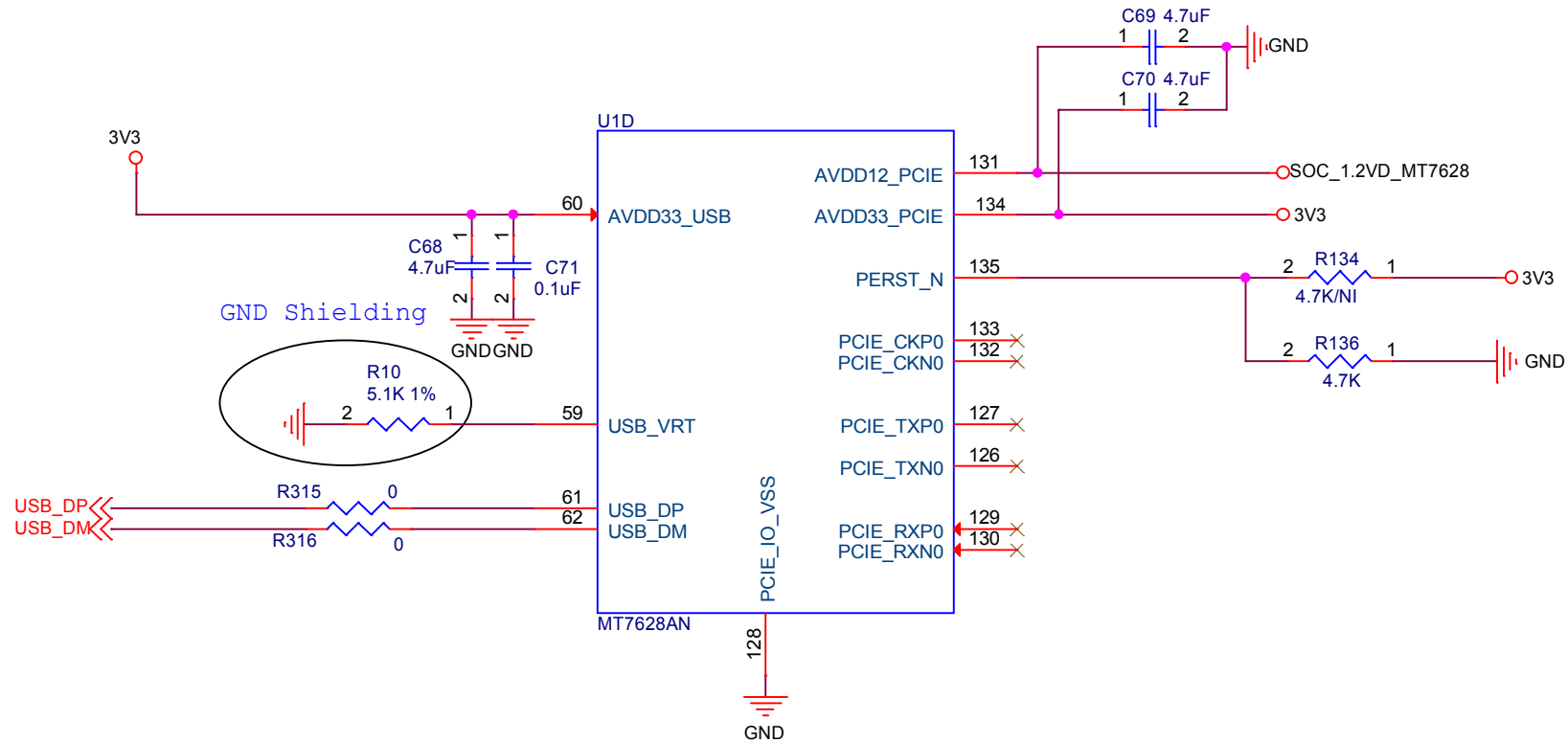
2-MEMORY

2-MEMORY

1-CPU-MT7628A

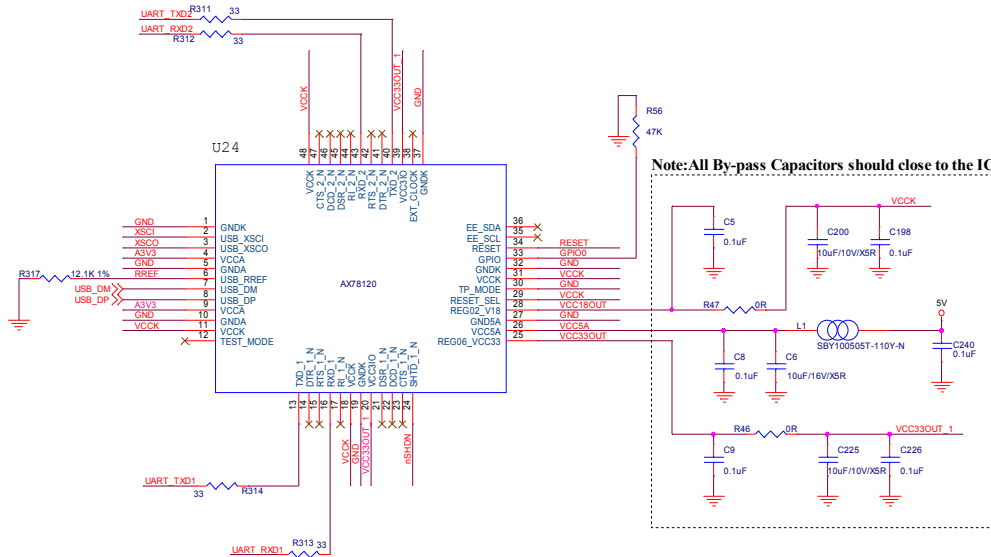




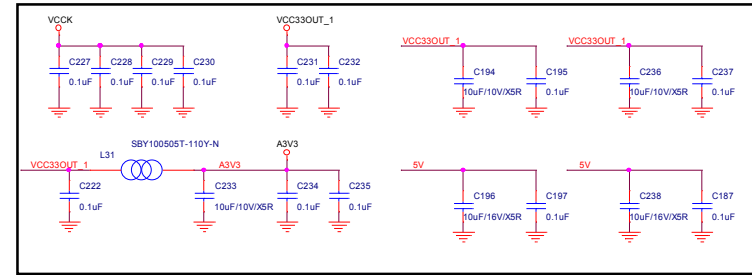


M481

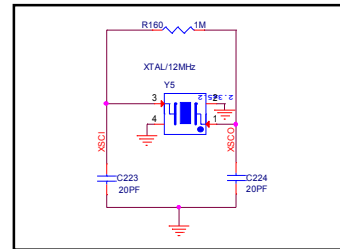
Size A	Document Number M481.SCH	Rev RD4
Date: Friday, November 08, 2019	Sheet 5 of 17	



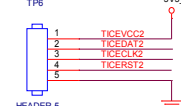
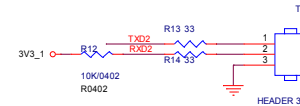
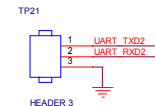
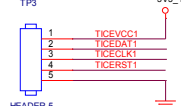
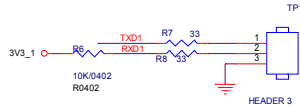
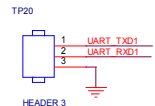
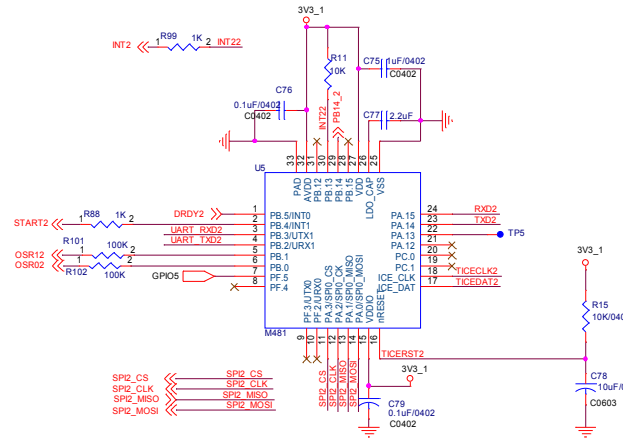
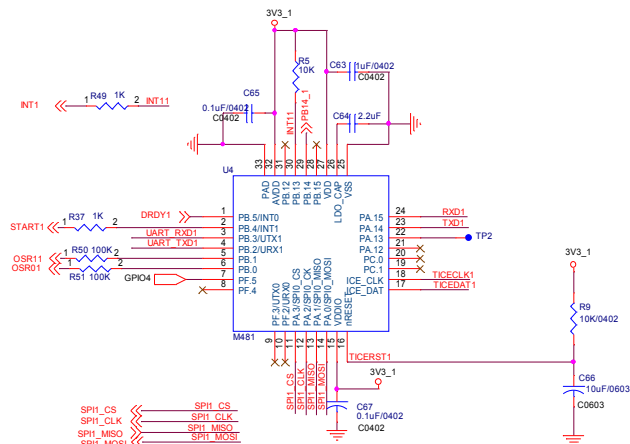
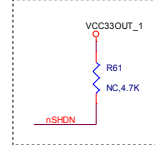
Power Circuit



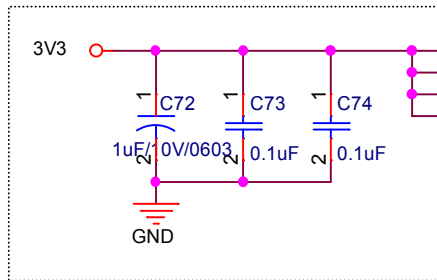
12MHz +/- 30ppm Crystal



Optional



Close to MT7628



U1E

AVDD33_TX_P0
AVDD33_COM
AVDD33_TX_P1234_1
AVDD33_TX_P1234_2

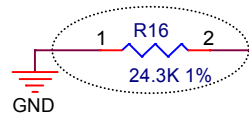
MDI_TN_P4
MDI_TP_P4
MDI_RN_P4
MDI_RP_P4

MDI_TN_P3
MDI_TP_P3
MDI_RN_P3
MDI_RP_P3

MDI_TN_P2
MDI_TP_P2
MDI_RN_P2
MDI_RP_P2

MDI_TN_P1
MDI_TP_P1
MDI_RN_P1
MDI_RP_P1

Close to MT7628



EPHY_VRT

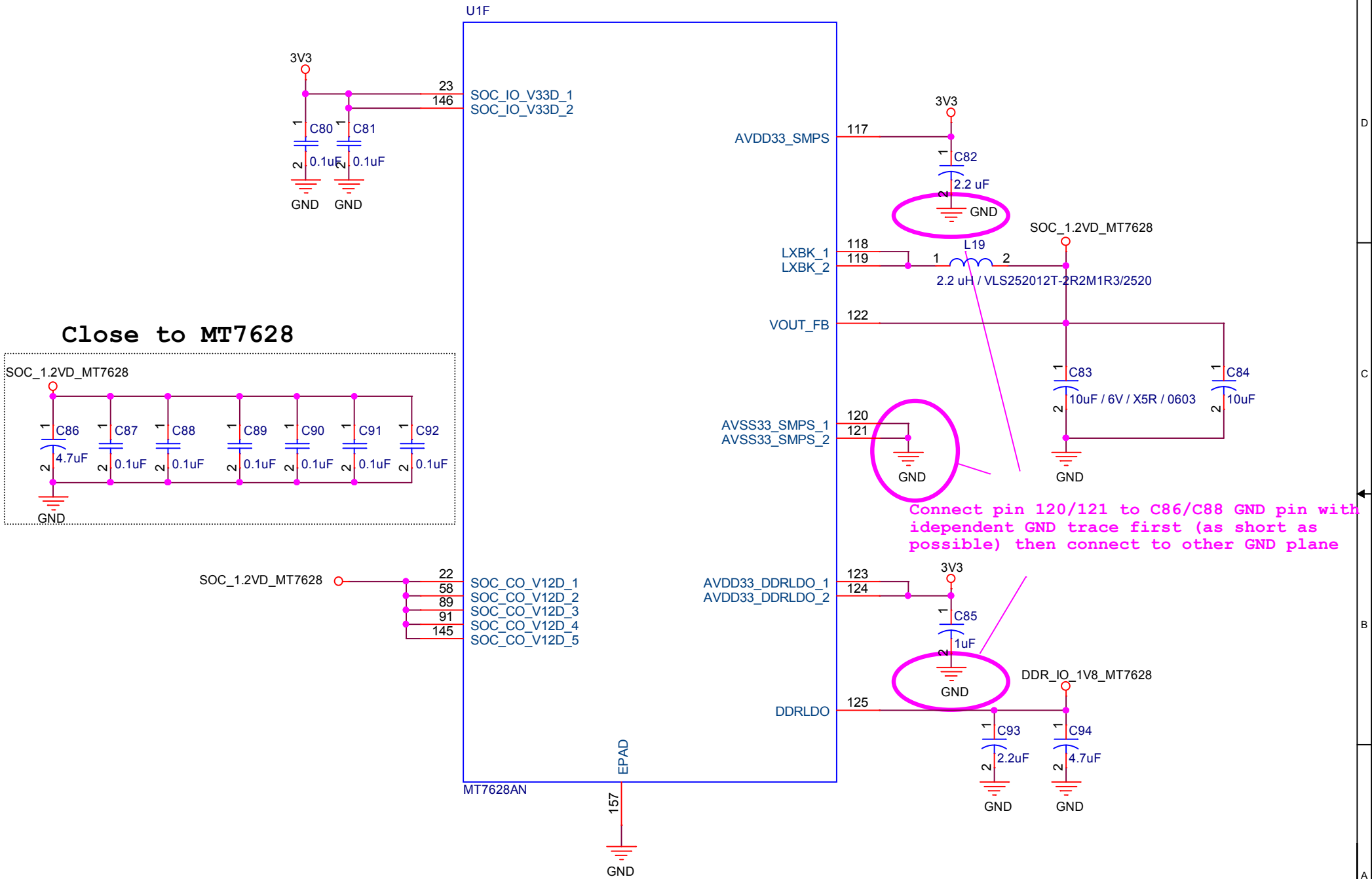
EPHY_LED4_N_JTRST_N
EPHY_LED3_N_JTCLK
EPHY_LED2_N_JTMS
EPHY_LED1_N_JTDI
EPHY_LED0_N_JTDO

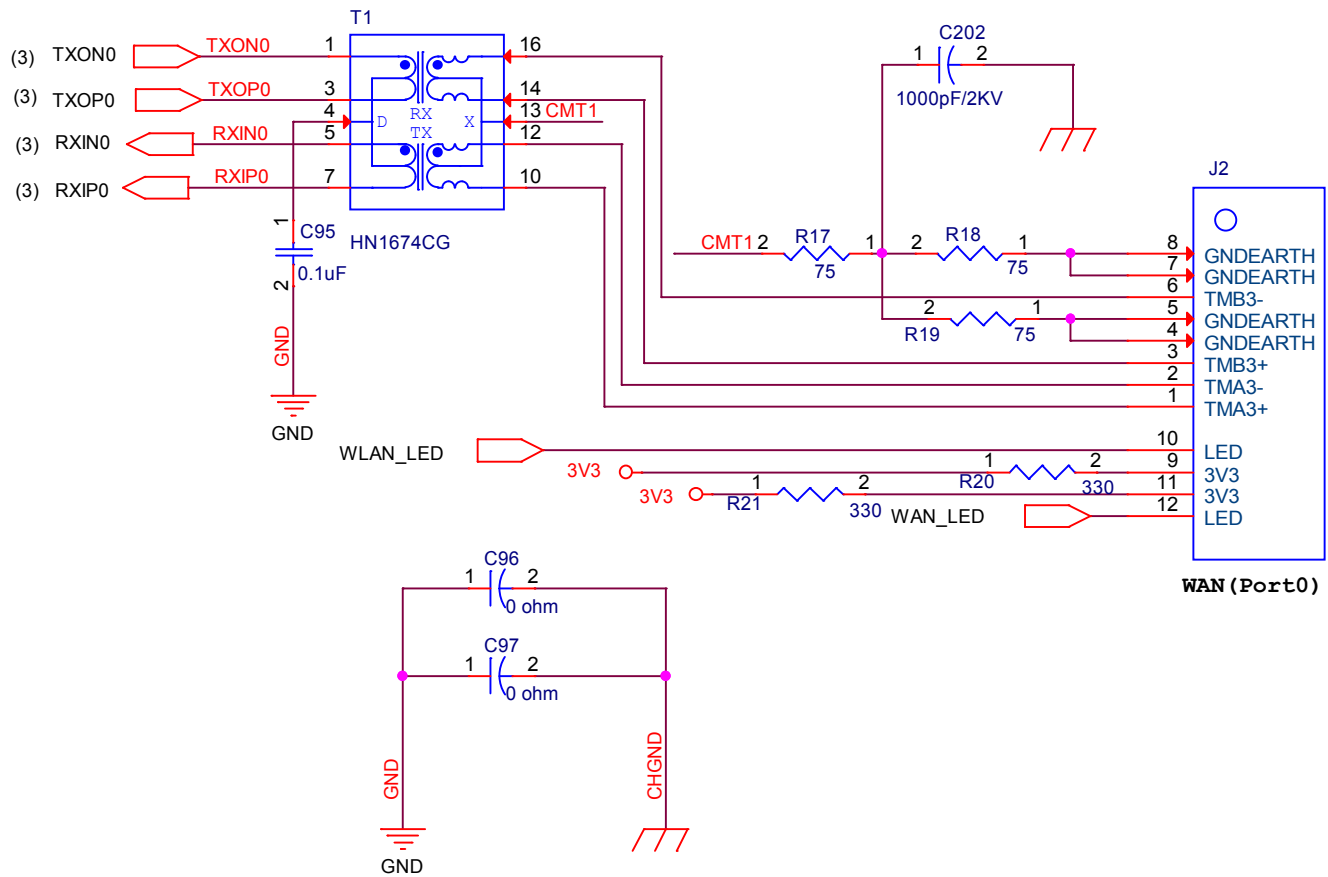
WAN_LED

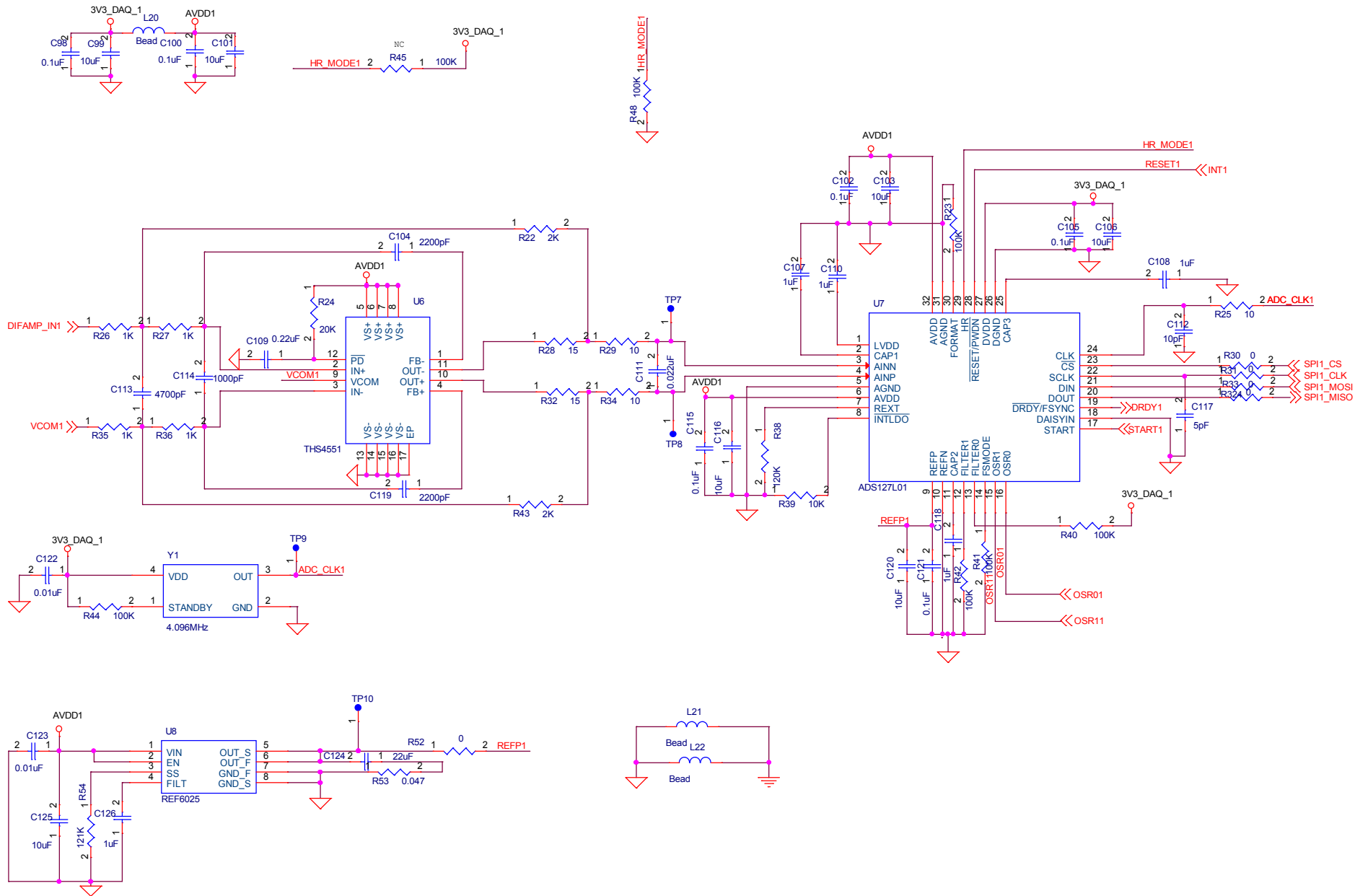
MT7628AN

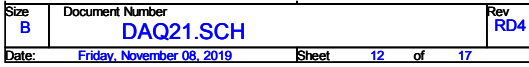
MDI_TN_P0
MDI_TP_P0
MDI_RN_P0
MDI_RP_P0

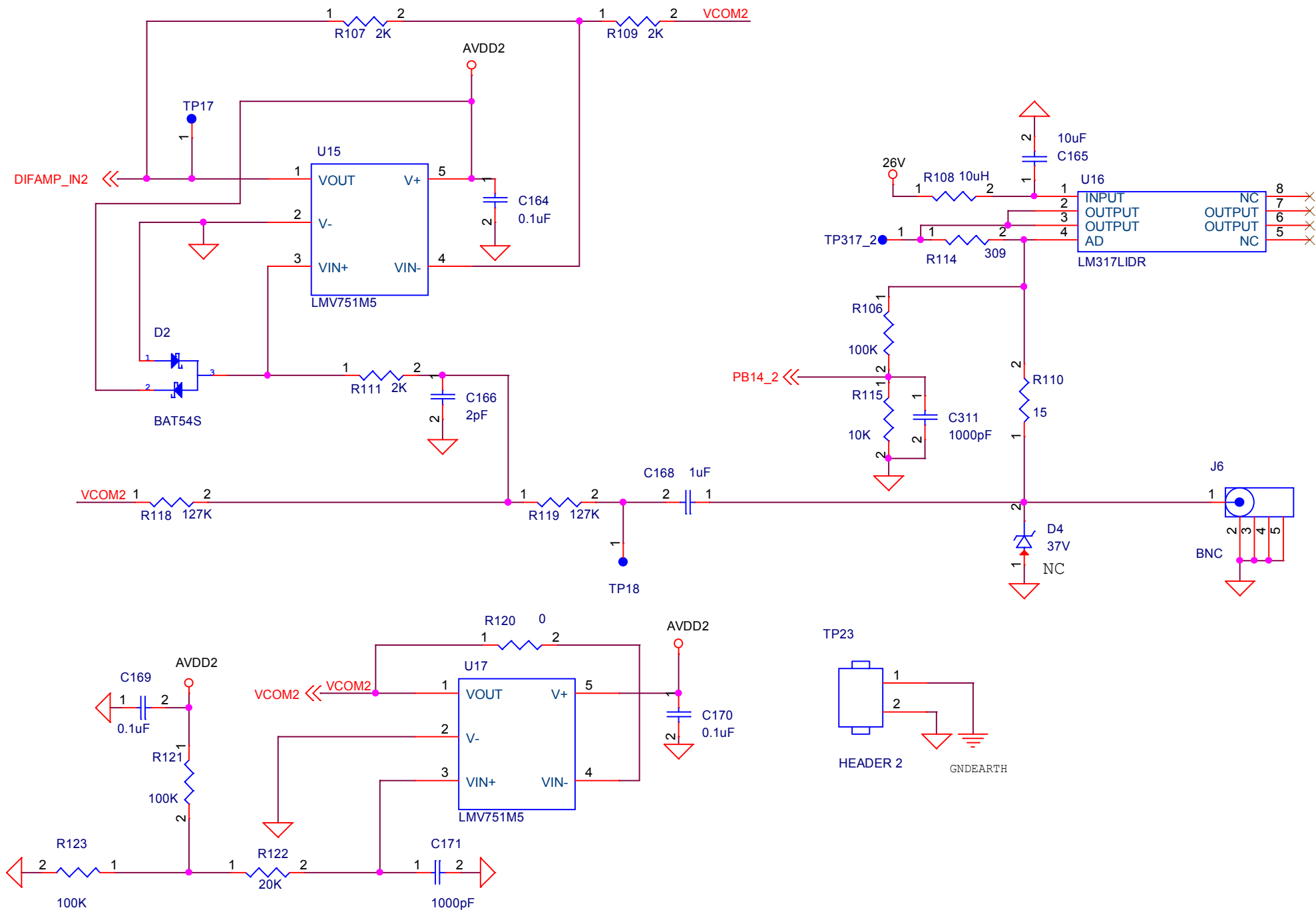
TXON0
TXOP0
RXIN0
RXIP0



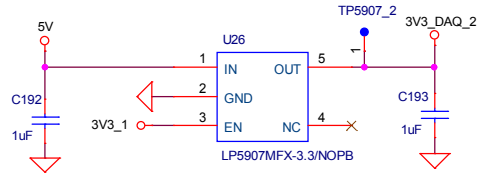
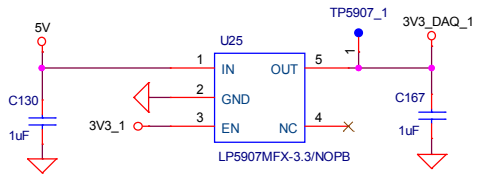
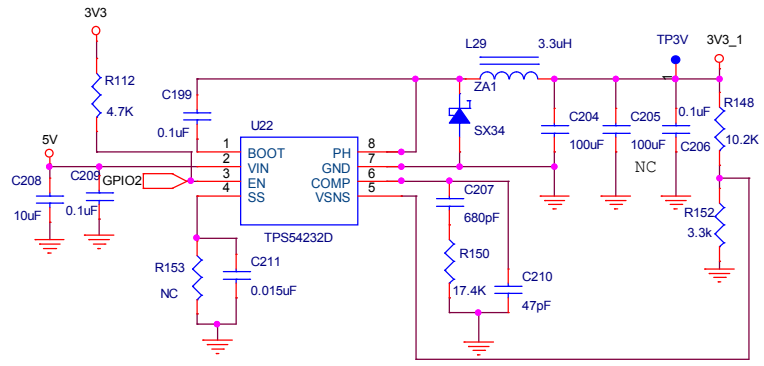
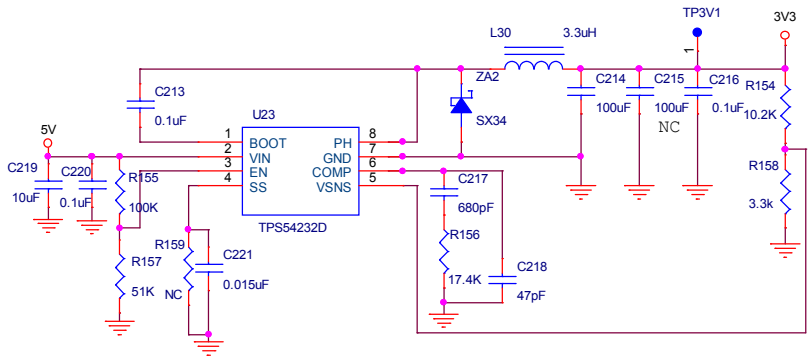
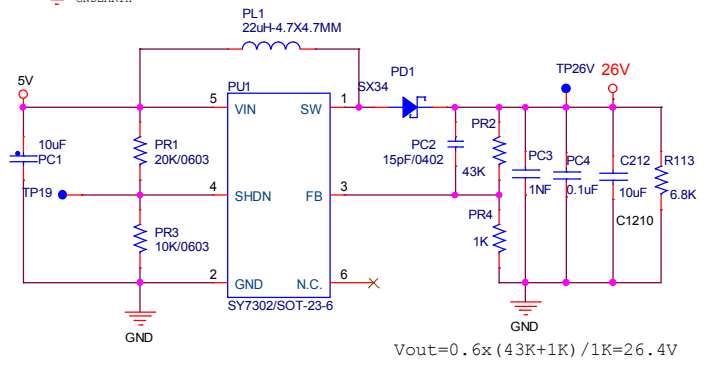
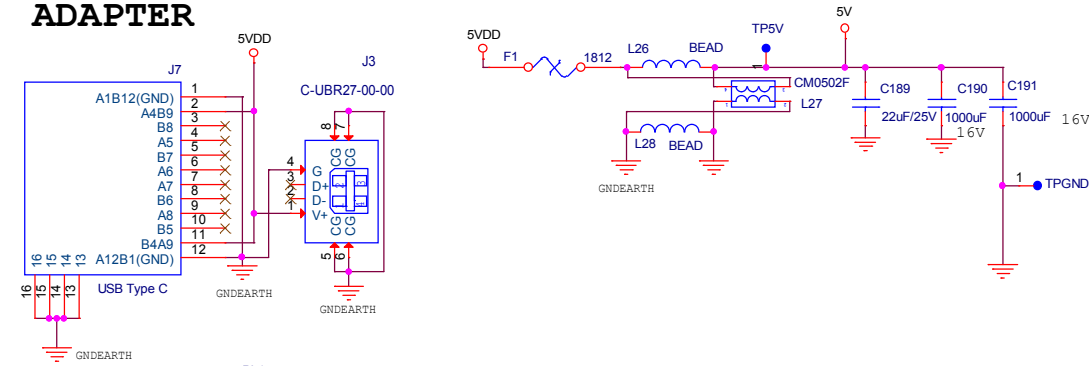


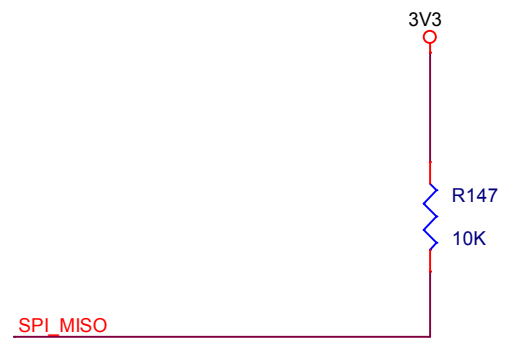
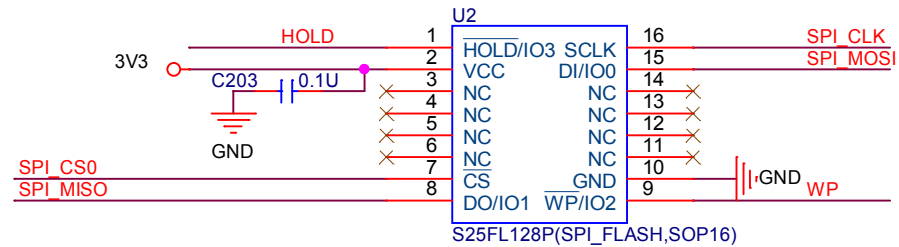
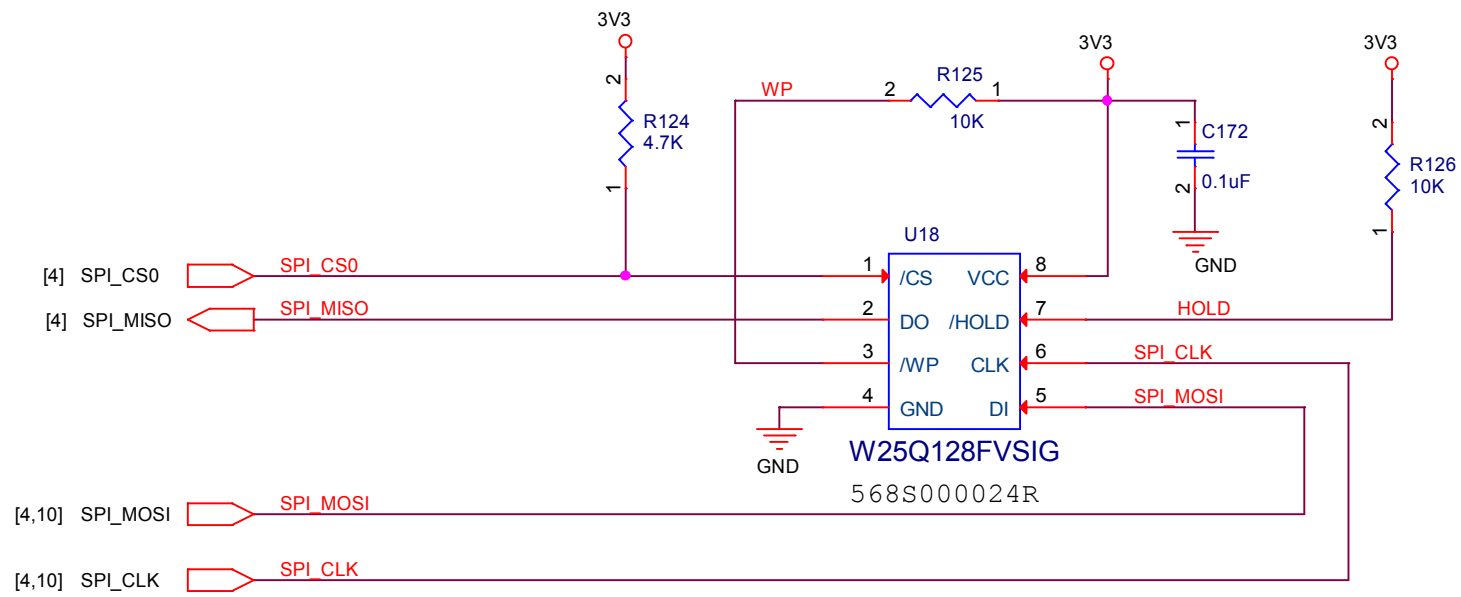






5V DC
ADAPTER





MDATA[0:15]

MDATA[0:15]

MADDR[0:13]

MADDR[0:13]

DDR_BA0
DDR_BA1
DDR_BA2
DDR_MCKE

DDR_CSN

DDR_RASN
DDR_CASN
DDR_WEN

M8 M7 M6 M5 M4 M3 M2 M1
M0 A0 A1 A2 A3 A4 A5 A6
A7 A8 A9 A10 A11 A12 A13 (2Gb)

DDR_BA0
DDR_BA1
DDR_BA2
DDR_MCKE

CLK_P
CLK_N

DDR_CSN

DDR_RASN
DDR_CASN
DDR_WEN

DDR_IO_1V8_MT7628

U19
[Winbond]W9751G6KB_64MB
FBGA84_8X14

512Mb (32Mb x 16)
~2Gb (128Mb x 16)
DDR2 SDRAM

GND

1. 1.8V for DDR2 (Default)
2. 2.5V for DDR1

CLK_P

CLK_P

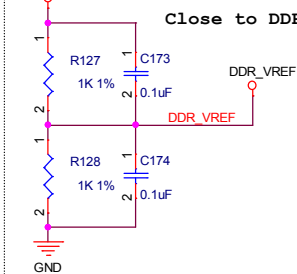
CLK_N

CLK_N

DDR_IO_1V8_MT7628

GND

DDR_IO_1V8_MT7628



DDR_MDQS0

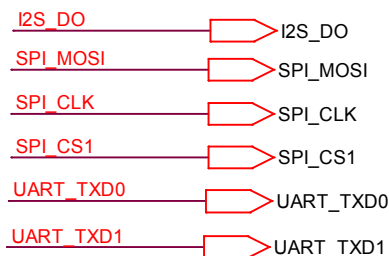
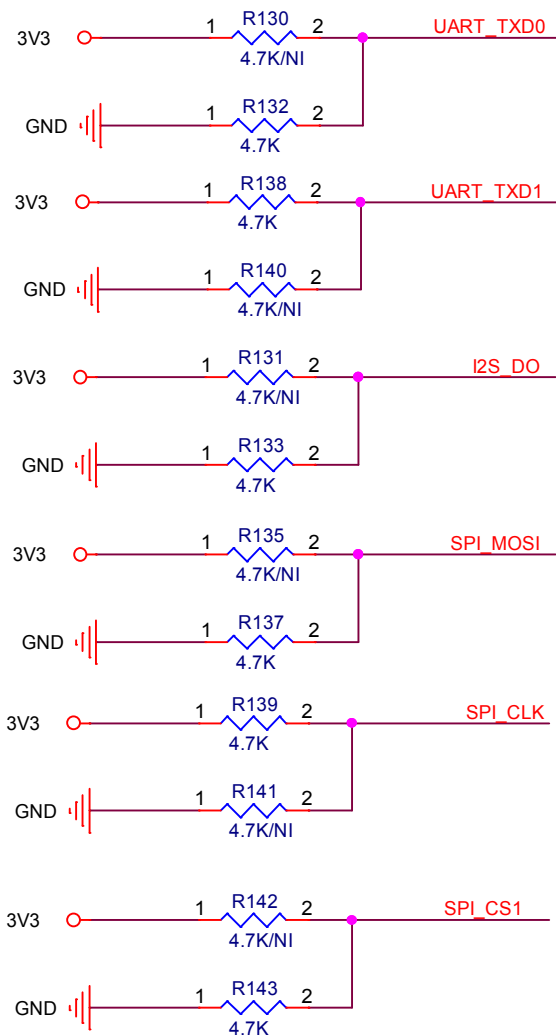
DDR_MDQM0

DDR_MDQS1

DDR_MDQM1

DDR_MODT

Size B	Document Number 22-DDR2-CFG.SCH	Rev RD4
Date:	Friday, November 08, 2019	Sheet 16 of 17



Bootstrapping Pins Description

Pin Name	Boot Strapping Signal Name	Description
UART_TXD1	DBG_JTAG_MODE	0: JTAG_MODE 1: EPHY_LED (default)
PERST_N	XTAL_FREQ_SEL	0: 25 MHz DIP 1: 40 MHz SMD
I2S_SDO	DRAM_TYPE	1: DDR1 0: DDR2 [note] This pin is valid for MT7628AN only. It needs to be pull-low for 7628KN which only supports DDR1.
{SPI_MOSI, SPI_CLK, SPI_CS1}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. 000: Boot from PLL (boot from SPI 3-Byte Addr) 001: Boot from PLL (boot from SPI 4-Byte Addr) 010: Boot from XTAL (boot from SPI 3-Byte Addr) 011: Boot from XTAL (boot from SPI 4-Byte Addr)
PAD_TXD0	EXT_BGCK	1: Test Mode 0: Normal (default)