Welcome!
Texas Instruments New Product Update

- This webinar will be recorded and available at www.ti.com/npu
- Phone lines will be muted
- Please post questions in the chat or contact your sales person or field applications engineer

New Product Update:

High Speed SAR ADCs

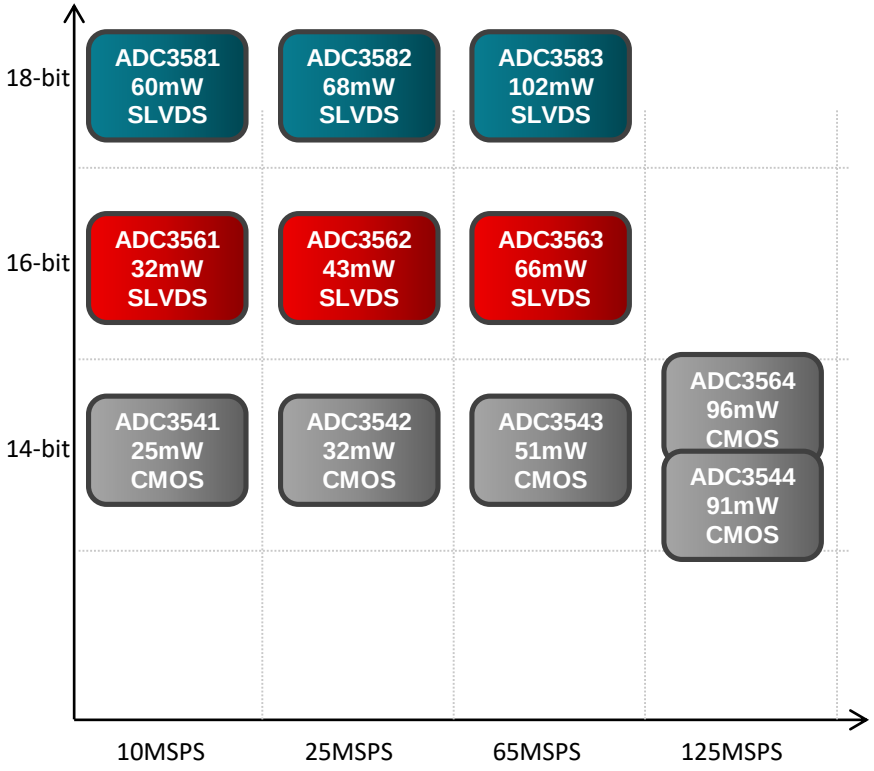
Paul McCormack

February 4th 2021

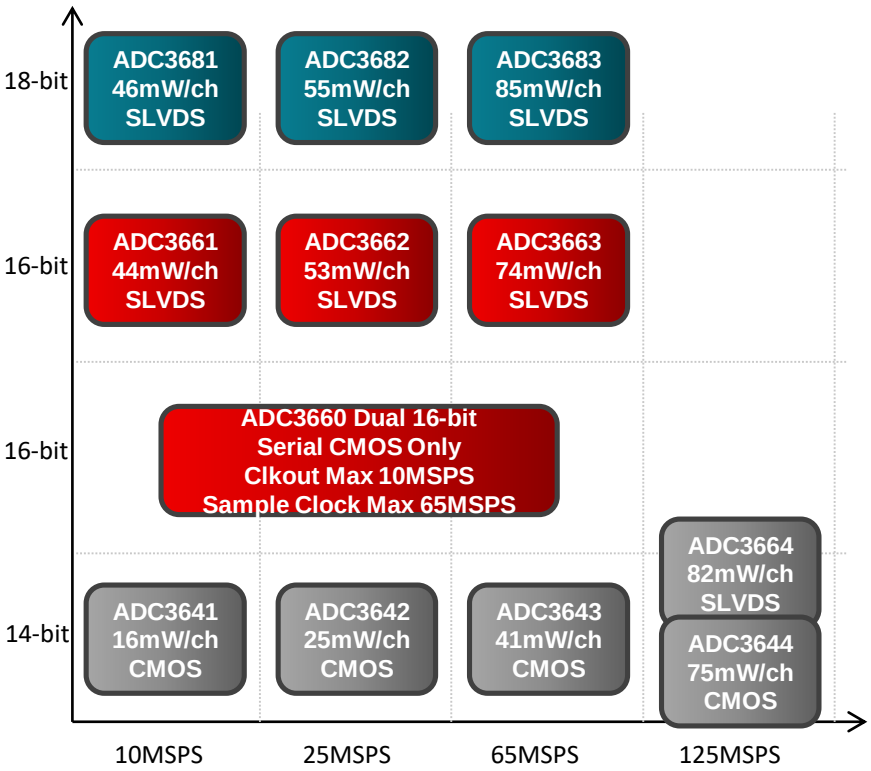
Agenda

- New ADC family overview
  - Key features and target applications
  - Digital Interface
- Internal decimation filter
  - Oversampling and simplification of anti-aliasing filter
  - Oversampling and SNR improvement
- Evaluation tools
- Evaluation measurements

Complete Family



ADC35XX – 1 CHANNEL ADCS



ADC36XX – 2 CHANNEL ADCS

ADC35/36 Single/Dual 14/16/18 Bit, 0.5MSPS to 125 MSPS

Features

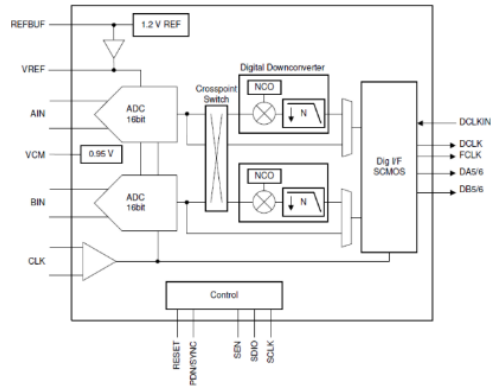
• Sample range:	0.5 – 65/125 MSPS (14 bit)
	0.5 – 65 MSPS (16/18 bit)
• Low Latency:	1 – 2 clock cycles
• Low Power:	29mW to 100mW per channel
• No missing codes	
• Input Bandwidth	900 MHz (up to 65MSPS)
	1400 MHz (125MSPS)
• Wake Up time	14 us
• INL/DNL	0.5/0.2, 2.0/0.2, 7/0.7 LSB
	(14/16/18bit typ)
• Reference options	Int and Ext 1.2/1.6V
• SNR	79/82/85 dB (14/16/18 bit)
• SFDR/THD	95dB at 1 MHz
• DDC	Decimation by 2, 4, 8, 16, 32
	32-bit NCO
• Digital Interface:	SDR/DDR CMOS & SLVDS
• Power supply:	1.8V (14/16/18 bit)
• Package:	40QFN (5x5mm)
• Low cost Sitara based reference design available in Q1 2021	

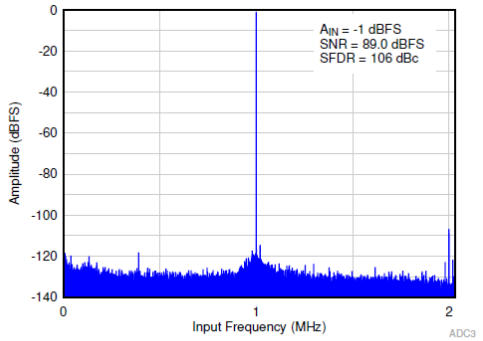
Applications

- Data Acquisition
- Power Quality Analyzer / meter
- Imaging (Thermal, MRI, PET)
- Ultrasonic Flow Metering
- Motor diagnostics & monitoring
- Sonar & Radar
- High-speed Control Loops
- OTDR
- Wireless Communicaitons
- Single 1.8V power supply

Key features

High dynamic range (85dB SNR, 95dB SFDR)
>90dB SNR, > 100dB SFDR (on chip 32x decimation)
Low power consumption 29mW to 100mW/ch
Excellent Linearity 0.2 LSB DNL, 0.5 LSB INL
Internal or external reference options
Programmable decimation and NCO
900MHz / 1400MHz (65/125MSPS) input bandwidth
1 – 2 clock cycle latency
CMOS or SLVDS interface



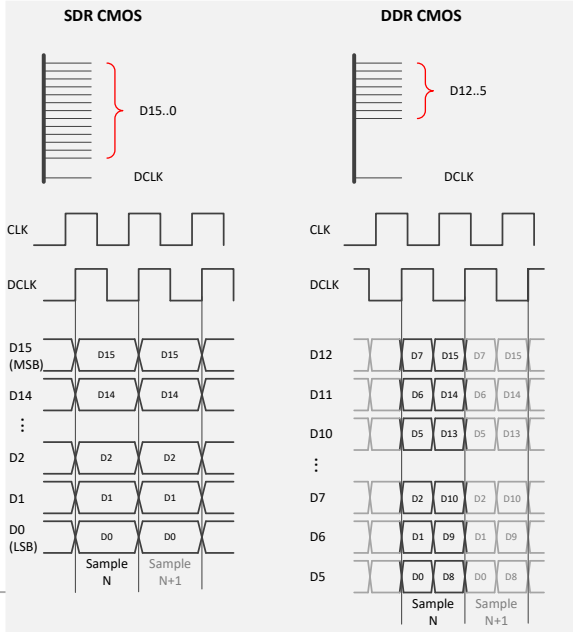


FS = 65 MSPS, F_{in} = 1 MHz, 16x Decimation, real

Digital Interface Options

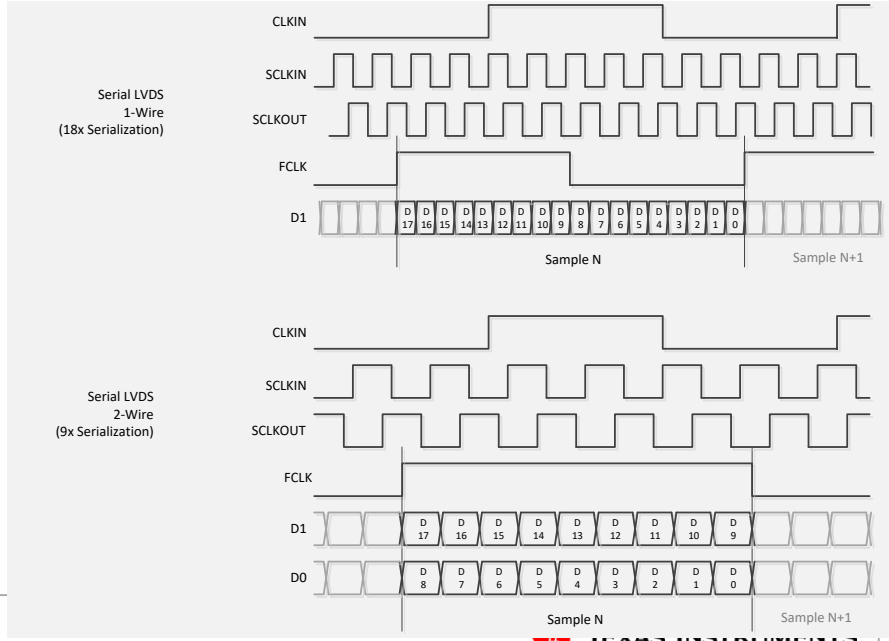
Single ended CMOS (example)

CMOS Interface	ADC Sampling Rate	DCLK	FCLK	Dout
SDR CMOS	65Msps	65Msps	-	65Msps
DDR CMOS	65Msps	65Msps	-	130Msps



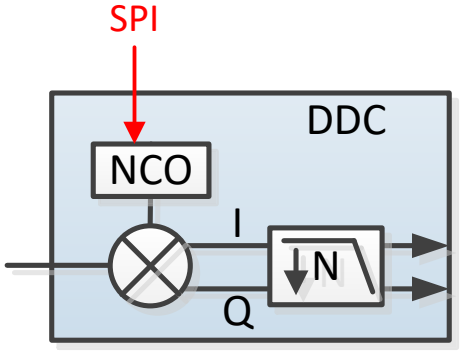
Serial LVDS (example)

CMOS Interface	ADC Sampling Rate	FCLK Rate	SCLKIN	SCLKOUT	D0/D1
1 wire SLVDS	32.5Msps	32.5Msps	292.5Msps	292.5Msps	585Msps
2 wire SLVDS	65Msps	32.5Msps	292.5Msps	292.5Msps	585Msps

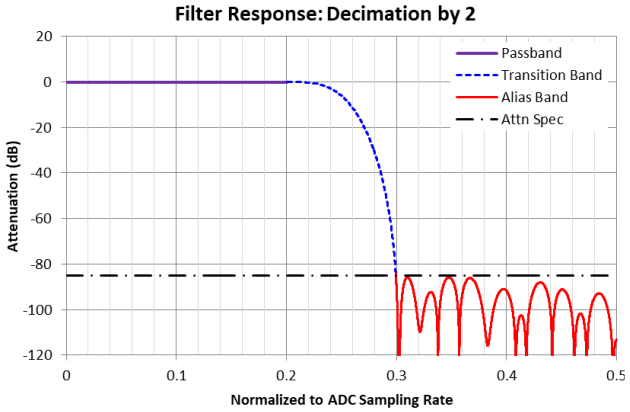


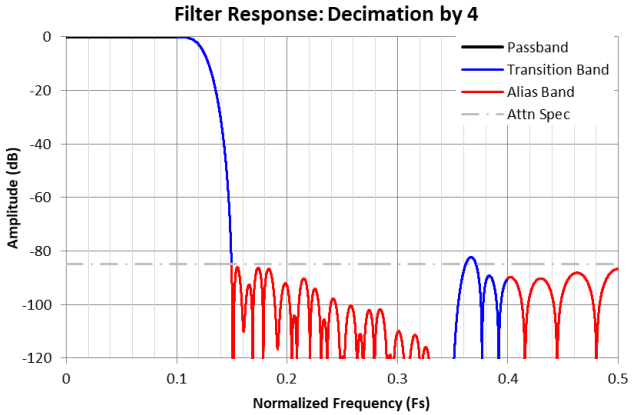
Internal Decimation Filter

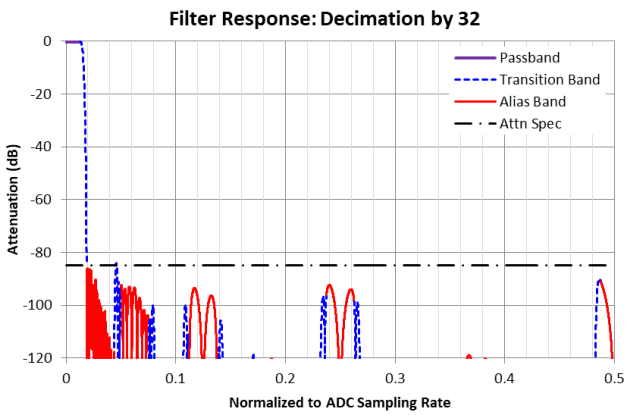
- Complex Decimation by 2, 4, 8, 16 and 32
- 32-bit NCO: Frequency Resolution
- Supports real output decimation w/o NCO
  - 2, 4, 8, 16, 32 decimation
- Passband: ~42%
- Stopband attenuation ~ 85dB min

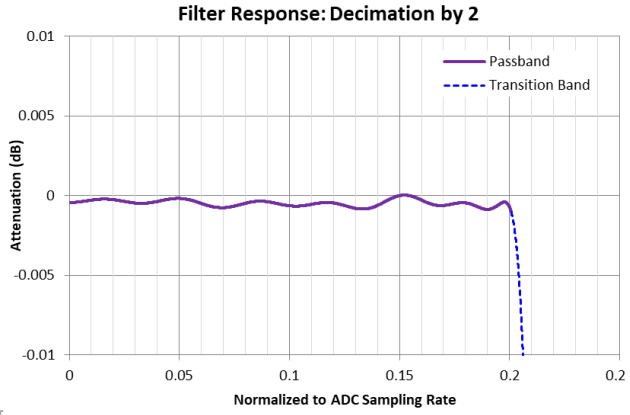


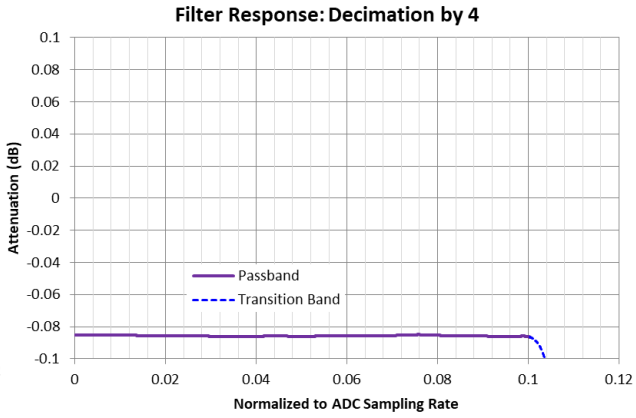
Decimation Filter Response (/2, /4 and /32 examples)

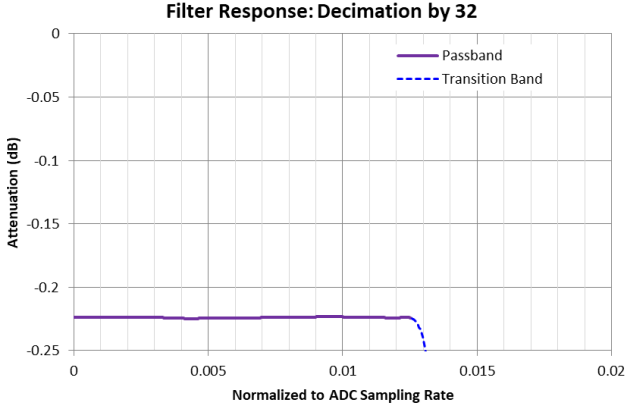








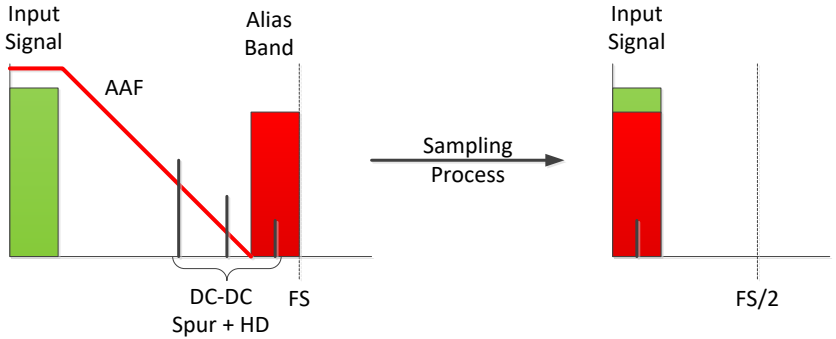


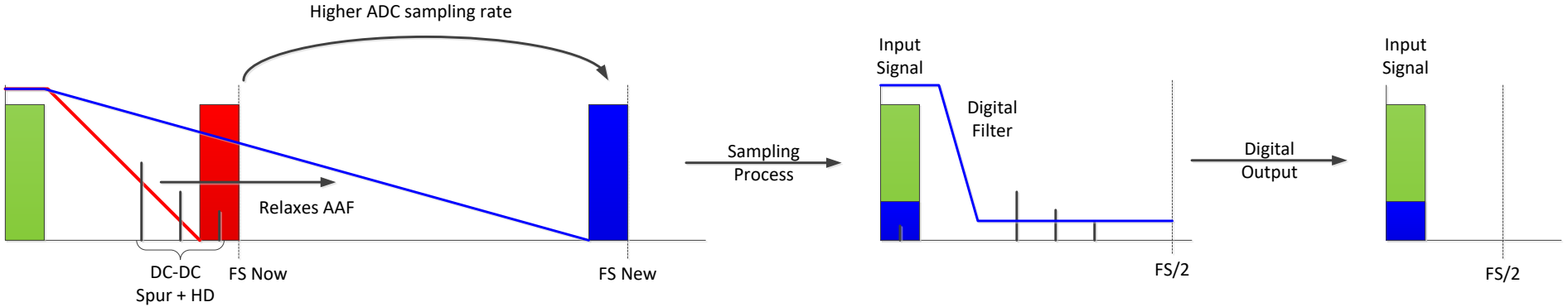


Faster SAR ADC Sampling Rate

Faster ADC sampling rate:

- Relaxes AAF filter requirements
- Reduces susceptibility to power supply spurs/noise inside ADC



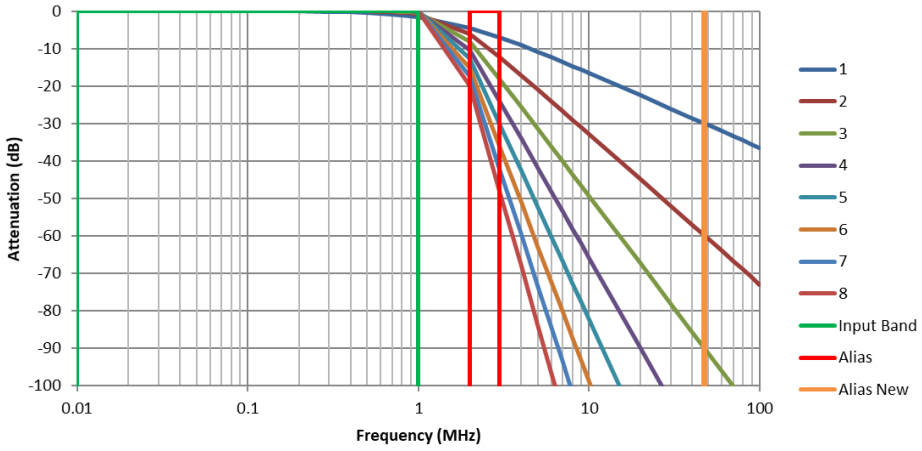


Oversample + Decimate Configuration

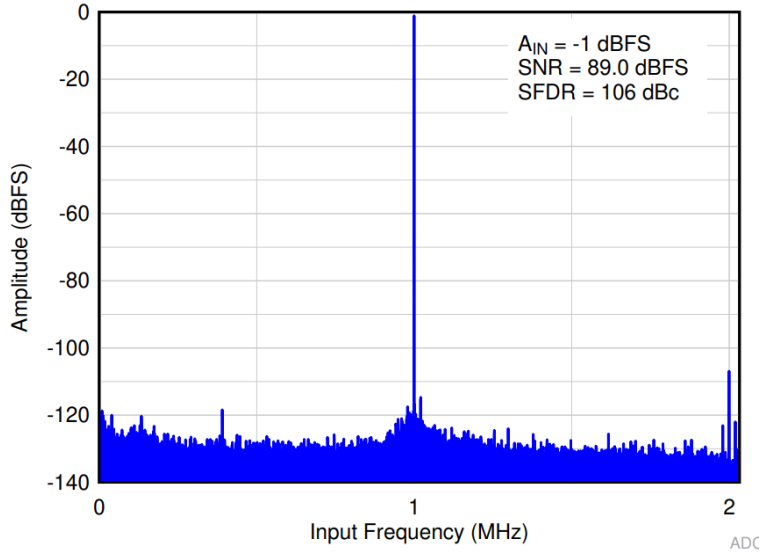
Operate ADC at a faster clock rate and use internal digital decimation

- Relaxes external anti alias filter
- Improves SNR (3dB/2x decimation)
- Reduces output data rate

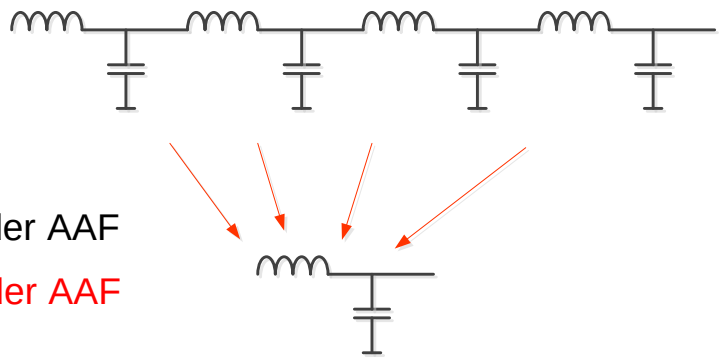
$F_{S,old}$ = 3 MSPS: Alias at 2-3MHz => heavy filter
$F_{S,new}$ = 24 or 48 MSPS: Alias at 23/47MHz => relaxed filter



FS = 65 MSPS, FIN = 1.0 MHz, 16x Decimation



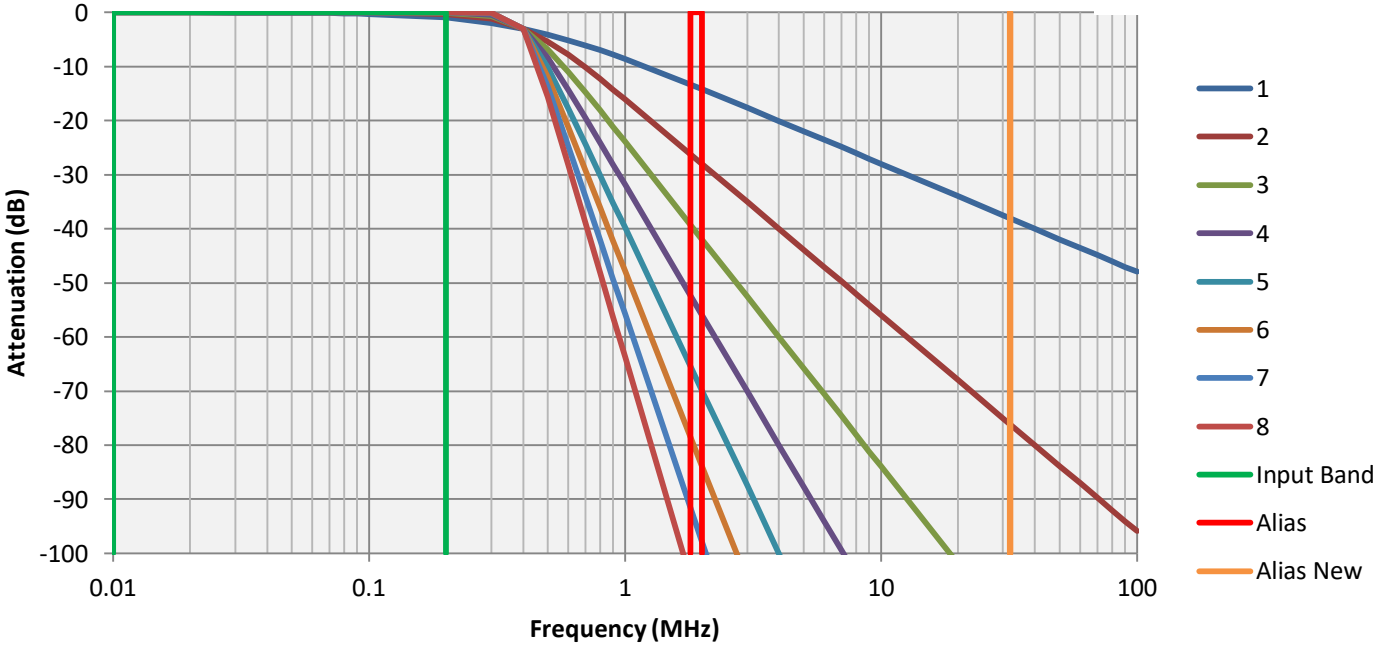
AAF Filter relaxation



Fin = 0-200kHz

Fs = 2Msps => Alias = 1.8-2MHz => requires 8th order AAF

Fs_{New} = 32Msps => Alias = 31.8-32MHz => requires 3rd order AAF



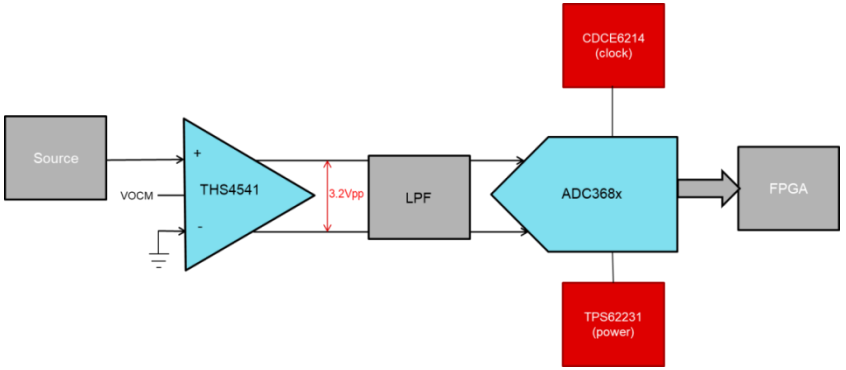
Evaluation tools (EVMs)

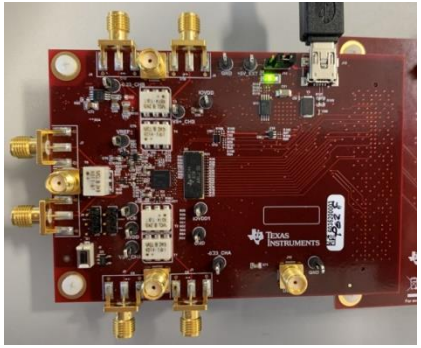
ADC3683EVM - Industries Fastest 18-bit Digitizer – Dual 18 bit 65MSPS

Exceptional SNR & SFDR at Ultra Low Power Consumption

Features

• **Sample range:**	**0.5 – 65 MSPS (18 bit)**
• Input driver options:	AC coupled through ADT1-6T+ (125MHz BW)
	Supports SE to DIFF or DIFF to DIFF conversion
	DC coupled through THS4541 (20 MHz BW)
	Supports SE to DIFF or DIFF to DIFF conversion
	0V to 3.2V p-p input range
• **ADC Voltage Reference options:**	**Internal 1.2/1.6V (lowest cost)**
	External 1.2/1.6V (highest performance)
• Time doman applications	DC coupled FDA input (0Hz to 20MHz)
• Freq domain applications	AC coupled transformer input (30kHz to 125MHz)
• **Clocking options**	**On board clock (350fs jitter typical)**
	Option to connect external clock (<350fs clock jitter)
• Low Power consumption:	95mW/ch (ADC)
	800mW (Complete Digitizer)
• **Low Latency for control loop applications:**	**2 clock cycles (30.77ns at 65MSPS)**
• Signal Chain SNR @ 1MHz fin	85 dB (Nyquist) – transformer/FDA input
Includes input driver, onboard clock & INT voltage reference	9x dB (32x decimation) – transformer/FDA
• **Signal Chain SFDR @ 1MHz fin**	**95 dB (transformer/FDA)**
Includes input driver, onboard clock & INT voltage reference	**10x dB (32x decimation) – transformer)/FDA**
• ADC INL, DNL	7 LSB, 0.7 LSB (typ)
• **Digital Interface:**	**SLVDS (ADC)**
	FMC connector (Digitizer)
• Power supply ADC/Board:	1.8V/5V
• **Operating Temperature:**	**-40 to +105degC**
• Design files:	Schematics & gerber files available on ti.com





Target Applications
Data Acquisition
Power Analyzer
Sonar
Radar
Optical Encoders
Control Loops
Imaging (MRI, Xray, PET)
Flow Metering (Ultrasonic)

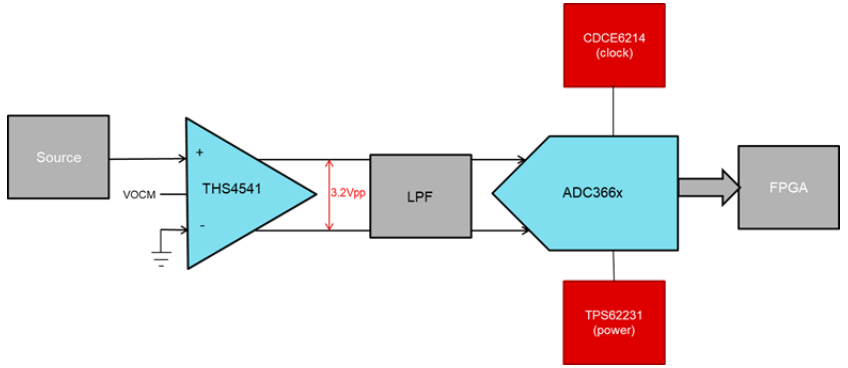
Texas Instruments

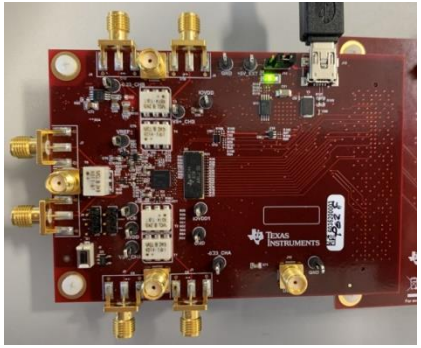
High dynamic range, low power, 16-bit Dual channel 65MSPS Digitizer

>90db SNR, 108dB SFDR @ 95mW/Ch (ADC3660/61/62/63EVM)

Features

• **Sample range:**	**0.5 – 65 MSPS (16 bit)**
• Input driver options:	AC coupled through ADT1-6T+ (125MHz BW)
	Supports SE to DIFF or DIFF to DIFF conversion
	DC coupled through THS4541 (20 MHz BW)
	Supports SE to DIFF or DIFF to DIFF conversion
	0V to 3.2V p-p input range
• **ADC Voltage Reference options:**	**Internal 1.2/1.6V (lowest cost)**
	External 1.2/1.6V (highest performance)
• Time doman applications	DC coupled FDA input (0Hz to 20MHz)
• Freq domain applications	AC coupled transformer input (30kHz to 125MHz)
• **Clocking options**	**On board clock (350fs jitter typical)**
	Option to connect external clock (<350fs clock jitter)
• Low Power consumption:	95mW/ch (ADC)
	800mW (Complete Digitizer)
• **Low Latency for control loop applications:**	**2 clock cycles (32ns at 62.5MSPS)**
• Signal Chain SNR @ 1MHz fin	82 dB (Nyquist) – transformer/FDA input
Includes input driver, onboard clock & INT voltage reference	90.7 dB (32x decimation) – transformer/FDA
• **Signal Chain SFDR @ 1MHz fin**	**90 dB (transformer/FDA)**
Includes input driver, onboard clock & INT voltage reference	**108 dB (32x decimation) – transformer)/FDA**
• ADC INL, DNL	2 LSB, 0.2 LSB (typ)
• **Digital Interface:**	**CMOS, SLVDS (ADC)**
	FMC connector (Digitizer)
• Power supply ADC/Board:	1.8V/5V
• **Operating Temperature:**	**-40 to +105degC**
• Design files:	Schematics & gerber files available on ti.com





Target Applications
Data Acquisition
Power Analyzer
Sonar
Radar
Optical Encoders
Control Loops
Imaging (Xray, Thermal, MRI)
Flow Metering (Ultrasonic)

Texas Instruments

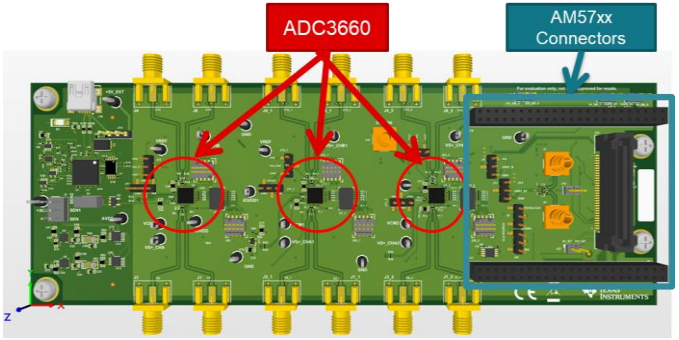
High dynamic range, 16-bit 6 - CH Digitizer interfaces to TI Sitara Processor

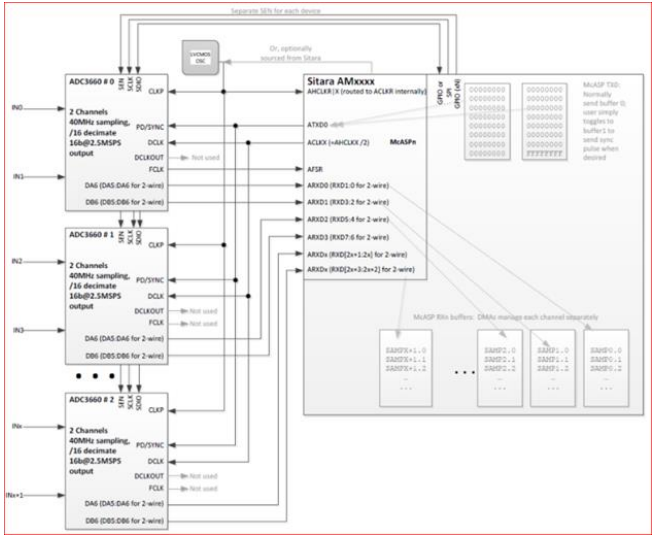
Exceptional SNR & SFDR @ 71mW/Ch (ADC3660)

Features

- ADC3660 paired with the AM57xx (Beagle Bone AI) utilizing McASP interface.
- Can support 3 synchronized ADC3660s with max data rate of 50 Mbps.
- Expected release in Q1 2021.

Sample range:	0.5 – 10 MSPS (16 bit) Max data rate of 50Mbps
Input driver options:	DC coupled through THS4541 (20 MHz BW) Supports SE to DIFF or DIFF to DIFF conversion 0V to 3.2V p-p input range
ADC Voltage Reference options:	Internal 1.2/1.6V (lowest cost) External 1.2/1.6V (highest performance)
Time doman applications	DC coupled FDA input (0Hz to 20MHz)
Clocking options	On board clock (350fs jitter typical) Option to connect external clock (<350fs clock jitter)
Low Power consumption:	71mW/ch (ADC) 800mW (Complete Digitizer)
Low Latency:	2 clock cycles
Signal Chain SNR @ 1MHz fin Includes input driver, onboard clock & INT voltage reference	82 dB (Nyquist) – transformer/FDA input X? dB (32x decimation) – transformer/FDA
Signal Chain SFDR @ 1MHz fin Includes input driver, onboard clock & INT voltage reference	90 dB X? dB (32x decimation)
ADC INL, DNL	2 LSB, 0.2 LSB (typ)
Digital Interface:	CMOS (ADC) connector (Digitizer)
Power supply ADC/Board:	1.8V/5V
Operating Temperature:	-40 to +105degC
Design files:	Schematics & gerber files available (Q1 2021) on ti.com



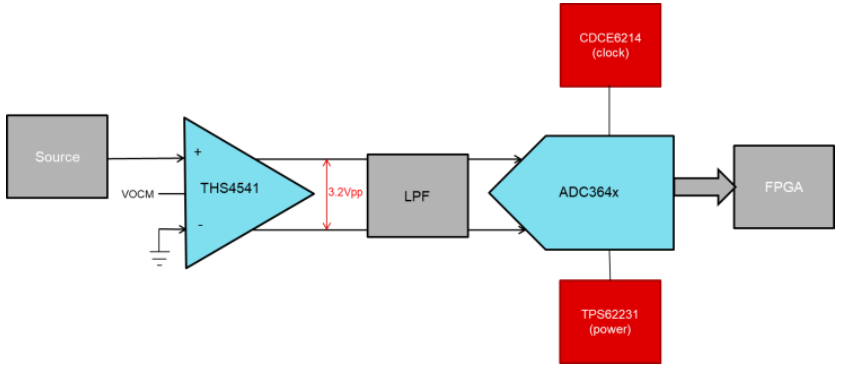


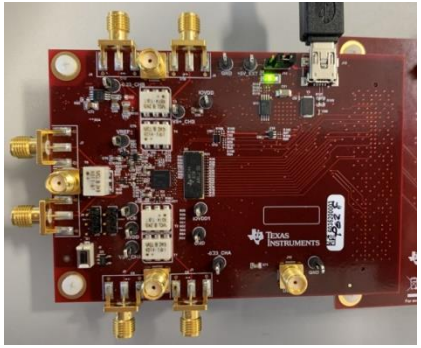
14-bit Digitizer with industry leading INL, DNL and SNR

Dual channel 14-bit 0.5 to 125MSPS (ADC3641/2/3/4EVM)

Features

• **Sample range:**	**0.5 – 125 MSPS (14 bit)**
• Input driver options:	AC coupled through ADT1-6T+ (125MHz BW)
	Supports SE to DIFF or DIFF to DIFF conversion
	DC coupled through THS4541 (20 MHz BW)
	Supports SE to DIFF or DIFF to DIFF conversion
	0V to 2.25V p-p input range
• **ADC Voltage Reference options:**	**Internal 1.2/1.6V (lowest cost)**
	External 1.2/1.6V (highest performance)
• Time doman applications	DC coupled FDA input (0Hz to 20MHz)
• Freq domain applications	AC coupled transformer input (30kHz to 125MHz)
• **Clocking options**	**On board clock (350fs jitter typical)**
	Option to connect external clock (<350fs clock jitter)
• Low Power consumption:	80mW/Ch (ADC @ 125MSPS)
	800mW (Complete Digitizer)
• **Low Latency for control loop applications:**	**1 clock cycle (8ns at 125MSPS)**
• Signal Chain SNR @ 1MHz fin	79 dB (Nyquist) – transformer/FDA input
Includes input driver, onboard clock & INT voltage reference	9x? dB (32x decimation) – transformer/FDA
• **Signal Chain SFDR @ 1MHz fin**	**93 dB (transformer/FDA)**
Includes input driver, onboard clock & INT voltage reference	**10x? dB (32x decimation) – transformer)/FDA**
• ADC INL, DNL	0.6 LSB, 0.2 LSB (typ @ 65MSPS)
• **Digital Interface:**	**CMOS (ADC)**
	FMC connector (Digitizer)
• Power supply ADC/Board:	1.8V/5V
• **Operating Temperature:**	**-40 to +105degC**
• Design files:	Schematics & gerber files available on ti.com



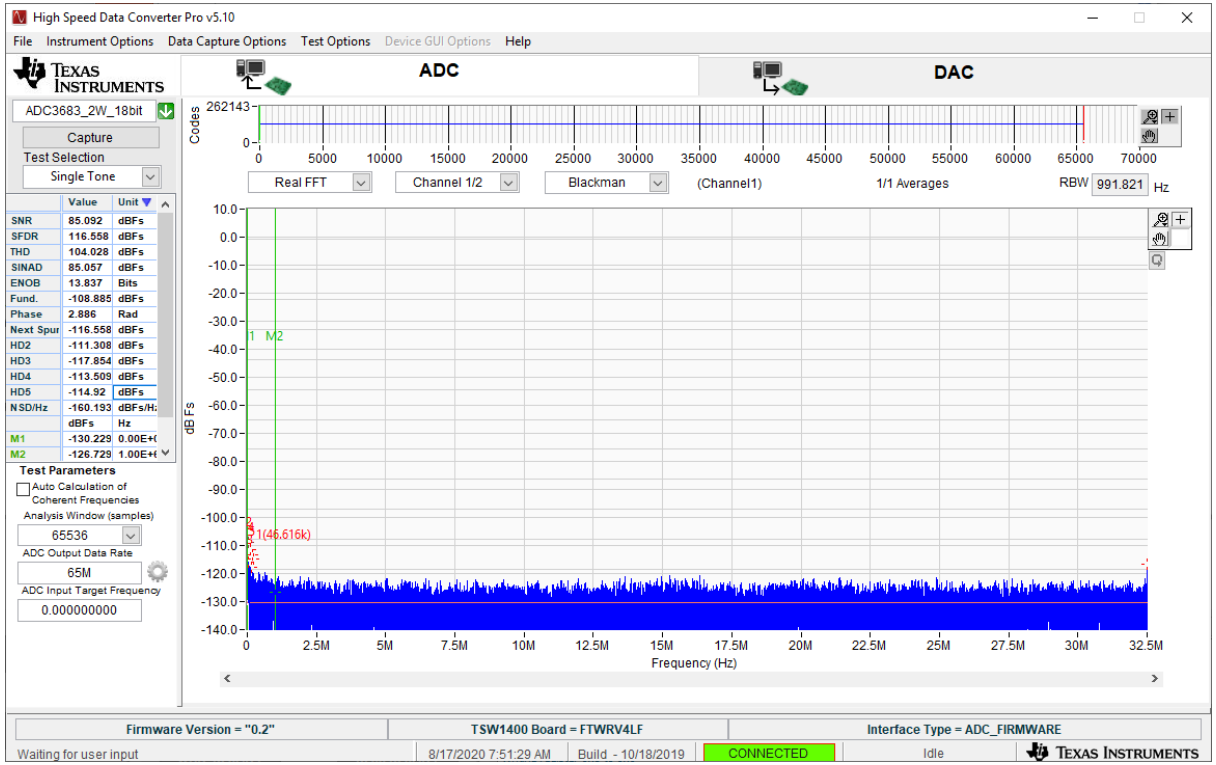


Target Applications
Thermal Imaging
Data Acquisition
Flow Metering (Ultrasonic)
Control Loops
Imaging (MRI, Xray, PET)
Sonar
Radar
Communications

EVM measurements

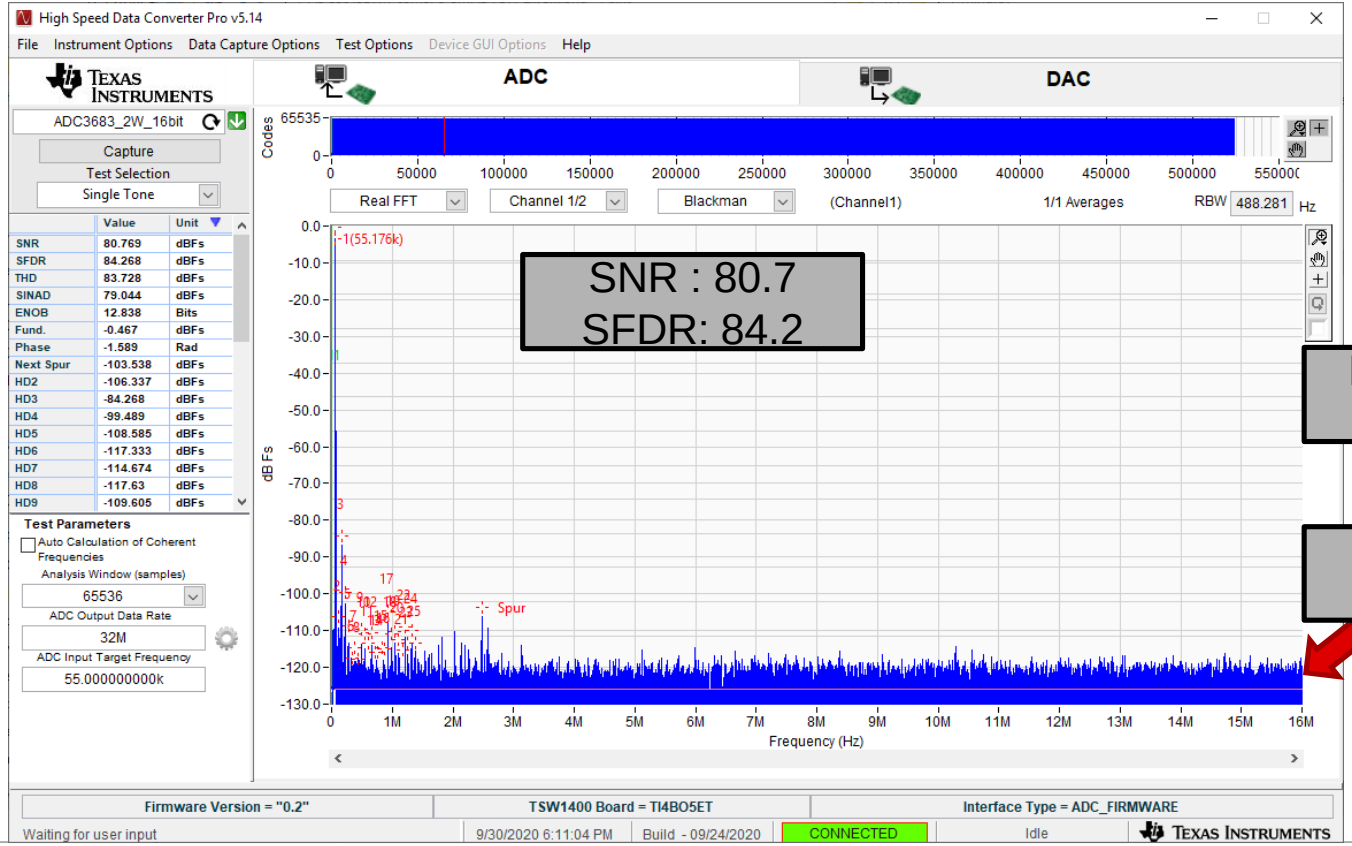
ADC3583

- 18-bit noise floor of -160dBFS

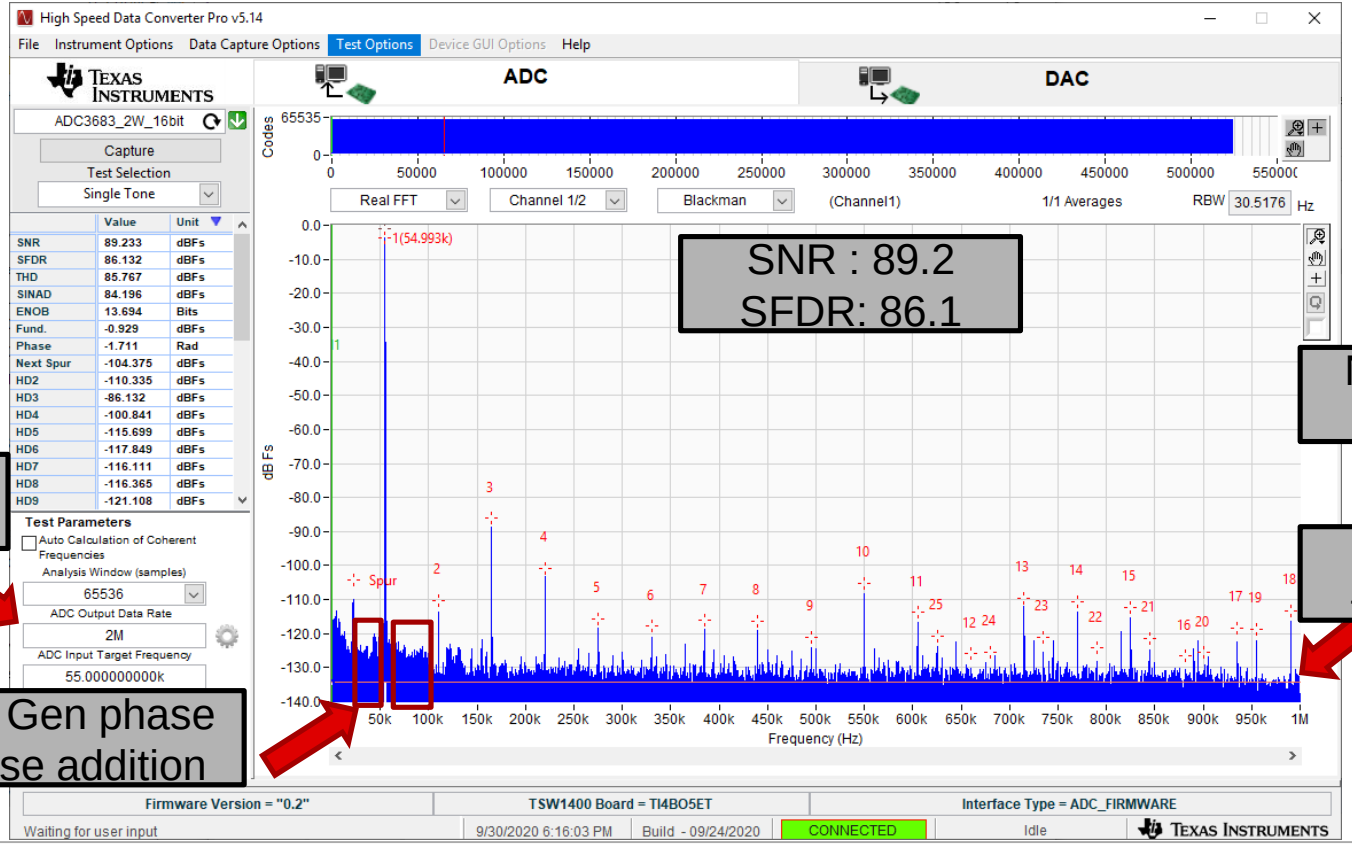


SNR: 85 dBFS
SFDR: 116 dBFS
NSD better than 160dbFS/Hz!

ADC3683EVM 32 MSPS: Bypass, 55KHz Fin



ADC3683EVM 32 MSPS: Decimation by 16, 55KHz Fin



Lower data rate

Sig Gen phase noise addition

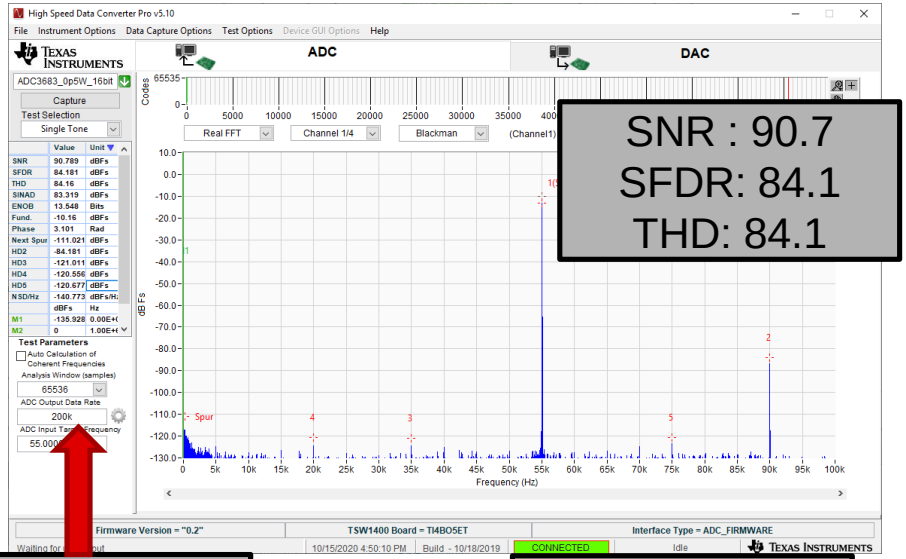
Nyquist Zone 1 MHz

Noise Floor ~ -130 dBFS

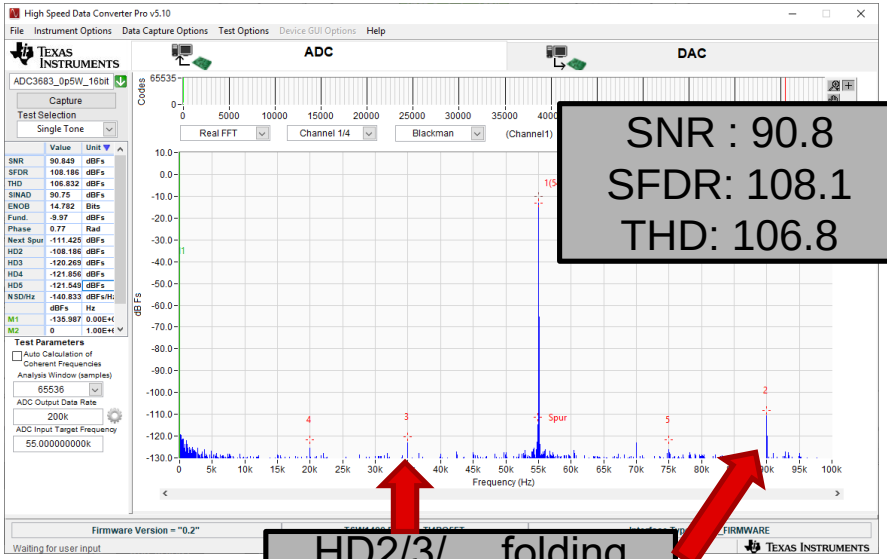
ADC3683EVM 6.4 MSPS, 32x Decimation, 55KHz Fin

No Filter

100 kHz LPF



SNR : 90.7
SFDR: 84.1
THD: 84.1



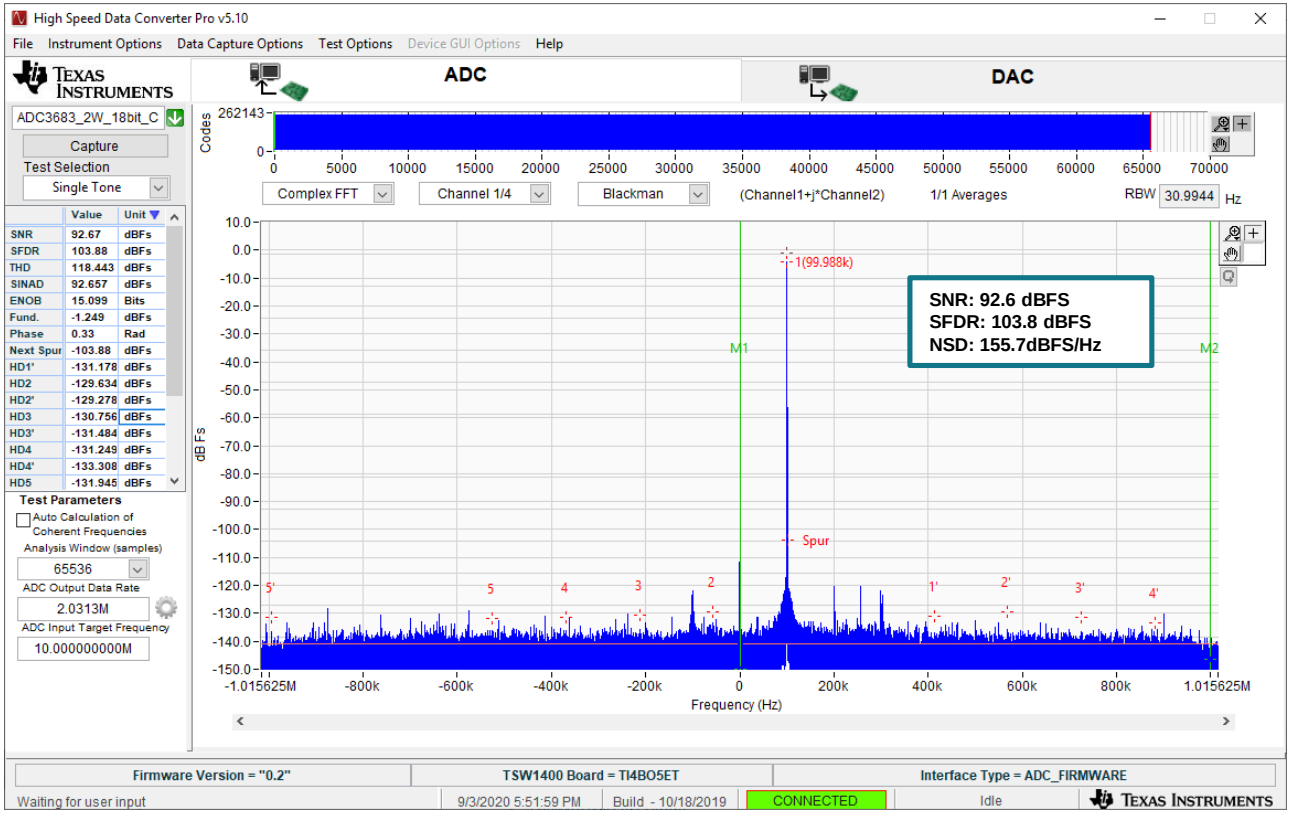
SNR : 90.8
SFDR: 108.1
THD: 106.8

Much lower data rate

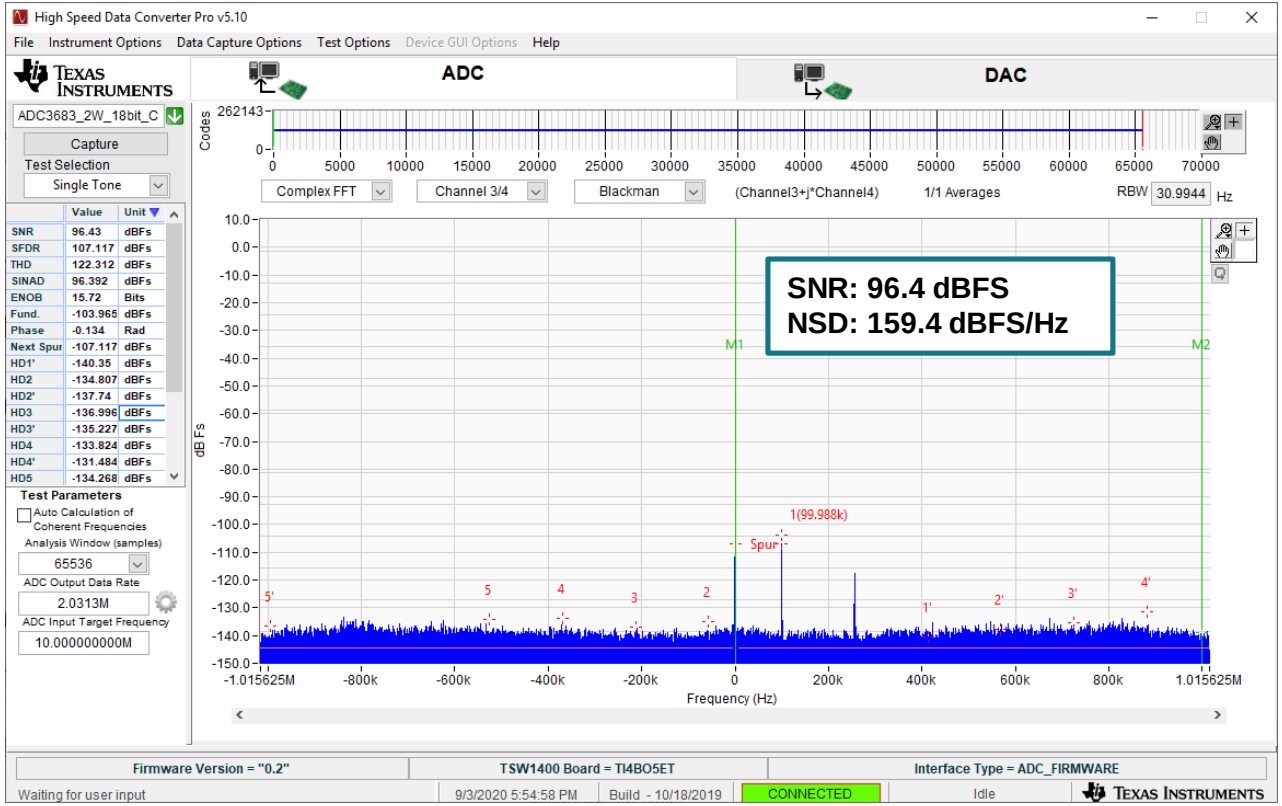
Nyquist Zone 100 kHz

HD2/3/… folding back into Nyquist Zone

ADC3683EVM – 18bit, 65MSPS, 32x Decimation, 10 MHz, Ain = -1.25dBFS



ADC3683EVM – 18bit, 65MSPS, 32x, Idle Channel



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