AM62D EVM

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BOARD REVISION	E2
SCHEMATIC VERSION	0.1

Note:
Verify the DNI components configuration with respect to the EVM schematics (Use PDF) after completion of design before board assembly

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REVISION HISTORY

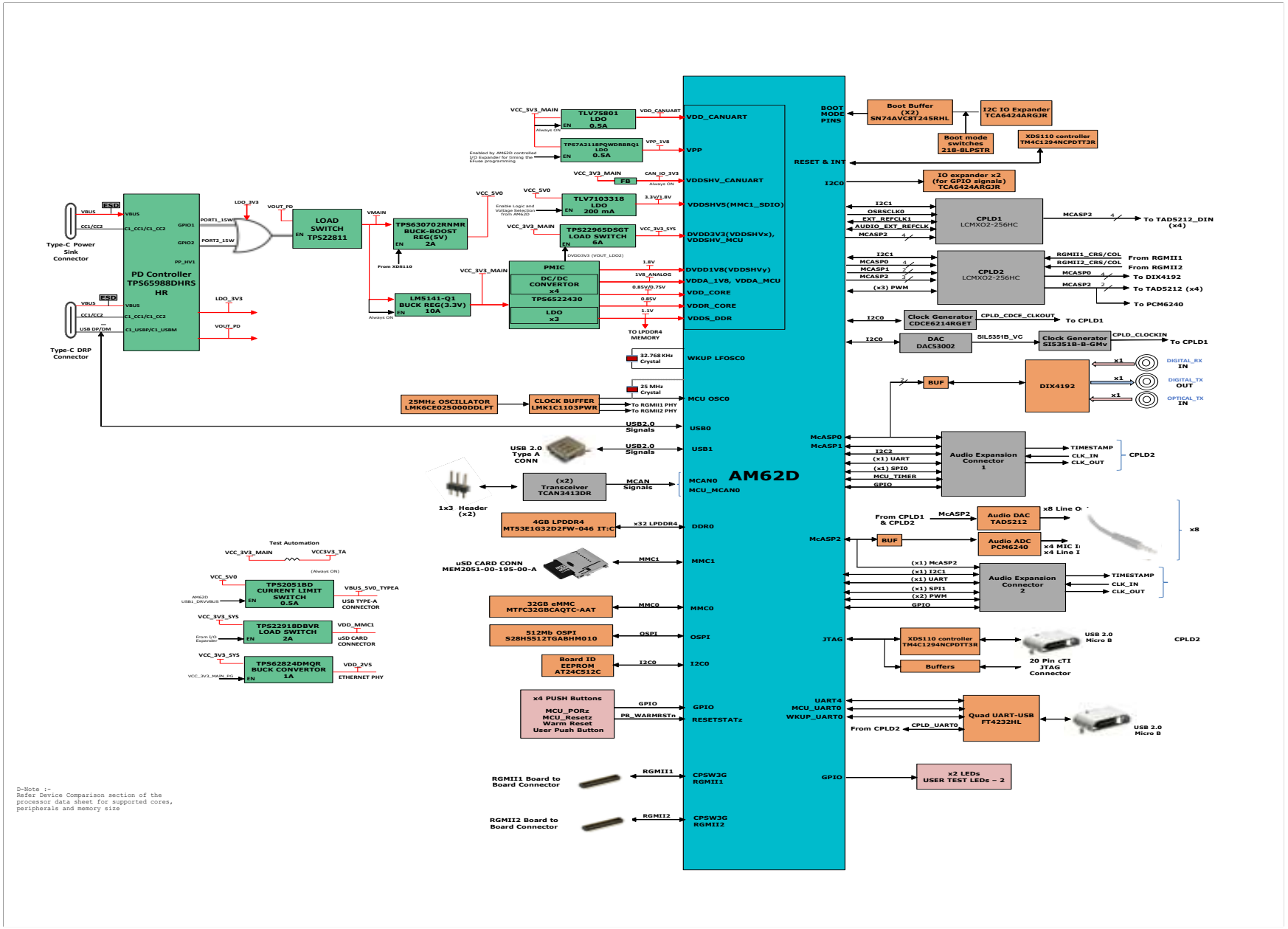
	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	0.1	14 NOV 2023	Initial Draft	Mistral Design Team		
	0.2	21 NOV 2023	Migrated to Burton PMIC and updated PDN as per AM62D EVM requirement	Mistral Design Team	Nishant	
	0.3	27 NOV 2023	Implemented Audio section as per AM62D EVM requirements	Mistral Design Team	Nishant	
	0.4	14 DEC 2023	Internally reviewed and shared with TI for review	Mistral Design Team	Nishant	Ajit MB
	0.5	27 DEC 2023	1. Implemented Audio Expansions & CPLD 2. Replaced Audio Lineout devices with TAD5212	Mistral Design Team		
	0.6	29 DEC 2023	Implemented review comments from TI	Mistral Design Team	Nishant	Ajit MB
	0.7	07 FEB 2024	Updated AEC, McASP Muxing, CPLD, Current Monitoring Sections	Mistral Design Team		
	0.8	21 FEB 2024	Updated Ethernet Expansion, FET Bus Switch & Voltage level translators	Mistral Design Team		
	0.9	03 MAR 2024	Updated Switch for fet selection and implemented TI comments	Mistral Design Team		
	0.10	22 MAR 2024	Updated Audio section,CPLD1 and CPLD2 connections removed FET switches as per TI comments.	Mistral Design Team		
	0.11	28 MAR 2024	Implemented review comments from TI	Mistral Design Team		
	0.12	04 APRIL 2024	Implemented review comments from TI	Mistral Design Team		
	0.13	17 APRIL 2024	Implemented modular approach	Mistral Design Team		
	1.0	10 MAY 2024	Baselined	Mistral Design Team		
E2	0.1	06 SEP 2024	1. ECR/ECN Implemented from E1 Revision 2. Removed RGMII1_INH and RGMII2_INH connection to "PMIC_EN" section 3. TXS0104EPWR(U32) IC replaced with TXB0104PWR 4. Implemented SYNC1_OUT resistor option as per the TI comments 5. Implemented PORT1 and PORT 2_15W_EN Status indication LED logic 6. Connected CPLD JTAG pins to GPIO expander 7. Changed 0.1uF decoupling caps on PMIC output to 0603 package 8. Changed package size for ADC input caps 9. DAC MCP47CVB02 U22 is changed to DAC53002 as per TI comments 10. Bootmode signals net names is been changed and default function of Bootmode is implemented as per the TI comments. 11. LCMXO2-256HC-4SG48I (U84 &U85) IC replaced with LCMXO2-640HC-4SG48I	Shrinivas	Pandiya Rajan	Ajit MB
	1.0	20 SEP 2024	Baselined	Shrinivas	Pandiya Rajan	Ajit MB

LINK TO DESIGN COLLATERALS

https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am62x-am62ax-custom-board-hardware-design---collaterals-for-reference-during-schematic-design-and-schematics-review

FAQs

BLOCK DIAGRAM AM62D EVM



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Title	BLOCK DIAGRAM AM62D_ SKEVM	
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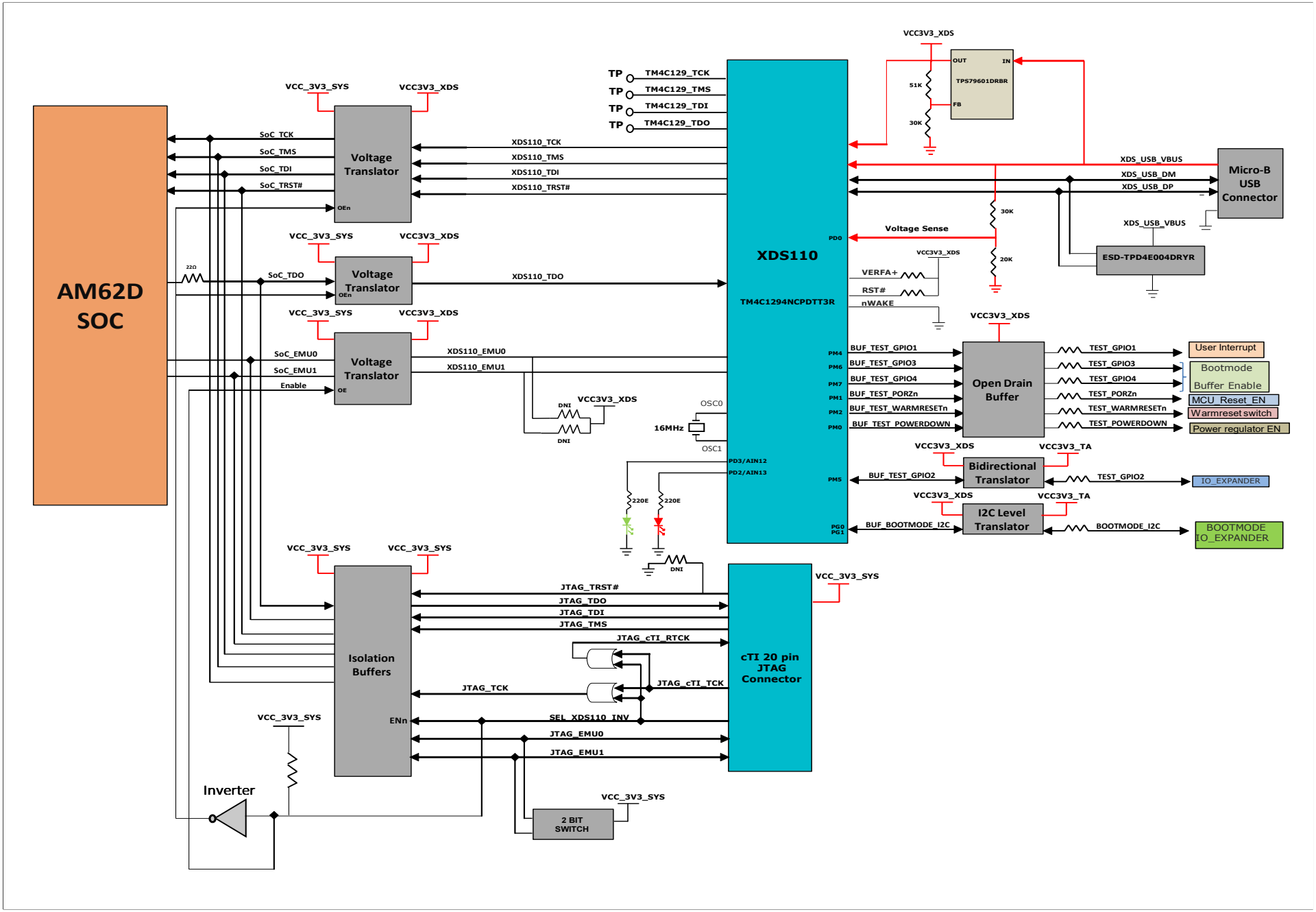
BLOCK DIAGRAM_XDS110



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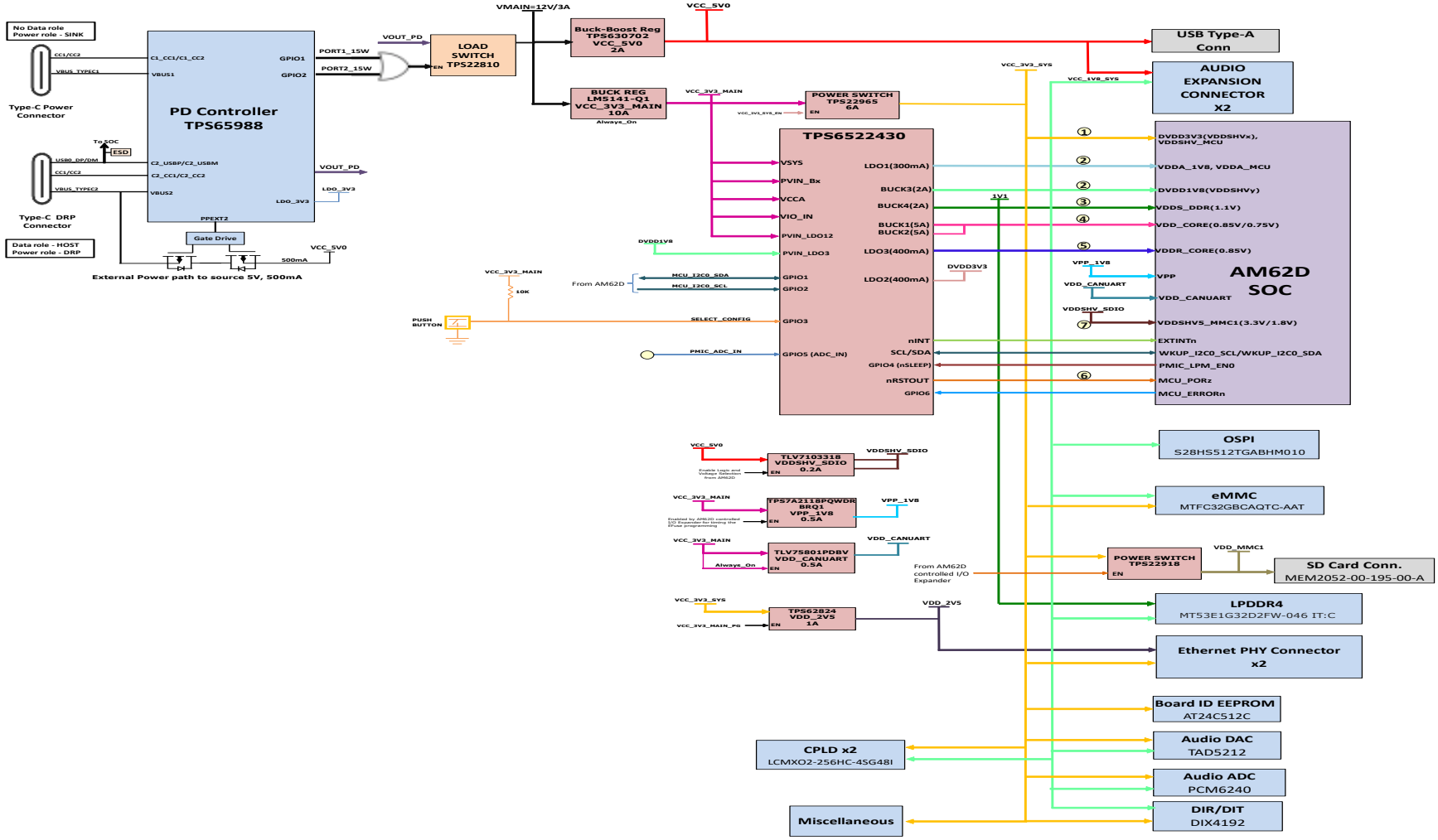
POWER ARCHITECTURE BLOCK DIAGRAM



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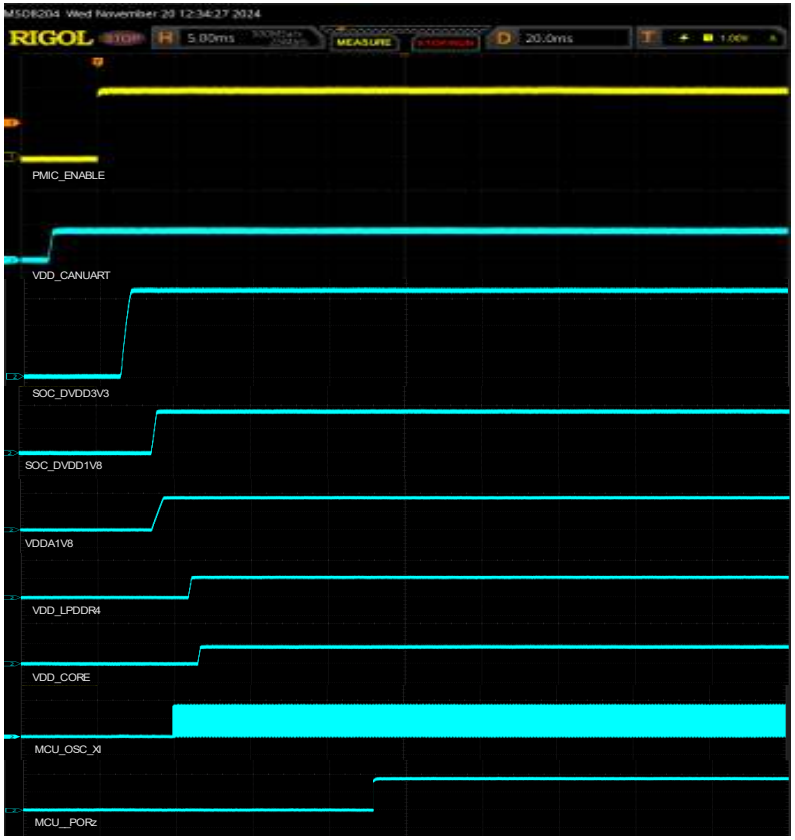
POWER UP SEQUENCE



POWER DOWN SEQUENCE

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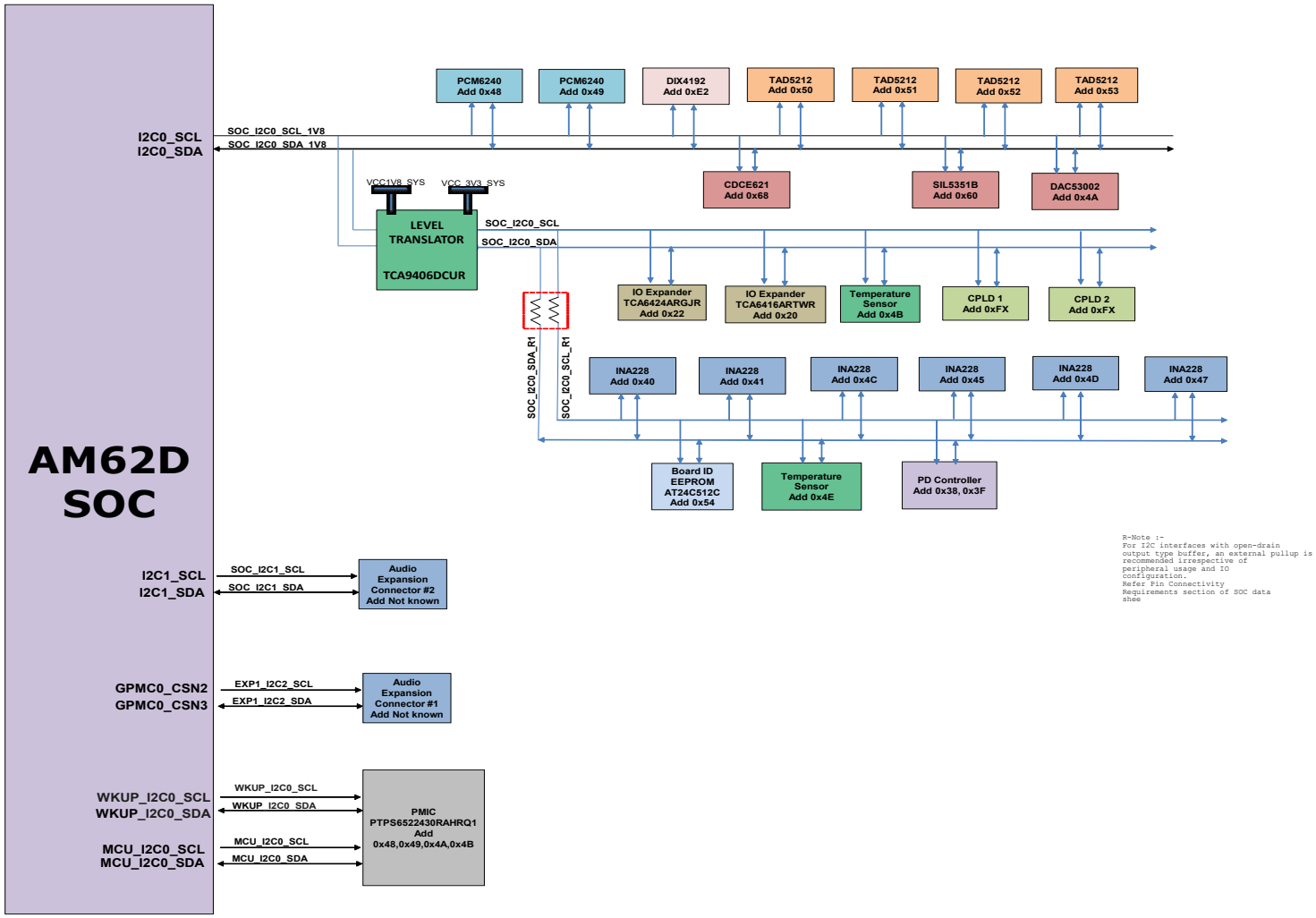
I2C TREE



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GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE RAIL CONNECTED ON SKEVM
1	Audio Expansion Connector 1	EXP1_GPIO0_1	GPIO	GPIO0_1	OSPI0_LBCLKO	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
2	OSPI Interrupt	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSN1	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
3	Audio Expansion Connector 1	EXP1_GPIO0_13	GPIO	GPIO0_13	OSPI0_CSN2	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
4	Audio Expansion Connector 1	EXP1_GPIO0_14	GPIO	GPIO0_14	OSPI0_CSN3	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
5	Audio Expansion Connector 1	EXP1_GPIO0_31	GPIO	GPIO0_31	GPMC0_CLK	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
6	Audio Expansion Connector 1	EXP1_GPIO0_32	GPIO	GPIO0_32	GPMC0_ADVN_ALE	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
7	Mcasp Header	SoC_GPIO0_33	GPIO	GPIO0_33	GPMC0_OEN_REN	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
8	Audio Expansion Connector 1									
9	Mcasp Header	SoC_GPIO0_34	GPIO	GPIO0_34	GPMC0_WEN	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
10	Audio Expansion Connector 1									
11	Audio Expansion Connector 1	EXP1_GPIO0_35	GPIO	GPIO0_35	GPMC0_BE0N_CLE	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
12	Audio Expansion Connector 1	EXP1_GPIO0_37	GPIO	GPIO0_37	GPMC0_WAIT0	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
13	Audio Expansion Connector 2	EXP1_GPIO0_45	GPIO	GPIO0_45	VOUT0_DATA0	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
14	Audio Expansion Connector 2	EXP1_GPIO0_46	GPIO	GPIO0_46	VOUT0_DATA1	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
15	Audio Expansion Connector 2	EXP1_GPIO0_47	GPIO	GPIO0_47	VOUT0_DATA2	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
16	Audio Expansion Connector 2	EXP1_GPIO0_48	GPIO	GPIO0_48	VOUT0_DATA3	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
17	Audio Expansion Connector 2	EXP1_GPIO0_55	GPIO	GPIO0_55	VOUT0_DATA10	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
18	Audio Expansion Connector 2	EXP1_GPIO0_56	GPIO	GPIO0_56	VOUT0_DATA11	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
19	Audio Expansion Connector 2	EXP1_GPIO0_57	GPIO	GPIO0_57	VOUT0_DATA12	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
20	Audio Expansion Connector 2	EXP1_GPIO0_58	GPIO	GPIO0_58	VOUT0_DATA13	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
21	User test LED control signal	SOC_GPIO1_49	ENABLE	GPIO0_49	MMC1_SDWP	INPUT	LOW	HIGH	VDDSHV5	SoC_DVDD1V8
22	SD Card I/O Voltage Selection	VSEL_SD_SOC	SELECTION	GPIO0_59	VOUT0_DATA14	OUTPUT	NA	NA	VDDSHV2	SoC_DVDD3V3
23	Low power mode enable	PMIC_LPM_EN0	ENABLE	MCU_GPIO0_22	PMIC_LPM_EN0	OUTPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
24	PMIC Interrupt	PMIC_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
25	MCU Interrupt	MCU_INTn	INTERRUPT	MCU_GPIO0_23	WKUP_CLKOUT0	INPUT	HIGH	LOW	WKUP_MCU	SoC_DVDD3V3
				IO EXPANDER – 01						
1	GPIO_CPSW2_RST	RGMII2_RST	ENABLE	IO EXPANDER-P00		OUTPUT	HIGH	LOW		VCC_3V3_SYS
2	GPIO_CPSW1_RST	RGMII1_RST	ENABLE	IO EXPANDER-P01		OUTPUT	HIGH	LOW		VCC_3V3_SYS
3	PCM/EXP2_SEL	PCM/EXP2_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P02		OUTPUT	HIGH	-		VCC_3V3_SYS
4	MMC1_SD_EN	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
5	VPP_EN	VPP_EN	ENABLE	IO EXPANDER-P04		OUTPUT	NA	HIGH		VCC_3V3_SYS
6	GPIO_DIX_RST	DIX4192_RST	ENABLE	IO EXPANDER-P05		OUTPUT	HIGH	LOW		VCC_3V3_SYS
7	IO_EXP_OPT_EN	OPT_BUF_EN	ENABLE	IO EXPANDER-P06		OUTPUT	HIGH	LOW		VCC_3V3_SYS
8	DIX_INT	DIX4192_INT	INTERRUPT	IO EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS
9	GPIO_eMMC_RSTn	eMMC_RST	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	LOW		VCC_3V3_SYS
10	CPLD2_DONE	CPLD2_DONE	ENABLE	IO EXPANDER-P11		INPUT	HIGH	LOW		VCC_3V3_SYS
11	CPLD2_INTN	CPLD2_INT	INTERRUPT	IO EXPANDER-P12		INPUT	HIGH	LOW		VCC_3V3_SYS
12	CPLD1_DONE	CPLD1_DONE	ENABLE	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
13	CPLD1_INTN	CPLD1_INT	INTERRUPT	IO EXPANDER-P14		INPUT	HIGH	LOW		VCC_3V3_SYS
14	USB Type A overcurrent indicator	USB_TYPEA_OC_INDICATION	INTERRUPT	IO EXPANDER-P14		INPUT	HIGH	LOW		VCC_3V3_SYS
15	PCM1_INT	PCM6240_INT	INTERRUPT	IO EXPANDER-P16		INPUT	NA	NA		VCC_3V3_SYS
16	PCM2_INT	PCM6240_INT	INTERRUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
17	GPIO_PCM1_RST	HDMI_INTn	INTERRUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC_3V3_SYS
19	GPIO_PCM2_RST	PCM6240_RST	ENABLE	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC_3V3_SYS
20	CPLD/EXP2_SEL	CPLD/EXP2_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P23		OUTPUT	HIGH	-		VCC_3V3_SYS
21	IO_MCAN0_STB	MCAN_STB	ENABLE	IO EXPANDER-P24		OUTPUT	HIGH	LOW		VCC_3V3_SYS
22	IO_MCAN1_STB	MCAN_STB	ENABLE	IO EXPANDER-P25		OUTPUT	HIGH	LOW		VCC_3V3_SYS
23	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	ENABLE	IO EXPANDER-P26		OUTPUT	HIGH	LOW		VCC_3V3_SYS
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
				IO EXPANDER – 02						
1	PCM6240_BUFFER_ENABLE	PCM6240_BUF_IO_EN	ENABLE	IO EXPANDER-P00		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
2	CPLD1_JTAG_ENABLE	CPLD1_JTAGENB	ENABLE	IO EXPANDER-P02		OUTPUT	LOW	HIGH		VCC_3V3_SYS
3	CPLD1_JTAG_PROGRAM_ENABLE	CPLD1_PROGRAMN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	LOW		VCC_3V3_SYS
4	CPLD2_JTAG_ENABLE	CPLD2_JTAGENB	ENABLE	IO EXPANDER-P04		OUTPUT	LOW	HIGH		VCC_3V3_SYS
5	CPLD2_PROGRAM_ENABLE	CPLD2_PROGRAMN	ENABLE	IO EXPANDER-P05		OUTPUT	HIGH	LOW		VCC_3V3_SYS
6	CPLD1_TCK	CPLD1_TCK	GPIO	IO EXPANDER-P10		OUTPUT	-	HIGH		VCC_3V3_SYS
7	CPLD1_TMS	CPLD1_TMS	GPIO	IO EXPANDER-P11		OUTPUT	-	HIGH		VCC_3V3_SYS
8	CPLD1_TDI	CPLD1_TDI	GPIO	IO EXPANDER-P12		OUTPUT	-	HIGH		VCC_3V3_SYS
9	CPLD1_TDO	CPLD1_TDO	GPIO	IO EXPANDER-P13		INPUT	-	HIGH		VCC_3V3_SYS
10	CPLD2_TCK	CPLD2_TCK	GPIO	IO EXPANDER-P14		OUTPUT	-	HIGH		VCC_3V3_SYS
11	CPLD2_TMS	CPLD2_TMS	GPIO	IO EXPANDER-P15		OUTPUT	-	HIGH		VCC_3V3_SYS
12	CPLD2_TDI	CPLD2_TDI	GPIO	IO EXPANDER-P16		OUTPUT	-	HIGH		VCC_3V3_SYS
13	CPLD2_TDO	CPLD2_TDO	GPIO	IO EXPANDER-P17		INPUT	-	HIGH		VCC_3V3_SYS

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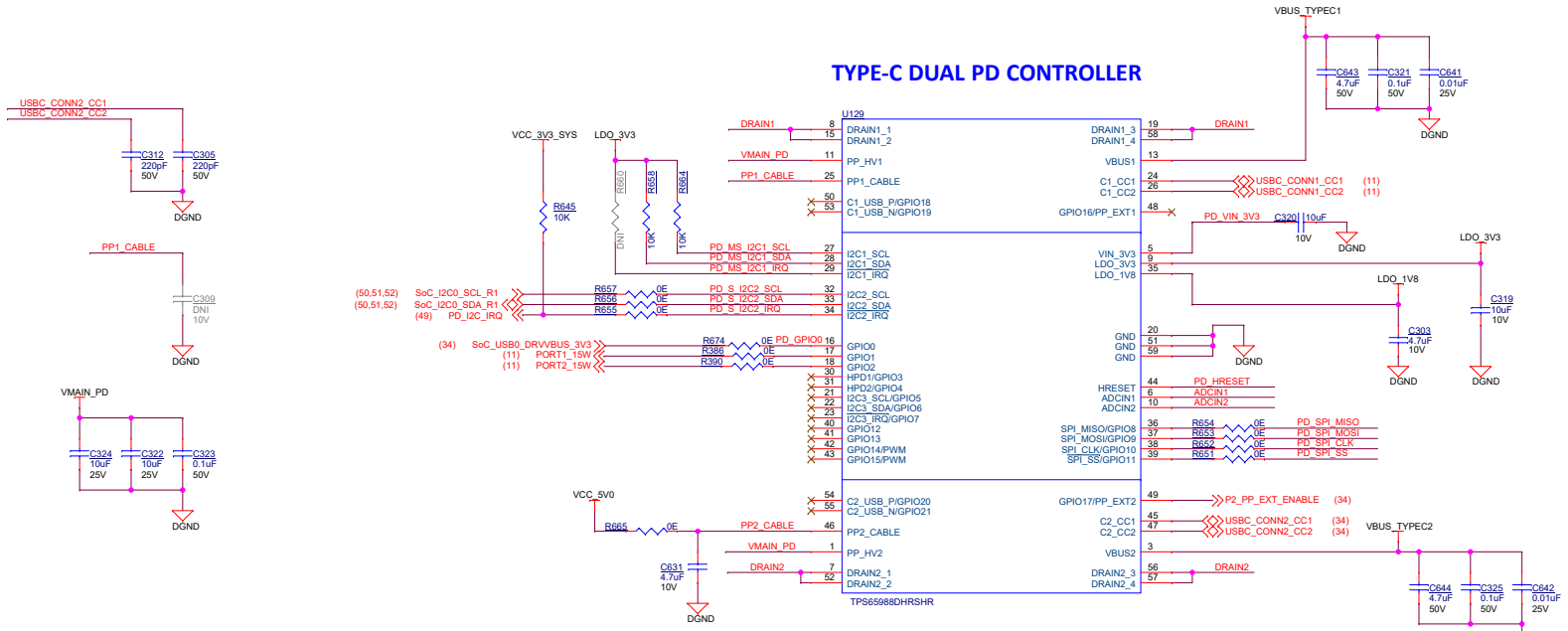
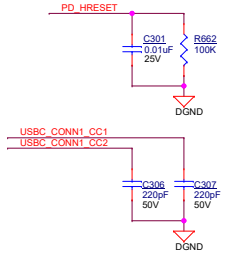
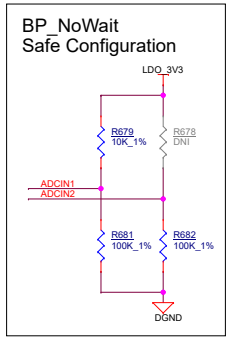
USB TYPE-C POWER

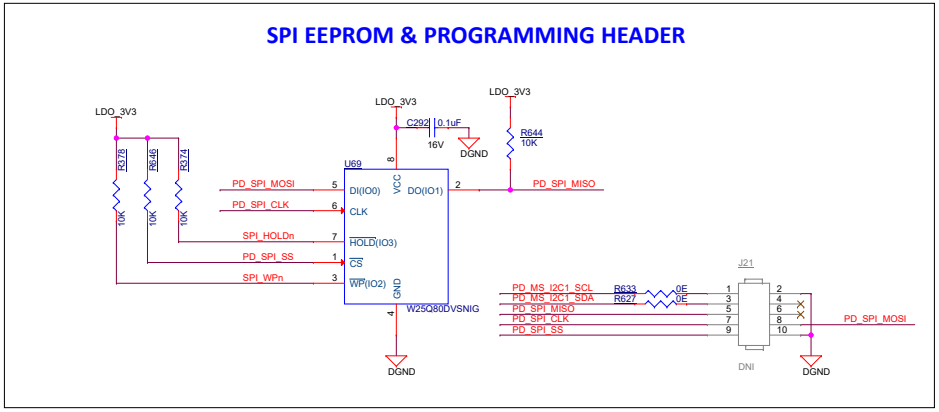






I2C Slave Address	Port1	Port2
I2C2(Default)	0x38	0x3F
I2C1	0x20	0x24

SPI EEPROM & PROGRAMMING HEADER



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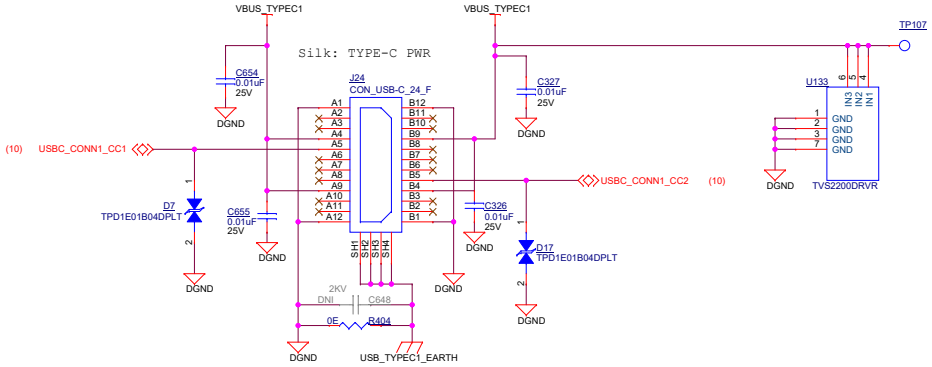
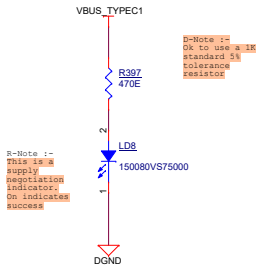
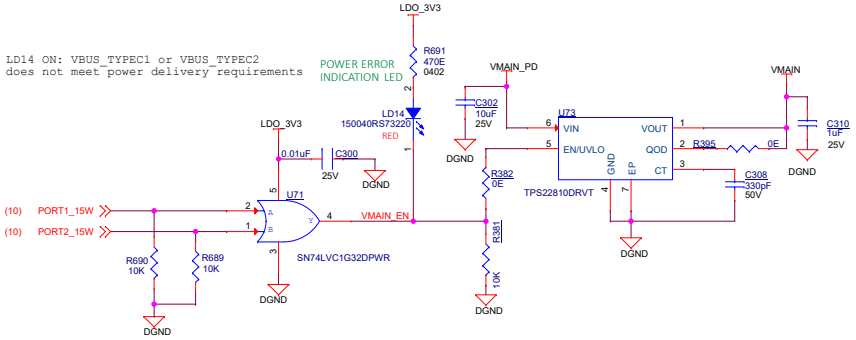
USB TYPE-C POWER CONNECTOR



POWER INDICATION LED: VBUS_TYPEC1



LOAD SWITCH FOR VMAIN



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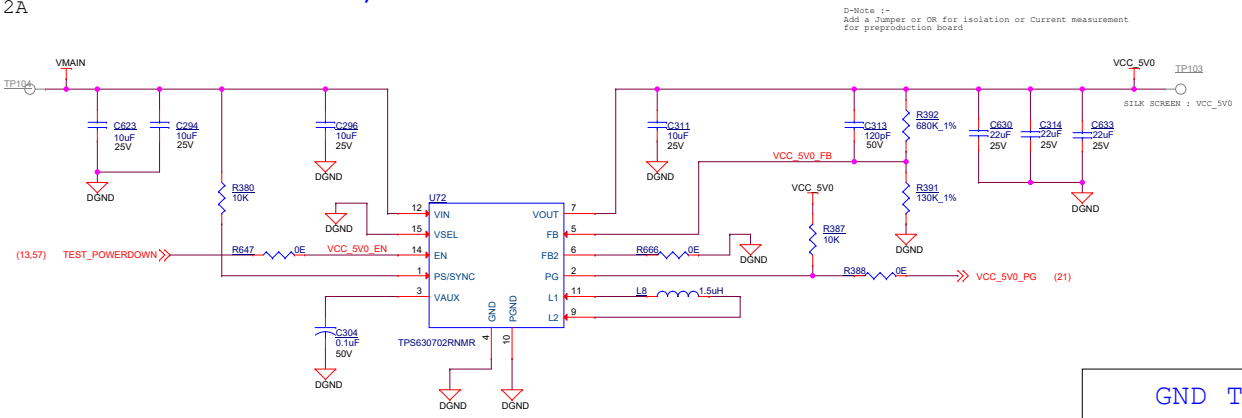
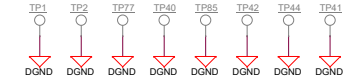
PERIPHERAL POWER SUPPLY - 1

VinMin = 4.5V
VinMax = 15V
Vout = 5V @ 2A

5V, 2.0 AMPS SUPPLY



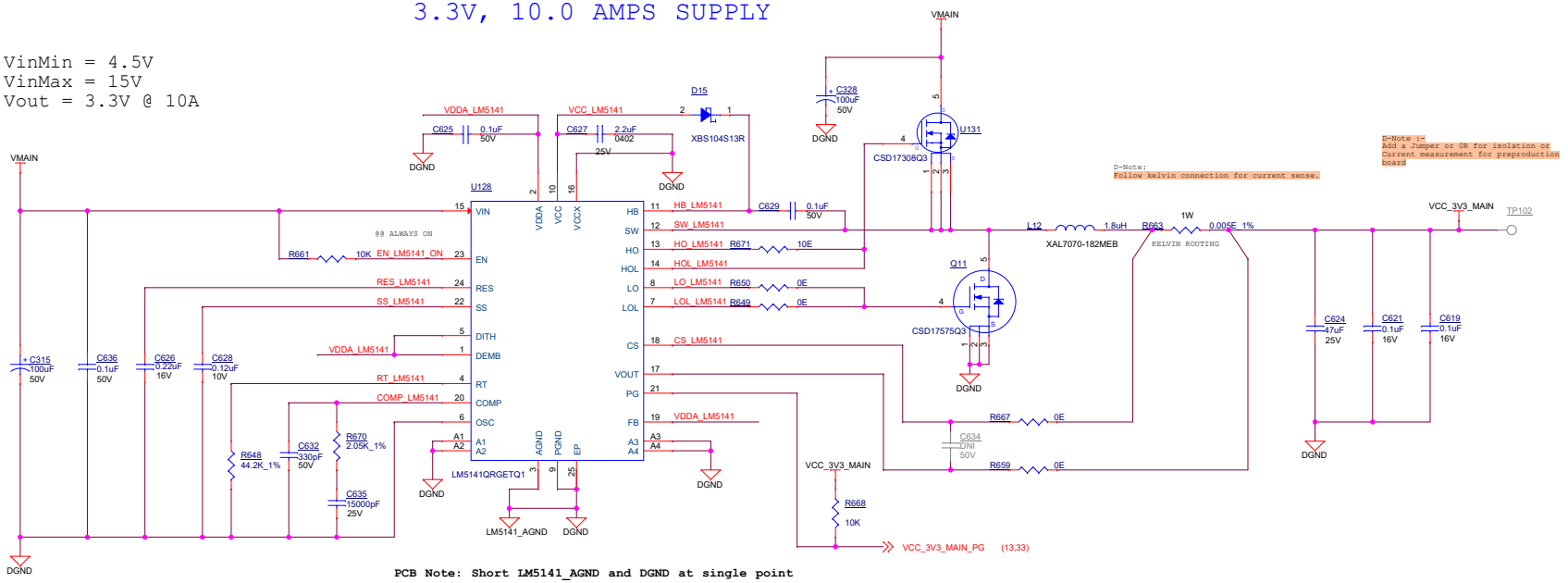
GND TEST POINTS



PERIPHERAL POWER SUPPLY - 2

VinMin = 4.5V
VinMax = 15V
Vout = 3.3V @ 10A

3.3V, 10.0 AMPS SUPPLY



PCB Note: Short LM5141_AGND and DGND at single point

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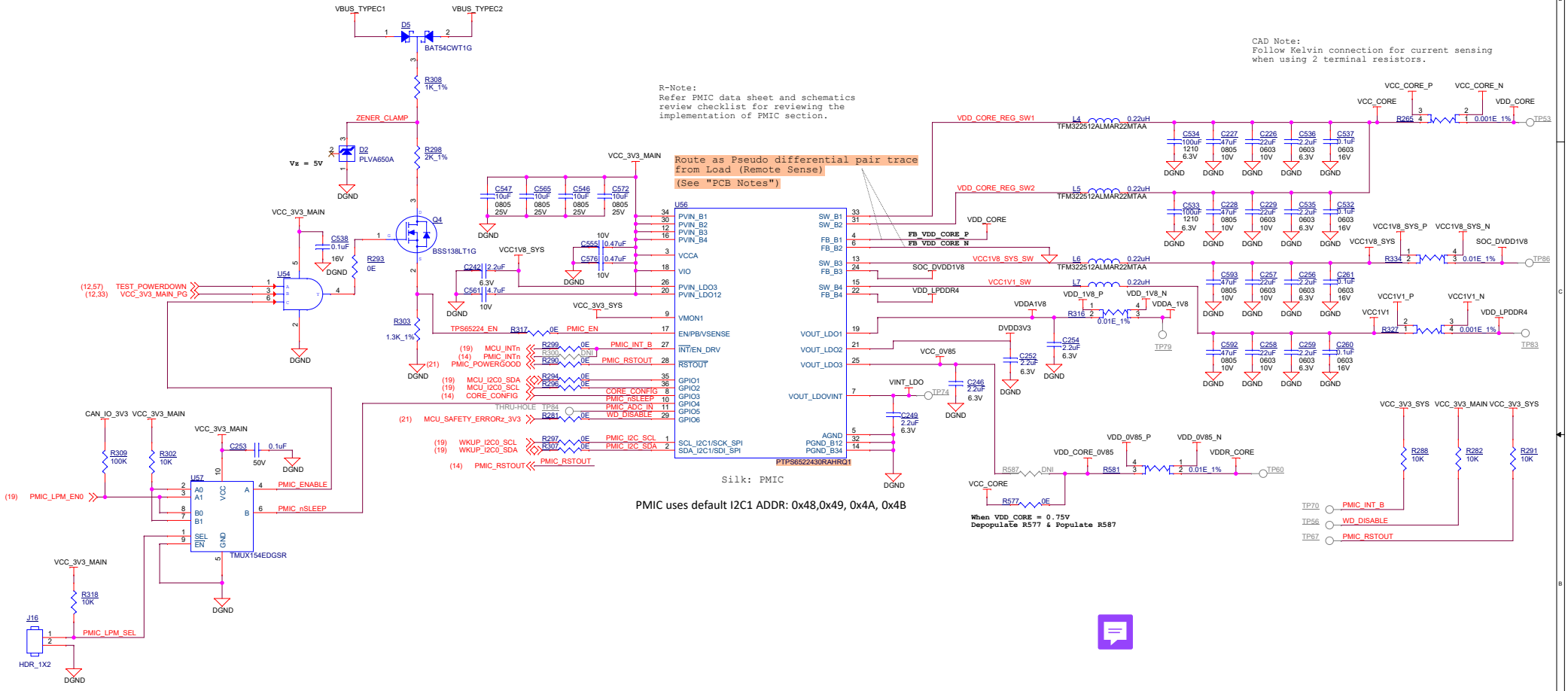
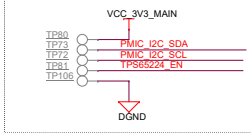
SOC POWER SUPPLY PMIC - 1



PMIC Config option



Silk: PMIC_PROG

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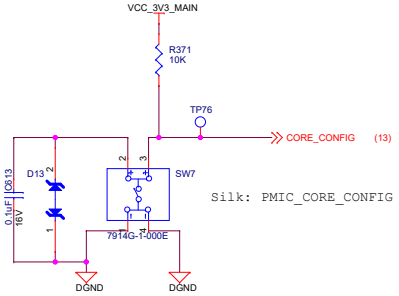
SOC POWER SUPPLY PMIC - 2

PMIC POWER INDICATION LED

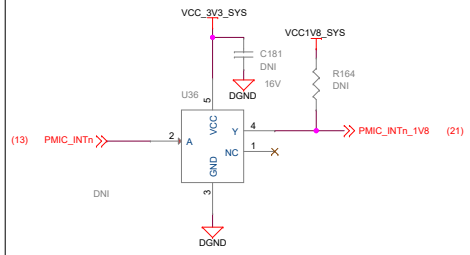
PMIC PUSH BUTTON LOGIC



Note: When R371 is DNI, Push Button (SW 7) becomes operational through internal pullup on PMIC GPIO3

R371	VDD_CORE VOLTAGE
Mounted	0.85 V (DEFAULT)
Not Mounted	0.75 V

PMIC INT SCHMIT TRIGGER



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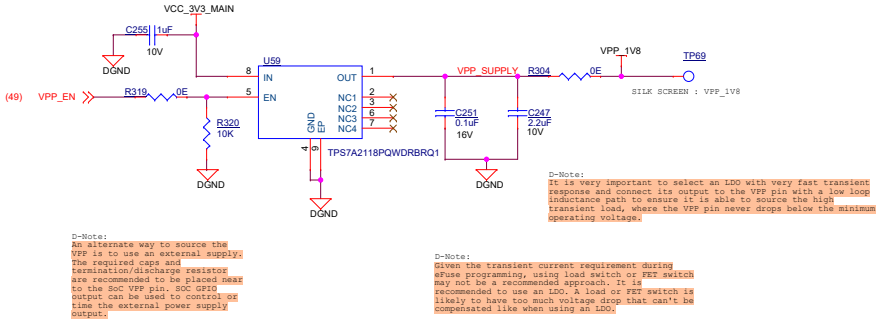
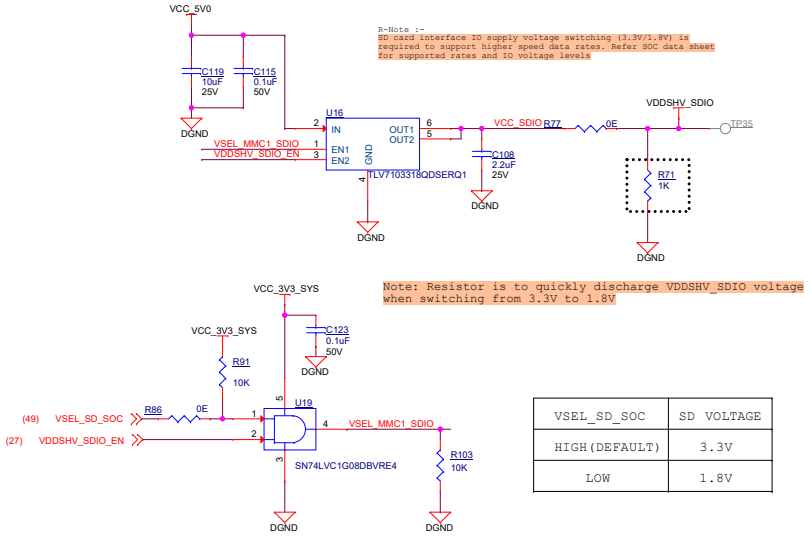
SOC POWER SUPPLIES - LDOs

1.8V VPP (eFUSE), 0.5AMPS SUPPLY

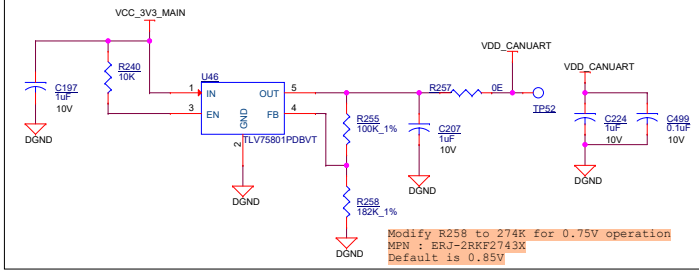


3.3V/1.8V SD CARD IO SUPPLY

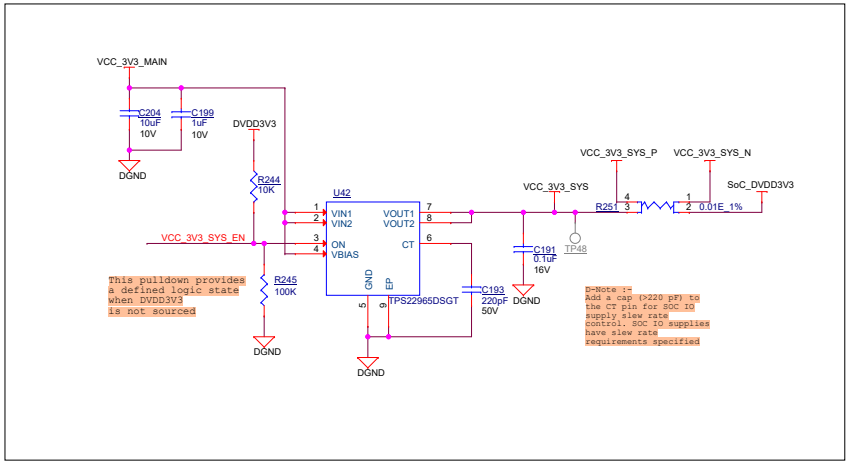


VSEL_SD_SOC	SD VOLTAGE
HIGH(DEFAULT)	3.3V
LOW	1.8V

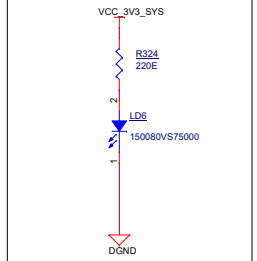
VDD_CANUART(0.85V),0.5 AMPS SUPPLY



VCC_3V3_SYS LOAD SWITCH



POWER INDICATION LED: VCC_3V3_SYS



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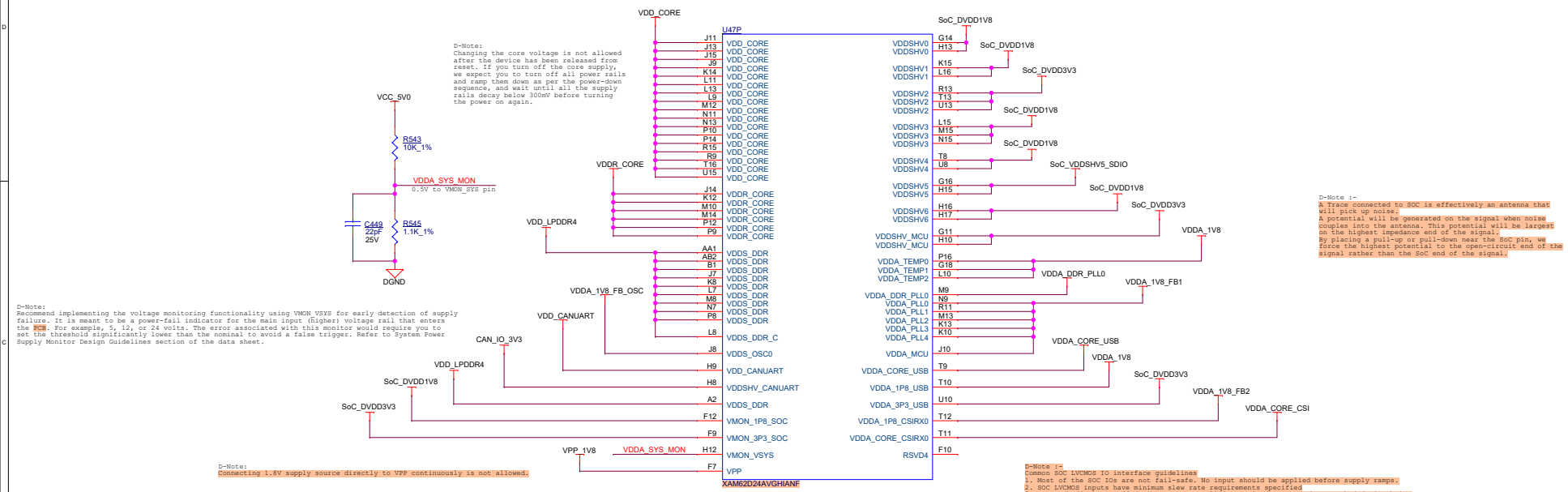
Title	SOC POWER SUPPLIES - LDOs & VCC_3V3_SYS LOAD SWITCH		
Size C	PROC180E2		Rev E2
Date:	Friday, June 06, 2025	Sheet 15 of 59	

SOC POWER SUPPLIES AND SUPPLY RAILS



D-Note:
Changing the core voltage is not allowed after the device has been released from reset. If you turn off the core supply, we expect you to turn off all power rails and ramp them down as per the power-down sequence, and wait until all the supply rails decay below 300mV before turning the power on again.

D-Note:
Recommend implementing the voltage monitoring functionality using VMON VSYS for early detection of supply failure. It is meant to be a power-fail indicator for the main input (higher) voltage rail that enters the PCB. For example, 5, 12, or 24 volts. The error associated with this monitor would require you to set the threshold significantly lower than the nominal to avoid a false trigger. Refer to System Power Supply Monitor Design Guidelines section of the data sheet.

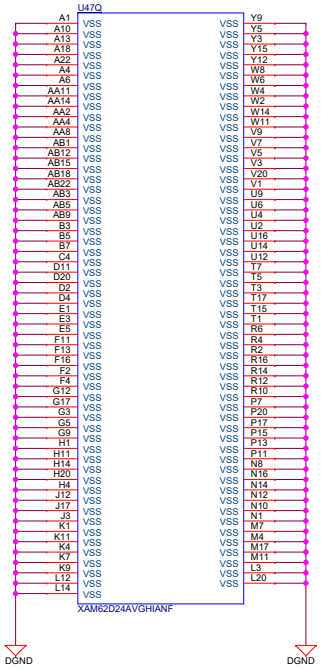
D-Note:
Connecting 1.8V supply source directly to VPP continuously is not allowed.

D-Note :-
A Trace connected to SOC is effectively an antenna that will pick up noise.
A potential will be generated on the signal when noise couples into the antenna. This potential will be largest on the highest impedance end of the signal.
By placing a pull-up or pull-down near the SoC pin, we force the highest potential to the open-circuit end of the signal rather than the SoC end of the signal.

D-Note :-
Common SOC LVCMOS IO interface guidelines
1. Most of the SOC IOs are not fail-safe. No input should be applied before supply ramps.
2. SOC LVCMOS inputs have minimum slew rate requirements specified
3. SOC IO buffers are off during Reset. A pull is required near to the attached device being driven by the SOC IOs
4. Any SOC IO that has a trace connected and not being actively driven needs a parallel pull. When adding pull is not feasible, ensure the traces are routed away from noisy signals

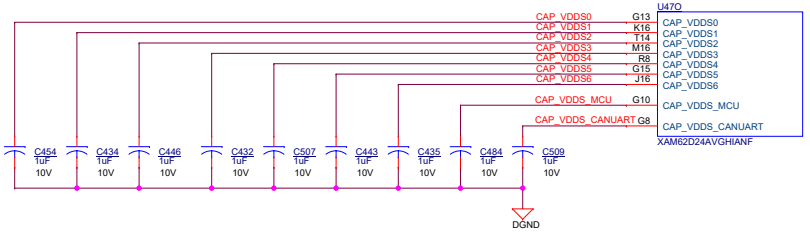
D-Note :-
It is very important to select an LDO with very fast transient response and connect its output to the VPP pin with a low loop inductance path to ensure it is able to source the high transient load, where the VPP pin never drops below the minimum operating voltage.

SOC VSS



D-Note :-
Refer pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used. It is acceptable to have the supplies connected and all the USB pins left unconnected provided the USB driver is not initialized any time and the USB calibration procedure does not happen. Grounding the USB supplies as per pin connectivity requirements when not used saves power when low power is a critical requirement.

D-Note :-
Refer Pin connectivity requirements to connect the CSI0 supplies (analog and core) when CSI0 interface is not used
Ferrite and Bulk Caps are optional when CSI0 is not used and Boundary scan functionality is required



D-Note :-
Select capacitor with ESR < 1 O
Ensure the PCB loop inductance is < 2.5 nH
Select 0201 package or smallest possible package
Refer SOC Data sheet

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Title	SOC POWER SUPPLIES, SUPPLY RAILS AND SOC GROUND VSS	
Size	PROC180E2	Rev E2
C		
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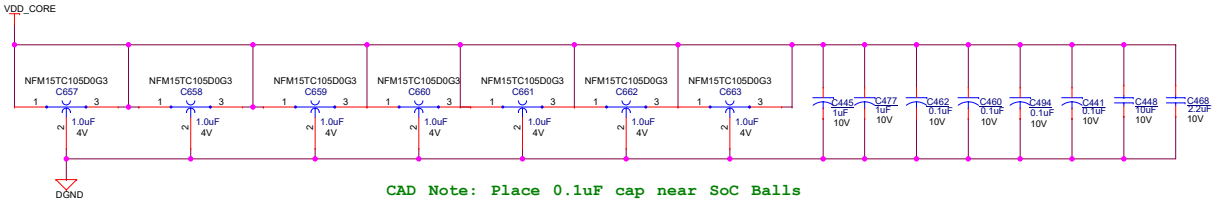
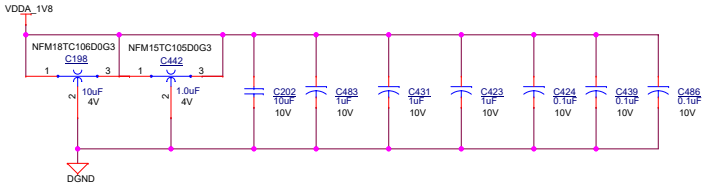
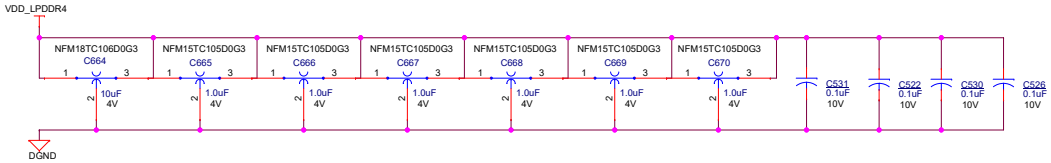
SOC POWER SUPPLIES - DECAPS 1



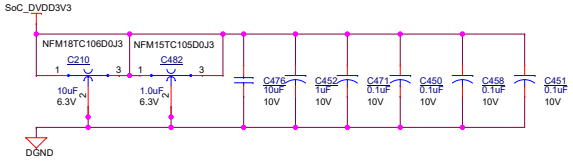
CAD Note: Place 0.1uF cap near SoC Balls



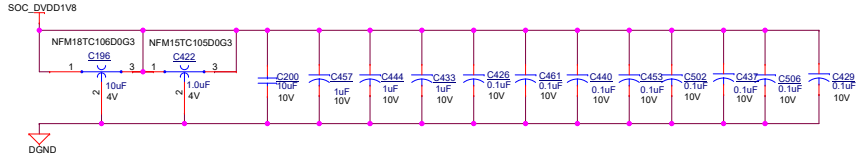
CAD Note: Place 0.1uF cap near SoC Balls



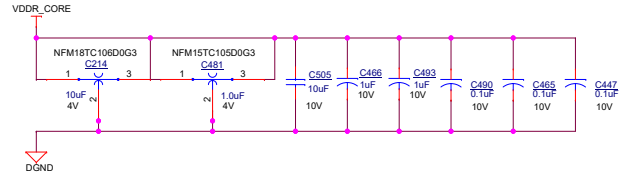
CAD Note: Place 0.1uF cap near SoC Balls



CAD Note: Place 0.1uF cap near SoC Balls



CAD Note: Place 0.1uF cap near SoC Balls



CAD Note: Place 0.1uF cap near SoC Balls

R-Note:
Usage of 3 terminal capacitors optimizes the usage of bulk capacitors and minimizes the PCB inductance.

E2

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Title	SOC POWER SUPPLIES - DECAPS 1		
Size C	PROC180E2		Rev
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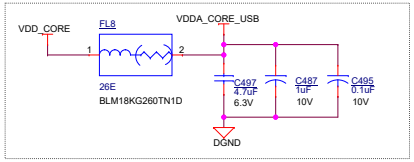
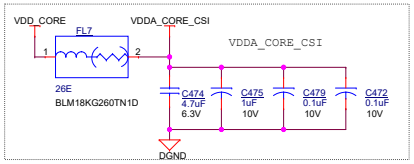
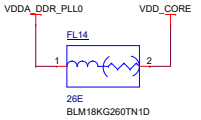
SOC POWER SUPPLIES - DECAPS 2

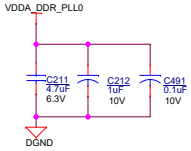
Peripherals - Core SUPPLY



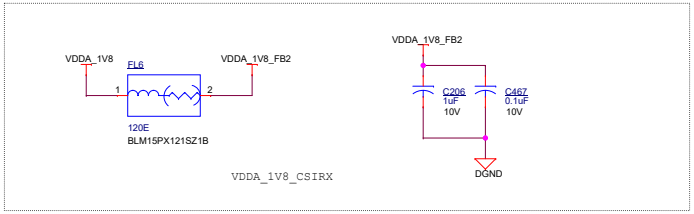


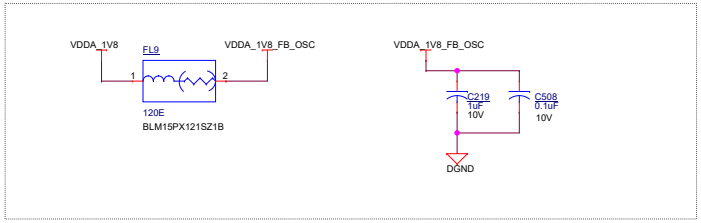
VDDA_DDR_PLL0

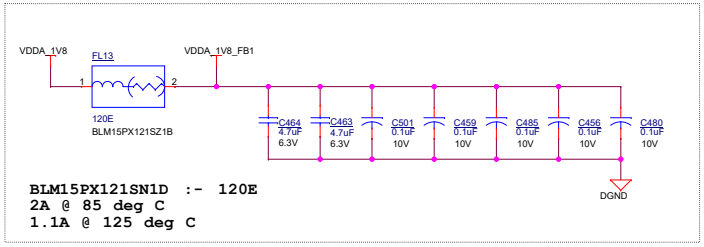




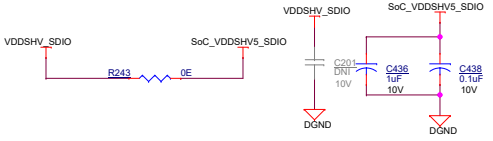
Peripherals - 1.8V Analog SUPPLY



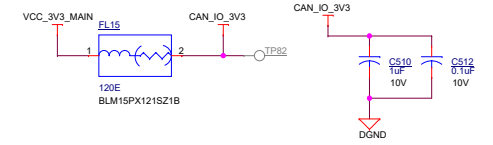


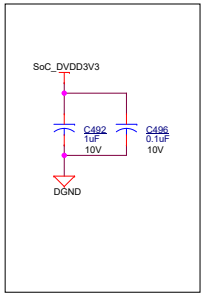


3.3V/1.8V MMC1 SUPPLY

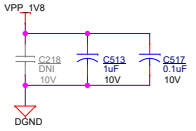


Always ON supply





VPP_1V8



Designed for TI by Mistral Solutions Pvt Ltd

Title	SOC POWER SUPPLIES - DECAPS 2		
Size C	PROC180E2		Rev E2
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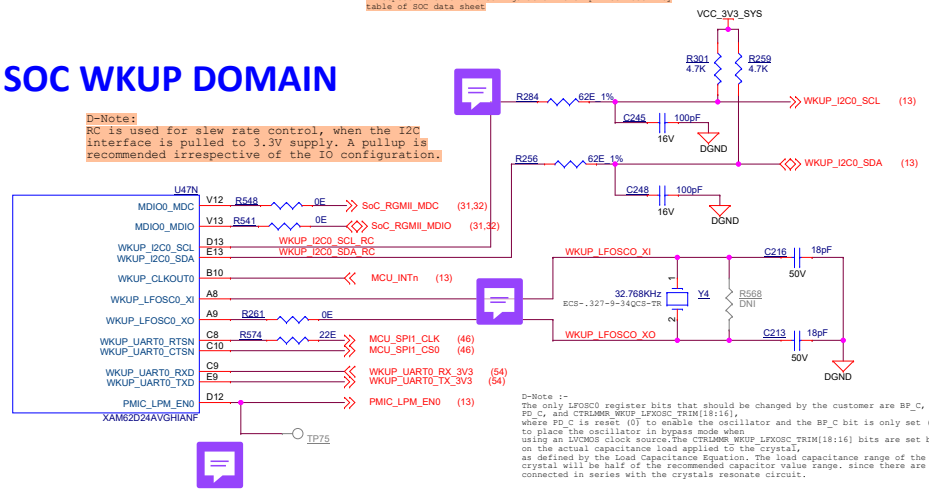
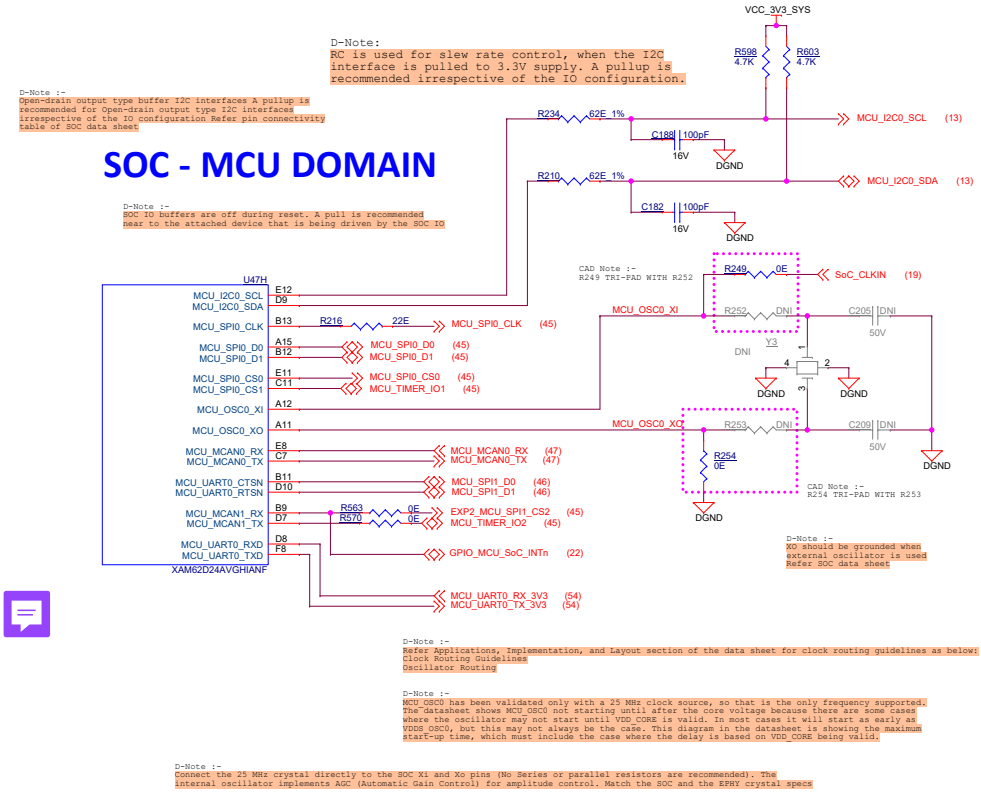
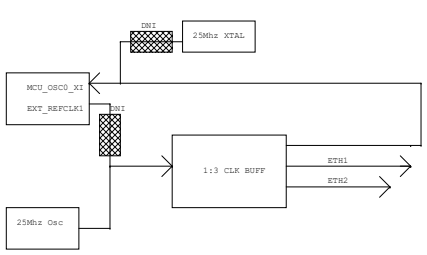
SOC WKUP DOMAIN

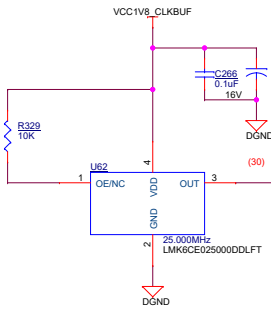


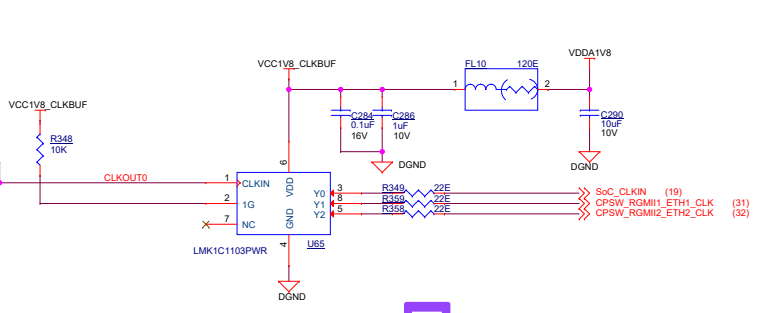
SOC - MCU DOMAIN



OSCILLATOR





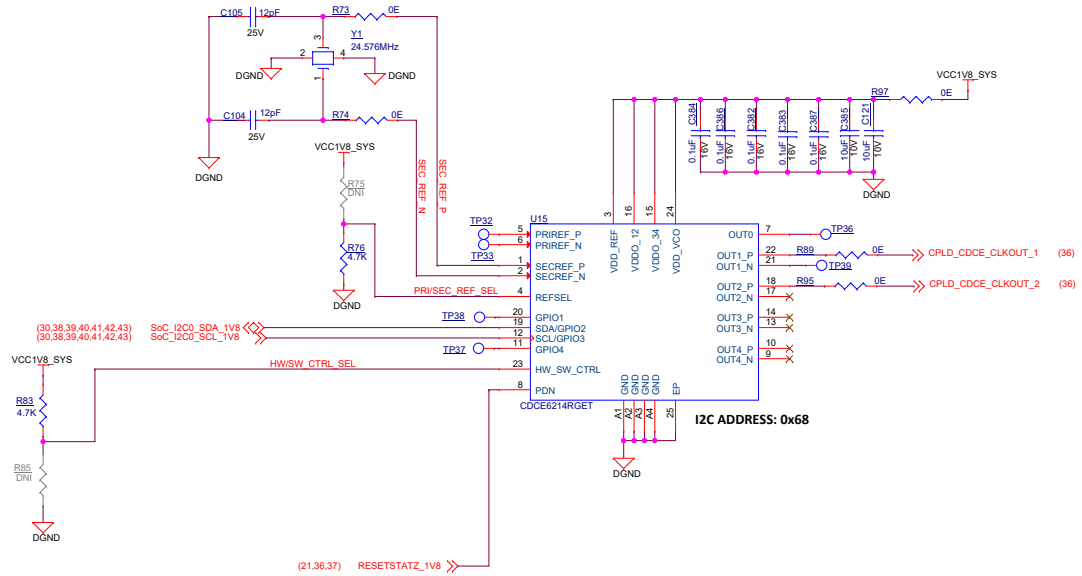


SOC & ETHERNET PHY CLOCK BUFFER

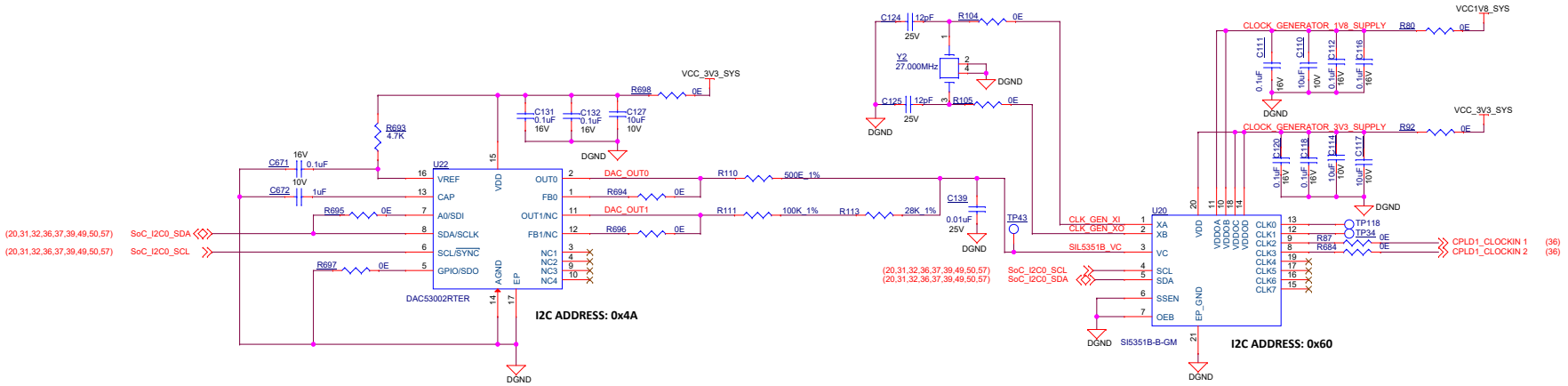
Designed for TI by Mistral Solutions Pvt Ltd

Title	SOC WKUP & GPMC		
Size	C	PROC180E2	Rev E2
Date:	Friday, June 06, 2025	Sheet 19 of 59	

CPLD CLOCK GENERATION



HW/SW CTRL SEL / PRI/SEC_REF_SEL	PAGE_SELECT	CLOCK_SOURCE
LOW	PAGE 0	SEC_REF
HIGH	PAGE 1	PRI_REF



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Title	CPLD CLOCK GENERATION	
Size C	PROC180E2	Rev E2
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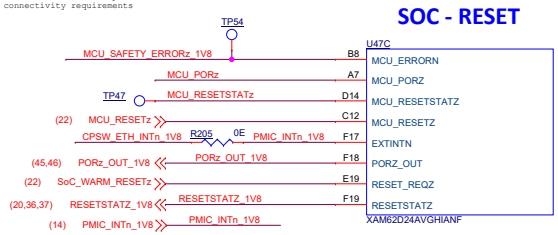
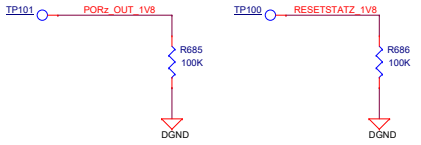
SOC RESET - 1

D-Note :- IO
Provision for a pulldown Populate
when attached device is connected
Refer SOC data sheet pin
connectivity requirements

SOC - RESET

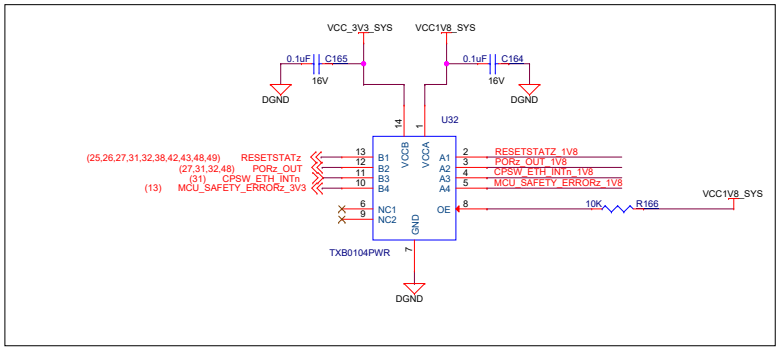


D-Note :-
Open drain output type IO EXTINTn has slew rate limit specified when
pulled to 3.3V supply. Add an RC at the input. Refer TMDS64EVM.

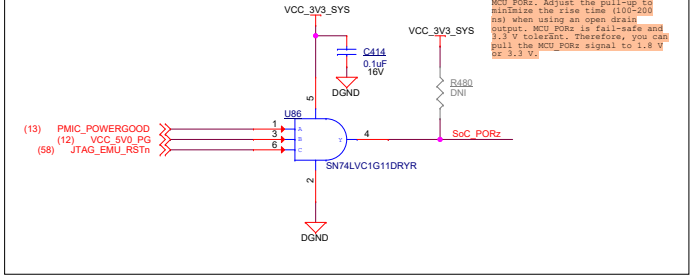


Pull-down resistor on PORz_OUT is provided to keep the signal
low until the processor is released from reset during the
power-up seqence

LEVEL TRANSLATOR

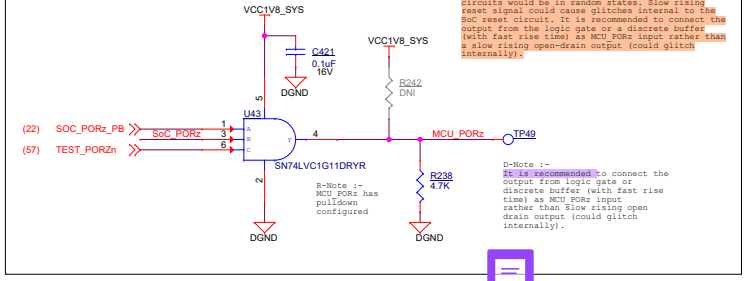


SOC POWER ON RESET



D-Note:
MCU_PORz inputs have maximum rise/fall time requirements when PMIC_POWERGOOD is connected to MCU_PORz. Adjust the pull-up to minimize the rise time (100-200 ns) when using an open drain output. MCU_PORz is fail-safe and 3.3 V tolerant. Therefore, you can pull the MCU_PORz signal to 1.8 V or 3.3 V.

MCU POWER ON RESET



D-Note:
Not connecting a valid MCU_PORz could cause unpredictable and probably random behavior. Since the device is not getting a valid reset, internal circuits would be in random states. Slow rising reset signal could cause glitches internal to the SoC reset circuit. It is recommended to connect the output from the logic gate or a discrete buffer (with fast rise time) as MCU_PORz input rather than a slow rising open-drain output (could glitch internally).

R-Note :-
MCU_PORz has
pulldown
configured

D-Note :-
It is recommended to connect the output from logic gate or discrete buffer (with fast rise time) as MCU_PORz input rather than Slow rising open drain output (could glitch internally).

Designed for TI by Mistral Solutions Pvt Ltd

Title	SOC RESET - 1		
Size	PROC180E2		Rev
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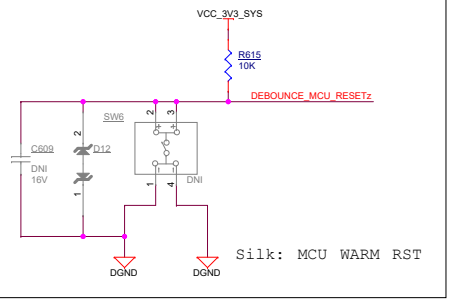
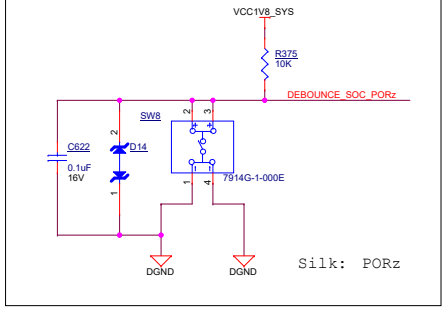
SOC RESET - 2

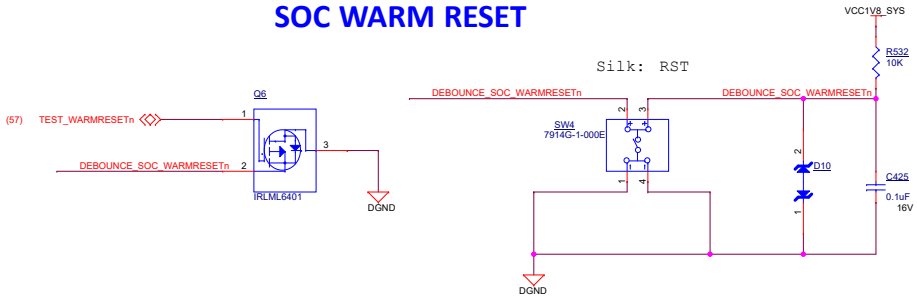
MCU WARM RESET



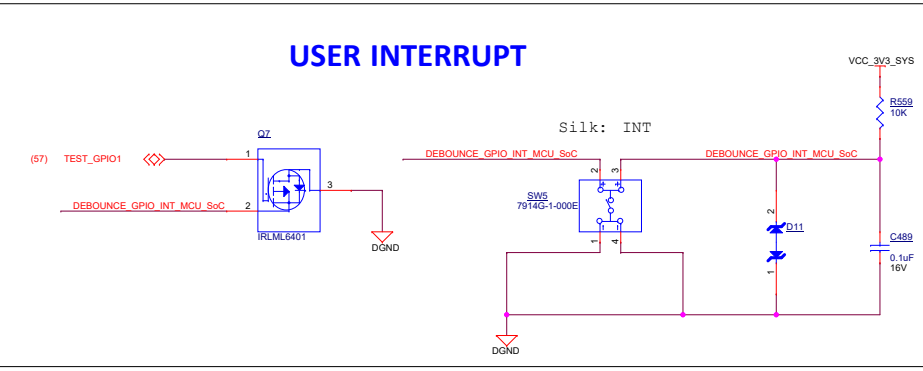
SOC PORZ



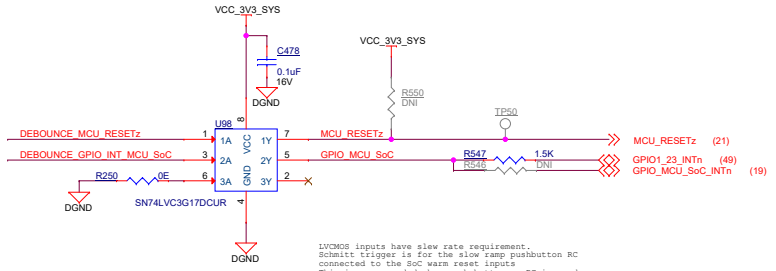
SOC WARM RESET

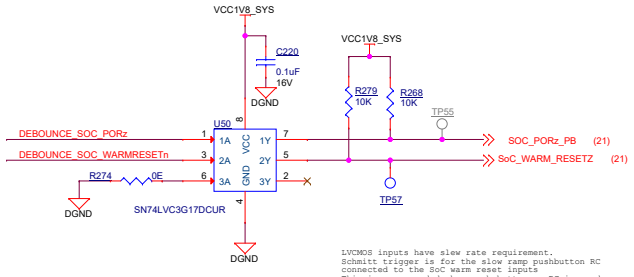


USER INTERRUPT



RESET & INT DEBOUNCE CIRCUIT





Designed for TI by Mistral Solutions Pvt Ltd

Title	SOC RESET - 2		
Size	PROC180E2		Rev
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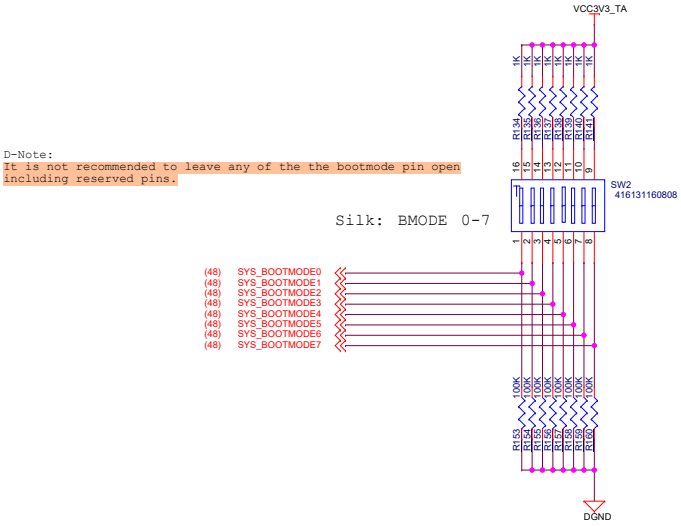
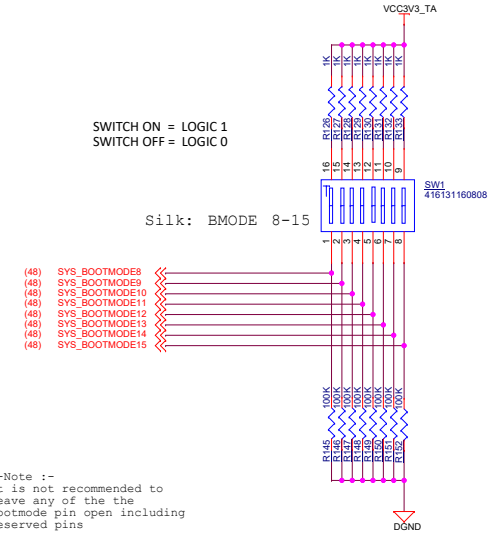
BOOT MODE SWITCHES

D-Note: VCC3V3_TA supply is used for test automation.
Connect SoC_DVDD3V3 in the custom board design when buffers are not used



D-Note:
It is not recommended to leave any of the the bootmode pin open including reserved pins.

SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0



D-Note :-
it is not recommended to leave any of the the bootmode pin open including reserved pins

BOOT MODES SUPPORTED

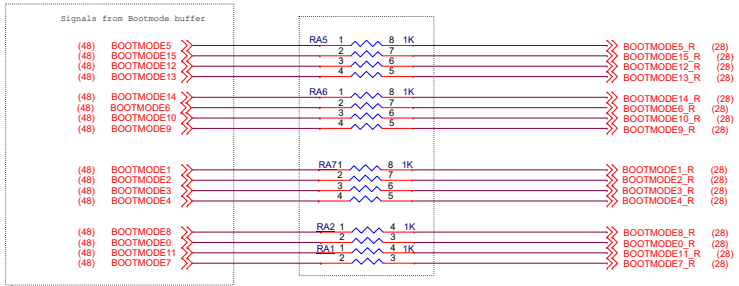
1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. ETHERNET
6. USB0 DFU
7. USB0 MS

D-Note:
1. Dip switches are optional and are used on the SK for ease of configuration. A pull-up or pull-down resistor can be used to set the bootmode configuration. Provide provisions for pull-up and pull-down resistors for the bootmode pins that have configuration capability.
2. When DIP switches are used on a custom board, an external ESD protection may be required if the DIP switches are expected to be configured in an uncontrolled ESD environment.
3. When DIP switches are used, reduce the resistor values used for the divider to 47k and 470R ohms for maintaining the ratio.

D-Note :-
Reduce the series resistor value when buffer is not used to 0R
This resistor is used to isolate the alternate function during testing

D-Note :-
Shorting of bootmode inputs (IOs) is not recommended or allowed since the IOs have alternate functions that could be configured after boot. Shorting the bootmode pins directly to VCC or ground directly is not recommended. Connect each of the bootmode pins through separate resistor. Choose the bootmode resistor value based on the use case (10K or similar)

BOOTMODE PINS



D-Note :
Connect SYS_BOOTMODE signals when bootmode buffers are not used

D-NOTE:
1. 1K Resistor at the output of the buffer is recommended when the bootmode pins are used for alternate functions
2. Replace 1K Resistor at the output of the buffer with resistor of value 0E when bootmode buffers are not used

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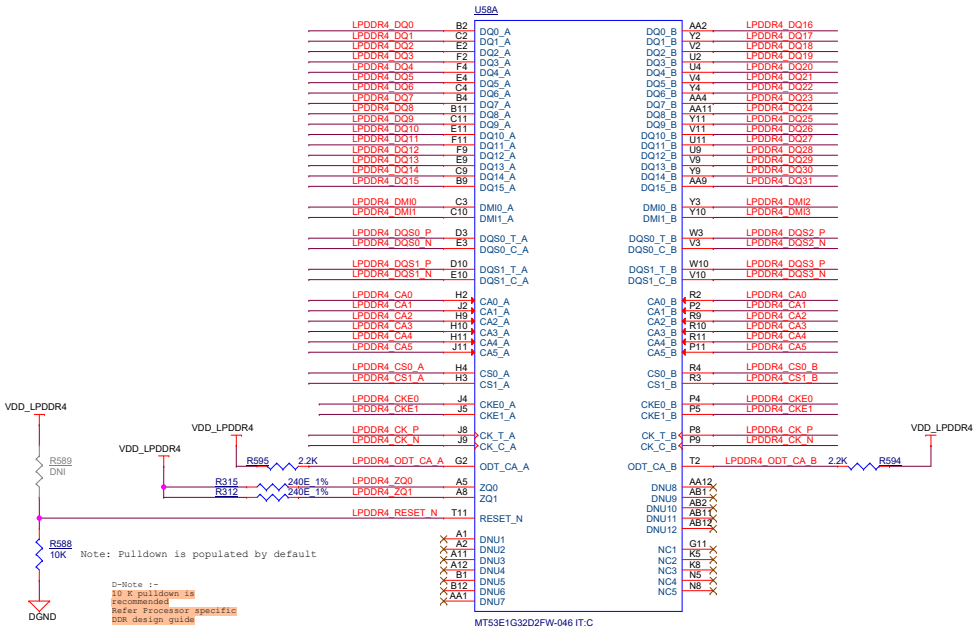
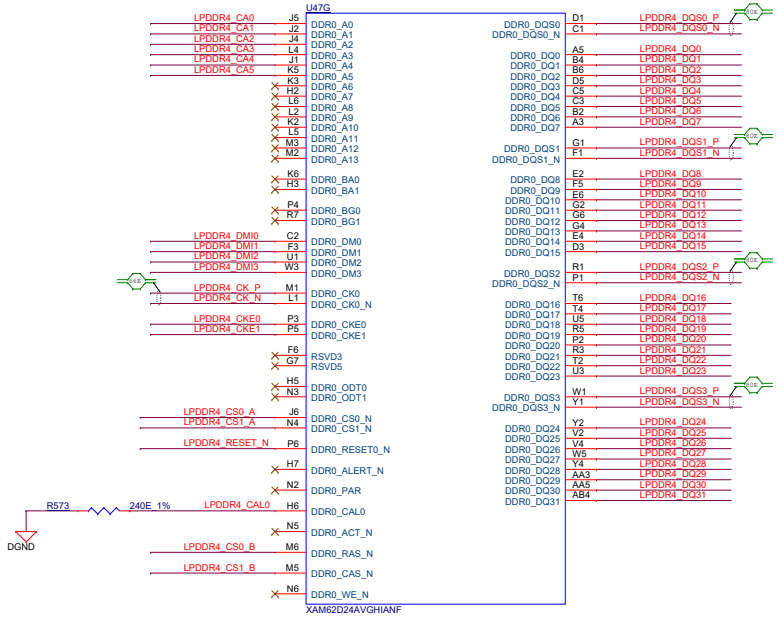
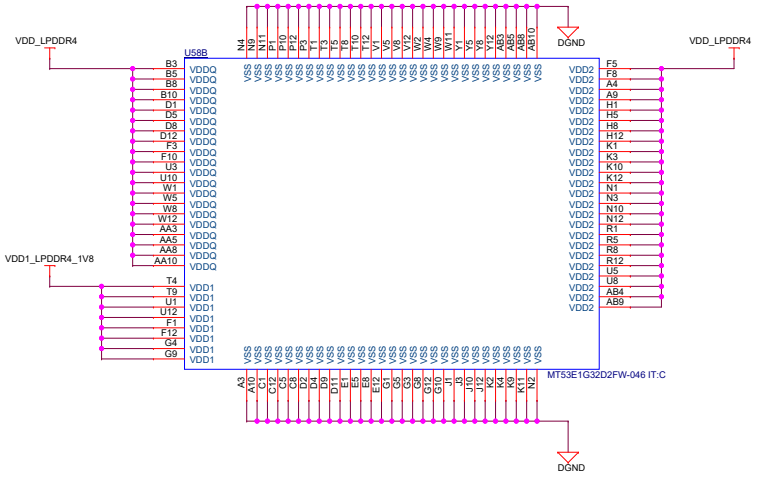
Title	BOOT MODE SWITCHES		
Size	C	PROC180E2	Rev E2
Date:	Friday, June 06, 2025	Sheet 23 of 59	

LPDDR4 DEVICE

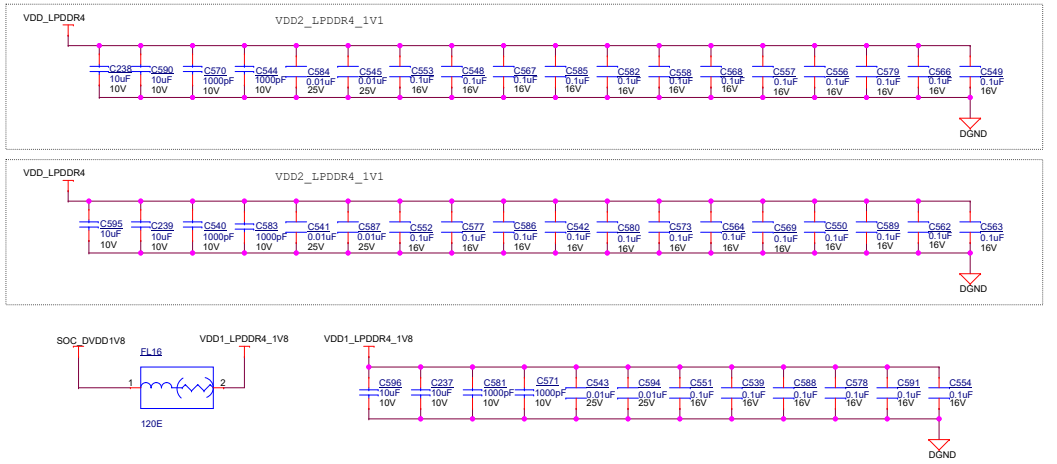


SOC LPDDR4 INTERFACE





LPDDR4 POWER DECAPS

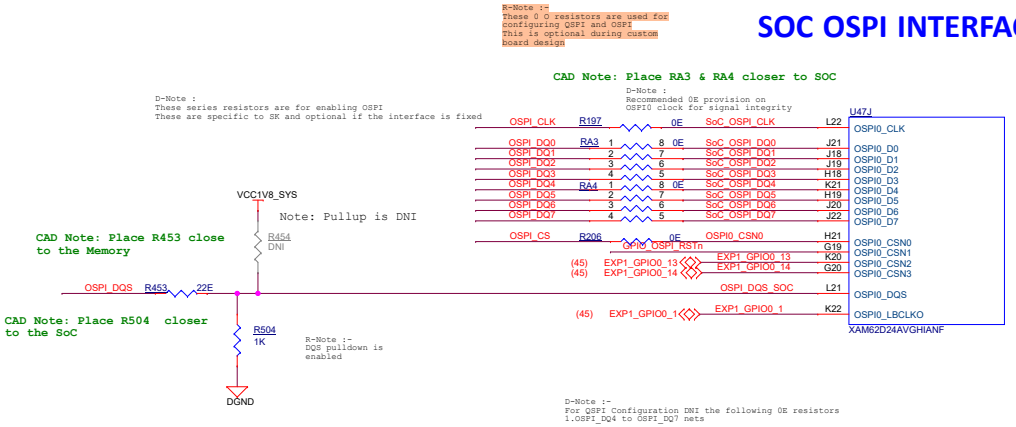


Designed for TI by Mistral Solutions Pvt Ltd

Title	SOC LPDDR4 INTERFACE		
Size	PROC180E2		Rev
C			E2
Date:	Friday, June 06, 2025	Sheet 24 of 59	

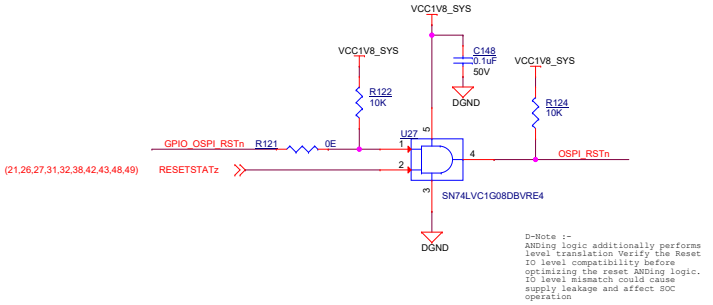
OSPI INTERFACE

SOC OSPI INTERFACE

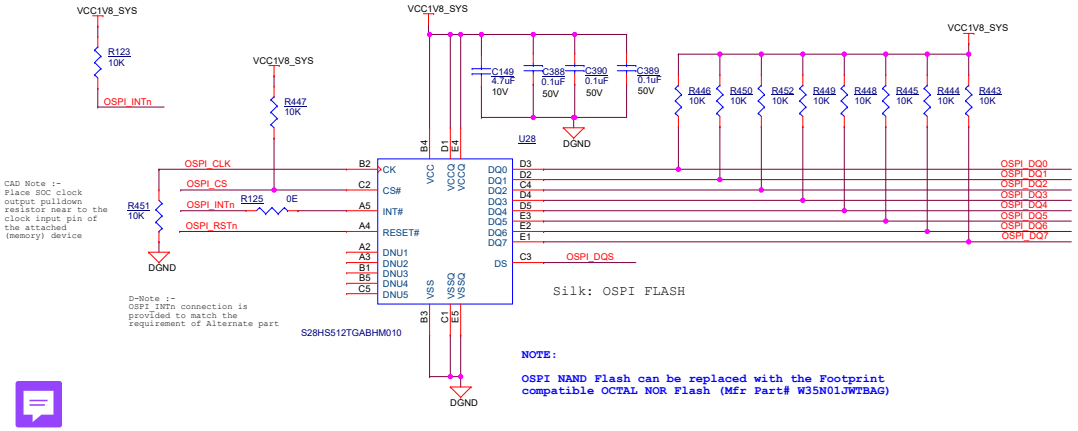


D-Note :-
Connecting OSPI interface to multiple devices is not recommended or supported

OSPI FLASH RESET



OSPI FLASH



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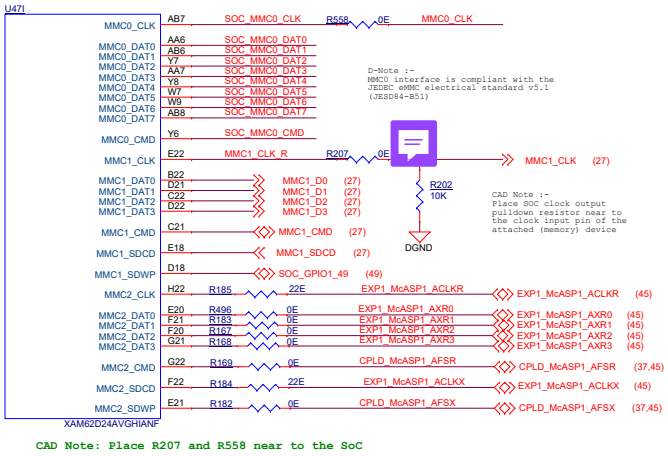
Title	OSPI INTERFACE		
Size	PROC180E2		Rev
C			E2
Date:	Friday, June 06, 2025	Sheet	25 of 59

eMMC INTERFACE

SOC - MMC Interface



D-Note :-
0E provision on MMC0_CLK
helps improve signal integrity

D-Note :-
MMC0 interface is compliant with the
JEDEC eMMC electrical standard v5.1
(JESD84-B51)

CAD Note :-
Place SOC clock output
pulldown resistor near to
the clock input pin of the
attached (memory) device

CAD Note: Place R207 and R558 near to the SoC

D-Note :-
This family of processor implements a soft PHY
for eMMC interface. The pulls required for D0,
Clock and other eMMC interface control signals
are recommended to be implemented externally.

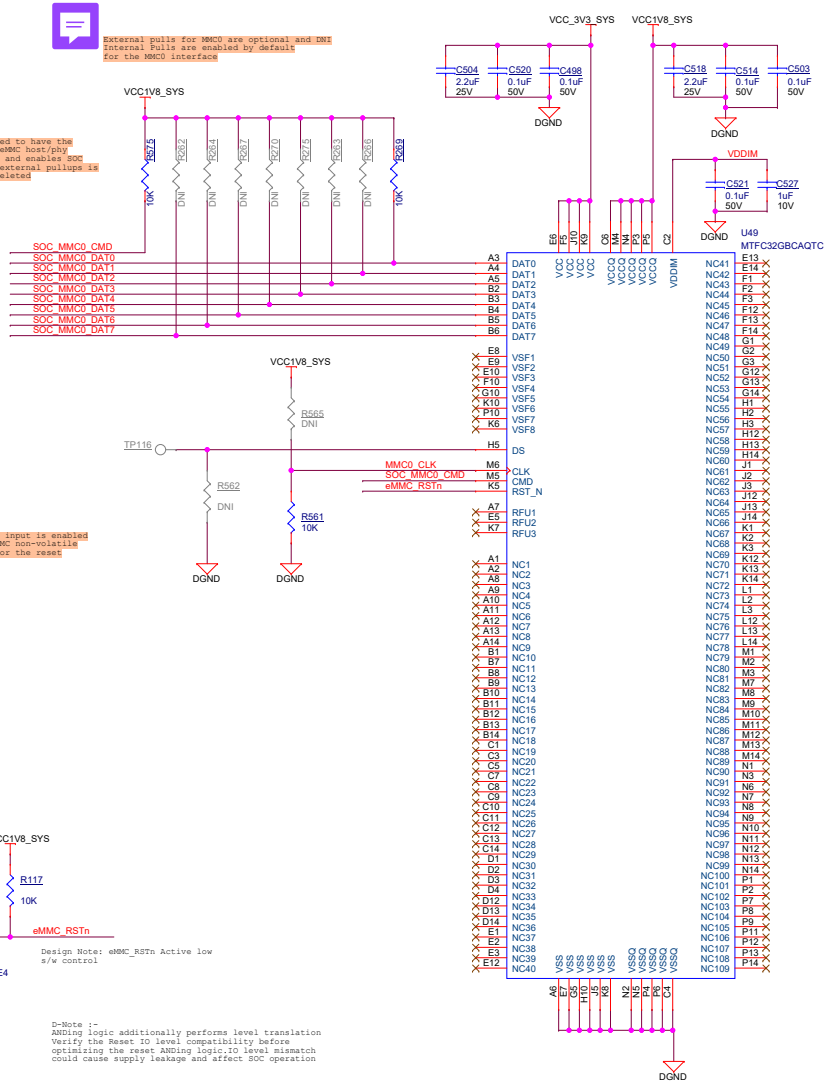
eMMC FLASH

External pulls for MMC0 are optional and DNI
Internal Pulls are enabled by default
for the MMC0 interface

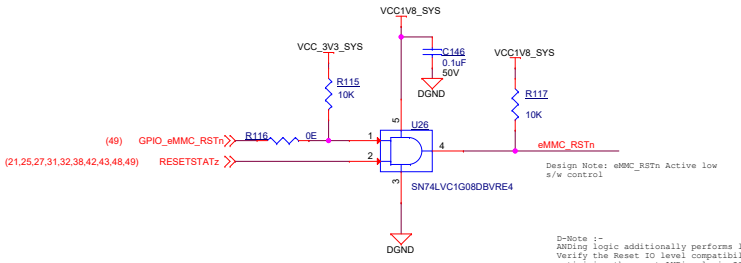
D-Note :-
For D7..D1 eMMC device is expected to have the
pullups enabled by default. The eMMC host/phy
disables the eMMC device pullups and enables SOC
internal pullups. Provision for external pullups is
optional or the pullups can be deleted

R-Note :-
What is the reason we selected
pulldown instead of pullup for EMMC,
SD card or other peripherals?
Because there are cases where the
clock is stopped or paused in a low
logic state and the pull-down option
is consistent with this logic state.

D-Note :-
Ensure eMMC_RSTn Reset input is enabled
in the eMMC device (eMMC non-volatile
configuration space) for the reset
logic to be functional



eMMC FLASH RESET



Design Note: eMMC_RSTn Active low
s/w control

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before
optimizing the reset ANDing logic.IO level mismatch
could cause supply leakage and affect SOC operation

D-Note :-
In case ANDing logic is not used and the processor
Main Domain warm reset status output (RESETSTATz)
is used to reset the attached device, ensure the
IO voltage level of the attached device matches
the RESETSTATz IO voltage level. A level
translator is recommended to match the IO voltage
level. A resistor divider could be used
alternatively, provided optimum impedance value of
the resistor divider is selected. If too high the
rise/fall time of the eMMC reset input could be
slow and introduce too much delay. If too low it
will cause the AM62x to source too much
steady-state current during normal operation.

D-Note:
1. You could eliminate the GPIO option and only use the reset
output (warm or cold), where the software forces a warm reset, if
the peripheral becomes unresponsive. However, this will reset the
entire device rather than trying to recover the specific peripheral
without resetting the entire device.
2. The GPIO reset option makes it possible for the software to
reset the attached device (eMMC or OSPI or SD card or
EPHY) without resetting the entire processor, if there is a case
where the peripheral becomes unresponsive.

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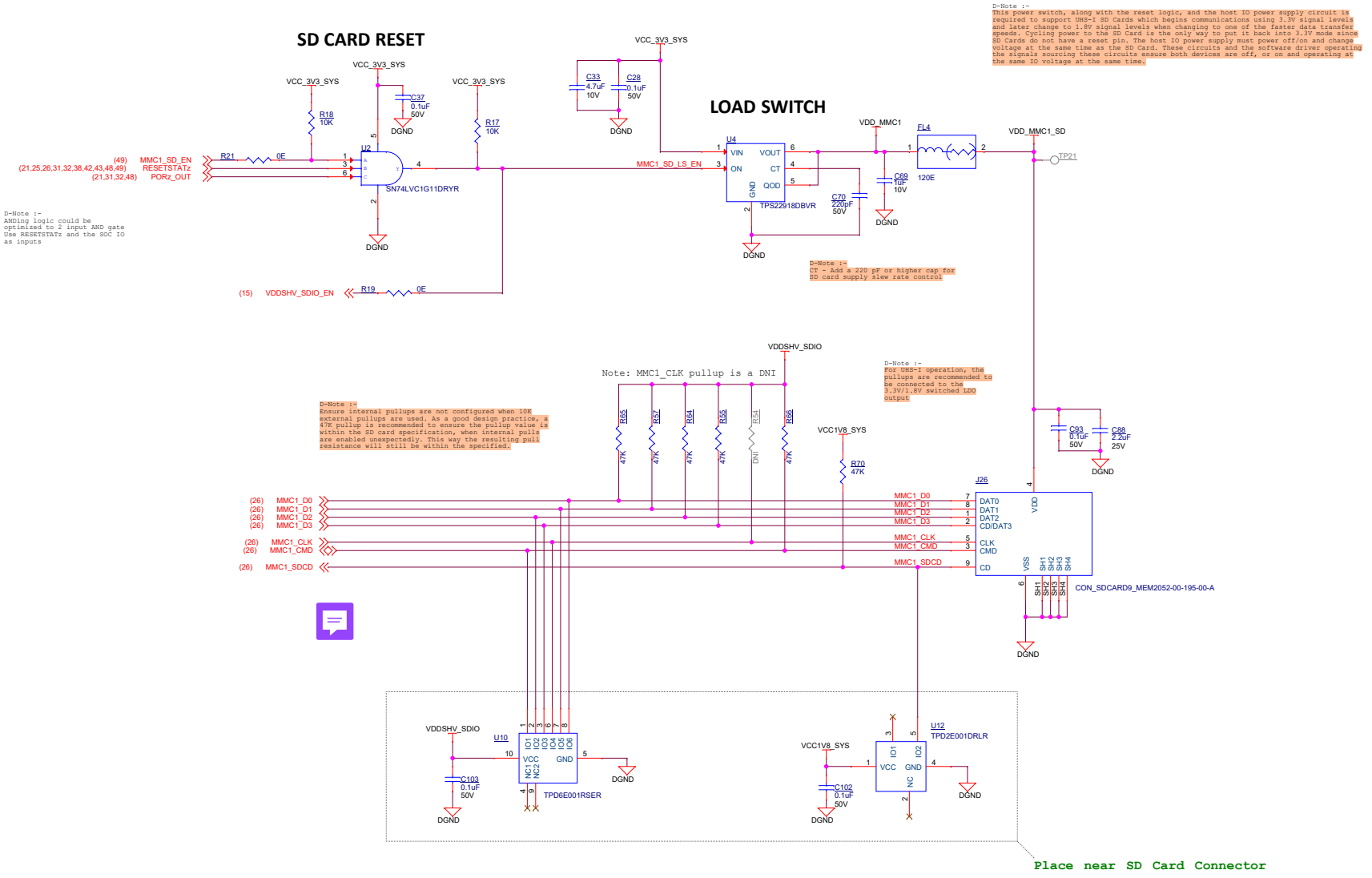
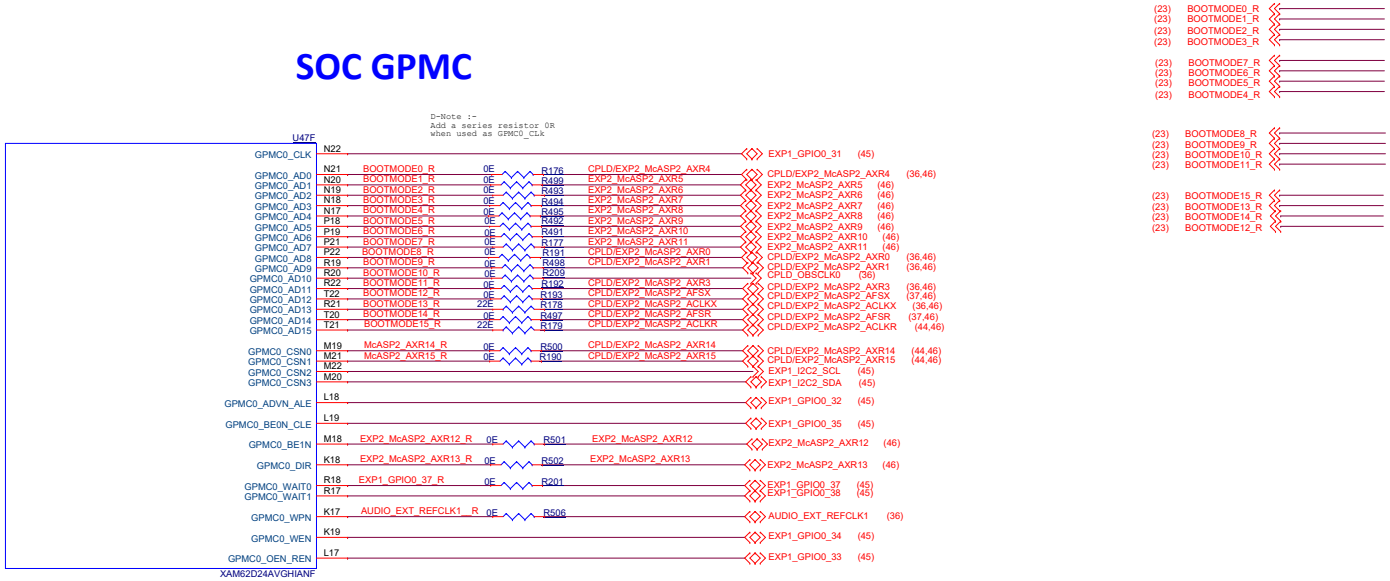
Title	eMMC INTERFACE	
Size C	PROC180E2	Rev E2
Date: Friday, June 06, 2025	Sheet 26 of 59	

SD CARD INTERFACE

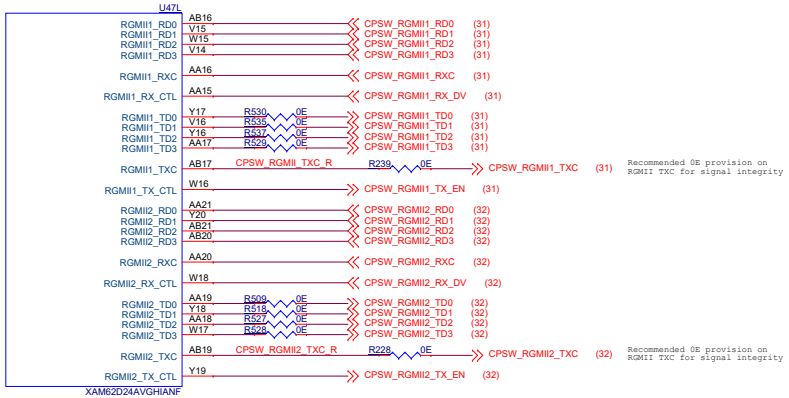


Designed for TI by Mistral Solutions Pvt Ltd	Title: SD CARD INTERFACE	
	Size: C	PROC180E2 — Rev: E2
	Date: Friday, June 06, 2025	Sheet 27 of 59

SOC GPMC



SOC CPSW3G ETHERNET INTERFACE



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Title	SOC PERIPHERALS 1		
Size	PROC180E2		Rev
C			E2
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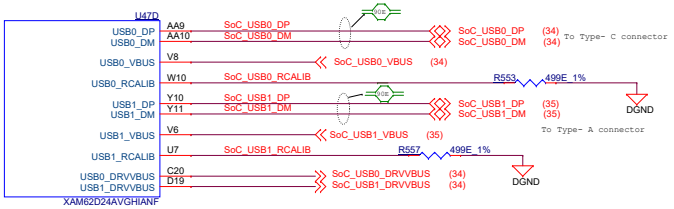
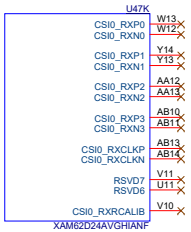
SOC - USB



SOC CSI UNUSED



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Title	SOC PERIPHERALS 2		
Size	PROC180E2		Rev
C			E2
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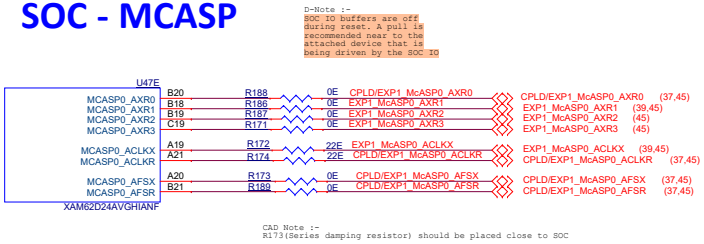
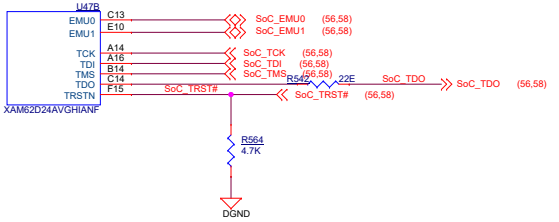
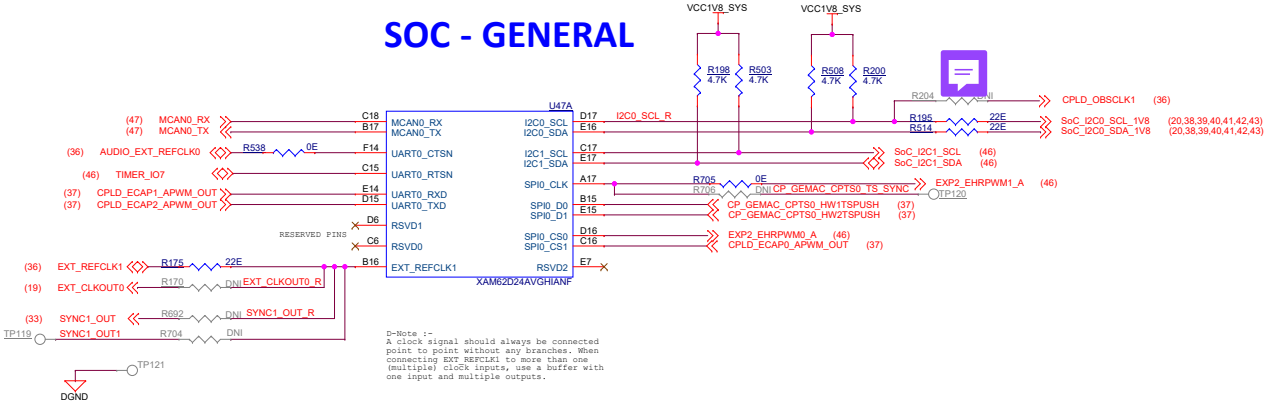
SOC - MCASP



SOC - JTAG

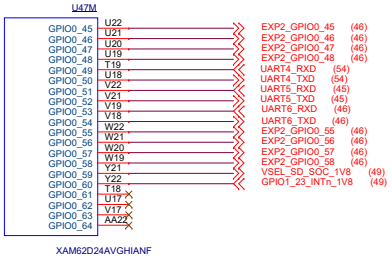


SOC - GENERAL



CAD-NOTE: QUADPAD R175, R170 , R692 and R704

SOC - UART , GPIOs



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Title	SOC PERIPHERALS 3		
Size	PROC180E2		Rev
C			E2
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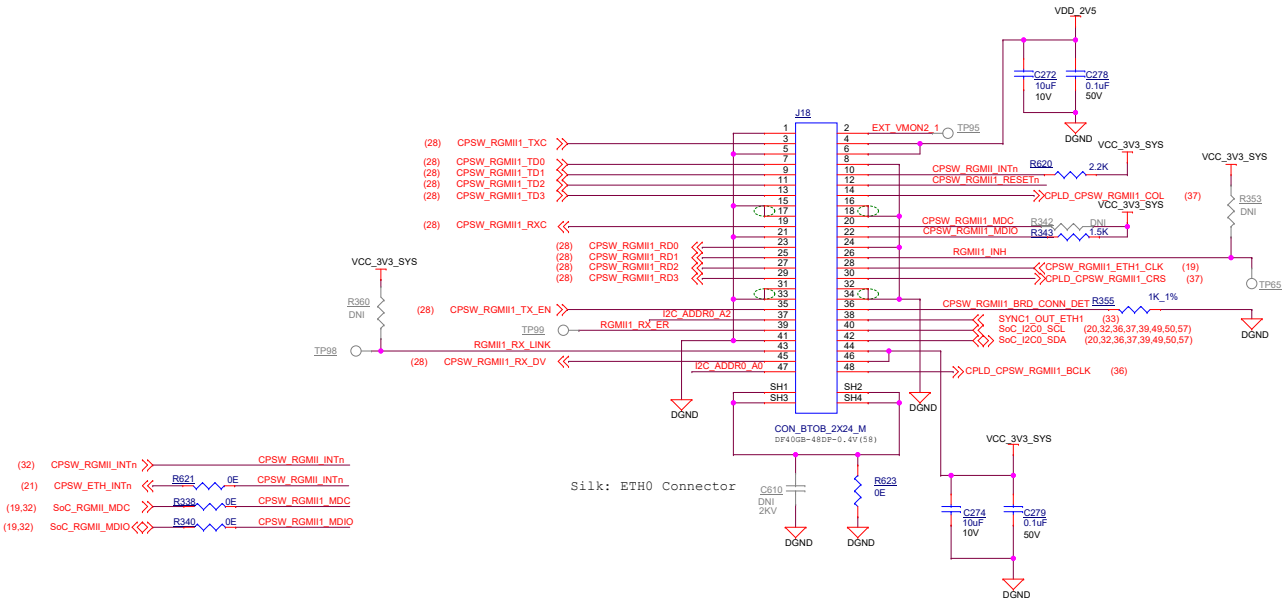
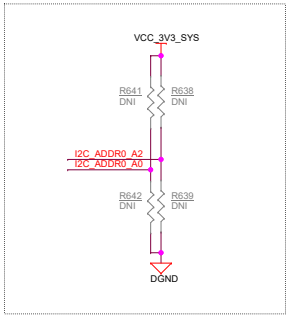
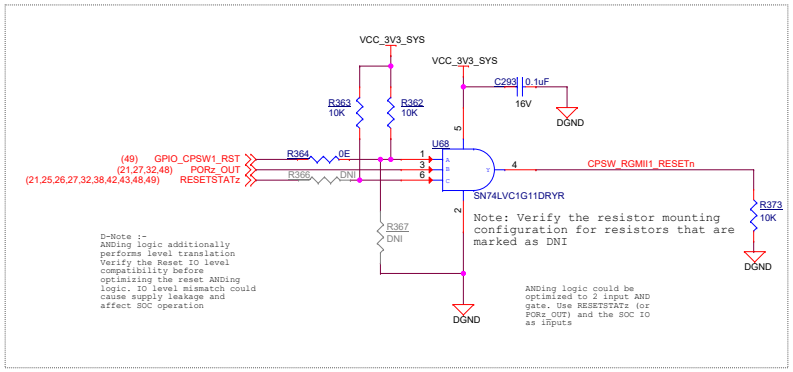
ETHERNET EXPANSION CONNECTOR CPSW3G RGMII 1



I2C Address Strap



CPSW3G RGMII 1 RESET



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Title	ETHERNET EXPANSION CONNECTOR CPSW3G RGMII 1		
Size C	PROC180E2		Rev E2
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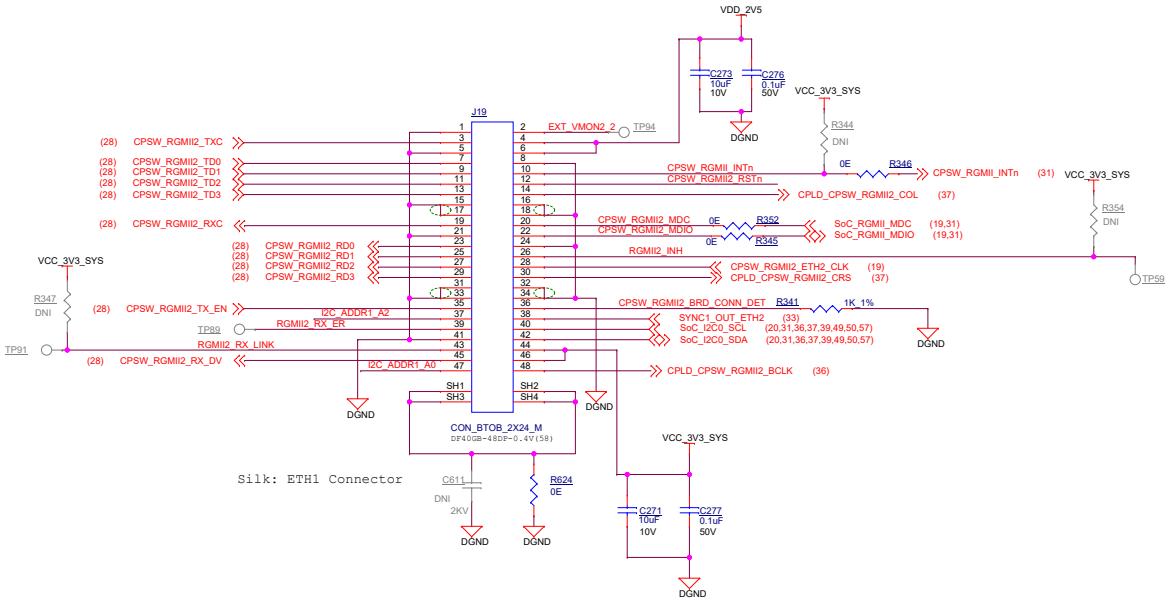
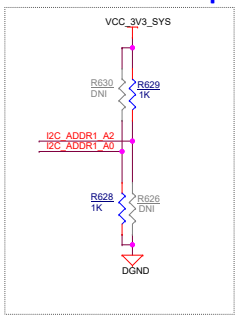
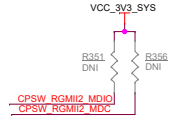
ETHERNET EXPANSION CONNECTOR CPSW3G RGMII 2



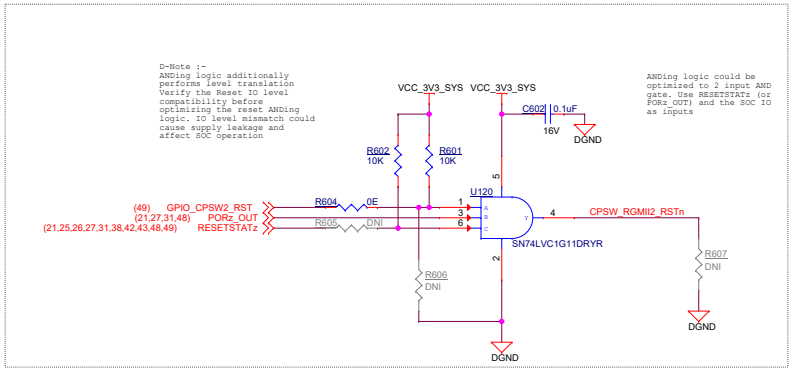
Silk: ETH1 Connector

I2C Address Strap

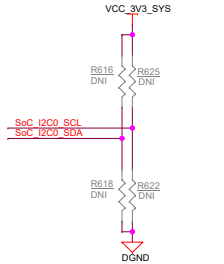




CPSW3G RGMII 2 RESET



Note: Verify the resistor mounting configuration for resistors that are marked as DNI



CAD Note: Thevnin's termination should be placed at the J19 Connector

Designed for TI by Mistral Solutions Pvt Ltd

Title	ETHERNET EXPANSION CONNECTOR CPSW3G RGMII 2		
Size C	PROC180E2		Rev E2
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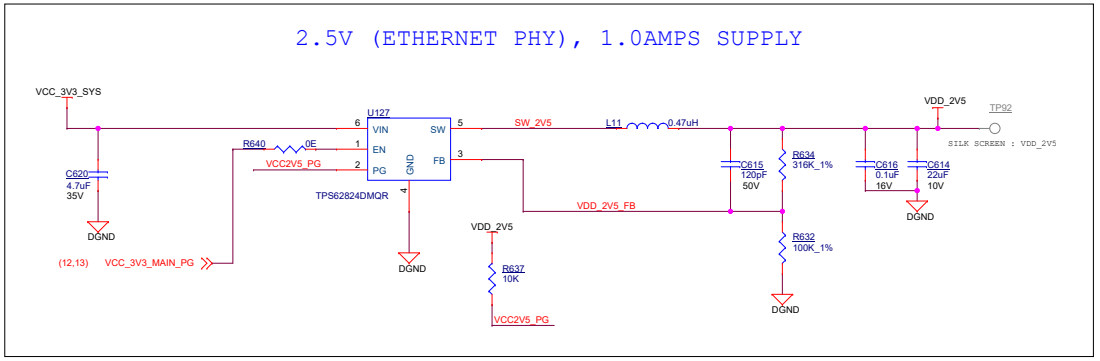
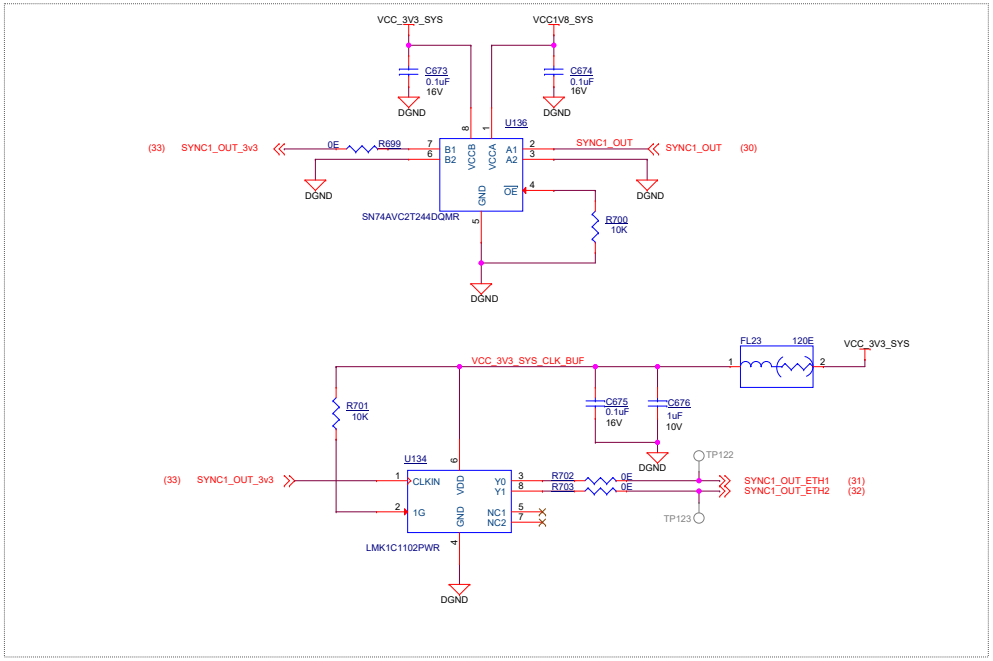
POWER SUPPLY (CORE) FOR ETHERNET PHY



D-Note : 2.5V Power supply for Ethernet PHY is generated by the PMIC



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Title	POWER SUPPLY (CORE) FOR ETHERNET PHY		
Size	PROC180E2		Rev
C			E2
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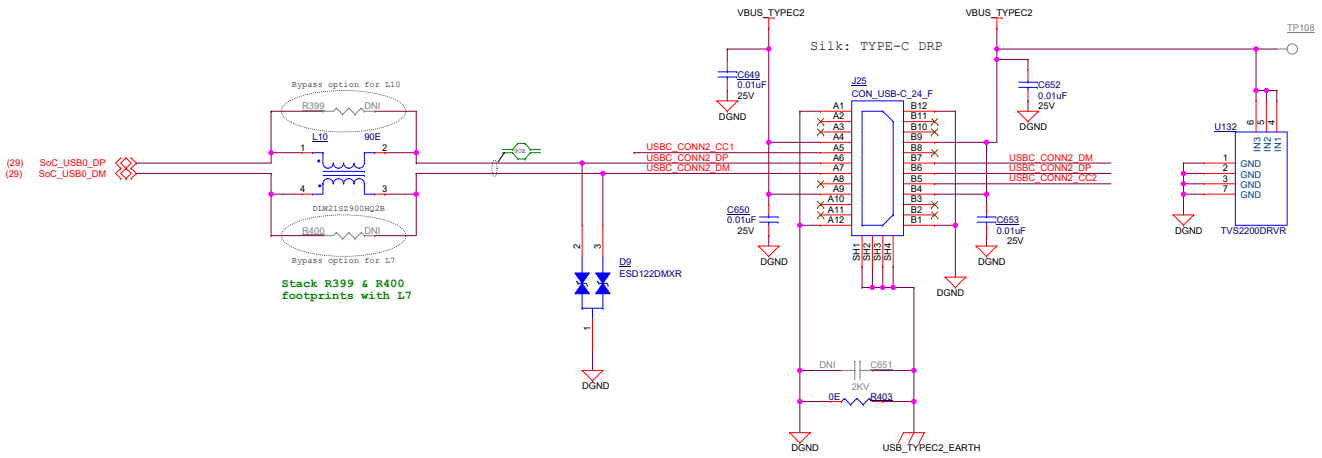
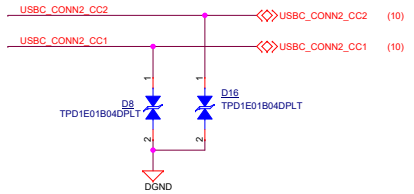
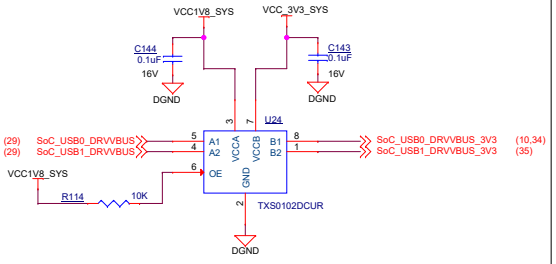
USB0 TYPE-C DRP



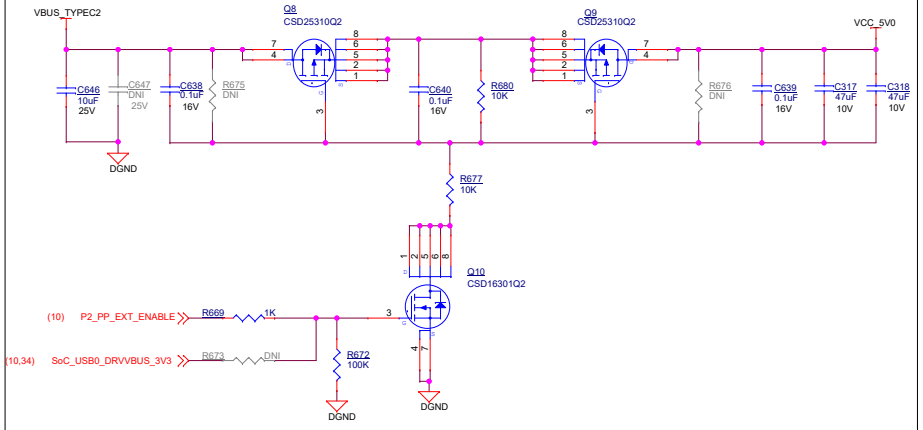


D-Note :-
VBUS connection is optional for Host configuration

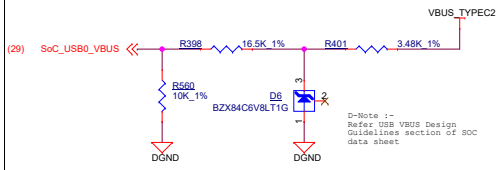
USB_DRV BUS LEVEL TRANSLATOR



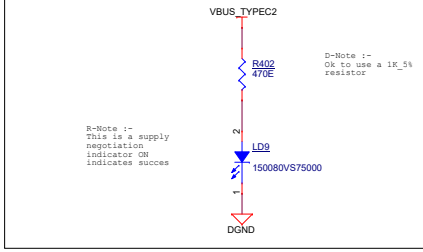
EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A



Note: Refer data sheet USB VBUS Design Guidelines section.



POWER INDICATION LED: VBUS_TYPEC2



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Title	USB0 TYPE-C DRP		
Size	PROC180E2		Rev
C			E2
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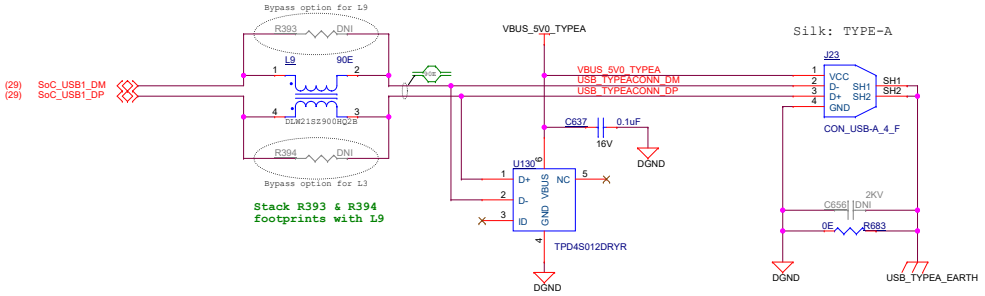
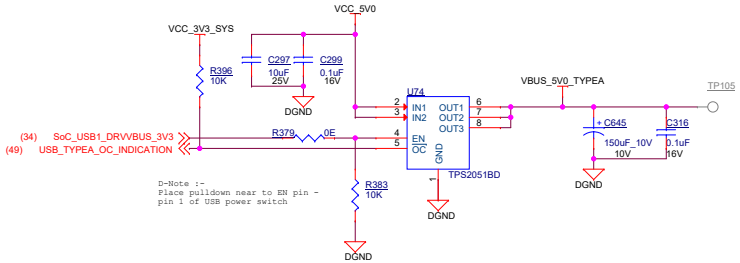
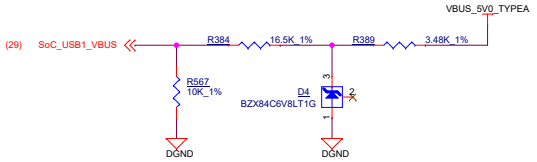
USB1 TYPE-A





Note: Refer data sheet USB VBUS Design Guidelines section.



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Title	USB1 TYPE-A		
Size	PROC180E2		Rev
C			E2
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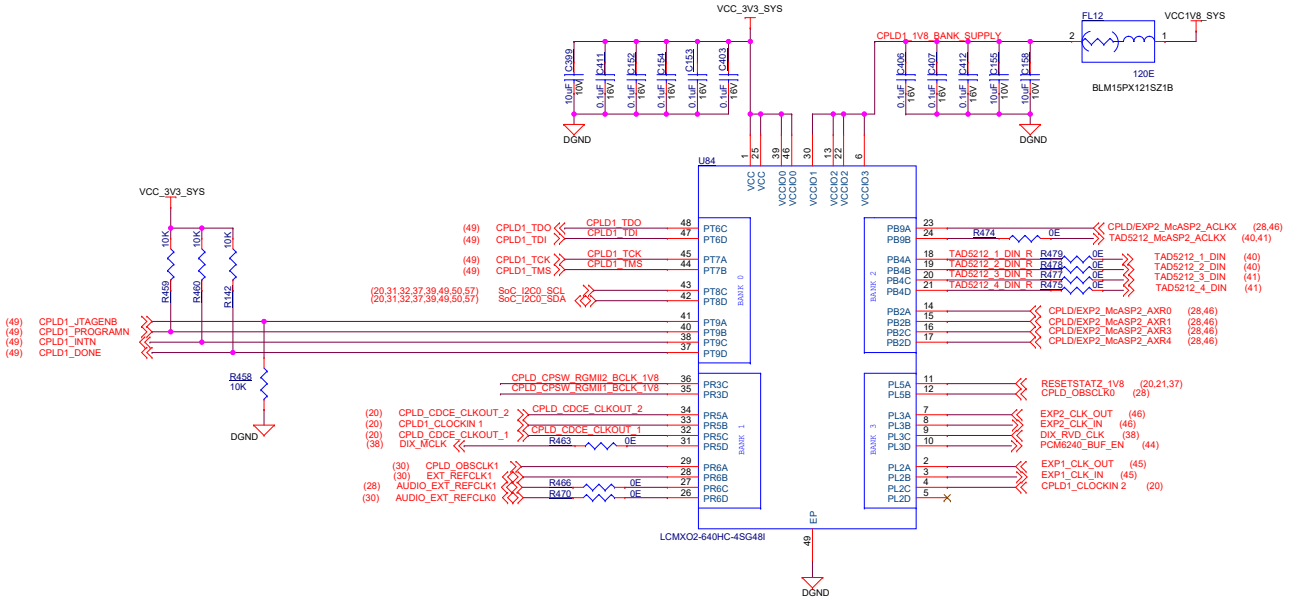
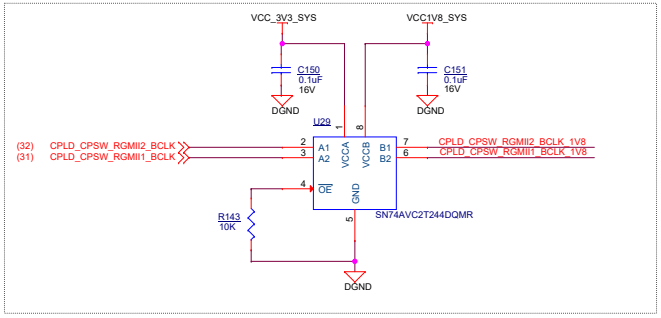
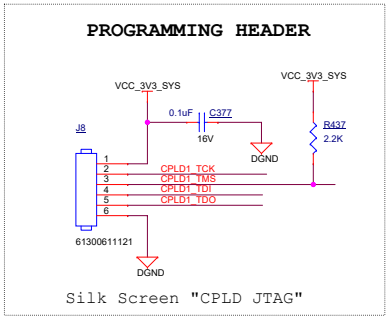
CPLD 1



CPLD 1 LEVEL TRANSLATOR



PROGRAMMING HEADER



Silk Screen "CPLD JTAG"

Designed for TI by Mistral Solutions Pvt Ltd

Title	CPLD 1		
Size	PROC180E2		Rev
C			E2
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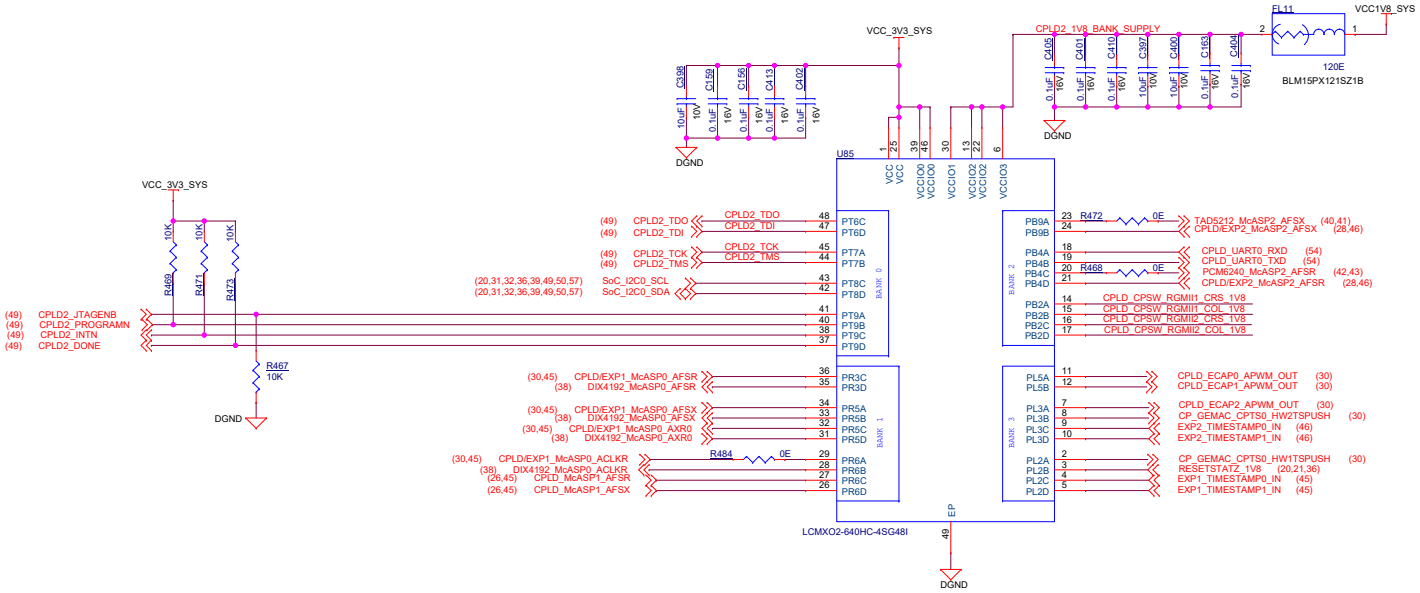
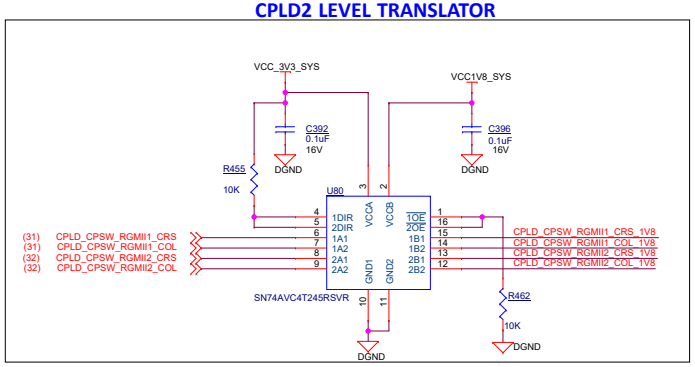
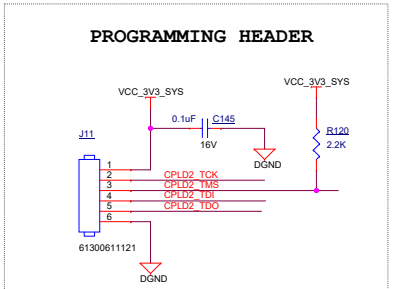
CPLD 2



CPLD2 LEVEL TRANSLATOR



PROGRAMMING HEADER



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Title	CPLD 2		
Size	PROC180E2		Rev
C			E2
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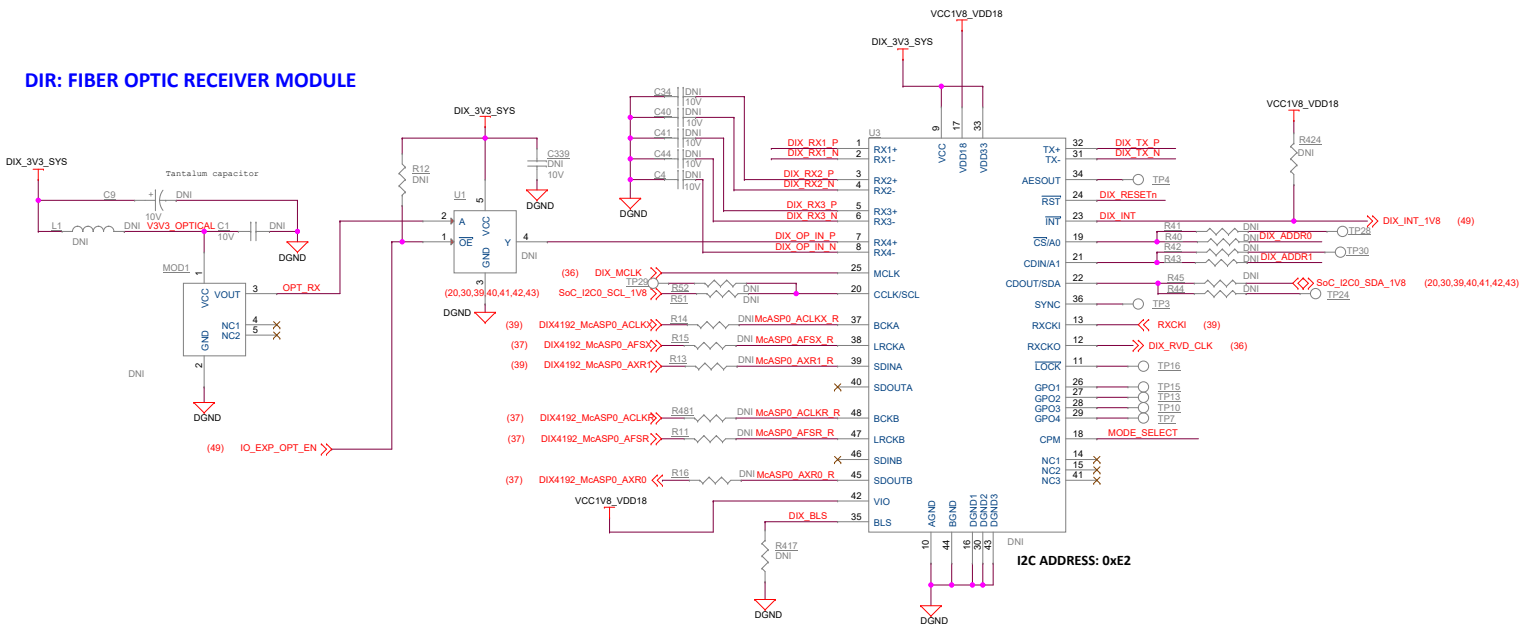
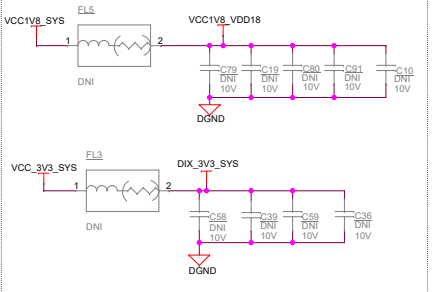
AUDIO - DIGITAL IN & OUT, OPTICAL IN -1

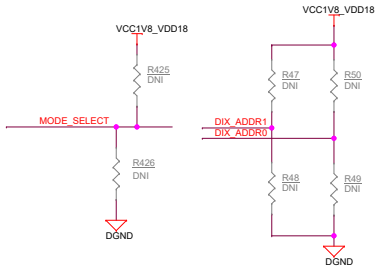
DIR: FIBER OPTIC RECEIVER MODULE



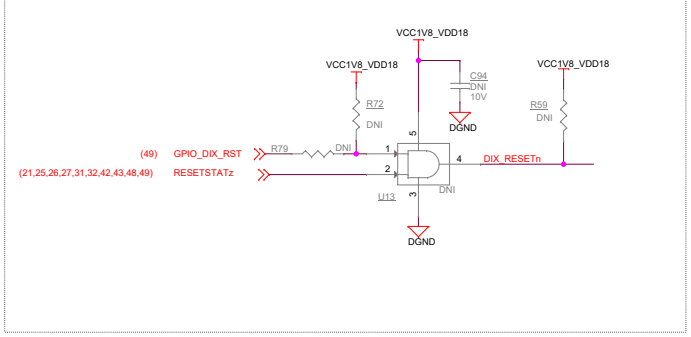
DIX Supply & Decaps



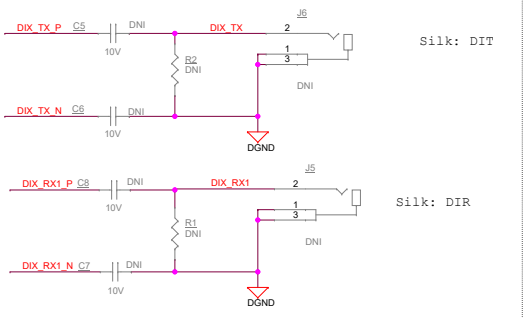
DEVICE STRAP



DIX4192 RESET



DIT & DIR COAXIAL INPUT



Designed for TI by Mistral Solutions Pvt Ltd

Title	AUDIO - DIGITAL IN & OUT, OPTICAL IN -1		
Size	PROC180E2		Rev
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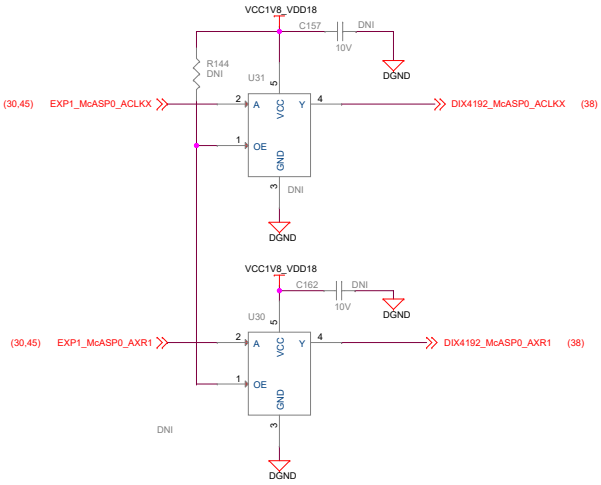
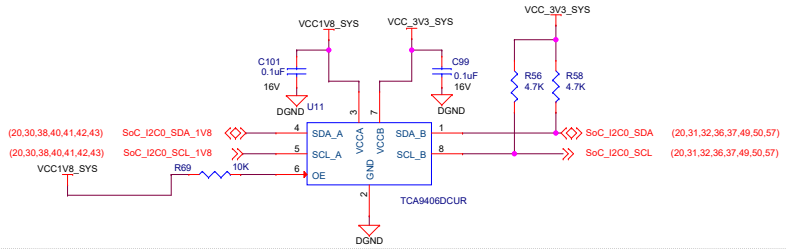
AUDIO - DIGITAL IN & OUT, OPTICAL IN - 2

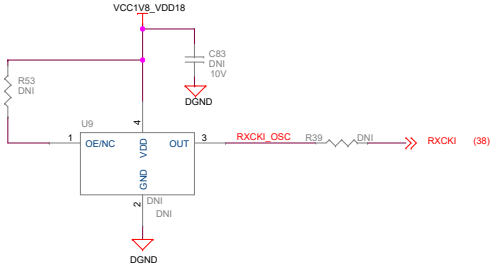
BUFFERS FOR DIX4192



I2C LEVEL TRANSLATOR



DIX4192 CLOCKING



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Title	AUDIO - DIGITAL IN & OUT, OPTICAL IN -2	
Size C	PROC180E2	Rev E2
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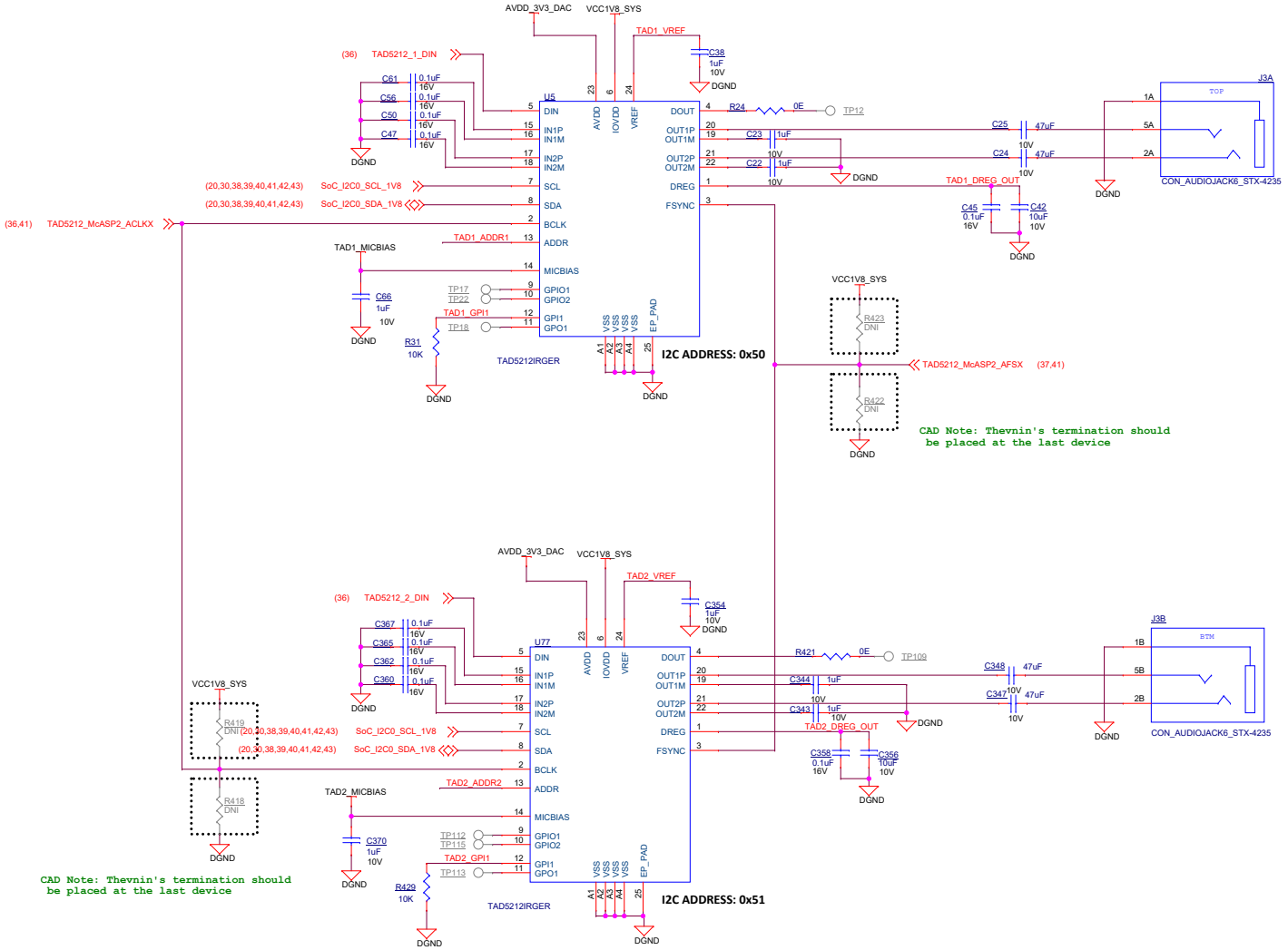
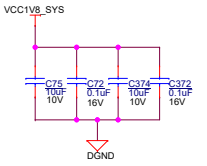
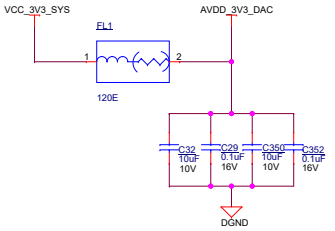
AUDIO - STEREO LINEOUT - 1



DAC Supply & Decaps

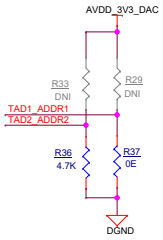


CAD Note: Place these decaps near the DVDD supply pin of DAC's



CAD Note: Place these decaps near the AVDD supply pin of DAC's

DAC I2C Address Straps



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Title	AUDIO - STEREO LINEOUT - 1		
Size	PROC180E2		Rev
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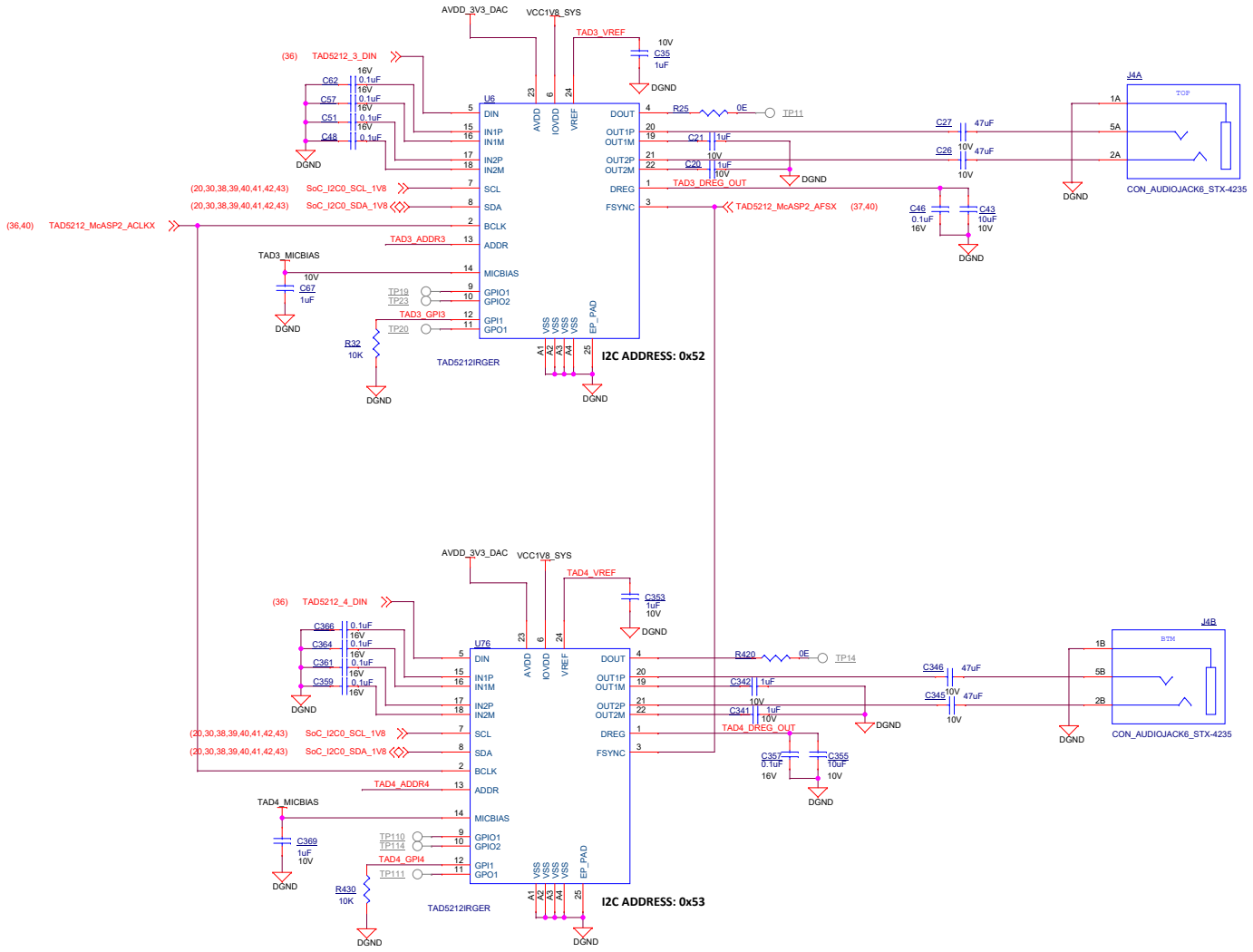
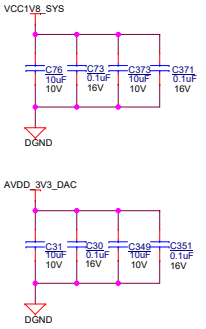
AUDIO - STEREO LINEOUT - 2

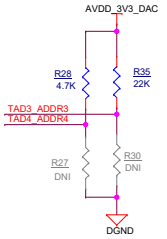


DAC Supply & Decaps



CAD Note: Place these decaps near the DVDD supply pin of DAC's

Device Straps



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Title	AUDIO - STEREO LINEOUT - 2		
Size C	PROC180E2		Rev E2
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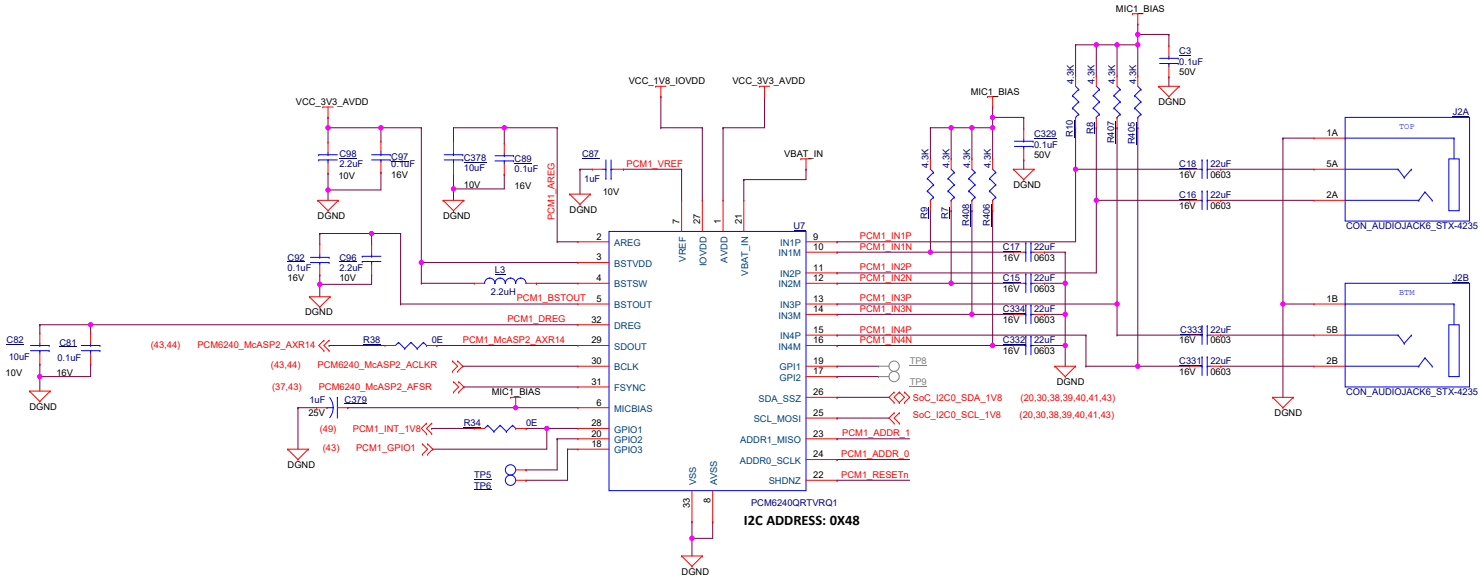
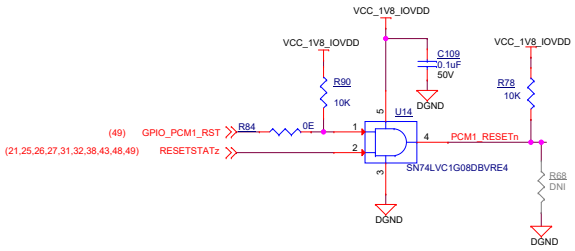
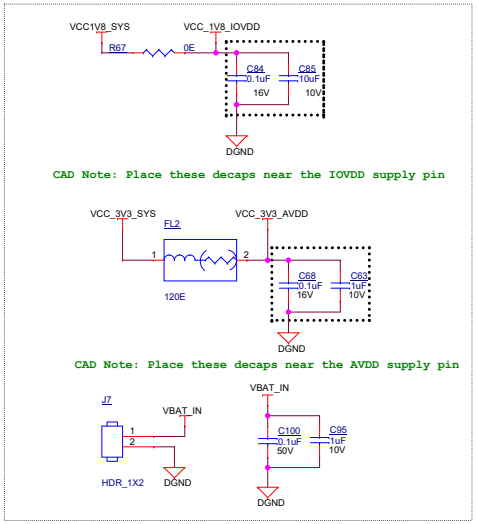
AUDIO - MICROPHONE/LINE IN 1



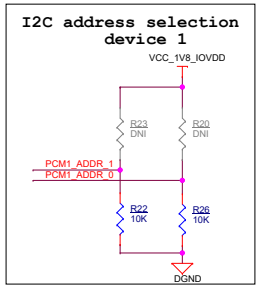
PCM1 RESET



ADC Supply & Decaps



I2C address selection device 1



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Title	AUDIO - MICROPHONE/LINE IN 1		
Size	PROC180E2		Rev
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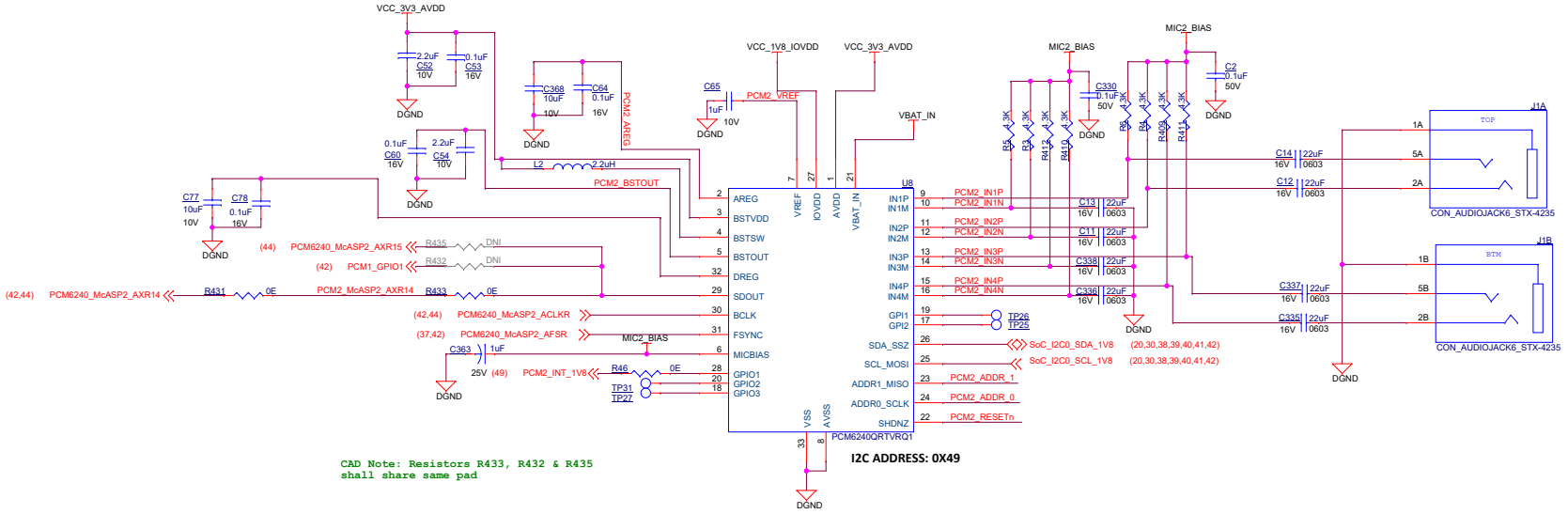
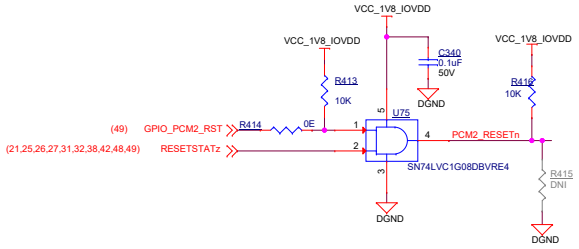
AUDIO - MICROPHONE/LINE IN 2



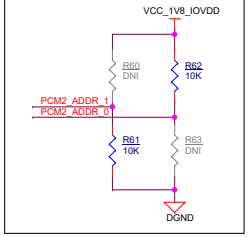
CAD Note: Resistors R433, R432 & R435 shall share same pad

I2C ADDRESS: 0X49

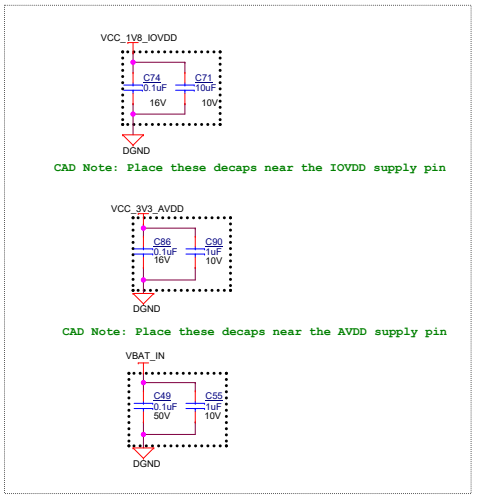
PCM2 RESET



I2C address selection device 2



ADC Supply & Decaps



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Title	AUDIO - MICROPHONE/LINE IN 2		
Size	PROC180E2		Rev
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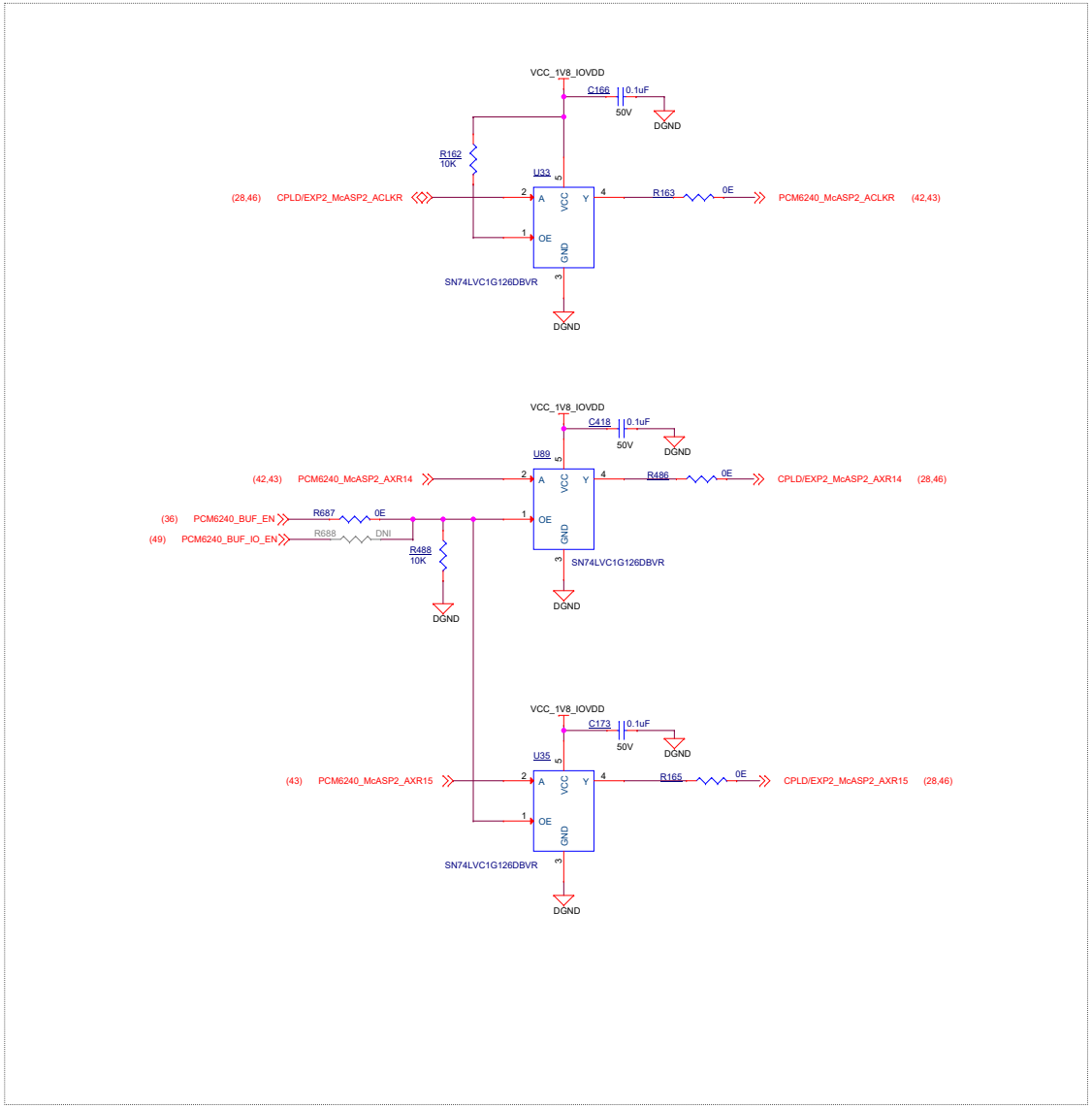
PCM6240 BUFFERS



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Title	PCM6240 BUFFERS	
Size C	PROC180E2	Rev E2
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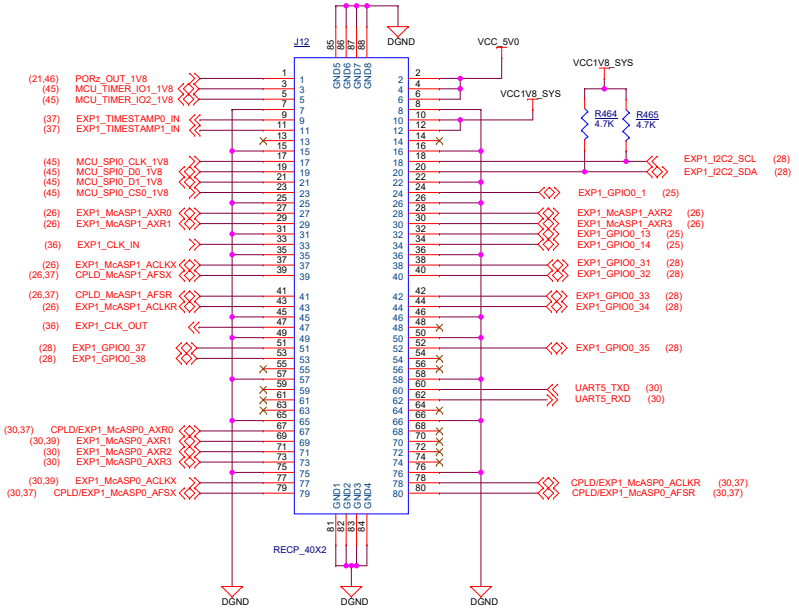
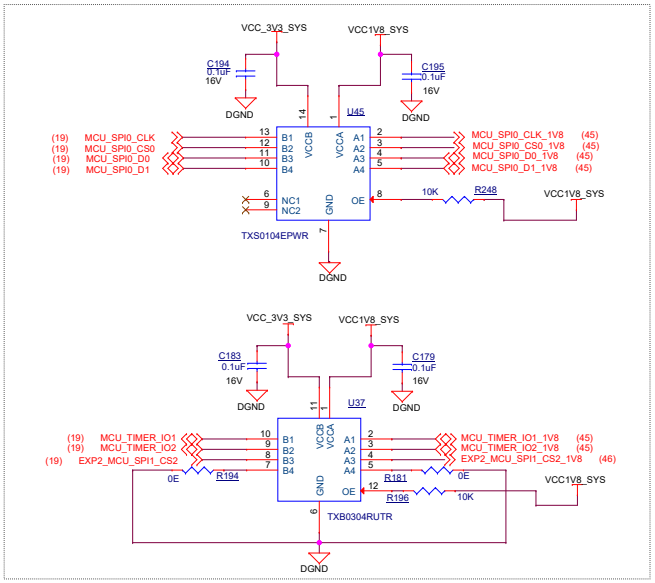
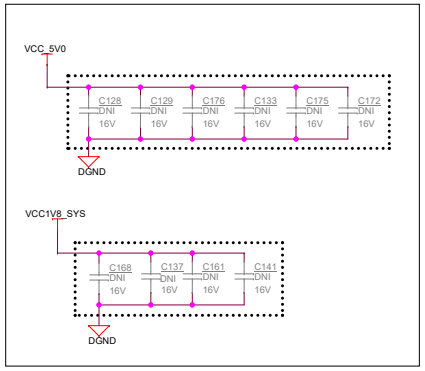
AUDIO EXPANSION CONNECTOR #1



AEC1 LEVEL TRANSLATORS



AUDIO EXPANSION DECAPS



Designed for TI by Mistral Solutions Pvt Ltd

Title	AUDIO EXPANSION CONNECTOR #1		
Size	PROC180E2		Rev
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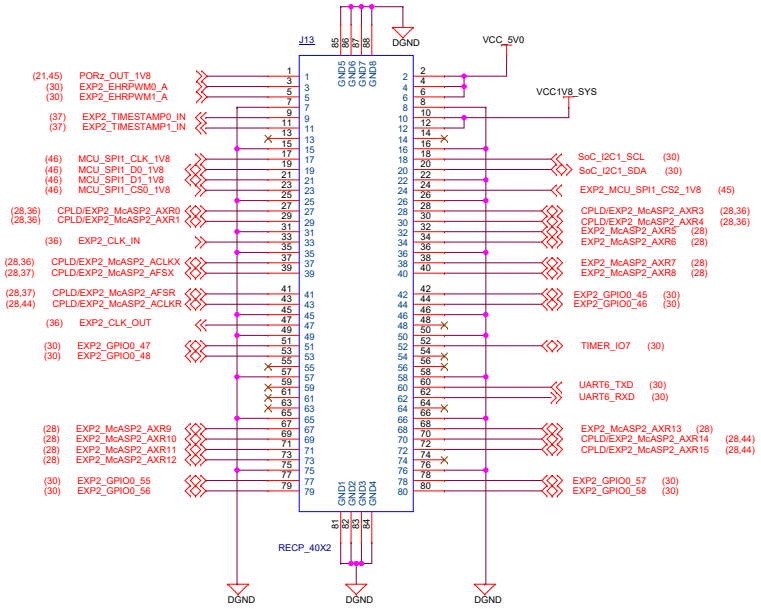
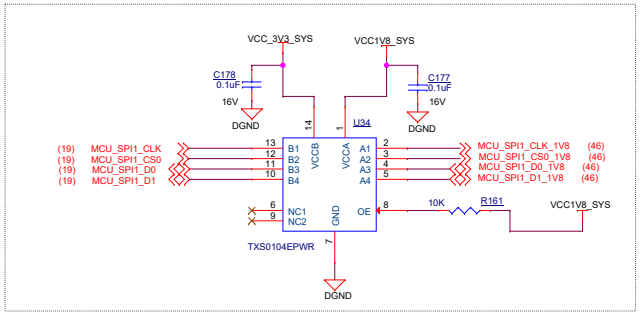
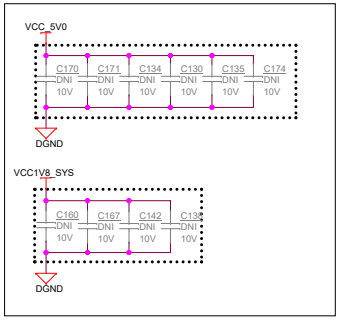
AUDIO EXPANSION CONNECTOR #2



AEC2 LEVEL TRANSLATOR



AUDIO EXPANSION DECAPS



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Title	AUDIO EXPANSION CONNECTOR #2		
Size	PROC180E2		Rev
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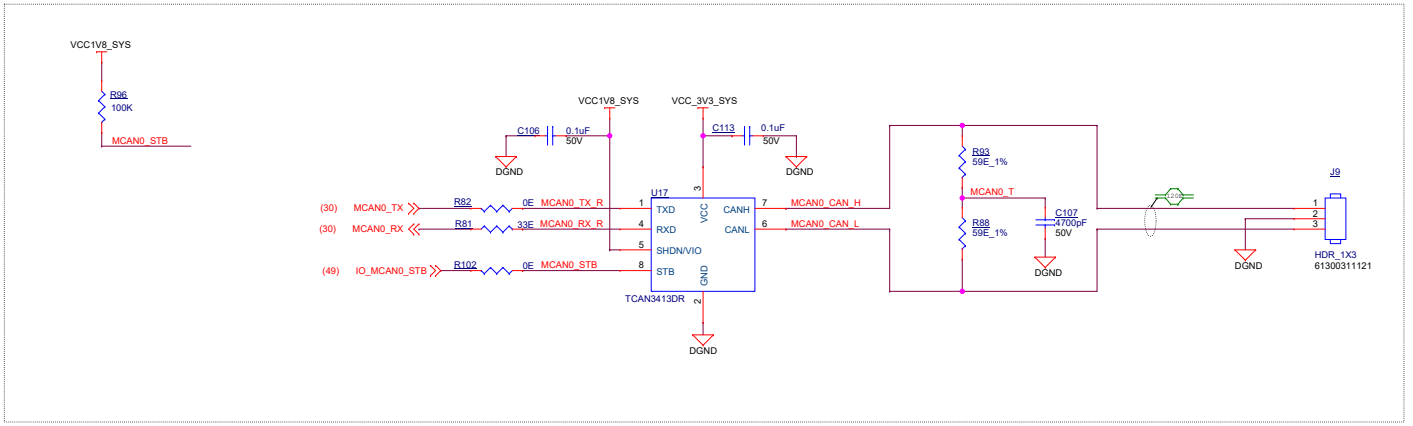
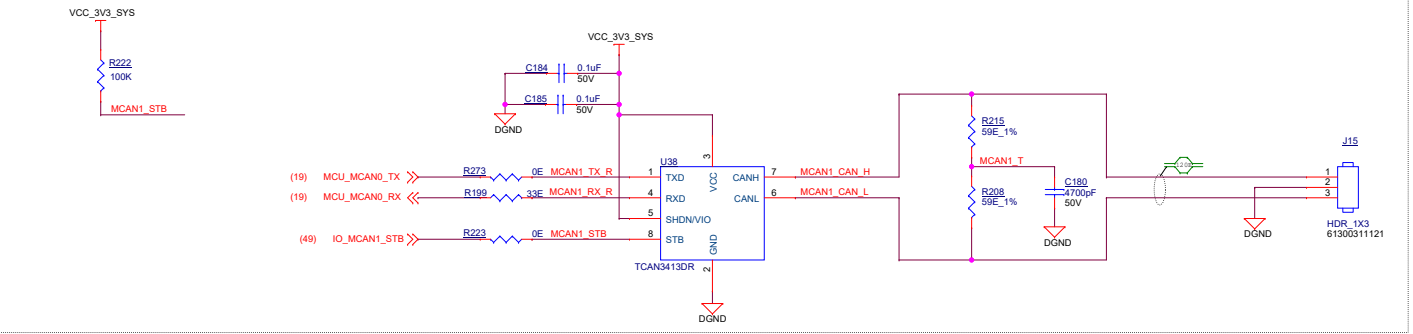
CAN TRANSCEIVER





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Title	CAN TRANSCEIVER		
Size	PROC180E2		Rev
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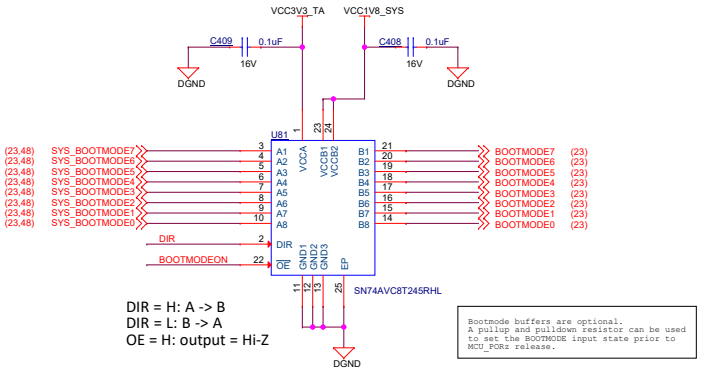
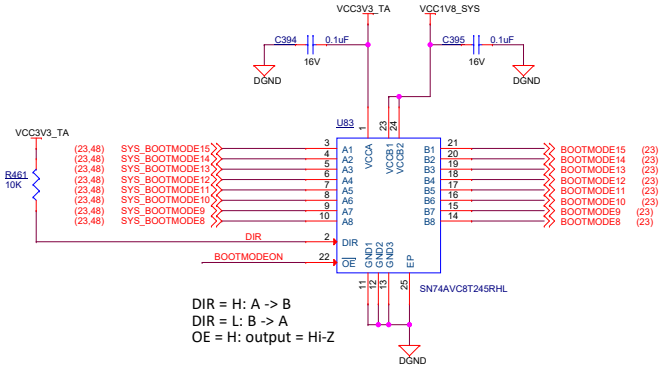
BOOTMODE BUFFERS AND IO EXPANDERS

BOOT MODE BUFFERS



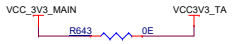
DIR = H: A -> B
DIR = L: B -> A
OE = H: output = Hi-Z

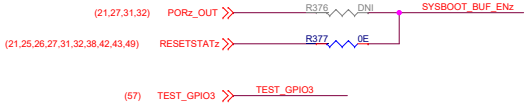
Bootmode buffers are optional.
A pullup and pulldown resistor can be used to set the BOOTMODE input state prior to MCU_PORz release.

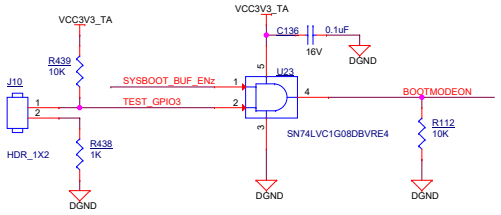


DIR = H: A -> B
DIR = L: B -> A
OE = H: output = Hi-Z

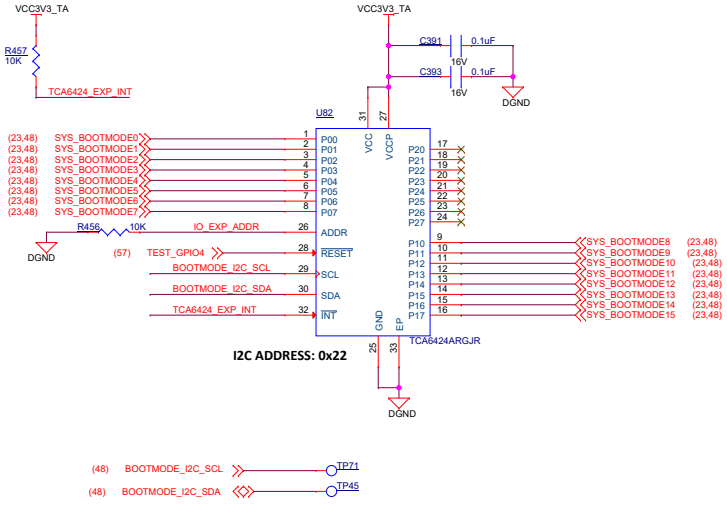
TEST AUTOMATION SUPPLY



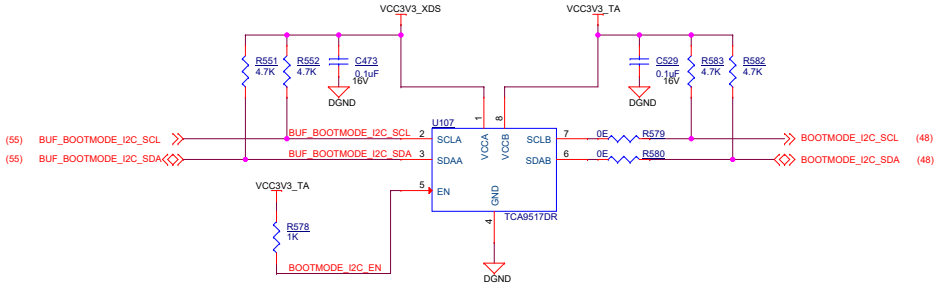




BOOTMODE IO EXPANDER



BOOTMODE I2C BUS BUFFER



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Title	BOOT MODE BUFFER & IO EXPANDERS		
Size	PROC180E2		Rev
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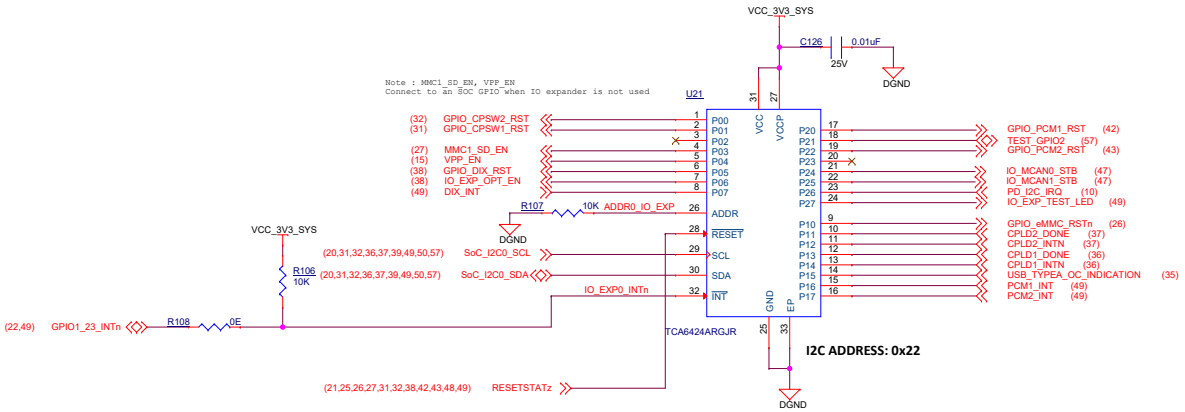
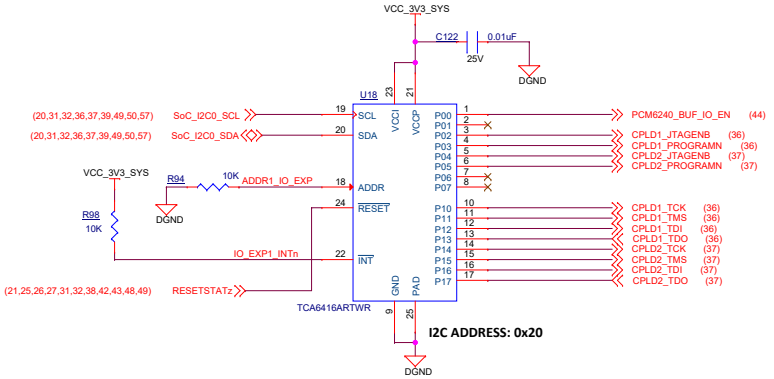
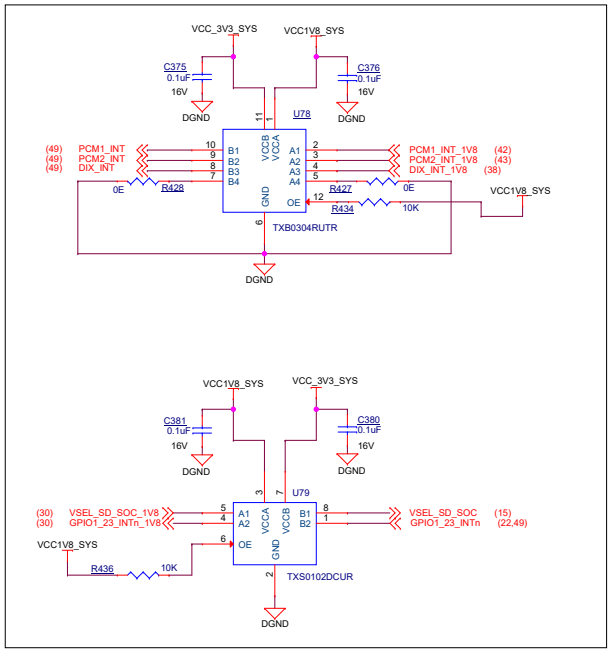
IO EXPANDER

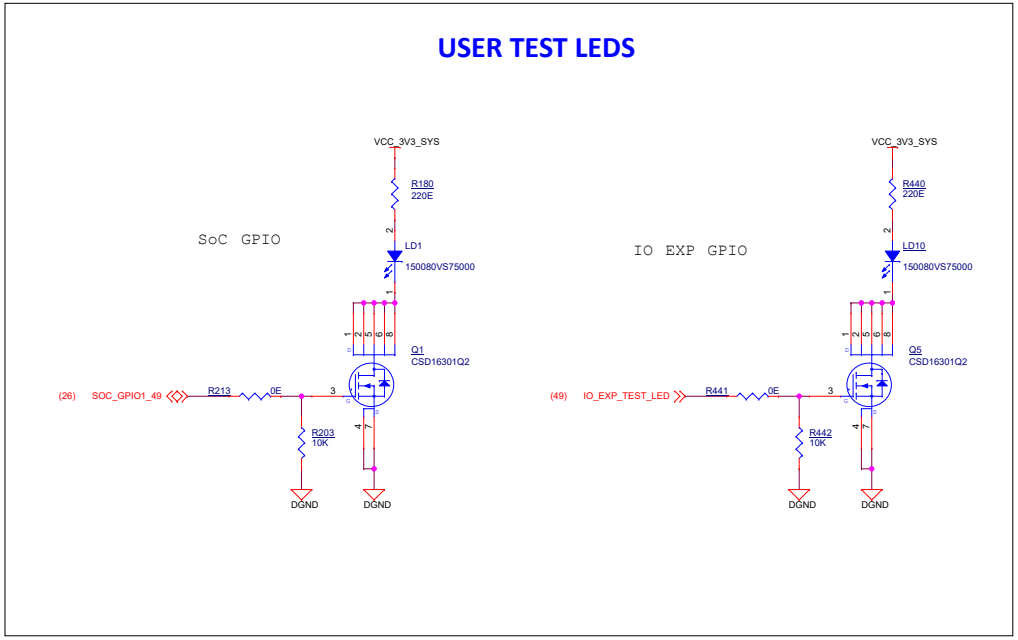




LEVEL TRANSLATOR



USER TEST LEDS



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Title	IO EXPANDER & USER TEST LEDS		
Size	PROC180E2		Rev
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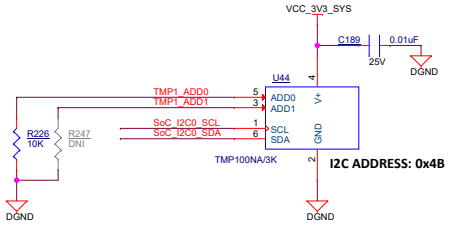
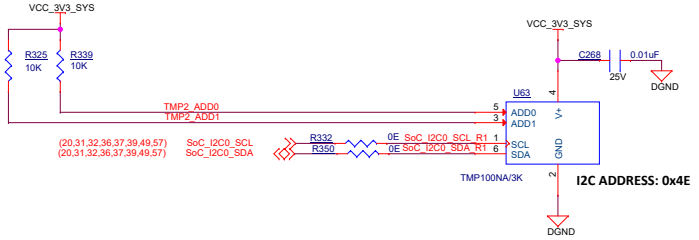
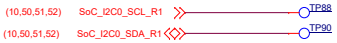
TEMPERATURE SENSORS



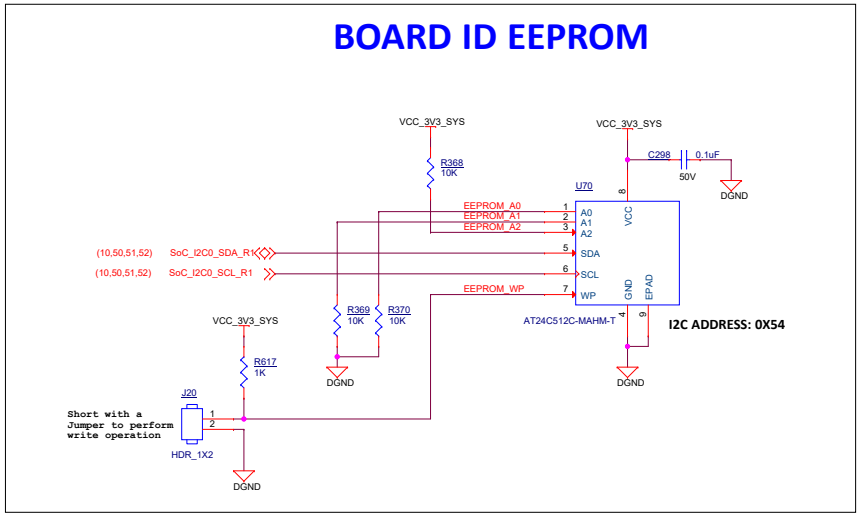
CAD NOTE: PLACE CLOSE TO SoC



CAD NOTE: PLACE CLOSE TO LPDDR4



BOARD ID EEPROM



PROC180E2

Designed for TI by Mistral Solutions Pvt Ltd

Title	TEMPERATURE SENSORS & BOARD ID EEPROM	
Size C	PROC180E1	Rev E2
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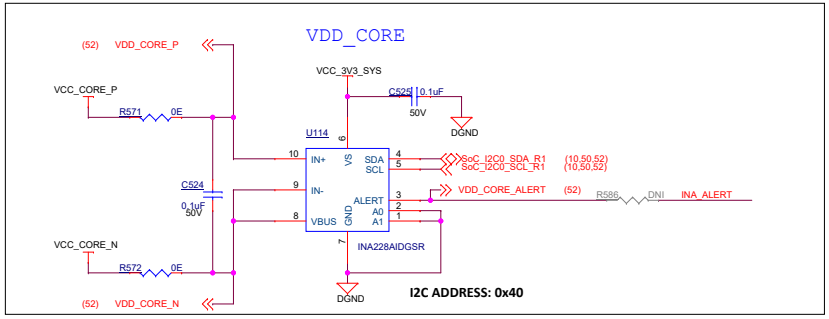
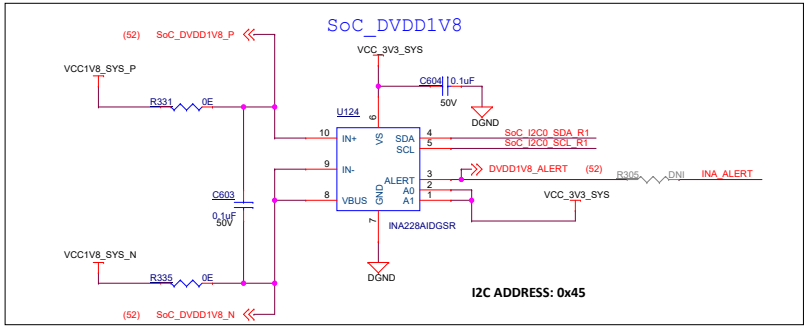
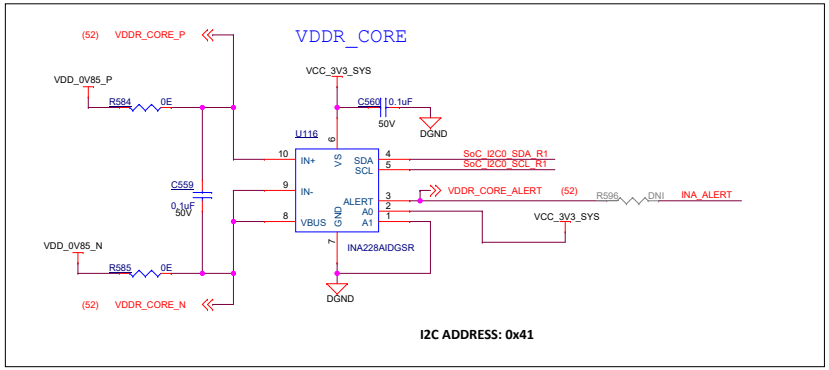
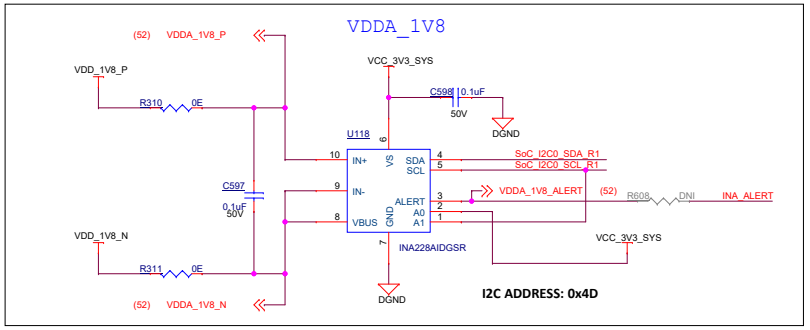
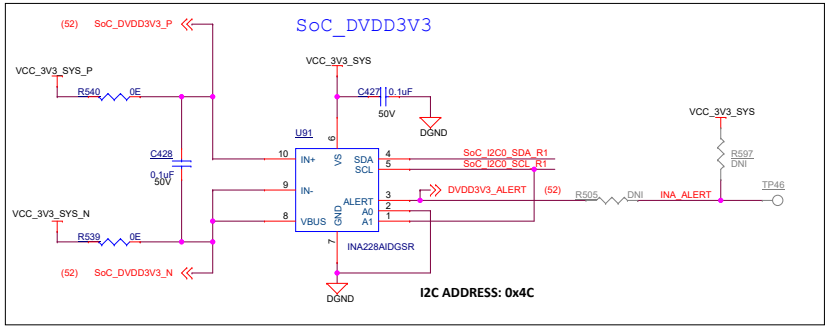
CURRENT MONITORING DEVICES - 1

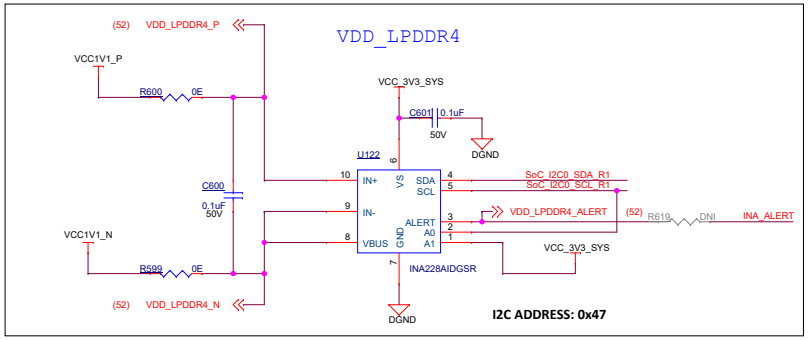












Note: The design supports current/voltage measurements using either INA228 or INA231. (Implemented via stacked PCB footprint).

INA I2C SLAVE ADDRESS

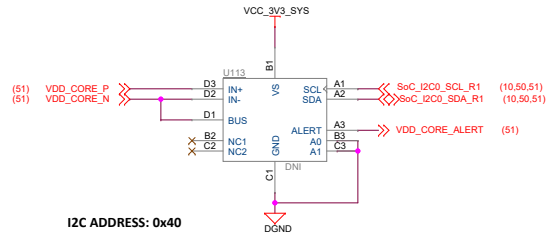
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

Designed for TI by Mistral Solutions Pvt Ltd

Title	CURRENT MONITORING DEVICES - 1	
Size C	PROC180E2_SCH	Rev E2
Date: Friday, June 06, 2025	Sheet 51 of 59	

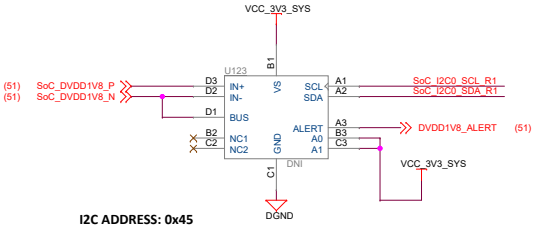
CURRENT MONITORING DEVICES - 1

VDD_CORE



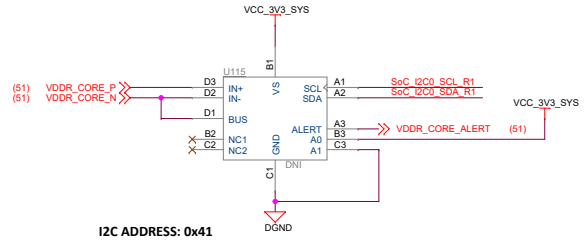
I2C ADDRESS: 0x40

SoC_DVDD1V8



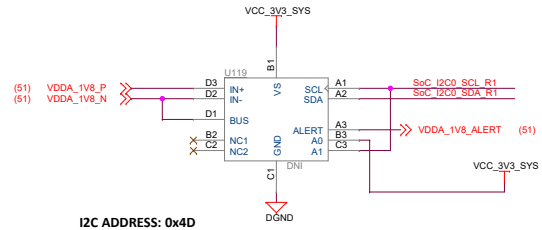
I2C ADDRESS: 0x45

VDDR_CORE



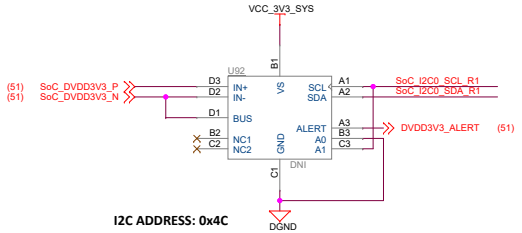
I2C ADDRESS: 0x41

VDDA_1V8



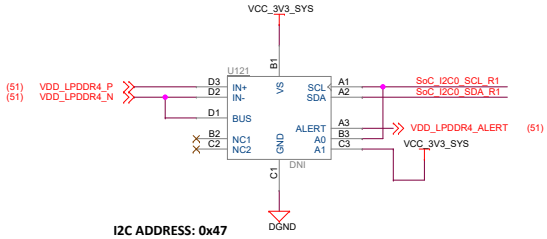
I2C ADDRESS: 0x4D

SoC_DVDD3V3



I2C ADDRESS: 0x4C

VDD_LPDDR4



I2C ADDRESS: 0x47

Note: The design supports current/voltage measurements using either INA228 or INA231. (Implemented via stacked PCB footprint).

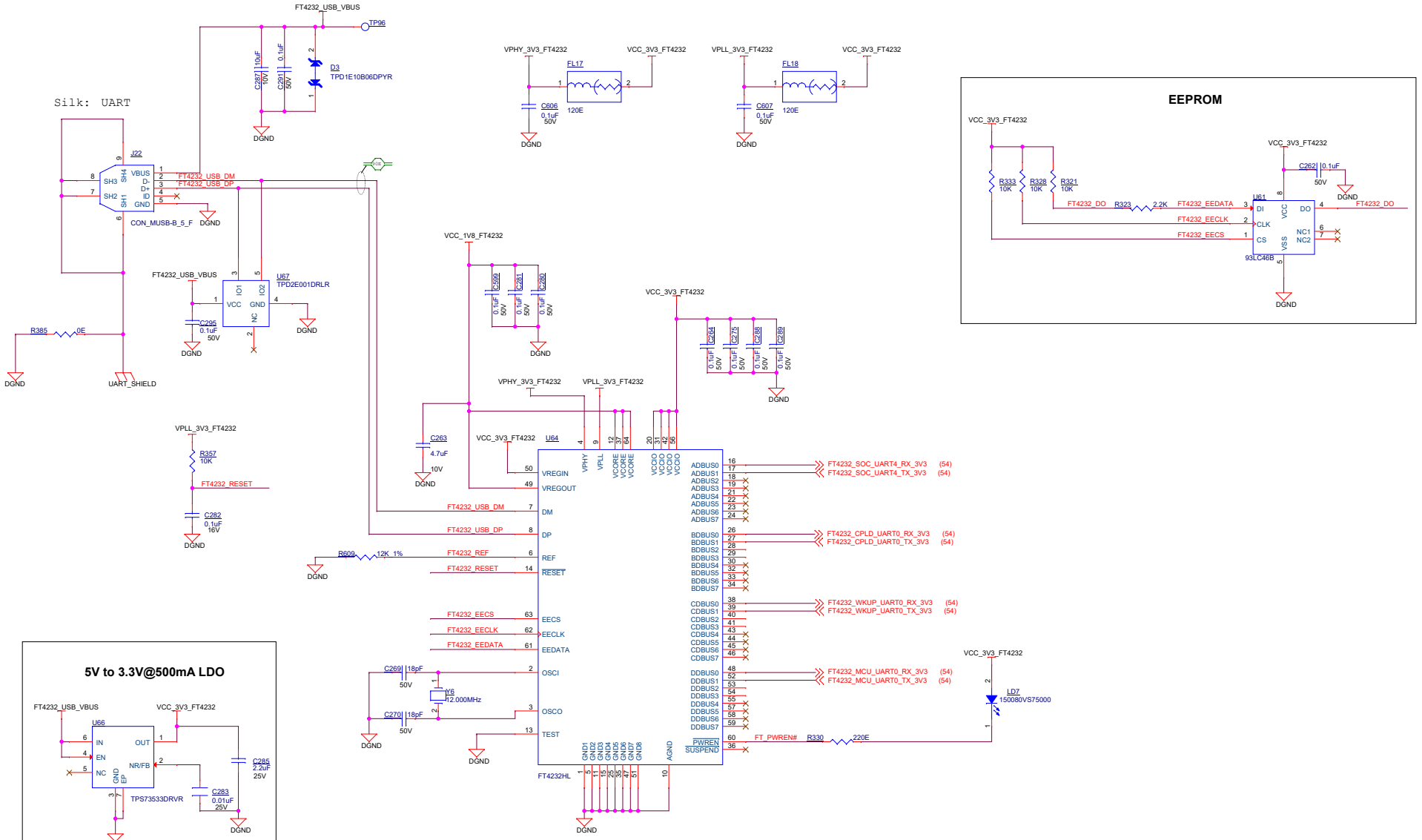
INA I2C SLAVE ADDRESS

POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

Designed for TI by Mistral Solutions Pvt Ltd

Title	CURRENT MONITORING DEVICES - 2	
Size C	PROC180E2_SCH	Rev E2
Date: Friday, June 06, 2025	Sheet 52 of 59	

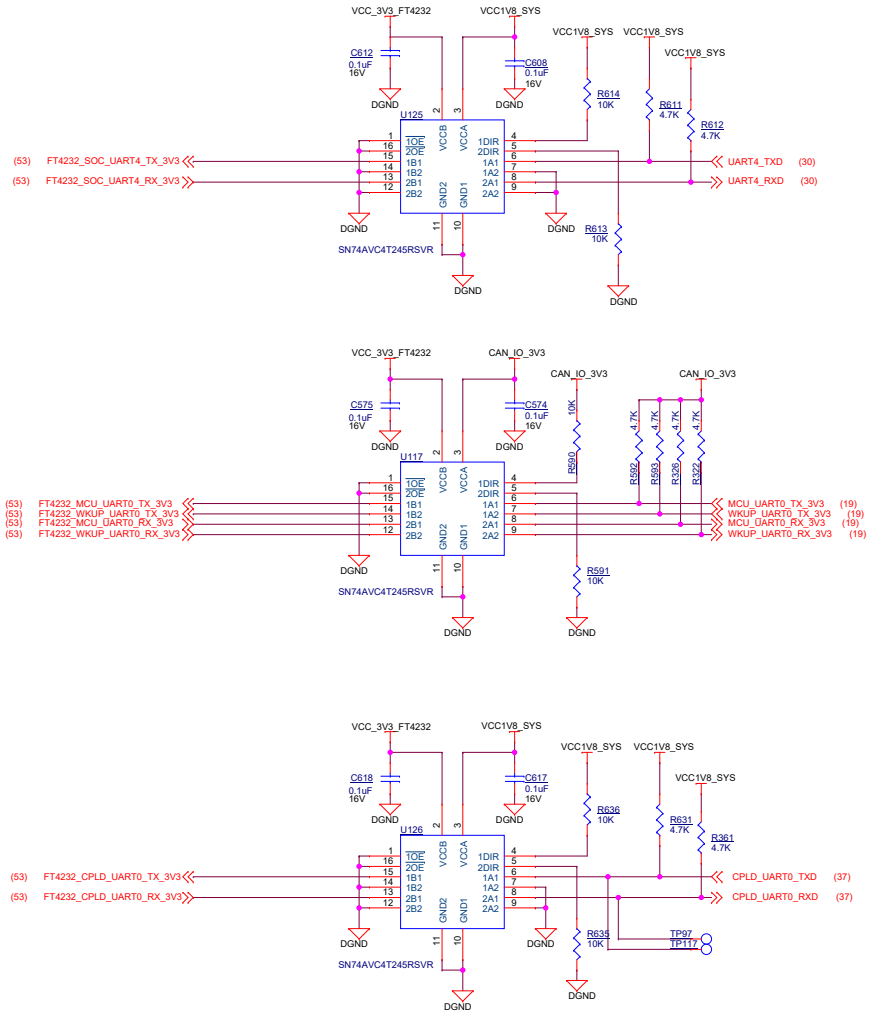
USB TO UART BRIDGE



Designed for TI by Mistral Solutions Pvt Ltd

Title	FT4232 UART TO USB BRIDGE	
Size C	PROC180E2	Rev E2
Date: Friday, June 06, 2025	Sheet 53 of 59	

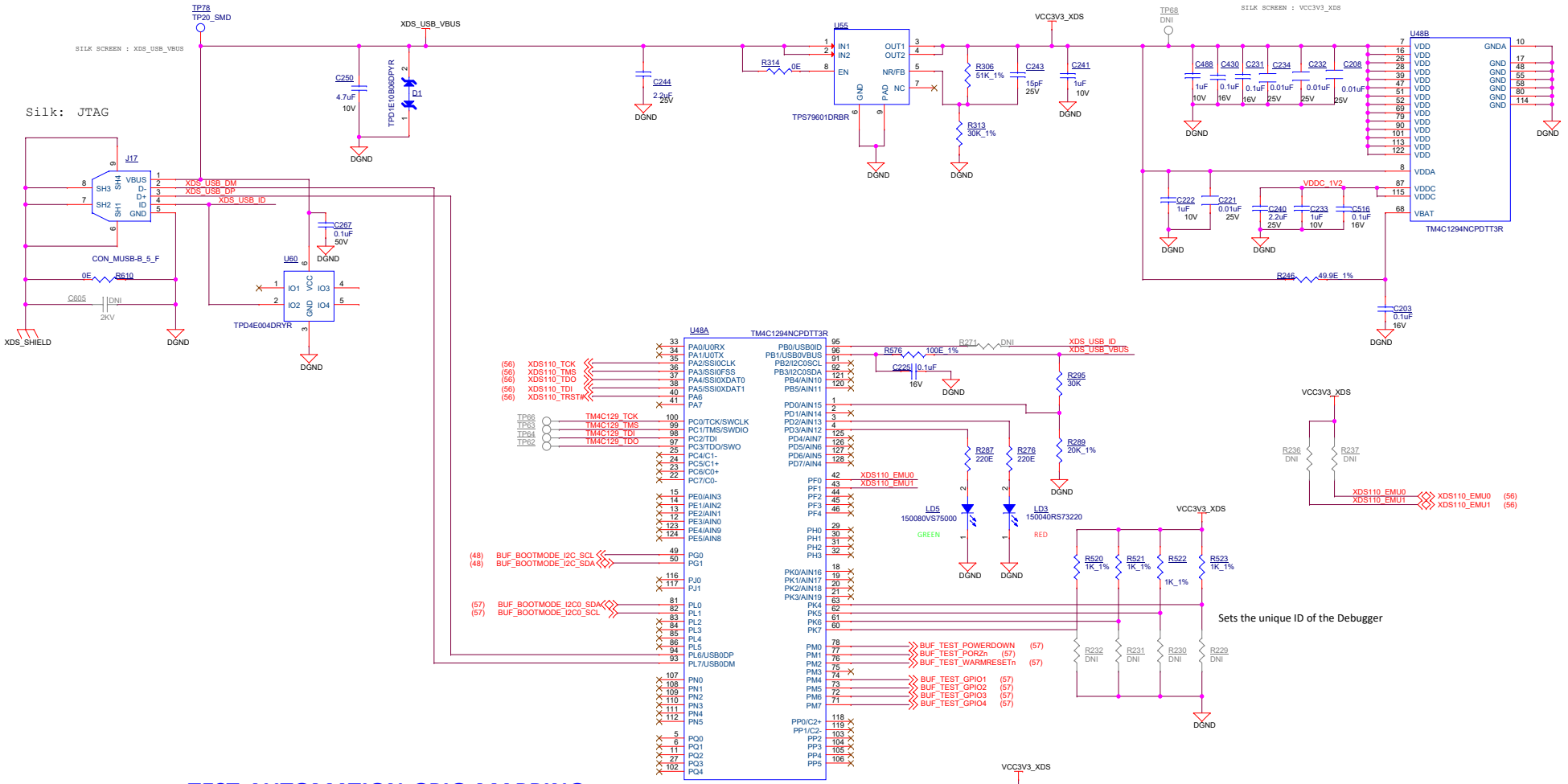
FT4232 UART BUFFERS



Designed for TI by Mistral Solutions Pvt Ltd

Title	FT4232 UART BUFFERS		
Size	PROC180E2		Rev
C			E2
Date:	Friday, June 06, 2025	Sheet 54 of 59	

XDS110 DEBUGGER



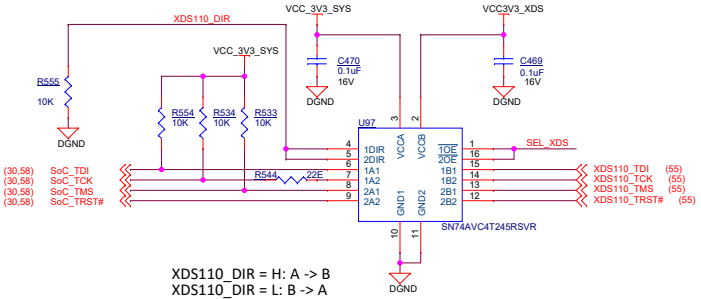
TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SOC_GPIO0_60 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

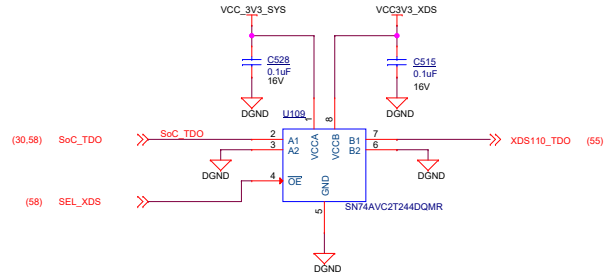
Designed for TI by Mistral Solutions Pvt Ltd

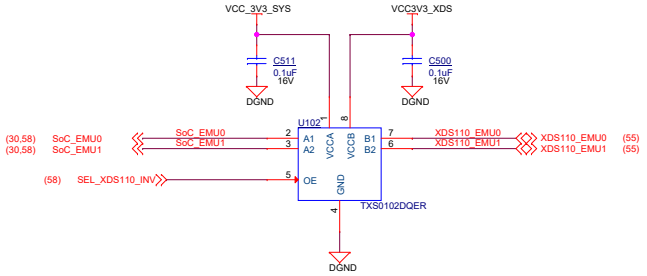
Title	XDS110 DEBUGGER	
Size C	PROC180E2	Rev E2
Date: Friday, June 06, 2025	Sheet 55 of 59	

XDS110 JTAG BUFFER



XDS110_DIR = H: A -> B
XDS110_DIR = L: B -> A
OE = H: output = Hi-Z

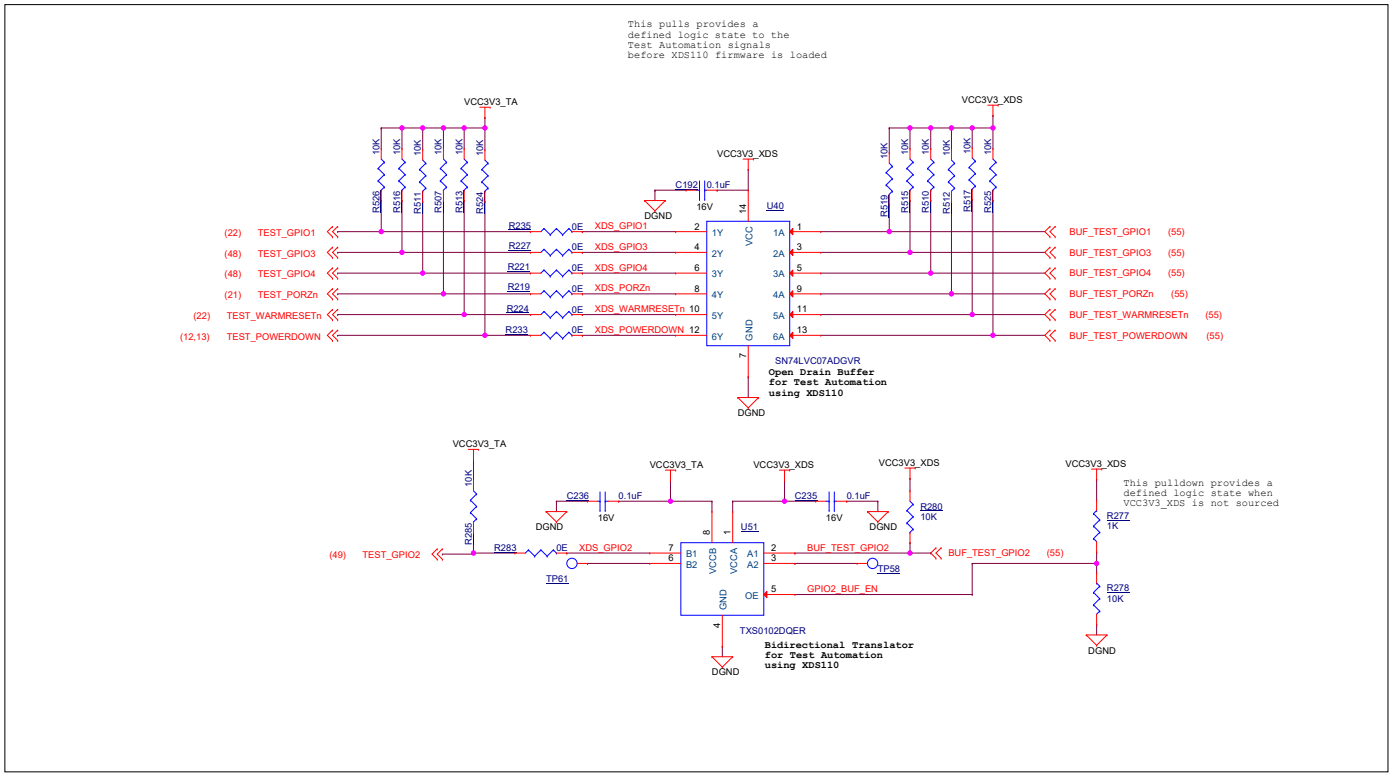




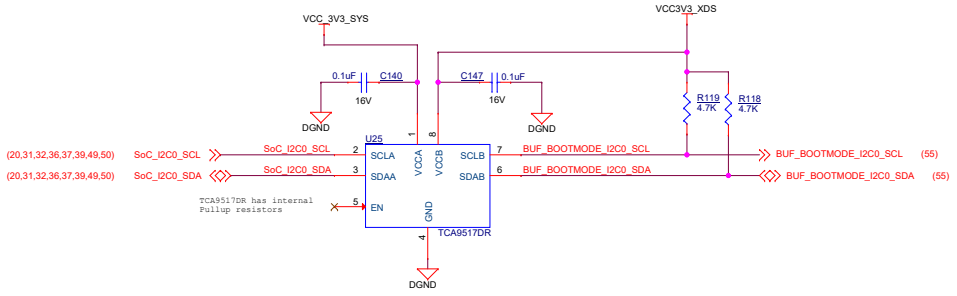
Designed for TI by Mistral Solutions Pvt Ltd

Title	XDS110 JTAG BUFFER	
Size: C	PROC180E2	Rev: E2
Date: Friday, June 06, 2025	Sheet 56 of 59	

XDS110 TEST AUTOMATION BUFFERS



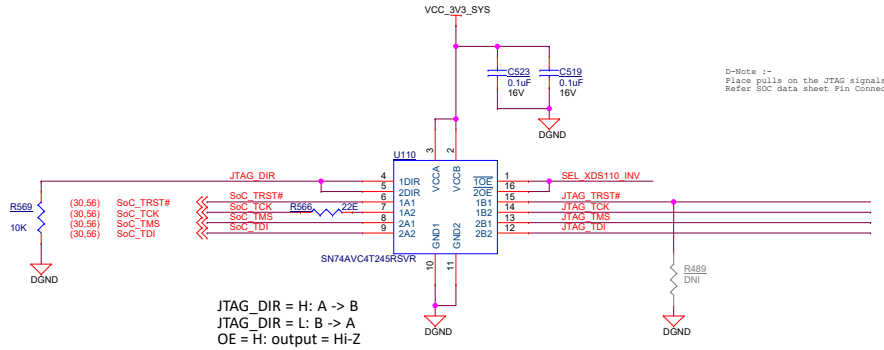
SOC I2C BUS BUFFER



Designed for TI by Mistral Solutions Pvt Ltd

Title	XDS110 TEST AUTOMATION BUFFERS		
Size	PROC180E2		Rev
C			E2
Date:	Friday, June 06, 2025	Sheet 57 of 59	

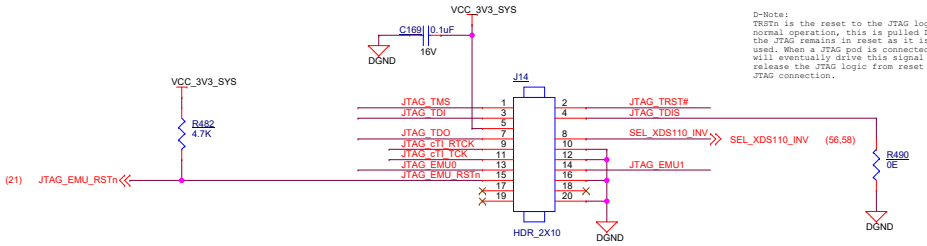
JTAG2 BUFFERS



D-Note :-
Place pulls on the JTAG signals near to the SOC
Refer SOC data sheet Pin Connectivity Requirements section

D-Note :-
Add an external ESD protection to provide system level ESD protection when external connector is used for debug
Add Test points and ESD protection when JTAG connector is not used

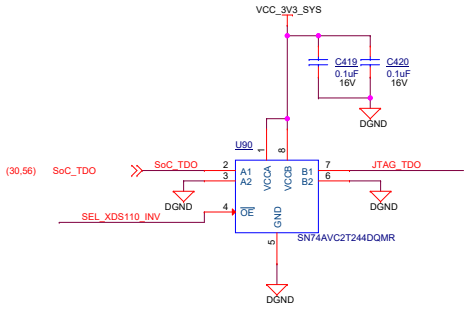
cTI20 JTAG CONNECTOR



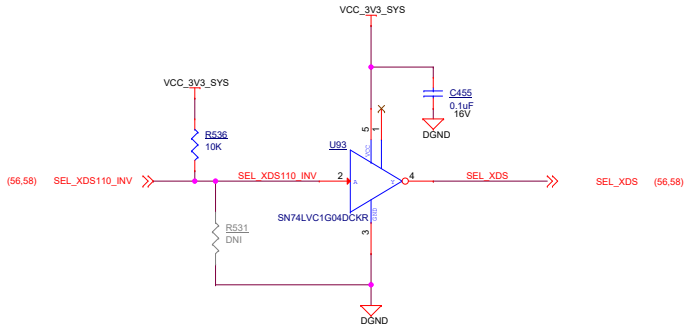
D-Note:
TRSTn is the reset to the JTAG logic. For normal operation, this is pulled LOW, and thus the JTAG remains in reset as it is not being used. When a JTAG pod is connected, the pod will eventually drive this signal HIGH to release the JTAG logic from reset and enable a JTAG connection.

Silk: cTI

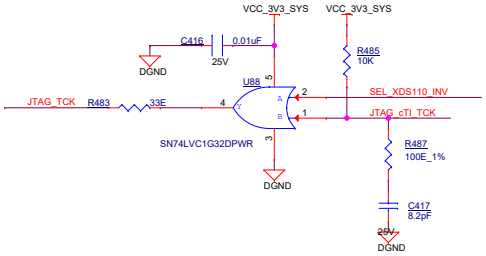
Add an external ESD protection to provide system level ESD protection

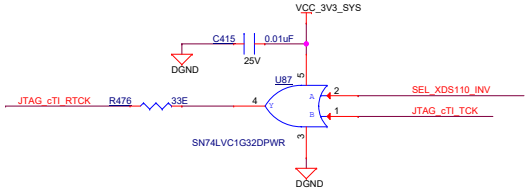


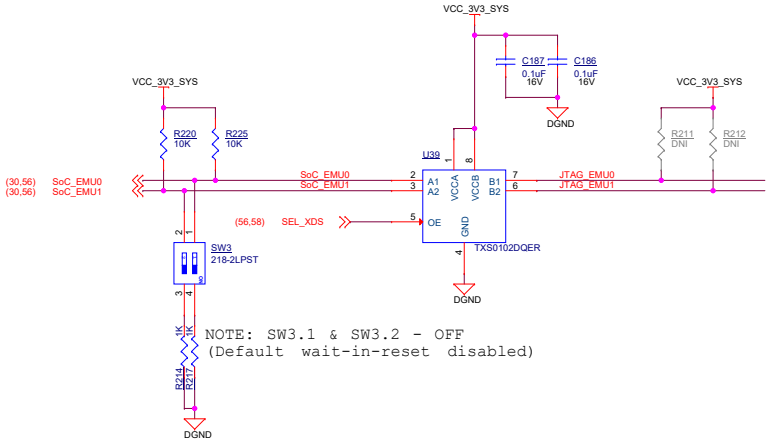
CAD NOTE: Buffers U110 and U90 need to be placed closer to the cTI-20pin connector J19 to reduce Stub length of the JTAG signals.



JTAG2 CLOCK BUFFER







NOTE: SW3.1 & SW3.2 - OFF
(Default wait-in-reset disabled)

Designed for TI by Mistral Solutions Pvt Ltd

Title	JTAG 20 PIN cTI CONNECTOR	
Size C	PROC180E2	Rev E2
Date: Friday, June 06, 2025	Sheet 58 of 59	

MOUNTING HARDWARE

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

BARE PCB

PROC180

PROC180E2

LOGOs

PCB LOGO DNI — Texas Intruments

PCB LOGO DNI — For Evaluation only; not FCC approved for resale

PCB LOGO DNI — WEEE Mark

PCB LOGO DNI — CE Mark

AM62D SOCKET

ACC1

DNI

JUMPERS

ACC2 DNI

ACC3 DNI

FIDUCIALS

FID1 DNI

FID2 DNI

FID3 DNI

FID4 DNI

FID5 DNI

FID6 DNI

LABELS

Board Serial No.

LBL1 PCB LABEL DNI

Assembly Revision

LBL2 PCB LABEL DNI

EVM Orderable No.

LBL3 PCB LABEL DNI

Orderable Part Numbers

Variant	Label Text
001	AUDIO-AM62D-EVM

Designed for TI by Mistral Solutions Pvt Ltd

Title	MOUNTING HARDWARE	
Size C	PROC180E2	Rev E2
Date: Friday, June 06, 2025	Sheet 59 of 59	