Application Report
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System-Level ESD Design Guidelines for FPD-Link Serializers and Deserializers

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ABSTRACT

This application note describes system-design guidelines that should aid in increasing the system level ESD performance of FPD-Link products in a system.

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1 Introduction

This application note describes the best practices that should be used in PCB layout for testing IEC 61000-4-2 on systems using FPD-Link products. Also included in this application note are suggested additions of external components to shunt or decrease severity of the ESD charge. The majority of the protection should come from shielding of the system as a whole. The key is to keep ground reference as stable as possible and at the same potential throughout the whole system.

2 System-Level ESD PCB Guidelines and Recommendations

- Do not have any floating metal on the PCB or near the PCB. Check for floating metal on the PCB and stitch it to the ground plane with multiple vias, or remove the floating metal.
- PCB stackup:
  - At minimum, a four-layer construction is recommended (see Figure 1).
    1. Top
    2. Ground or power plane
    3. Power or ground plane
    4. Bottom

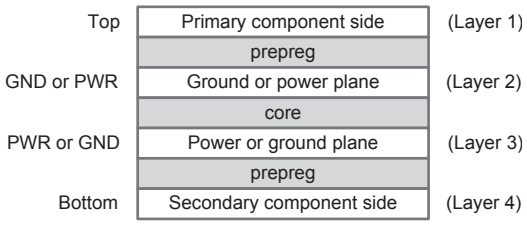
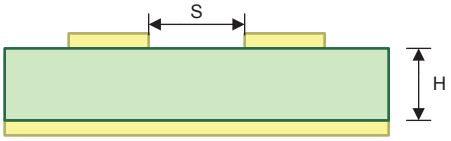


Figure 1. Example of Four-Layer PCB Construction

  - Do not cut up the power or ground plane, if possible; if it is not possible, minimize use of power and ground islands. Use a ground guard when separating power planes.
  - Keep power and ground plane surface areas equal in size and shape. Keep power and ground shapes on top of each other to create board capacitance.

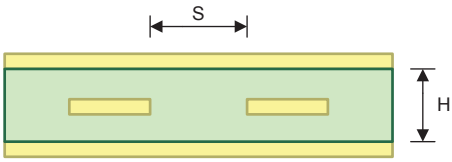
- FPD-Link III high-speed differential traces:
  - Traces should be 100-Ω (±5%) differential impedance of differential microstrip or differential stripline (see Figure 2, Figure 3, and Figure 4).



Differential Microstrip

$$Z_{diff} = 2 \times Z_0 \times \left[1 - 0.48 \times e^{-0.96 \times \frac{S}{H}}\right]$$

Figure 2. Edge Coupled Differential Microstrip



Differential Stripline

$$Z_{diff} = 2 \times Z_0 \times \left[1 - 0.347e^{-2.9 \times \frac{S}{H}}\right]$$

Figure 3. Edge Coupled Differential Stripline

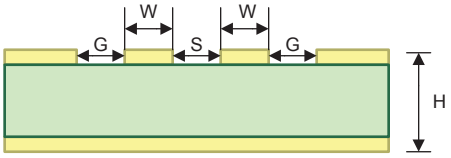


Figure 4. Coplanar Coupled Microstrips

  - Minimize snaking of differential traces. Keep differential pairs closely coupled to each other.
  - Keep differential pair skews to ±30 ps, but do not snake one side of the differential pair to match skew.
  - Place high-speed differential traces on an inner layer on long runs. For example, in a four-layer PCB construction, the high-speed differential trace can be on layer two or layer three. The high-speed vias should be constructed with controlled impedance. With the help of a 3D electromagnetic field solver, it is possible to design a via structure with controlled impedance.
  - Do not layout high-speed differential traces on the edge of the PCB.
  - Use ground guards with plenty of stitching to protect the differential traces on the outer layer (top or bottom).
  - Do not run high-speed differential traces near the edge of the PCB.
  - Use common-mode choke near 0.1-µF AC capacitors (for example, Murata DLW21SN900HQ2L).

- Power connections must be as short as possible and go immediately to the power plane. Power connections must not be made with controlled impedance traces. Each power or ground lead of a high-speed device must be connected to the PCB through a low-inductance path. For best results, one or more vias should be used to connect a power pin or ground pin to the nearby plane. Ideally, place vias immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance. Minimize use of power trace connections. If using a short trace, do not make trace a controlled impedance trace; TI recommends making a connection with the largest connection area (see Figure 5).

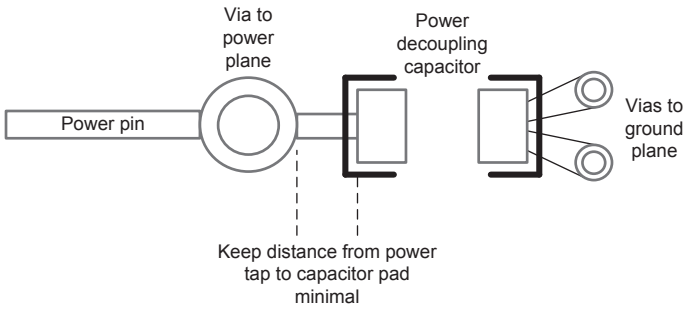


Figure 5. Example of Power Connection and Decoupling Layout Placement

- Ground connections:
  - Must be as short as possible and go immediately to the ground plane. Minimize use of ground trace connections. Ground connections must not be made with controlled impedance traces.
  - Use at least two vias per ground connections.
  - For optimal signal integrity, connect the cable shield to ground on both sender and receiver. For limiting the high DC currents possible in case of a ground loss, a filter can be used at the risk of bit errors. This risk can be mitigated by dimensioning the filter so the frequency determined by the used data rate of the FPD-Link the filter acts a hard ground.

NOTE: For direct GND connections, the traces and vias must be sized appropriately to handle the worst-case current.

- Use decoupling capacitors with low effective series resistance (ESR) and effective series inductance (ESL) to decouple the IC power from the rest of the supply system. Add at least an additional 10-µF to 22-µF capacitance on each power pin from the minimum recommended. Place the smallest package-sized capacitors closest to the power pin.
- All IC pins should be connected and never left floating. For example, input pins must be tied to a HIGH or LOW logic state; do not float input pins.
- Minimize current loops. An electrical circuit is always a closed loop. Every signal path has a return path back to the source (also called the return current). With DC, the return current takes the lowest resistance path back. With higher frequency, the return current flows along the lowest impedance (that is directly beneath the forward signal path [12]). Current loops in the layout generate noise and should be minimized by keeping forward and return currents together; this helps EMI and ESD performance. Solid ground plane provides a continuous, low-impedance path for return current.
- Associated regulators should be as close as possible to the IC. If using a regulator that has a FB (feedback pin), add an upper and lower capacitor to the resistor divider network. For example, if a resistor divider network has a 1:2 ratio, the capacitor should have a 2:1 ratio.
- High-speed connectors:
  - Use connectors that have complete shielding around the connector interface. For example, a Rosenberger HSD type connector (such as D4S20A-40ML5-Z or D4S10A-400L5-Y) or equivalent.
- High-speed cables:
  - Use cables with high shield coverage. For example, a DACAR 535-2 (such as a Rosenberger LD5-101-xx000-Z-Z_flex cable, where xx is in meters) or equivalent.

- External ESD protection components include passive components like series resistors, decoupling capacitors, ferrite beads, and suppression devices (such as filters, transient voltage suppressors (TVS), varistors, thyristors, diodes, polymers, SCRs, and so on). These components block ESD currents, clamp ESD-induced voltages, and shunt ESD-induced currents in the system, minimizing the effects of ESD pulses in the system. Guidelines for choosing onboard ESD protection devices that help to minimize ESD effects in a system:
  - Serial resistors
    - Use series resistors to attenuate indirect or secondary ESD stress in the system. Series resistors have proven to be effective for system-level ESD protection and can be used with voltage clamps and decoupling capacitors.

      NOTE: If series resistors are forced to conduct currents from direct ESD events, large voltages can build up across the resistors, causing arcs between the terminals and potentially shorting these series resistors; therefore, for handling direct discharges in the system use primary clamping devices (TVS devices) in addition to the series resistor or use resistors designed for high voltages (which will usually come in larger footprint sizes). These passive components should be placed as close as possible to the potential ESD stress points in the layout.

      NOTE: Small SMD passive components usually do not provide good protection against direct 8-kV IEC pulses, but they can be used to protect against secondary pulses in the system [2].
    - Identify the maximum capacitance that can be applied to signal lines in the system and place appropriate filters or TVS on sensitive signals (like resets, interrupts, edge triggered signals, and so on).
      - Place filters or transient suppressors on off-board receivers and drivers for cables that are susceptible to direct discharge (including signals that enter opto-isolators).
      - Choose protection components for the system based on clamping voltage levels achievable, breakdown voltage, response time, capacitance, dynamic resistance, and ability to withstand multiple ESD strikes. Texas Instruments™ offers a wide range of ESD and EMI protection devices and solutions. For more information regarding the ESD and EMI protection product portfolio, see Reference [5].
  - TVS diodes
    - TVS diodes have lower capacitance and lower dynamic resistance values compared to other transient suppression devices. They demonstrate high ESD multi-strike absorption capability; that is, once the ESD strike is absorbed, the protection device returns to its high-impedance state very quickly. These devices offer low clamping and breakdown voltages and have excellent response times.
  - Varistors
    - When an ESD event occurs, the varistors resistance changes from a high standby value to a low conducting value, absorbing the ESD energy and limiting ESD-induced voltages. Varistors typically have trigger voltages over 50 V, clamping voltages over 100 V, and a dynamic resistance over 20 Ω (after turn on)[2]. Varistors feature lower capacitance but have significant leakage currents after an ESD stress.
  - Polymers
    - These devices are similar to varistors in operation but have low capacitance (0.05 to 1 pF), making them a good fit for high-frequency applications. The breakdown voltages are higher (compared to varistors) and have lower endurance to multiple ESD strikes.

- ESD protection using series resistors
  - Consider a system where an IC is interfaced to an LCD that is susceptible to ESD (secondary or residual ESD stress in the system). In this case, LCD pins represent the ESD entry points in the system; TI recommends placing series resistors on the LCD pins. When an ESD event occurs in the system, the series resistor limits the current that finally strikes the IC I/O pin. The larger the value of resistance, the lower the residual current seen at the interface I/O pin.

NOTE: If standalone resistors are used for primary ESD protection, they must withstand the full electrostatic voltage; this requires resistors that are designed for high voltages, and these resistors usually have a larger footprint. The series resistors can be combined with additional diodes and primary clamping devices for added protection. The diodes at the I/O pins divert the ESD current to the primary clamp (between VCC and VSS), and only the residual stress appears at the device I/O pins. The decoupling capacitor at the supply pins helps limit the initial fast transients of the ESD pulse.

NOTE: The simple series resistor protection technique works for low levels of ESD stress (secondary protection of indirect ESD or residual ESD current); however, for higher ESD stress (primary protection of direct ESD), suppression devices (such as TVS diodes, varistors, and polymers) should be considered.

3 General System-Level ESD Guidelines and Recommendations

System-level ESD protection strategies depend strongly on physical design, operational requirements, and overall cost of the end-product. There are different disciplines of protection that can be considered to minimize ESD coupling into the system. A robust ESD system design involves factoring multiple elements, such as:

- Enclosure
- PCB design and layout
- ESD ground paths
- On-board ESD protection devices
- System wiring and interconnects
- Software design
- ESD testing

The key to an ESD-robust system design is to consider the effects of ESD in the system early on during design and development of the board by following ESD-immune design guidelines. ESD testing throughout development helps identify and fix weak ESD spots in the system through different stages.

3.1 Enclosures

Identifying the ESD entry points in the system and designing enclosures such that any direct or indirect electrostatic discharge into the system is minimized, is key to any system-level ESD protection design.

Figure 6 through Figure 11 show various enclosure cases and respective ESD entry scenarios.

Figure 6 represents an ideal case where the conductive enclosure is properly shielded and grounded; ESD does not influence the system at all. This is an ideal case, but it is not applicable in most systems.

Figure 7 represents the direct discharge case where a conductive block in the system is protruding out of the enclosure and the electrostatic discharge gets coupled onto the system right through this block. A good design would make sure that the conductive block penetrating out of the enclosure is properly shielded to minimize ESD coupling.

Figure 8 represents the indirect discharge case where the electromagnetic fields that are generated enter the system through the enclosure holes. These electromagnetic fields can couple to internal circuits or wires and propagate through the system. Providing sufficient a air gap between the enclosure holes and the electronics within the enclosure can help minimize this coupling effect.

Figure 9 represents direct discharge to cables that in turn generate electromagnetic fields in the system. See Section 3.1.2 for recommended design guidelines.

Figure 10 represents secondary discharge from isolated metal bracket or panel that gets coupled to the system. See Section 3.1.1 for recommended design guidelines.

Figure 11 represents electrostatic discharge close to a plastic enclosure that generates an electromagnetic field. Keeping a sufficient air gap between the non-conductive enclosure and the electronics within the enclosure can help minimize electromagnetic noise coupling into the system.

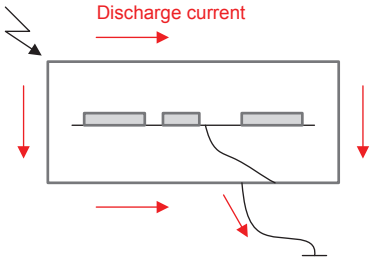


Figure 6. Enclosure Scenario (Ideal Case)

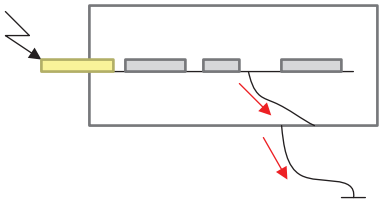


Figure 7. Enclosure Scenario (Direct Discharge)

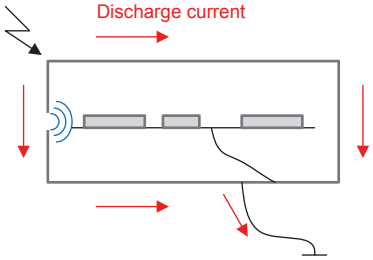


Figure 8. Enclosure Scenario (Electromagnetic Influences Through Holes)

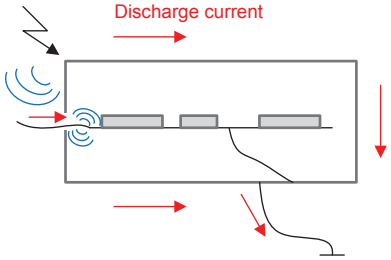


Figure 9. Enclosure Scenario (Direct Discharge to Cables)

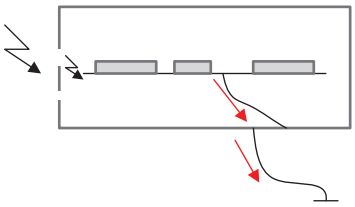


Figure 10. Enclosure Scenario (Secondary Discharge From Isolated Metal)

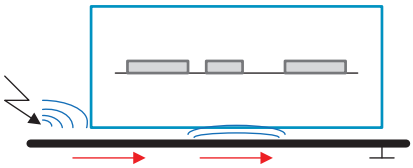


Figure 11. Enclosure Scenario (Discharge Close to Plastic Case)

3.1.1 Enclosure Openings

The following are general enclosure guidelines that can help to minimize ESD and EMI coupling onto the system (a PCB, in this case):

- Provide direct ground path to conductive enclosures to minimize ESD coupling into the system. The direct ground path should be short with a low inductance.
- Choosing plastic and other non-conductive enclosures, air space and insulation can prevent ESD arcs from penetrating inside the system.
- Keep sufficient air gap between points on the enclosure that are susceptible to ESD (including ventilation holes, mounting holes, seams, and so on) and the PCB.
- Choose switches and user controls with plastic shafts or cover metal shafts with plastic knobs.
- With plastic being used as the enclosure material, LEDs and LCDs that are exposed through the nonconductive cases form a direct discharge path to the system. This is less severe in cases where the enclosure material is metal, as an ESD would arc to the metal case instead of the LED or LCD. In cases where the plastics is used as the enclosure material, because there is no metal panel available, the ESD would arc the exposed LEDs or LCD and their leads connected to the system directly. This discharge path can mostly be avoided by:
  - Using gaskets around LCD openings in the enclosures
  - Shielding LEDs that are exposed on plastic enclosures with transparent and non-conductive lens covers (see Figure 12)

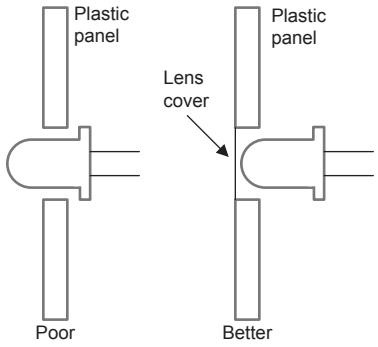


Figure 12. Shielding LEDs

- Upon direct discharge to enclosures with an isolated metal bracket or panel (which represent a high impedance path to ground):
  - Secondary discharge occurs within the enclosure, thus coupling the ESD to the PCB.
  - High-frequency electromagnetic noise is generated and can couple onto the internal wiring or PCB. A good design should properly ground the isolated metal brackets to minimize ESD or EMI coupling.

- Physical Opening: Reduce the overall aperture of the physical opening in the enclosure to minimize ESD coupling or electromagnetic noise coupling onto the system within (see Figure 13).

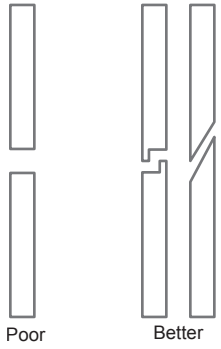


Figure 13. Enclosure Opening Considerations

- Beneath plastic bezels air discharge can reach metal back-plates beneath the plastic bezels and generate secondary discharges that can couple to the PCB behind. In this case, spraying conductive coating to the back of the plastic bezel can help direct the discharge to the enclosure ground and minimize ESD coupling onto the system.

3.1.2 Enclosure Cables

ESD can arc to the connectors on the cables, while indirect ESD can couple into cables through induction or radiation. General enclosure cable guidelines that can help to minimize ESD coupling onto the system (PCB in this case) are as follows (see Figure 14):

- Shield connector cables to reduce coupling (use foil or foil and braid shields).
- Keep cables as short as practicable.
- Ground cables entering the enclosure.
- Use transient suppressors and filters at cable entry points.

The best case in Figure 14 shows use of varistors as discharge suppressors at the cable entry points.

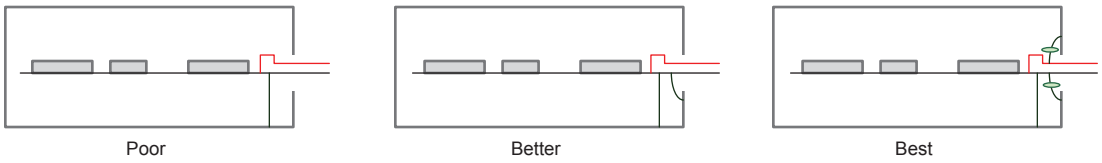


Figure 14. Enclosure Cable Considerations

3.2 PCB Design and Layout

Good PCB design and layout can be effective in suppressing ESD in the system. The following are general guidelines for ESD- and EMI-immune PCB layouts:

- Use ground planes instead of ground traces where possible to lower the current-path inductance.
- Use multipoint and thicker grounds where you want ESD currents to flow, and single-point and thinner grounds where you don't.
- If it is not practicable to create a continuous ground plane by using copper pour in the layout, then create smaller copper pour sections that are in turn connected to the rest of the ground. However, do not create isolated copper pour islands; they can induce noise and arc in presence of ESD.
- If possible, use multi-layer PCBs with paired power and ground planes.
- If possible, place solid or filled vias into power and ground planes. These vias provide excellent thermal dissipation in case of an ESD event and also ensure good electrical and power supply connections. For the plated through-hole components, use thermal vias.
- Keep traces as short as possible to reduce trace inductance.

- Avoid routing traces at right angles to component pins or other traces. Right angle traces should be avoided as they are known to cause more radiation; this becomes more critical in high-speed designs (see Figure 15).

Figure 15. Avoid Right-Angle Traces

- Keep sensitive signal traces away from PCB edges.
- Place all connectors and external wires on one edge of the PCB.
- Place ESD susceptible circuitry at the center of the PCB away from the edges of the board, external wires, connectors, and power.
- Decoupling (see Figure 16):
  - Use decoupling capacitors with low effective series resistance (ESR) and effective series inductance (ESL) to decouple the IC power from the rest of the supply system.
  - Place the decoupling capacitor close to the IC power pins.
  - Keep the traces from decoupling caps to GND as short (and thick) as possible.

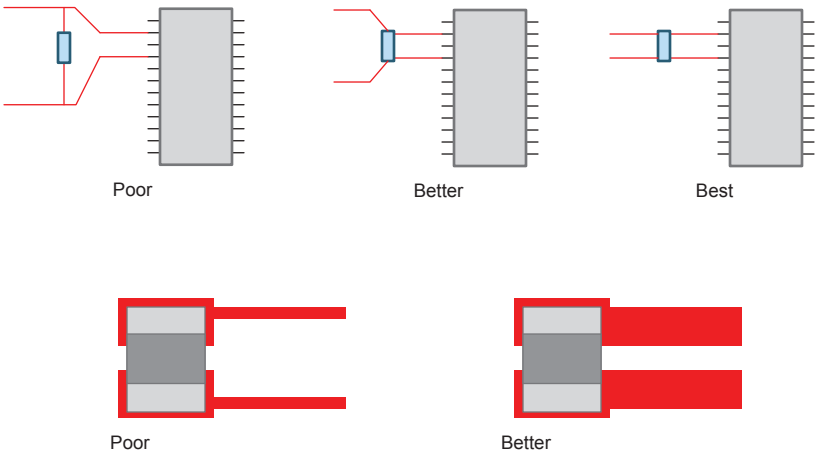


Figure 16. Decoupling Basics

- Current loops

An electrical circuit is always a closed loop. Every signal path has a return path back to the source; also called the return current. With DC, the return current takes the lowest resistance path back. With higher frequency, the return current flows along the lowest impedance; that is directly beneath the forward signal path [12]. Current loops in the layout generate noise and should be minimized by keeping forward and return currents together. It helps both EMI and ESD performance. Solid ground plane provides continuous, low-impedance path for return current.

3.3 Onboard ESD Protection Devices

External ESD protection components include passive components like series resistors, decoupling capacitors, ferrite beads, suppression devices such as filters, transient voltage suppressors (TVS), varistors, thyristors, diodes, polymers, SCRs, and so on. These components block ESD currents, clamp ESD-induced voltages and shunt ESD-induced currents in the system, thus minimizing the effects of ESD pulses in the system. Here are some general guidelines towards choosing on-board ESD protection devices that help to minimize ESD effects in the system.

3.4 Circuit Design and Software Considerations

Because the majority of the system-level ESD failures are soft failures (system upset without any physical damage), circuit design and software considerations should be taken to identify and handle these soft failures and also enable for safe recovery. The following sections list general guidelines for circuit design and software considerations.

3.4.1 Circuit Design

- Properly terminate unused pins of the IC.
- Avoid connecting sensitive signals (such as reset, interrupts, or edge-triggered signals) to long traces or cables.
- If possible avoid edge-triggered logic in the system.
- Isolate outside signals by using opto-couplers or transformers.
- If required, include deglitch filters to prevent inadvertent triggers in the system (such as power monitors).
- Allow for the system to reset or recover from deadlock state after an ESD event (for example, by using watchdog timers or non-maskable interrupts).

3.4.2 Software Considerations

- Use watchdog timer to monitor any software lockups. Ensure software does not stop watchdog timer once started. Design the software or firmware to reset the watchdog timer periodically (preferably in one or two places in the main loop).
- Enable smaller time-outs in functions to identify fault states and regain control (before watchdog timer time-outs).
- Oversample critical hardware inputs and do simple averaging of results to confirm input states.
- Check parity and framing on incoming data.
- Acknowledge reception of correct data; else return error code for incorrect data reception.
- Retransmit data if acknowledge is not received.

3.5 ESD Testing

ESD testing throughout design and development helps identify and fix weak ESD spots in the system. Onboard LEDs and switches can be used to debug different ESD failure categories. Listed below are the different system-level ESD failure criteria as per IEC 61000-4-2 [1] and example failure conditions when using an FPD-Link III device in the system:

- Normal performance within specification limits
  - FPD-Link III is not affected by the system-level ESD stress and continues to execute without any intervention.
- Temporary degradation or loss of function or performance which is self-recoverable
  - Device reset can occur (for example, caused by low pulse on the FPD-Link III reset pin that causes the device to reset).
  - Oscillator disturbance can occur (for example, caused by on-board crystal dropping out). This condition can be identified by on-chip watchdog or oscillator fault detection.

NOTE: In this case, the onboard LEDs and the reset interrupt vector (that helps identify the last cause of a reset: BOR, POR, or PUC) can be used to the identify the failure and recovery conditions.

- Temporary degradation or loss of function or performance that requires operator intervention or system reset.
  - Device upset that requires user to manually apply a low pulse on the reset pin or a power-cycle.

NOTE: In this case, onboard switches can be used on the test board to recover the device.

- Degradation or loss of function that is not recoverable due to damage of equipment (components) or software, or loss of data.
  - Damage of FPD-Link III I/O pin structure. This might result in system upsets such as non-operational interrupts associated with the I/O pins.
  - Increased leakage current caused by degradation or damage of integrated components and circuits connected to I/O pins or power supply pins.
  - Loss of CODE or DATA on device RAM or non-volatile memory.
  - Device enters deadlock state by poorly designed software.

See IEC standards [1] for the standard system-level ESD tests, thresholds, and ratings.

4 References

1. International Electrotechnical Commission, IEC 61000-4-2, Electromagnetic capability (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test, Ed. 2.0
2. JEDEC Publication (White Paper 3) JEP161: System-level ESD Part I: Common Misconceptions and Recommended Basic Approaches
3. ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Human Body Model –Component Level, ANSI ESDA/JEDEC JS-001-2011
4. JESD22-C101 Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components
5. Texas Instruments Inc., ESD and EMI Device Protection Product Portfolio, www.ti.com/emi
6. ISO Standard 10605 Road vehicles – Test methods for electrical disturbances from electrostatic discharge, International Organization for Standardization, 2008
7. S. Marum, C. Duvvury, J. Park, A. Chadwick, A. Jahanzeb; Protection Circuits from the Transient Voltage Suppressor's Residual Pulse During IEC 61000-4-2 Stress, Proc. EOS/ESD Symposium 2009 (2009)
8. Lifang Lou, Charvaka Duvvury, Agha Jahanzeb, Jae Park; SPICE Simulation Methodology for Systemlevel ESD Design, Proc EOS/ESD Symposium 2010 (2010)
9. Industry Council on ESD Target Levels, White Paper 1: A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements, August 2007, at www.esda.org or JEDEC publication JEP155, Recommended ESD Target Levels for HBM/MM Qualification, www.jedec.org
10. Industry Council on ESD Target Levels, White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements, Revision 2, April 2010, at www.esda.org or JEDEC publication JEP157, ‘Recommended ESD-CDM Target Levels', www.jedec.org
11. MSP430 32-kHz Crystal Oscillator (SLAA322)
12. High-Speed Layout Guidelines (SCAA082)
13. ESD Association Standard for the development of an Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices), ANSI/ESD S20.20-2007
14. International Electrotechnical Commission, IEC 61340 standards family, Electrostatics - Part 2-1 to 5-3 15. Industry Council on ESD Target Levels, http://www.esdindustrycouncil.org
15. TI Application note SLAA530 http://www.ti.com/lit/an/slaa530/slaa530.pdf
16. TI LVDS Owner’s Manual http://www.ti.com/lit/ml/snla187/snla187.pdf

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