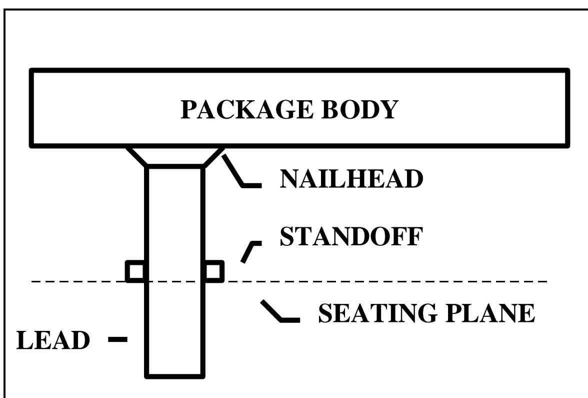
Texas Instruments

Solder Dip Lead Finish For Ceramic Pin Grid Array Packages

Texas Instruments performs hot solder dip of Ceramic Pin Grid Array (CPGA) packages in accordance with MIL-PRF-38535. Some customers have misinterpreted the specification with respect to the amount of solder covering the device pins. Per MIL-PRF-38535, (General Specification For Integrated (Microcircuits) Manufacturing), Paragraph A.3.5.6.3.4 Hot Solder Dip, Subparagraph (a) All outlines with hot solder dip over compliant coating, "The hot solder dip shall extend beyond the effective seating plane." There is no maximum specification.



Due to normal variations in the solder dip process, some devices will have gold plate exposed on the nail-head, some will not, and some devices will have both gold and soldered nail-heads. As illustrated on the left, the nail-head is above the seating plane of the device therefore the presence or absence of solder on the nail-head is not an issue.

The devices in question fully meet the requirements of MIL-PRF-38535 and MIL-STD-883 (Test Method Standard [for] Microcircuits), Method 2009, "External Visual", for solder finish and external visual inspection.

TI Devices receive 100% hermetic testing during production and the presence or absence of solder on the nail-head will not degrade the part. Please note that Texas Instruments cannot be responsible for any third-party processing of devices including solder dip.

Devices are warranted as meeting MIL-PRF-39535 in accordance with the Texas Instruments Incorporated Terms of Sale for Semiconductor Products. For more information please contact TI customer support at www.ti.com.

The following photographs are examples of CPGA packages that fully meet the requirements for solder finish and external visual inspection as described above.