

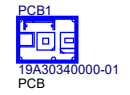
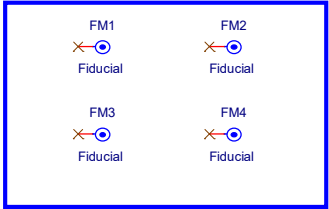
Revision History:



EKI-3400 Rev.A1 01-1 Date 2022/08/19

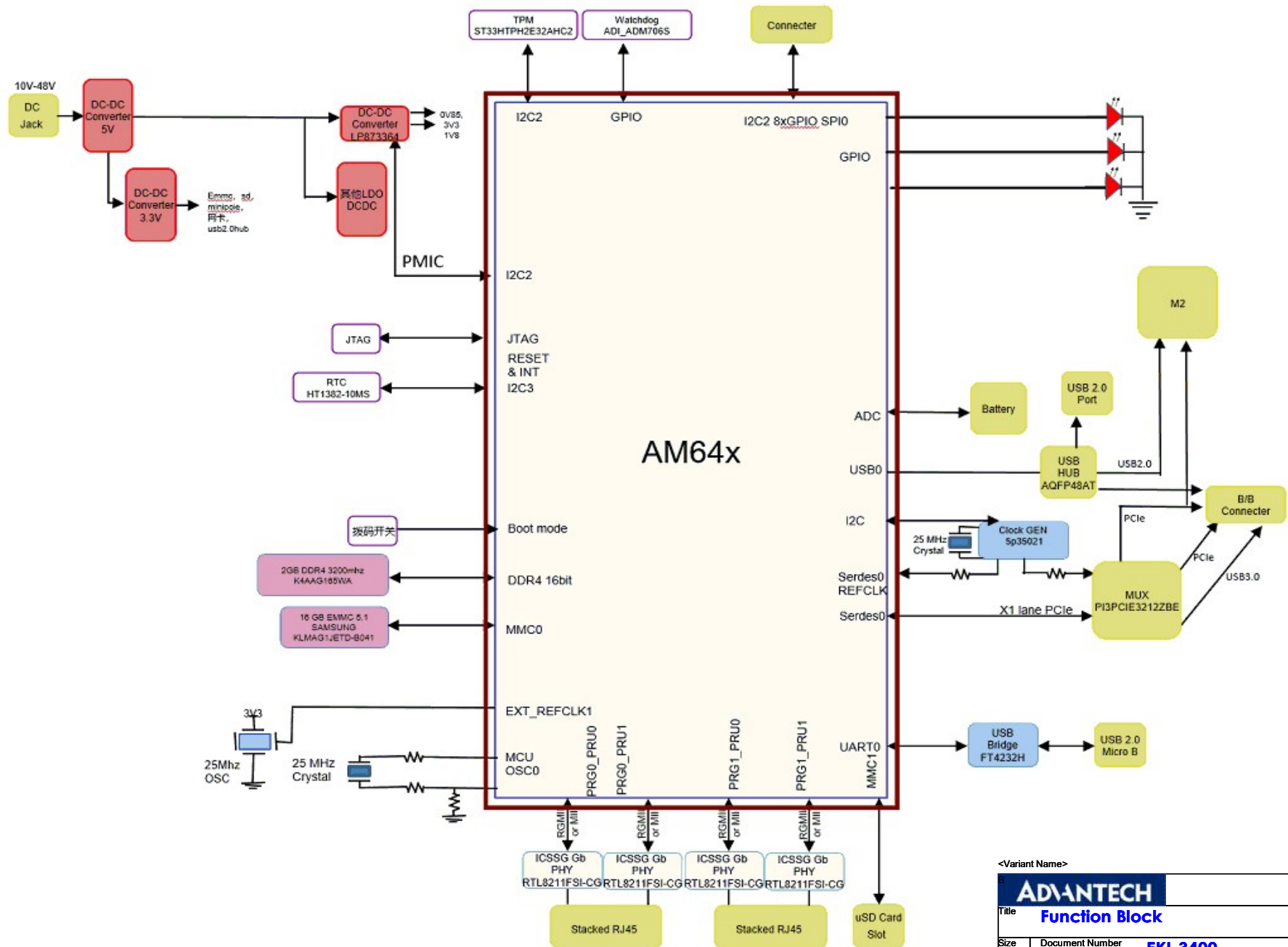
PCB version: A101-1 P/N: 19A30340000-01 96933400000

Fiducial Mark



<Variant Name>

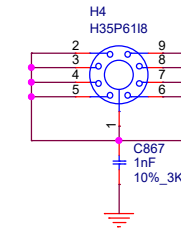
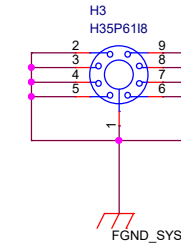
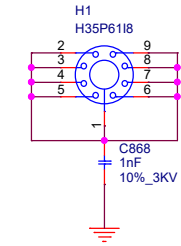
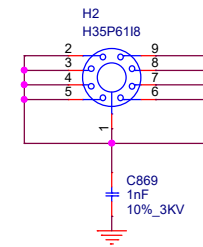
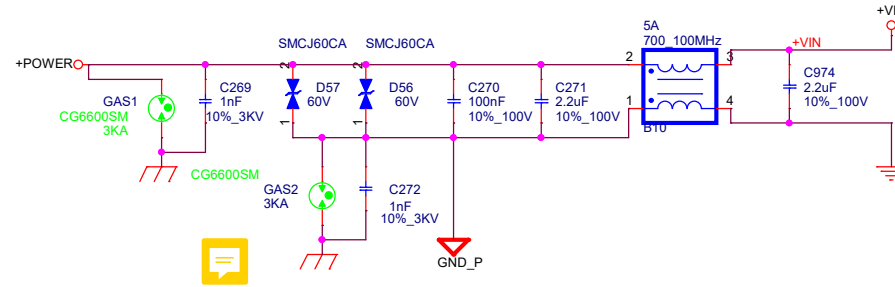
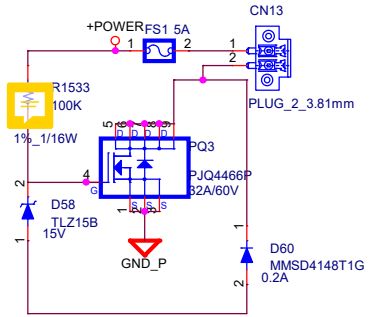
ADVANTECH		
Title Rev History		
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ADVANTECH	
Function Block	
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POWER

10~48VDC

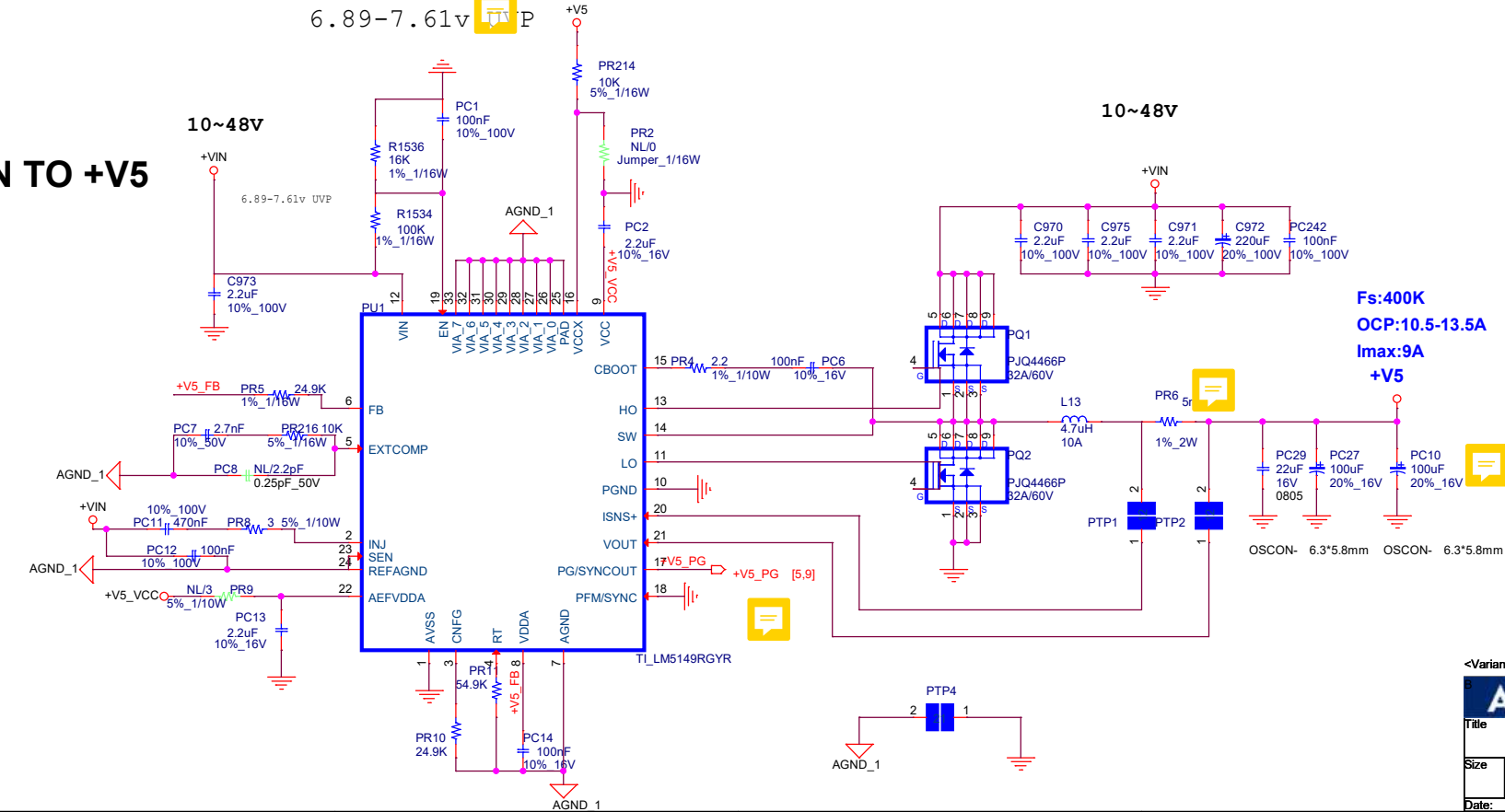


6.89~7.61V UVP

+VIN TO +V5

10~48V

10~48V



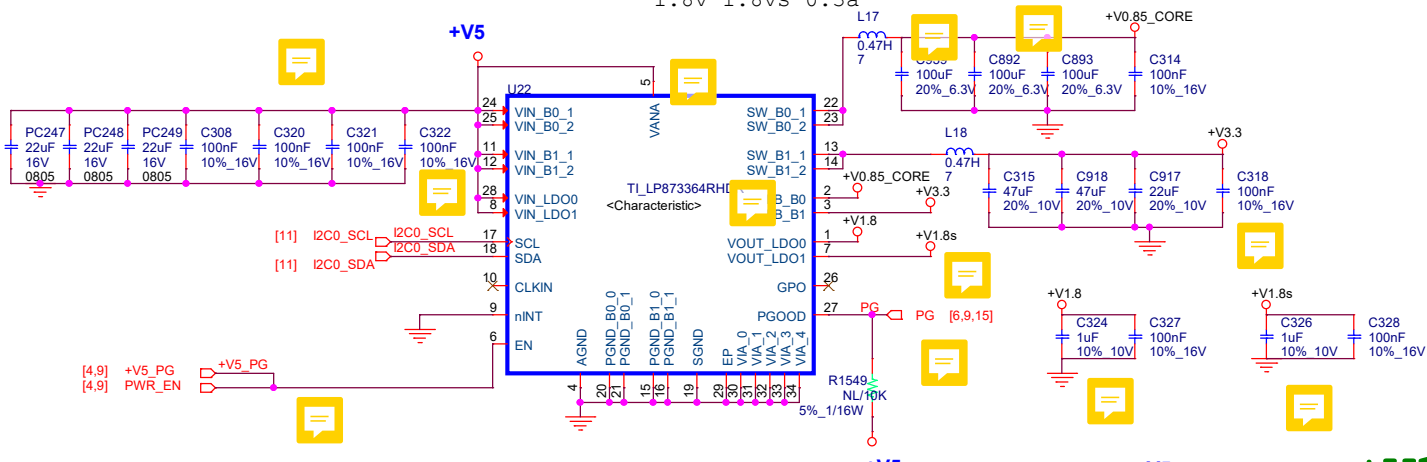
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OCP:10.5-13.5A
Imax:9A
+V5

<Variant Name>

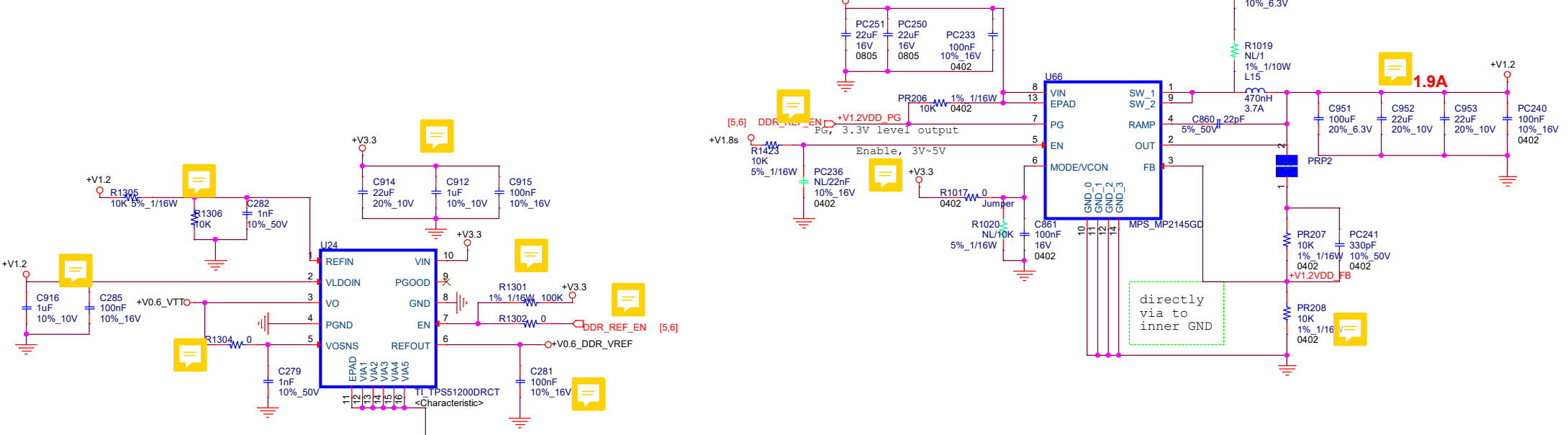
ADVANTECH	
POWER IN V5	
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PMIC

0.85v, 3.3v 3a
1.8v 1.8vs 0.3a



+V1.2V DDR



3.3v原则
给cpu供电的支路用3.3
给其他设备供电的用3.3a
3.3a与cpu core一起上电，为时序最后一个

DDR Vtt 0.6V

ADVANTECH	
POWER PMIC V1.2 V0.6	
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+V5 TO +V3.3

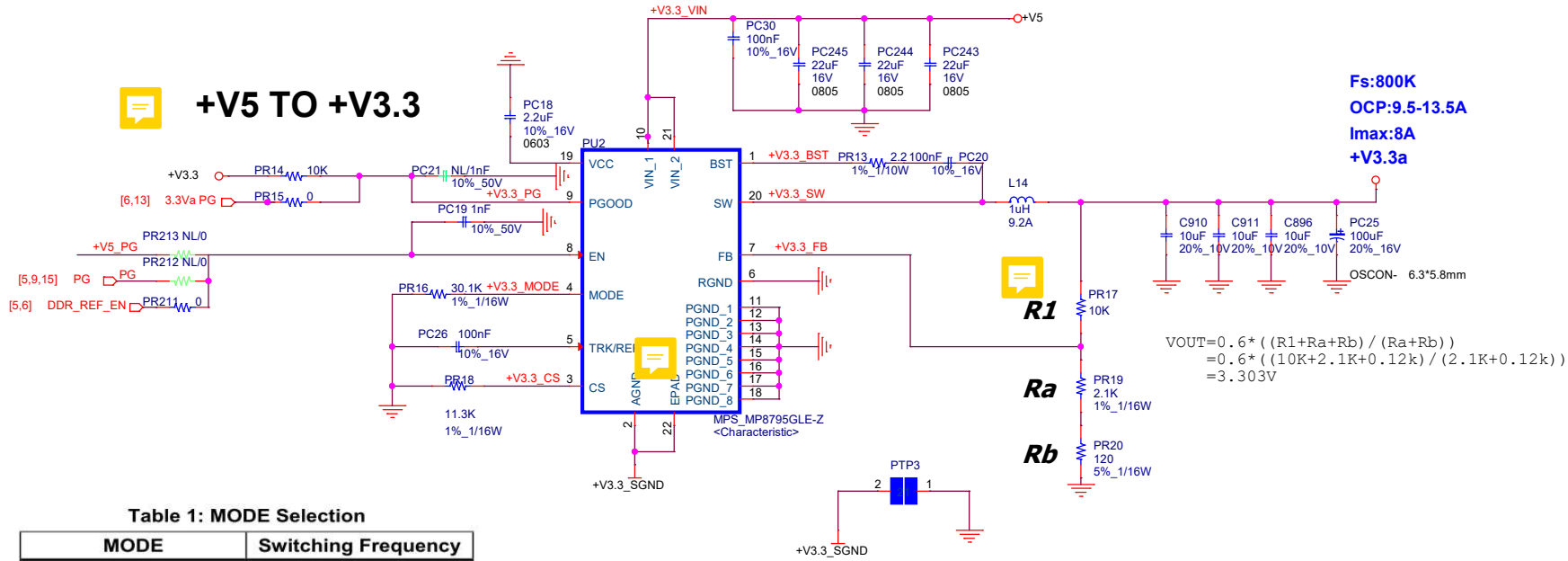
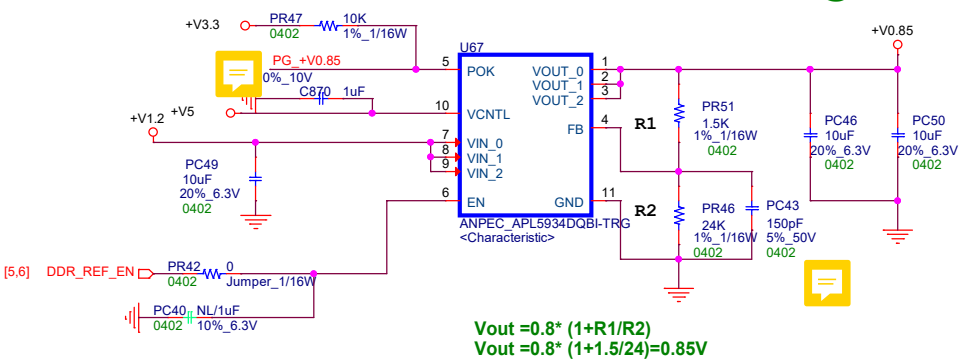


Table 1: MODE Selection

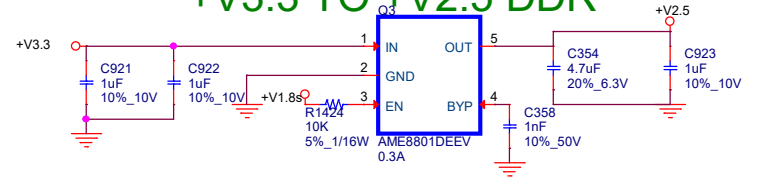
MODE	Switching Frequency
GND	600kHz
30.1kΩ (±20%) to GND	800kHz
60.4kΩ (±20%) to GND	1000kHz

+V1.2 TO +V0.85

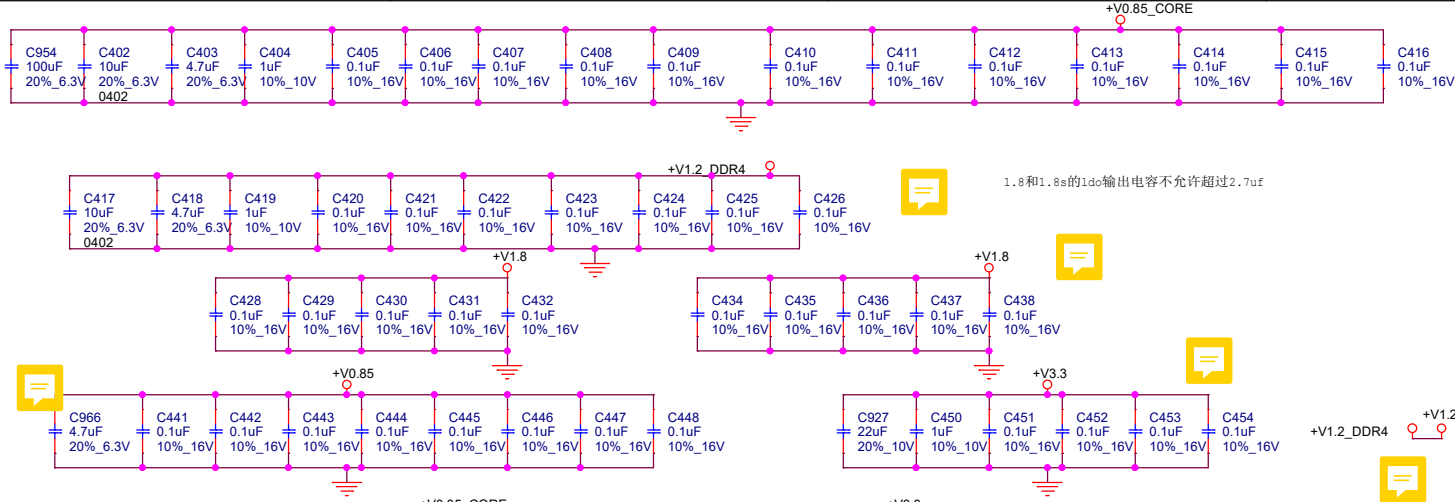
+V0.85@0.3A



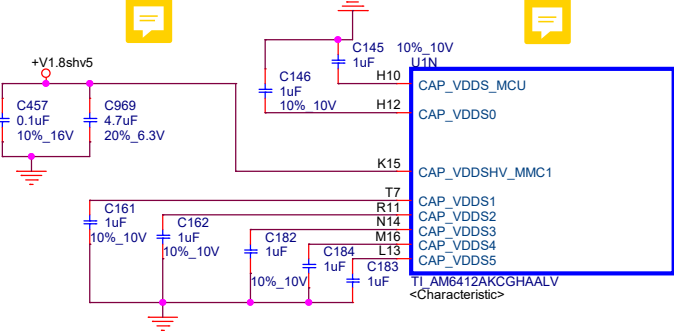
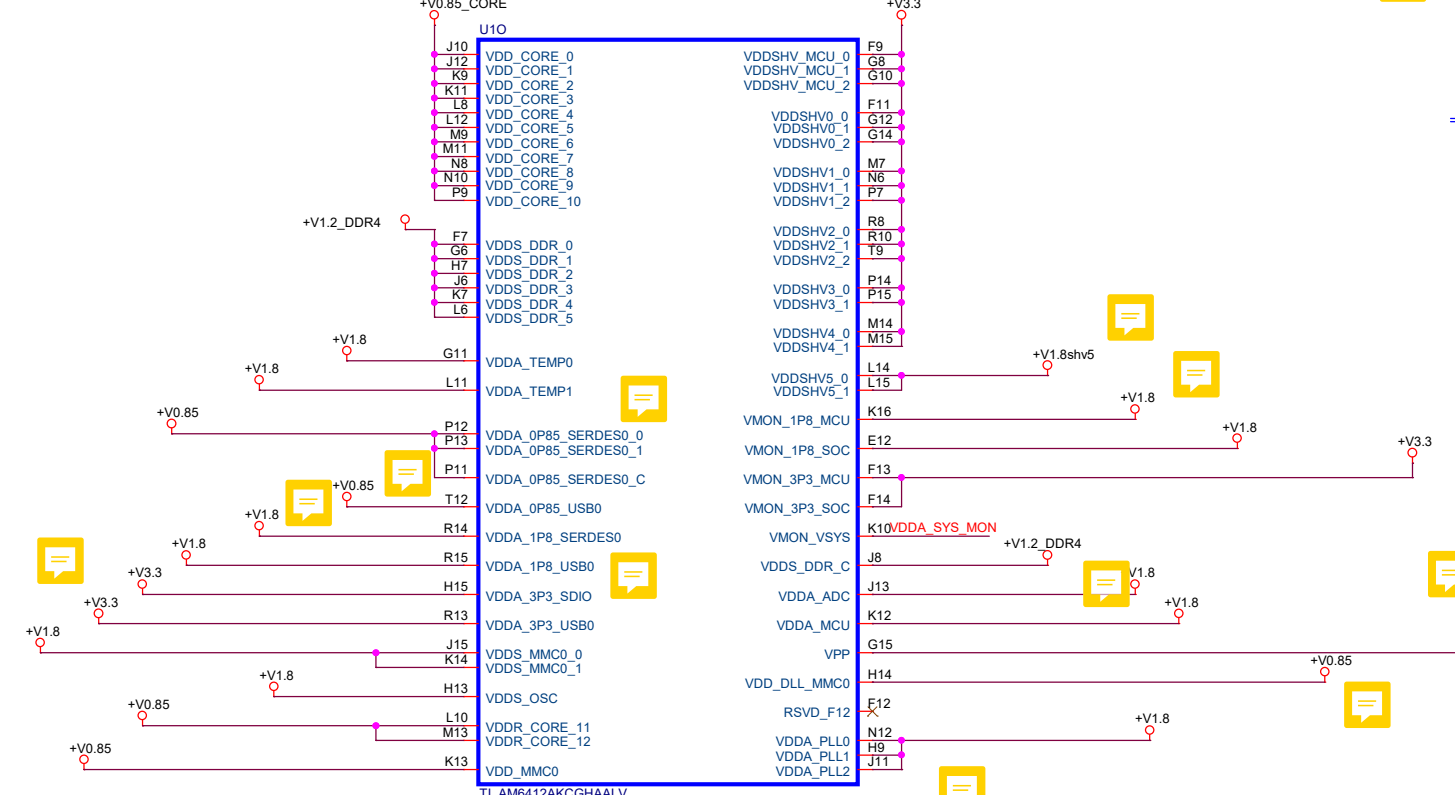
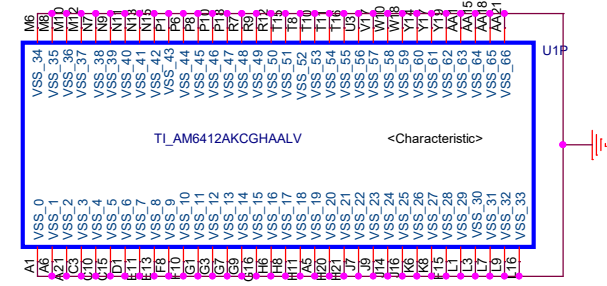
+V3.3 TO +V2.5 DDR



ADVANTECH		
Title POWER 2.5 0.85 1.8 3.3		
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1.8和1.8s的1dc输出电容不允许超过2.7uF



当5v低于4.668v时触发
fixed 0.45 V (+/-3%)

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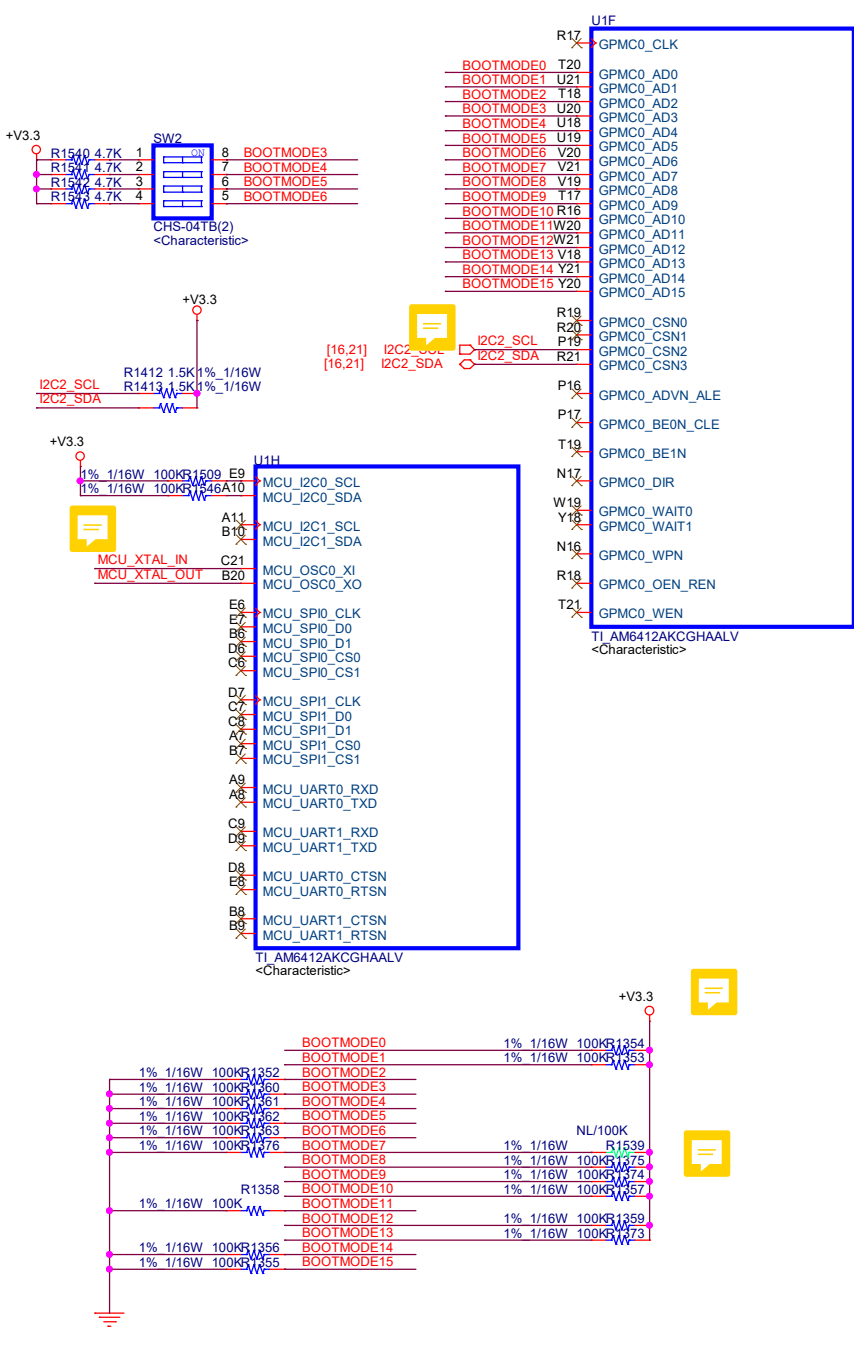


Table 4-4. Primary Boot Mode Selection (continued)

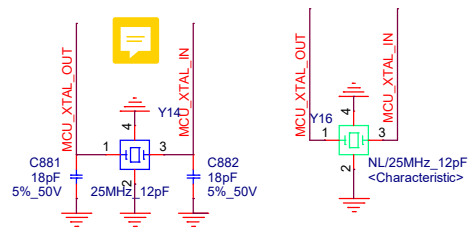
Primary Boot Mode Config							Primary Boot Mode
B9	B8	B7	B6	B5	B4	B3	
Reserved	Iclk	Csel	0	0	1	0	QSPI
Reserved	Mode	Csel	0	0	1	1	SPI
Clkout	0	Link Info	0	1	0	0	Ethernet RGMII
Clkout	Clk src	0	0	1	0	1	Ethernet RMII
Bus reset	Reserved	Addr	0	1	1	0	I2C
Reserved	Reserved	Reserved	0	1	1	1	UART
1	Reserved	Fs/raw	1	0	0	0	MMCSD card
Reserved	Reserved	Reserved	1	0	0	1	eMMC
Core Volt	Mode	Lane Swap	1	0	1	0	USB
Reserved	Reserved	Reserved	1	0	1	1	GPMC NAND
Reserved	Reserved	Reserved	1	1	0	0	GPMC NOR
Reserved	Reserved	Clocking	1	1	0	1	PCIe
SFPD	Read Cmd	Mode	1	1	1	0	xSPI
Reserved	Reserved	No/Dev	1	1	1	1	No-boot/Dev boot

4.3.1.2 Backup Boot Mode Selection and Configuration

The backup boot mode is selected via pins within the main BOOTMODE map. Table 4-5 lists all possible backup boot modes.

Table 4-5. Backup Mode Selection

Backup Boot Config	Backup Boot Mode Selection				Backup Boot Mode Selected
B13	B12	B11	B10		
Reserved	0	0	0	None	
Mode	0	0	1	USB	
Reserved	0	1	0	Reserved	
Reserved	0	1	1	UART	
IF	1	0	0	Ethernet	
Port	1	0	1	MMCSD	
Reserved	1	1	0	SPI	
Reserved	1	1	1	I2C	



<Variant Name>

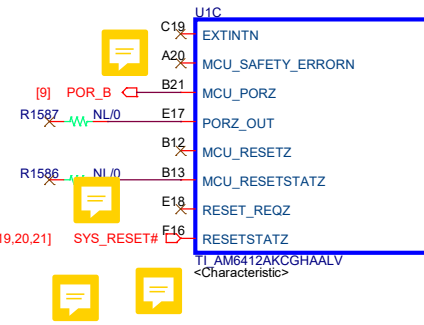
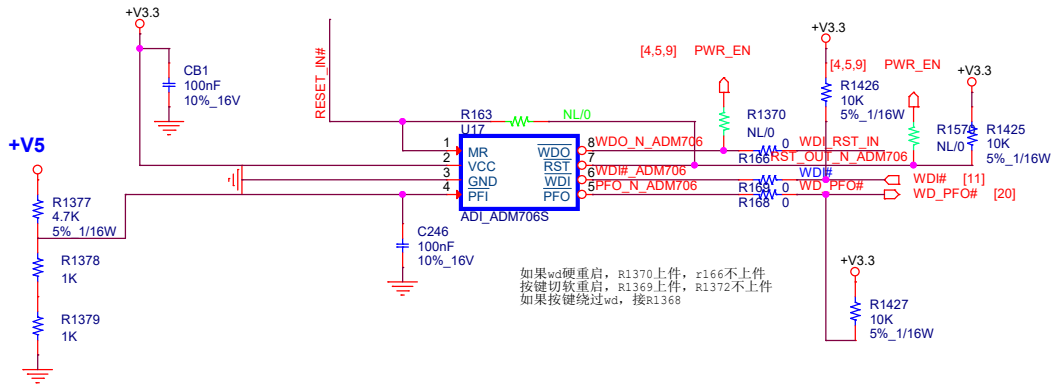
ADVANTECH

Title: **AM6412 BOOT&OSC**

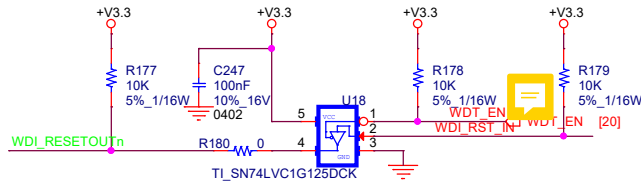
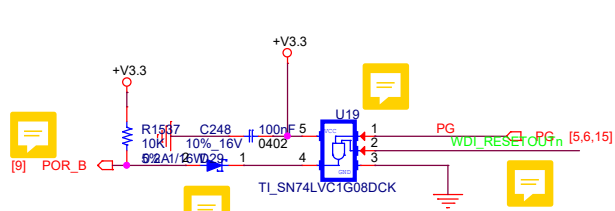
Size: Document Number **EKI-3400** Rev: A101-1

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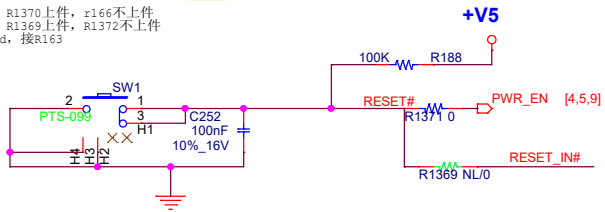
WD&reset



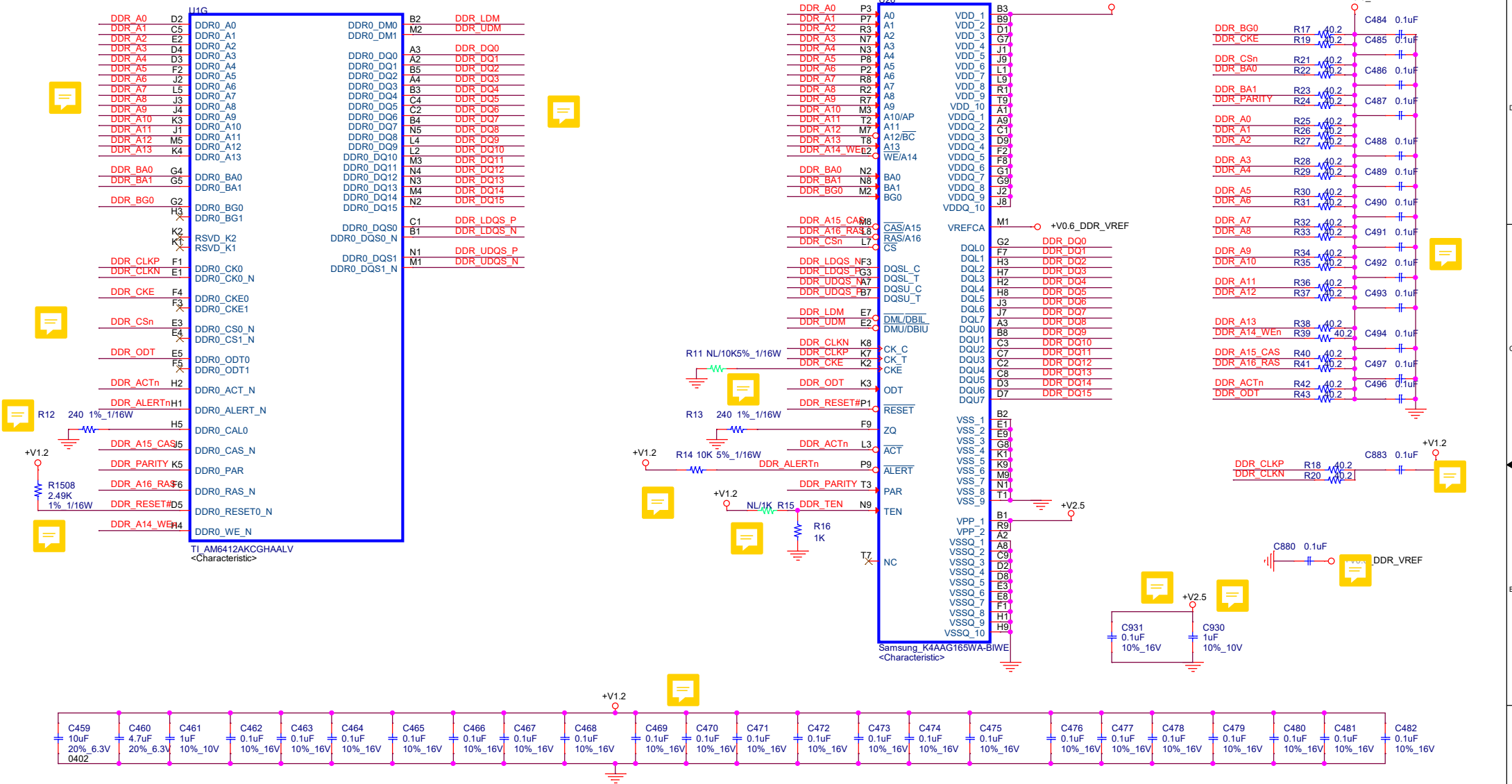
Move up as far as possible



如果wd硬重启, R1370上件, r166不上件
 按键切软重启, R1369上件, R1372不上件
 如果按键绕过wd, 接R163



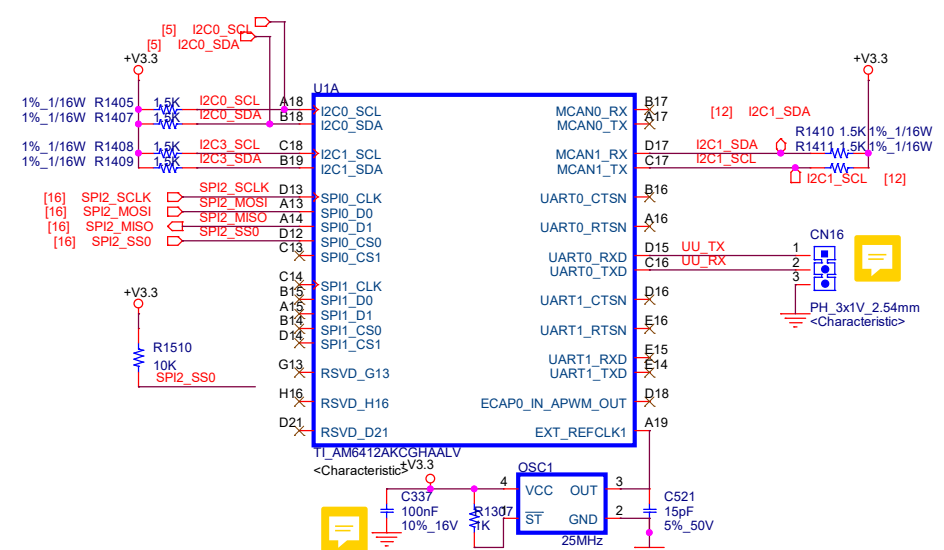
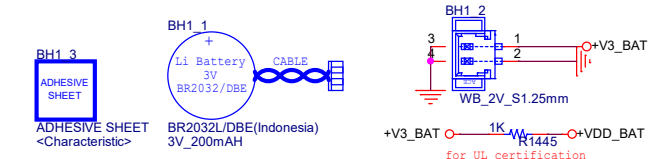
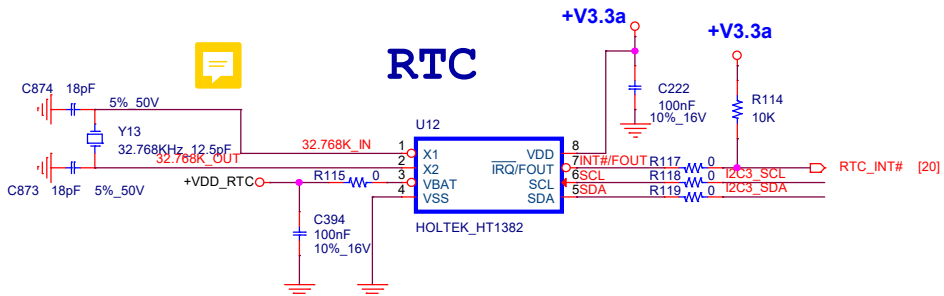
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Title WD&RESET		
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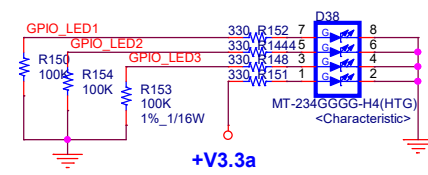
DDR4 16bit 16Gb

ADVANTECH		
Title DDR4		
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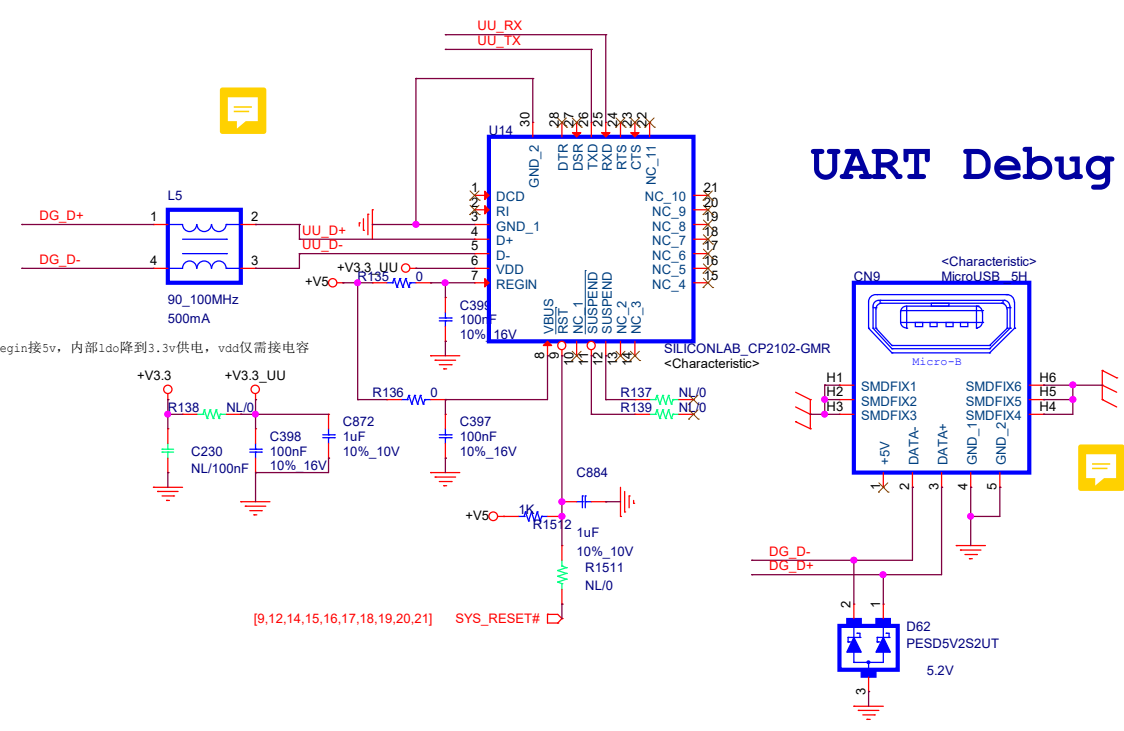
RTC



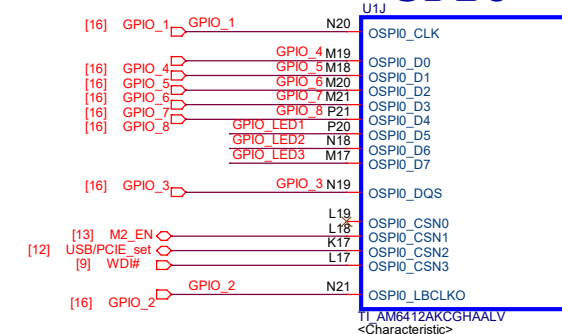
LED



UART Debug

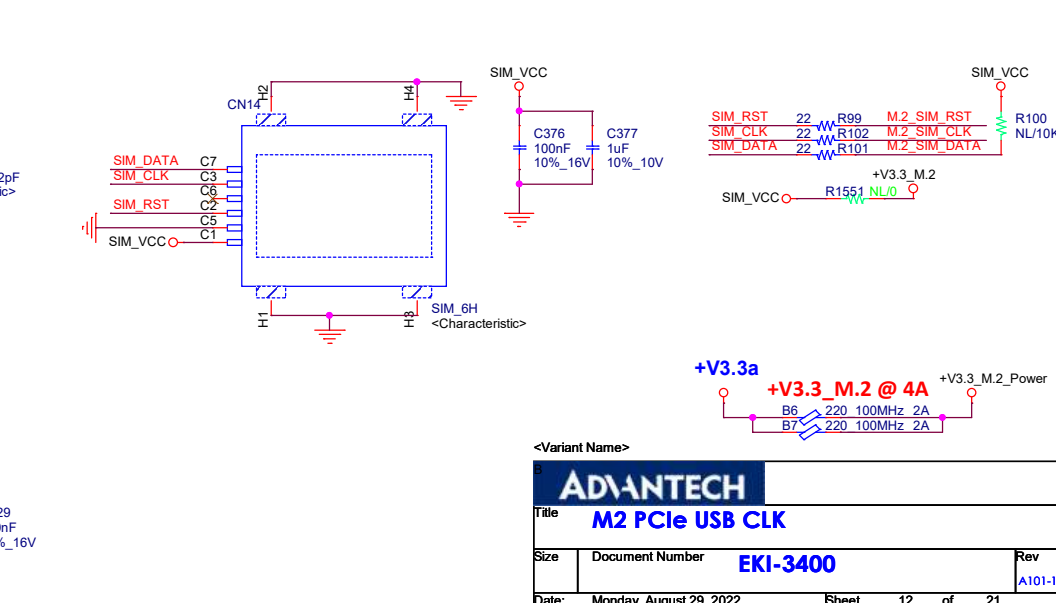
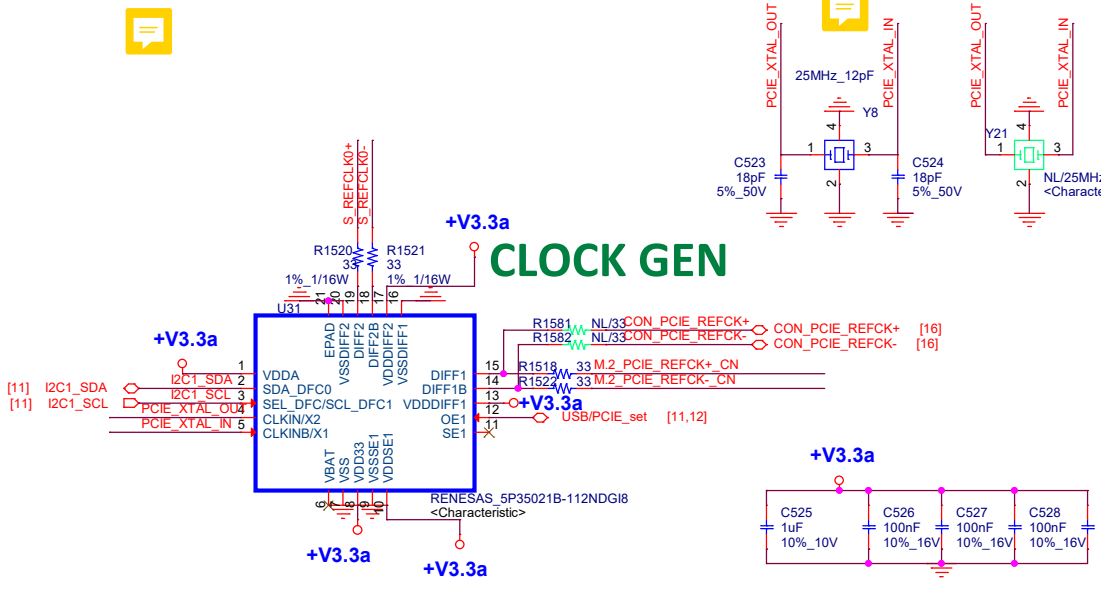
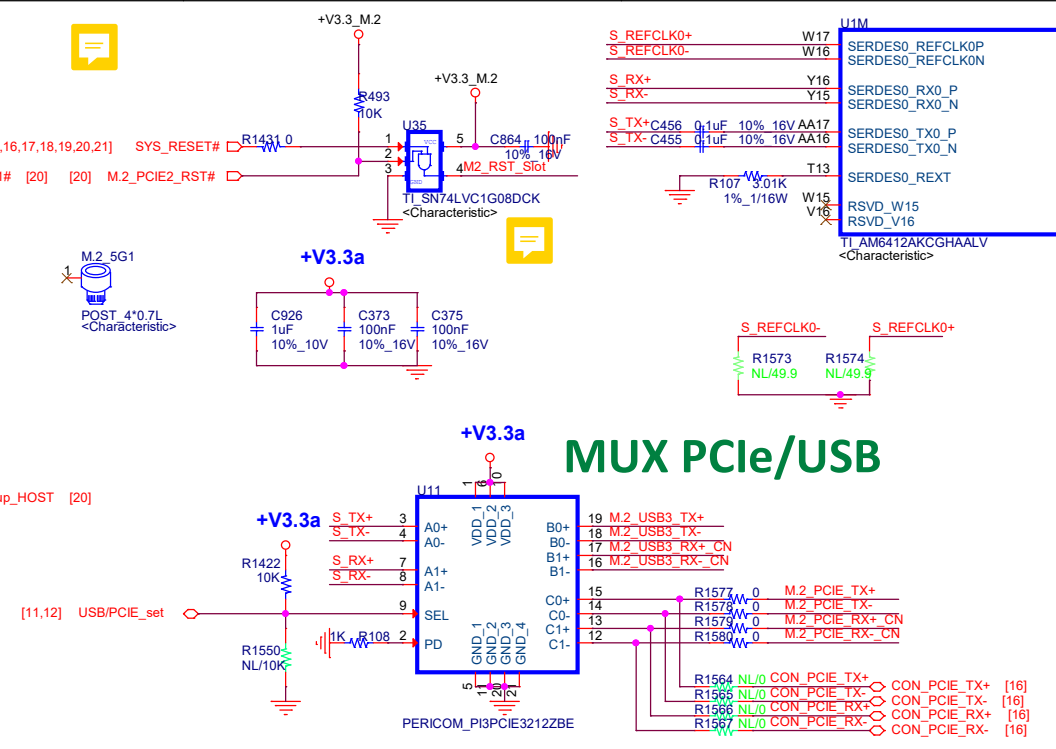
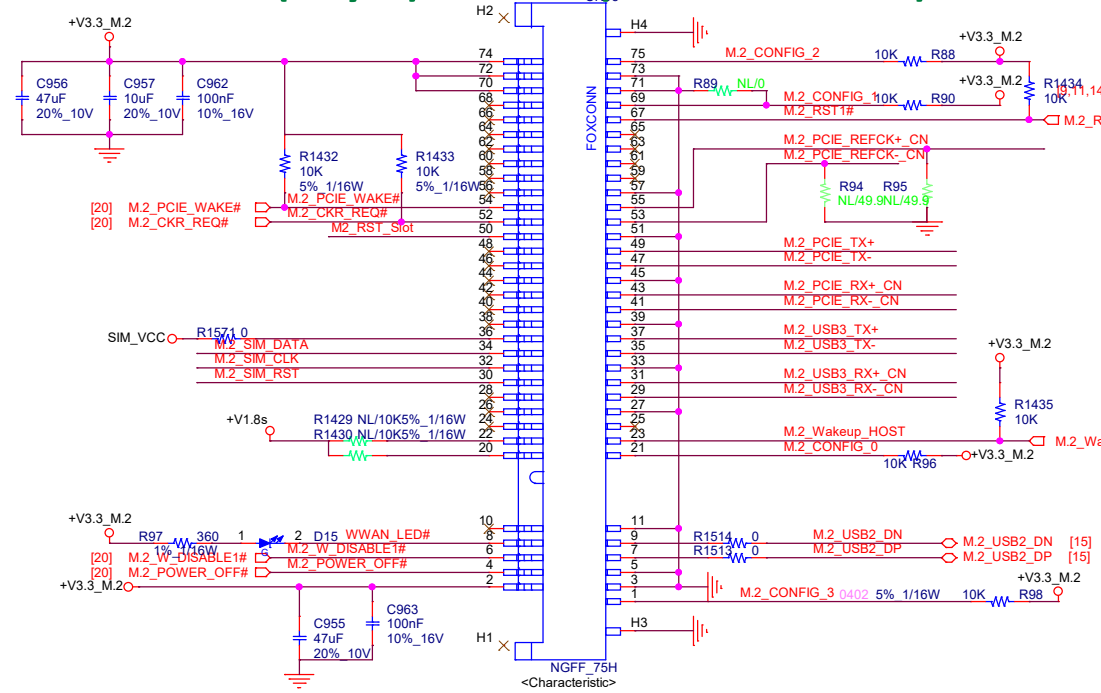


GPIO



ADVANTECH		
Title UART&I2C&RTC&LED&GPIO		
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M.2 socket 2 (Key B)-WWAN(PCie & USB3.0)



<Variant Name>

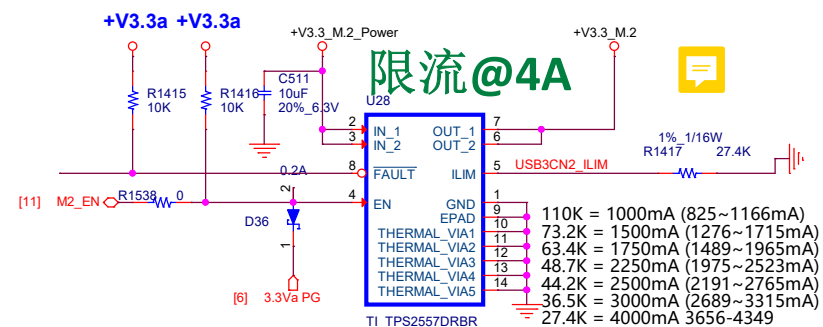
ADVANTECH		
Title M2 PCIe USB CLK		
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Table 48. Socket 2 Pinout Diagram (Mechanical Key B)

74	3.3V	CONFIG_2	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	CONFIG_1	69
66	SIM Detect (O)	Reset# (O)(0/1.8V)	67
64	COEX1 (I/O)(0/1.8V)	ANTCTL3 (I)(0/1.8V)	65
62	COEX2 (I/O)(0/1.8V)	ANTCTL2 (I)(0/1.8V)	63
60	COEX3 (I/O)(0/1.8V)	ANTCTL1 (I)(0/1.8V)	61
58	N/C	ANTCTL0 (I)(0/1.8V)	59
56	N/C	GND	57
54	PEWake# (IO)(0/3.3V)	REFCLKP	55
52	CLKREQ# (IO)(0/3.3V)	REFCLKN	53
50	PERST# (O)(0/3.3V)	GND	51
48	GPIO_4 (IO)(0/1.8V*)	PETp0/SATA-A+	49
46	GPIO_3 (IO)(0/1.8V*)	PETn0/SATA-A-	47
44	GPIO_2 (IO)(0/1.8V*)	GND	45
42	GPIO_1 (IO)(0/1.8V*)	PERp0/SATA-B-	43
40	GPIO_0 (IO)(0/1.8V*)	PERn0/SATA-B+	41
38	DEVSLP (O)(0/3.3V)	GND	39
36	UIM-PWR (I)	PETp1/USB3.0-Tx+/SSIC-TxP	37
34	UIM-DATA (IO)	PETn1/USB3.0-Tx-/SSIC-TxN	35
32	UIM-CLK (I)	GND	33
30	UIM-RESET (I)	PERp1/USB3.0-Rx+/SSIC-RxP	31
28	GPIO_8 (IO) (0/1.8V)	PERn1/USB3.0-Rx-/SSIC-RxN	29
26	GPIO_10 (IO) (0/1.8V)	GND	27
24	GPIO_7 (IO) (0/1.8V)	GPIO_12 (IO) (0/1.8V)	25
22	GPIO_6 (IO)(0/1.8V)	GPIO_11 (IO) (0/1.8V)	23
20	GPIO_5 (IO)(0/1.8V)	CONFIG_0	21
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
10	GPIO_9/DAS/DSS# (I)(OD)	GND	11
8	W_DISABLE#1 (O)(0/3.3V)	USB_D-	9
6	Full_Card_Power_Off# (O)(0/1.8V)	USB_D+	7
4	3.3V	GND	5
2	3.3V	GND	3
		CONFIG_3	1

	Pin	Port Config_0 ¹	Port Config_1 ²	Port Config_2 ³	Port Config_3 ⁴
GPIO_0	40	GNSS_SCL	GNSS_SCL	SIM_DET2	IPC_0
GPIO_1	42	GNSS_SDA	GNSS_SDA	UIM_DTA2	IPC_1
GPIO_2	44	GNSS_IRQ	GNSS_IRQ	UIM_CLK2	IPC_2
GPIO_3	46	SYSCLK	GNSS_0	UIM_RST2	IPC_3
GPIO_4	48	TX_BLANKING	GNSS_1	UIM_PWR2	IPC_4
GPIO_5	20	AUDIO_0	AUDIO_0	RFU	AUDIO_0
GPIO_6	22	AUDIO_1	AUDIO_1	RFU	AUDIO_1
GPIO_7	24	AUDIO_2	AUDIO_2	RFU	IPC_5/AUDIO_2
GPIO_8	28	AUDIO_3	AUDIO_3	RFU	IPC_6/AUDIO_3
GPIO_9 ^{5,6}	10	LED_1#	LED_1#	LED_1#	IPC_7
GPIO_10	26	W_DISABLE2#	W_DISABLE2#	W_DISABLE2#	HSIC_STROBE
GPIO_11	23	WAKE_ON_WWAN#	WAKE_ON_WWAN#	WAKE_ON_WWAN#	HSIC_DATA

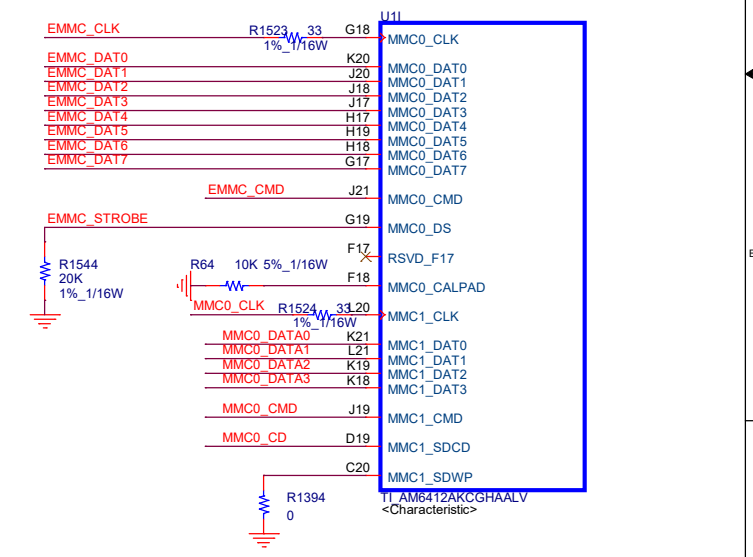
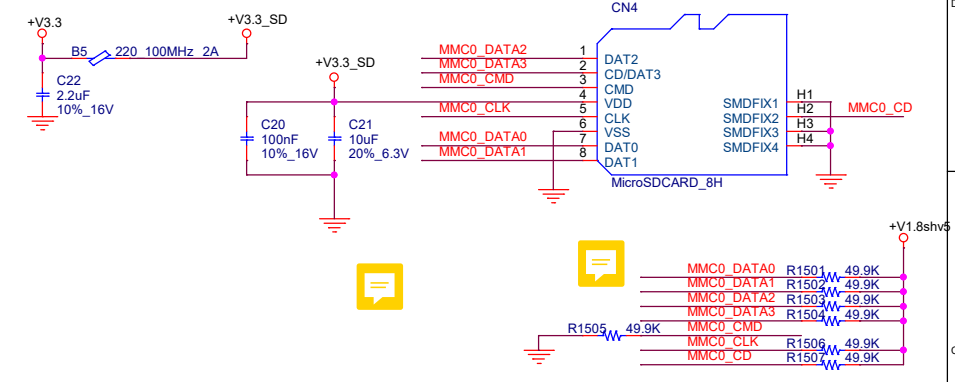
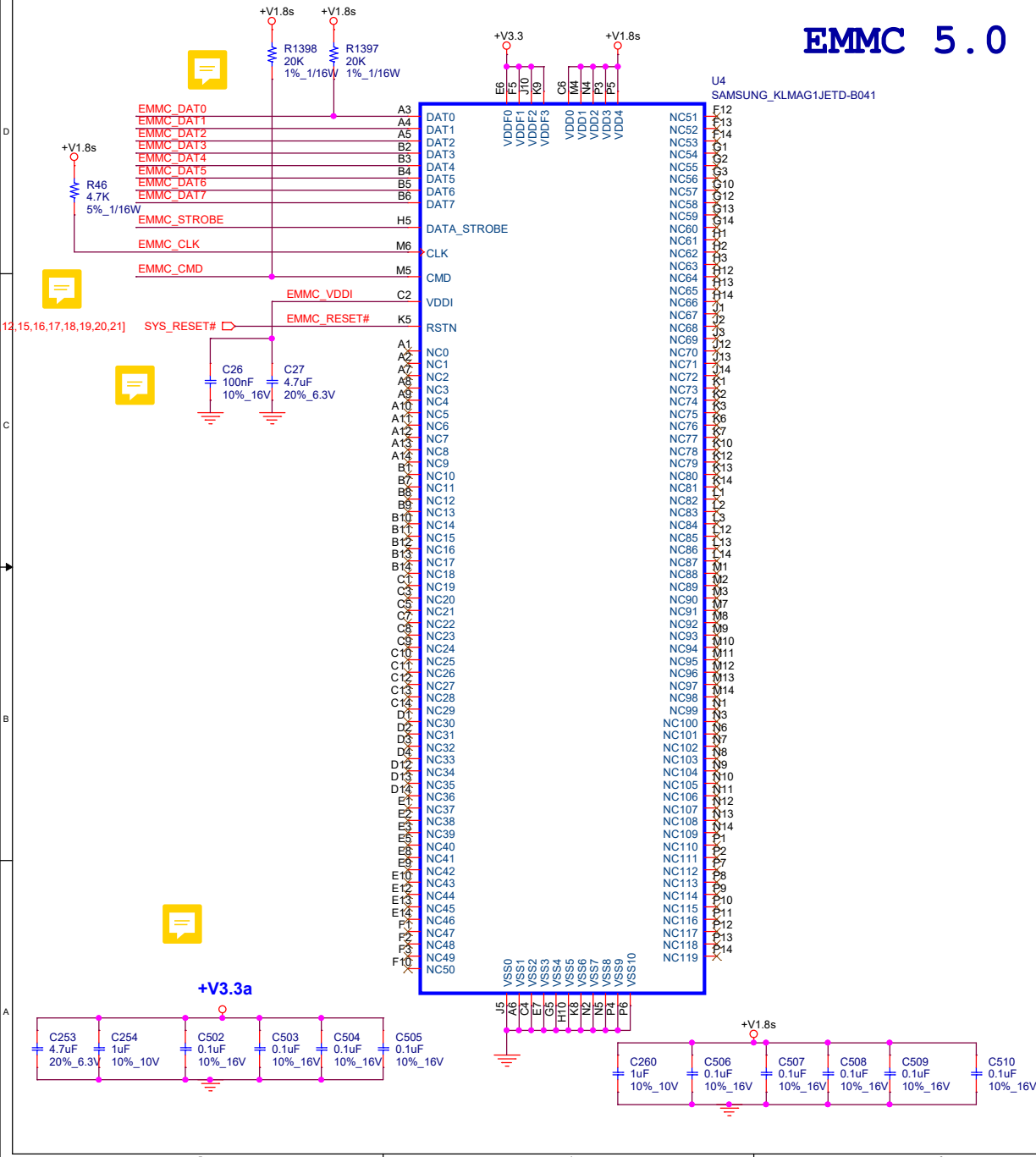
State #	Module Configuration Decodes				Module Type and Main Host Interface ¹	Port Configuration ²
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A
2	GND	GND	N/C	GND	WWAN – PCIe	0
3	GND	N/C	N/C	GND	WWAN – PCIe	1
12	N/C	GND	GND	N/C	WWAN – PCIe	2
13	N/C	N/C	GND	N/C	WWAN – PCIe	3
14	N/C	GND	N/C	N/C	RFU	N/A
15	N/C	N/C	N/C	N/C	No Module Present	N/A



ADVANTECH		
Title M2 Pin Definition&Power		
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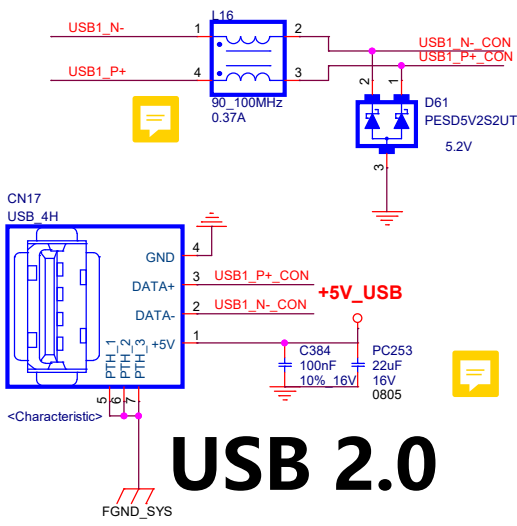
EMMC 5.0

SD Card

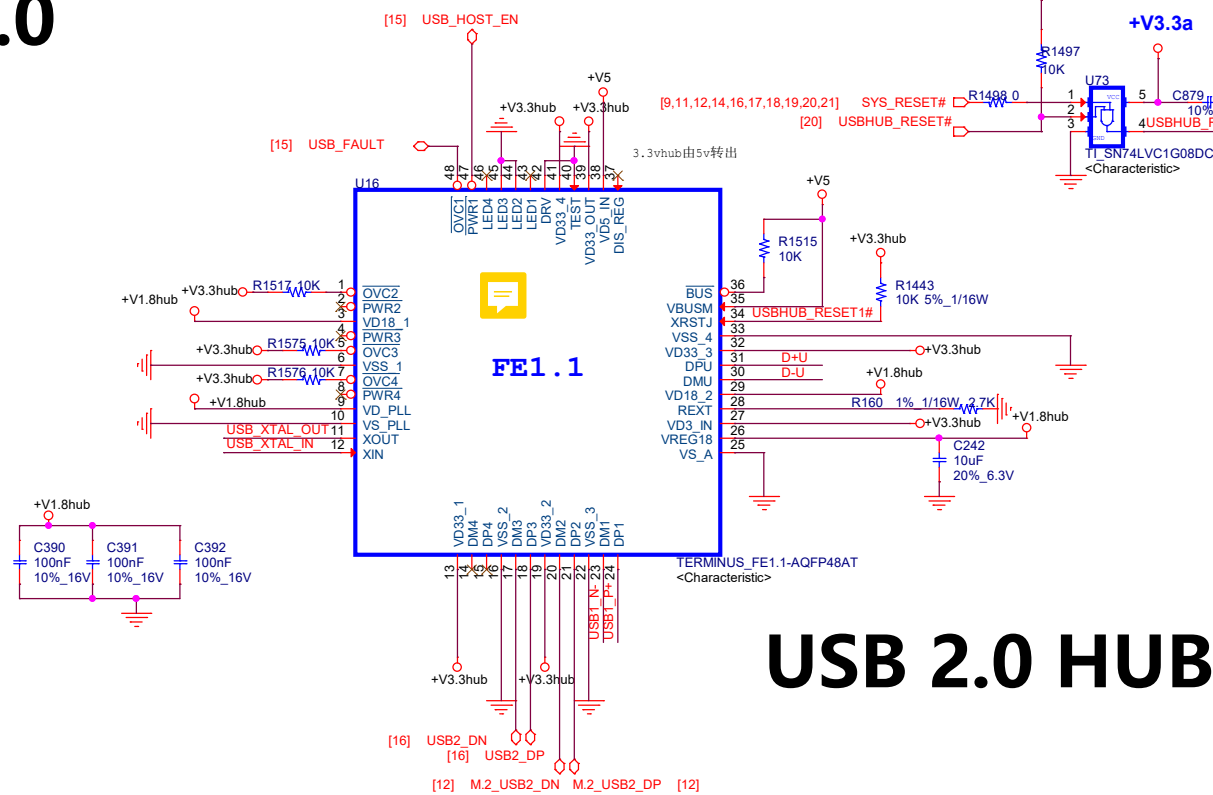
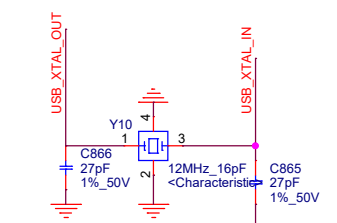
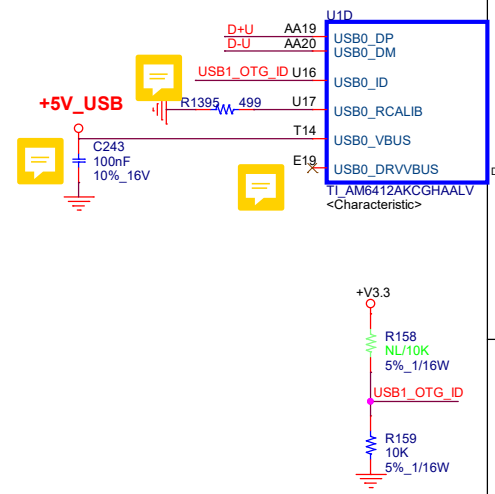
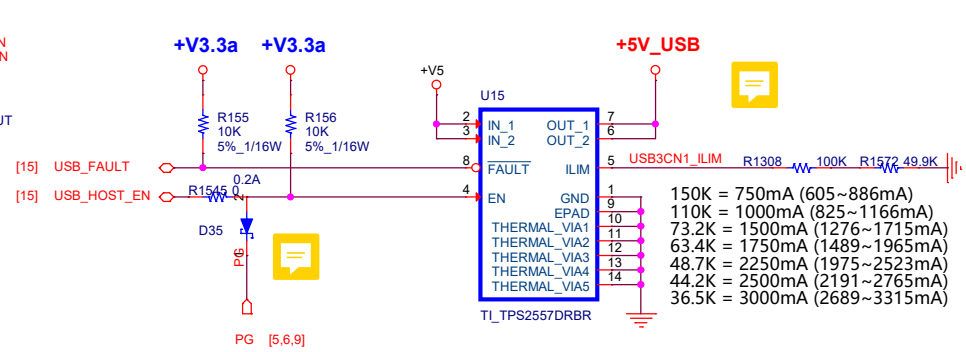


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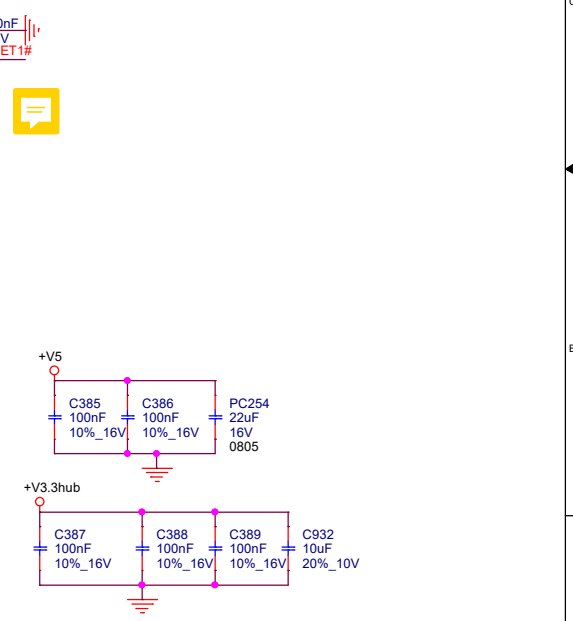
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USB 2.0



USB 2.0 HUB



<Variant Name>

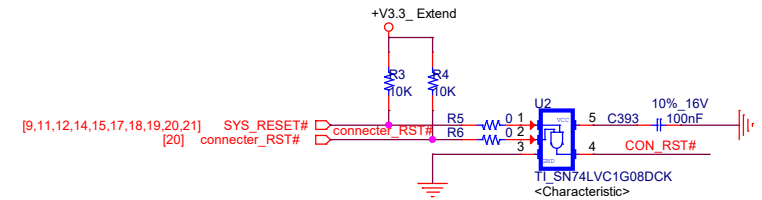
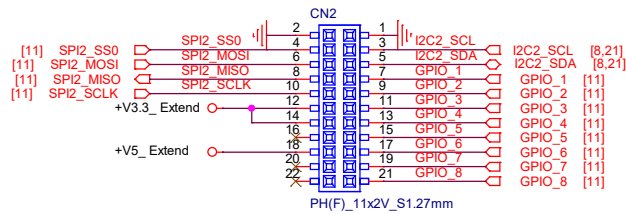
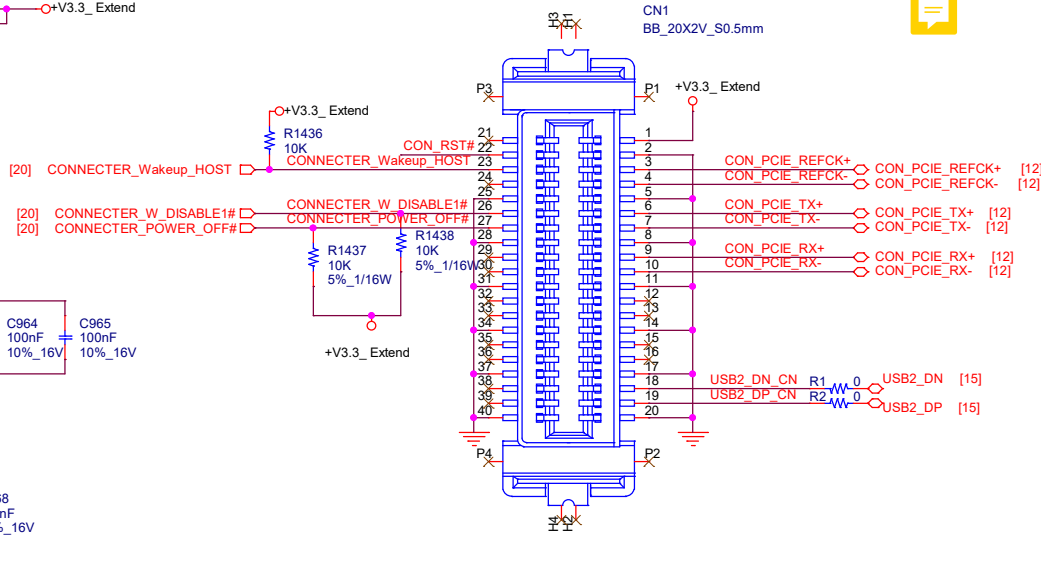
ADVANTECH	
Title USB2.0&HUB	
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Extend Interface

+V5 +V5_Extend

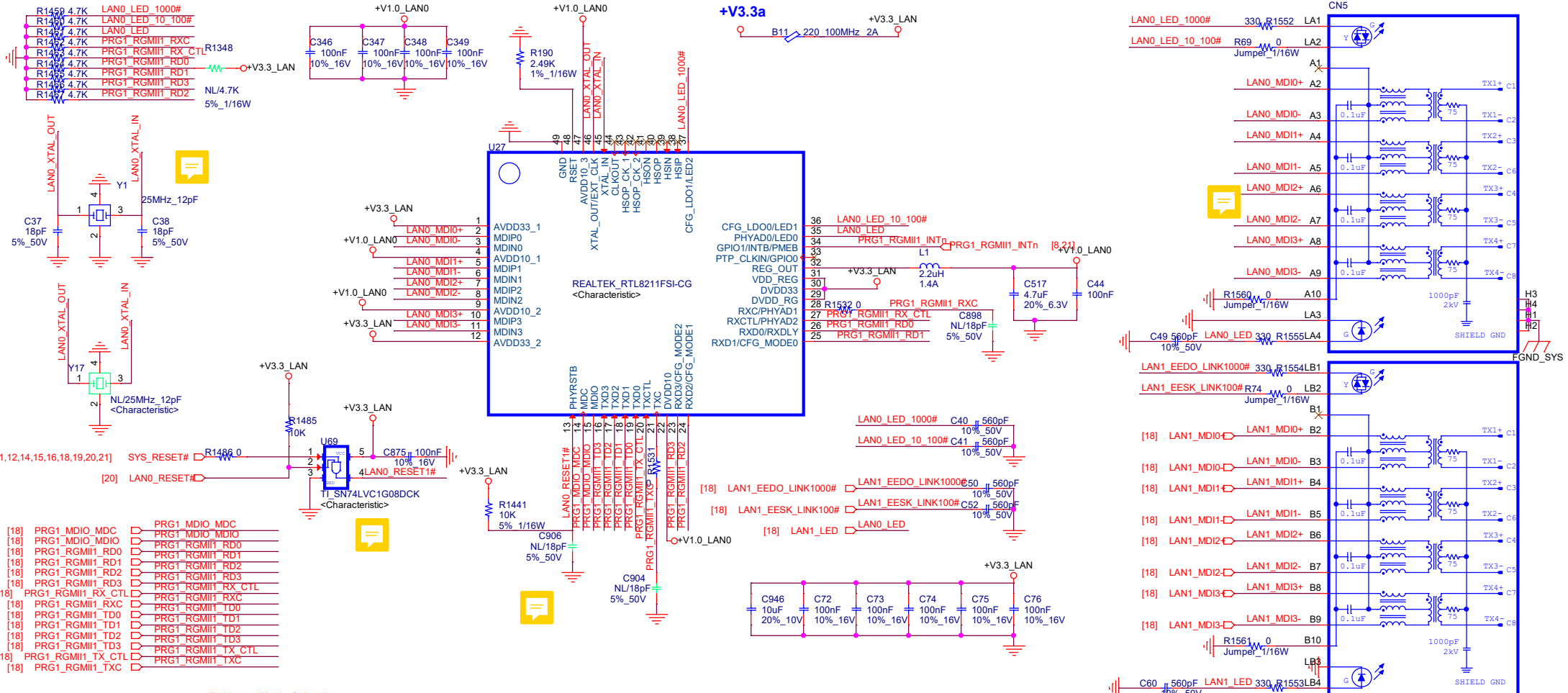
+V3.3a

+V3.3_Extend



<Variant Name>

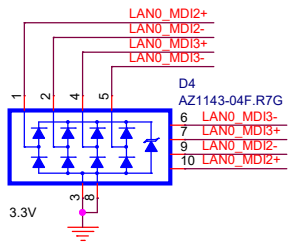
ADVANTECH		
CONNECTER		
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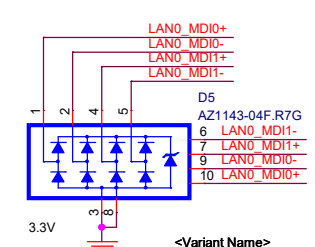
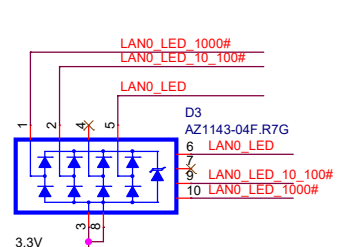
- [18] PRG1_MDIO_MDC ○ PRG1_MDIO_MDC
- [18] PRG1_MDIO_MDIO ○ PRG1_MDIO_MDIO
- [18] PRG1_RGMII1_RD0 ○ PRG1_RGMII1_RD0
- [18] PRG1_RGMII1_RD1 ○ PRG1_RGMII1_RD1
- [18] PRG1_RGMII1_RD2 ○ PRG1_RGMII1_RD2
- [18] PRG1_RGMII1_RD3 ○ PRG1_RGMII1_RD3
- [18] PRG1_RGMII1_RX_CTL ○ PRG1_RGMII1_RX_CTL
- [18] PRG1_RGMII1_RXC ○ PRG1_RGMII1_RXC
- [18] PRG1_RGMII1_TD0 ○ PRG1_RGMII1_TD0
- [18] PRG1_RGMII1_TD1 ○ PRG1_RGMII1_TD1
- [18] PRG1_RGMII1_TD2 ○ PRG1_RGMII1_TD2
- [18] PRG1_RGMII1_TD3 ○ PRG1_RGMII1_TD3
- [18] PRG1_RGMII1_TX_CTL ○ PRG1_RGMII1_TX_CTL
- [18] PRG1_RGMII1_TXC ○ PRG1_RGMII1_TXC

Table 8. Mode Selection

Pin No.	Pin Name	Type	Description
35	PHYAD0	O/LI/PU	PHYAD[2:0]. PHY Address Configuration.
28	PHYAD1	O/LI/PD	
27	PHYAD2	O/LI/PD	
26	RXDLY	O/LI/PU	RGMII Receiver Clock Timing Control. Pull up to add 2ns delay to RXC for RXD latching. <i>Note: On the other hand, enabling of TXDLY is left in the register setting: Page 0xd08, Reg 17, Bit[8] = 1.</i>
36	CFG_LDO0	O/LI/PU	Voltage Selection for I/O Pad. 2'b00: 3.3V.
37	CFG_LDO1	O/LI/PD	2'b01: 2.5V. 2'b10: 1.8V. 2'b11: 1.5V.
25	CFG_MODE0	O/PD	Operation Mode.
24	CFG_MODE1	O/PD	3'b000: UTP ↔ RGMII
23	CFG_MODE2	O/PD	3'b001: FIBER ↔ RGMII 3'b010: UTP/FIBER ↔ RGMII (Media Auto Detection) 3'b011: UTP ↔ SGMII 3'b100: SGMII (PHY side) ↔ RGMII (MAC side) 3'b101: SGMII (MAC side) ↔ RGMII (PHY side) 3'b110: UTP ↔ FIBER (Media Conversion auto mode) 3'b111: UTP ↔ FIBER (Media Conversion force mode)



PIN对应关系在LAN2



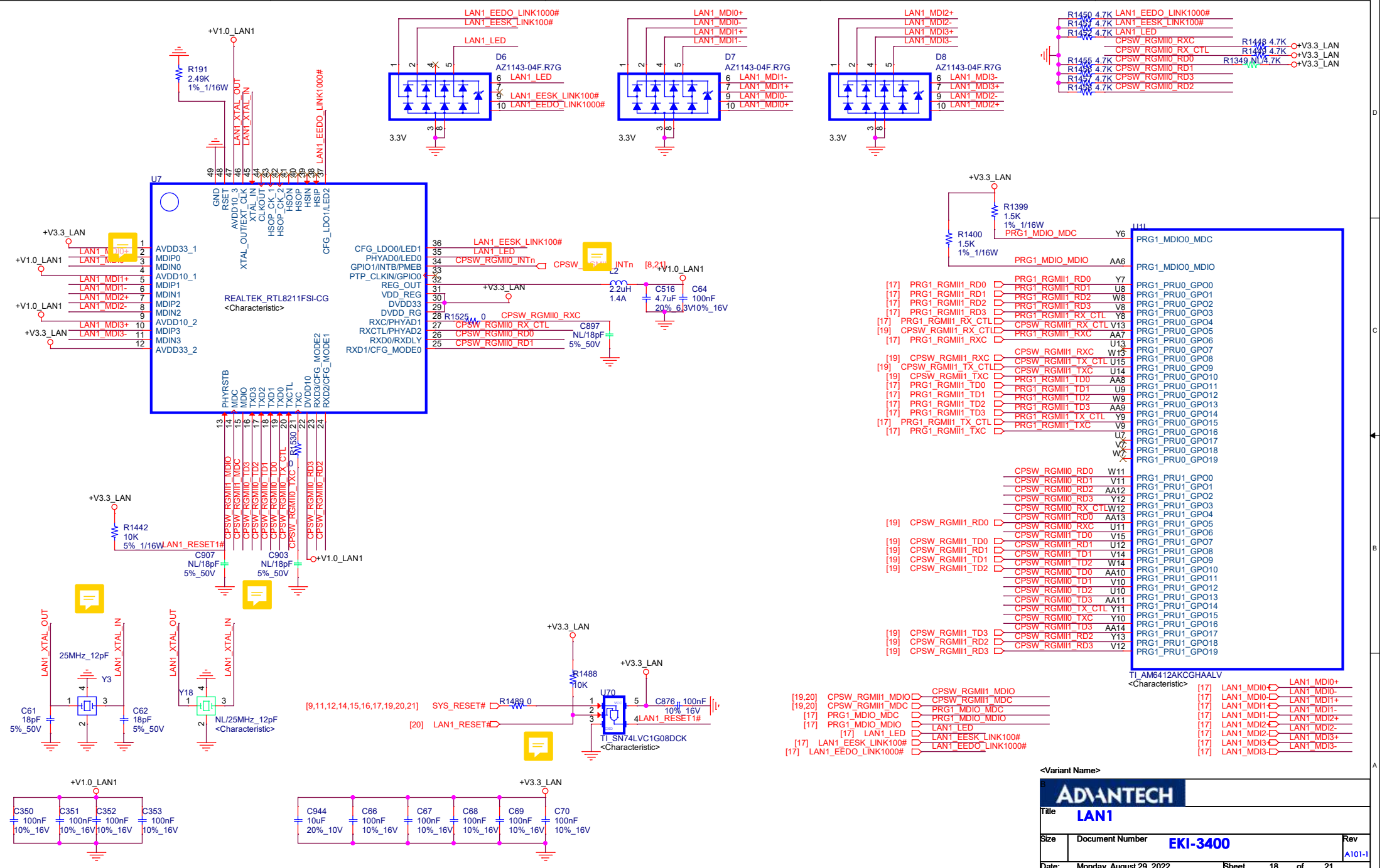
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[17] PRG1_RGMIIH_RD0	PRG1_RGMIIH_RD0	Y7	PRG1_PRU0_GP00
[17] PRG1_RGMIIH_RD1	PRG1_RGMIIH_RD1	U8	PRG1_PRU0_GP01
[17] PRG1_RGMIIH_RD2	PRG1_RGMIIH_RD2	W8	PRG1_PRU0_GP02
[17] PRG1_RGMIIH_RD3	PRG1_RGMIIH_RD3	V8	PRG1_PRU0_GP03
[17] PRG1_RGMIIH_RD3	PRG1_RGMIIH_RX_CTL	Y8	PRG1_PRU0_GP04
[17] PRG1_RGMIIH_RX_CTL	CPSW_RGMIIH_RX_CTL	V13	PRG1_PRU0_GP05
[19] CPSW_RGMIIH_RX_CTL	PRG1_RGMIIH_RXC	AA7	PRG1_PRU0_GP06
[17] PRG1_RGMIIH_RXC	U13	X	PRG1_PRU0_GP07
[19] CPSW_RGMIIH_RXC	CPSW_RGMIIH_RXC	W13	PRG1_PRU0_GP08
[19] CPSW_RGMIIH_TX_CTL	CPSW_RGMIIH_TXC	U15	PRG1_PRU0_GP09
[19] CPSW_RGMIIH_TXC	PRG1_RGMIIH_TD0	U4	PRG1_PRU0_GP10
[17] PRG1_RGMIIH_TD0	PRG1_RGMIIH_TD1	U9	PRG1_PRU0_GP11
[17] PRG1_RGMIIH_TD1	PRG1_RGMIIH_TD2	W9	PRG1_PRU0_GP12
[17] PRG1_RGMIIH_TD2	PRG1_RGMIIH_TD3	AA9	PRG1_PRU0_GP13
[17] PRG1_RGMIIH_TD3	PRG1_RGMIIH_TX_CTL	Y9	PRG1_PRU0_GP14
[17] PRG1_RGMIIH_TX_CTL	PRG1_RGMIIH_TXC	V9	PRG1_PRU0_GP15
[17] PRG1_RGMIIH_TXC	U7	X	PRG1_PRU0_GP16
	V7	X	PRG1_PRU0_GP17
	W7	X	PRG1_PRU0_GP18
	X	X	PRG1_PRU0_GP19
	CPSW_RGMIIH_RD0	W11	PRG1_PRU1_GP00
	CPSW_RGMIIH_RD1	V11	PRG1_PRU1_GP01
	CPSW_RGMIIH_RD2	AA12	PRG1_PRU1_GP02
	CPSW_RGMIIH_RD3	Y12	PRG1_PRU1_GP03
	CPSW_RGMIIH_RX_CTL	W12	PRG1_PRU1_GP04
	CPSW_RGMIIH_RXC	AA13	PRG1_PRU1_GP05
	CPSW_RGMIIH_TXC	V15	PRG1_PRU1_GP06
[19] CPSW_RGMIIH_RD0	CPSW_RGMIIH_RD1	U12	PRG1_PRU1_GP07
[19] CPSW_RGMIIH_RD1	CPSW_RGMIIH_RD2	V14	PRG1_PRU1_GP08
[19] CPSW_RGMIIH_RD2	CPSW_RGMIIH_TD1	W14	PRG1_PRU1_GP09
[19] CPSW_RGMIIH_RD3	CPSW_RGMIIH_TD0	AA10	PRG1_PRU1_GP10
	CPSW_RGMIIH_TD1	V10	PRG1_PRU1_GP11
	CPSW_RGMIIH_TD2	U10	PRG1_PRU1_GP12
	CPSW_RGMIIH_TD3	AA11	PRG1_PRU1_GP13
	CPSW_RGMIIH_TX_CTL	Y11	PRG1_PRU1_GP14
	CPSW_RGMIIH_TXC	Y10	PRG1_PRU1_GP15
	CPSW_RGMIIH_TD3	AA14	PRG1_PRU1_GP16
[19] CPSW_RGMIIH_TD3	CPSW_RGMIIH_RD2	Y13	PRG1_PRU1_GP17
[19] CPSW_RGMIIH_RD2	CPSW_RGMIIH_RD3	V12	PRG1_PRU1_GP18
[19] CPSW_RGMIIH_RD3			PRG1_PRU1_GP19

[19,20] CPSW_RGMIIH_MDIO	CPSW_RGMIIH_MDIO	[17] LAN1_MDIO0	LAN1_MDIO+
[19,20] CPSW_RGMIIH_MDC	CPSW_RGMIIH_MDC	[17] LAN1_MDIO0	LAN1_MDIO-
[17] PRG1_MDIO_MDC	PRG1_MDIO_MDC	[17] LAN1_MDIO1	LAN1_MDIO+
[17] PRG1_MDIO_MDIO	PRG1_MDIO_MDIO	[17] LAN1_MDIO1	LAN1_MDIO-
[17] LAN1_LED	LAN1_LED	[17] LAN1_MDIO2	LAN1_MDIO+
[17] LAN1_EESK_LINK1000#	LAN1_EESK_LINK1000#	[17] LAN1_MDIO2	LAN1_MDIO-
[17] LAN1_EEDO_LINK1000#	LAN1_EEDO_LINK1000#	[17] LAN1_MDIO3	LAN1_MDIO+
		[17] LAN1_MDIO3	LAN1_MDIO-

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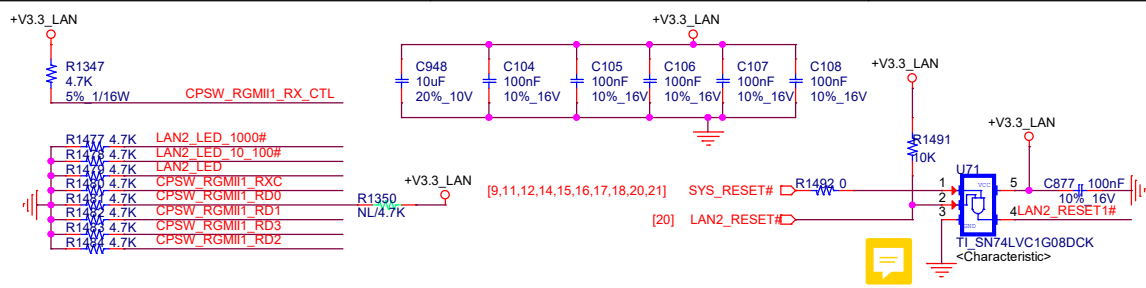
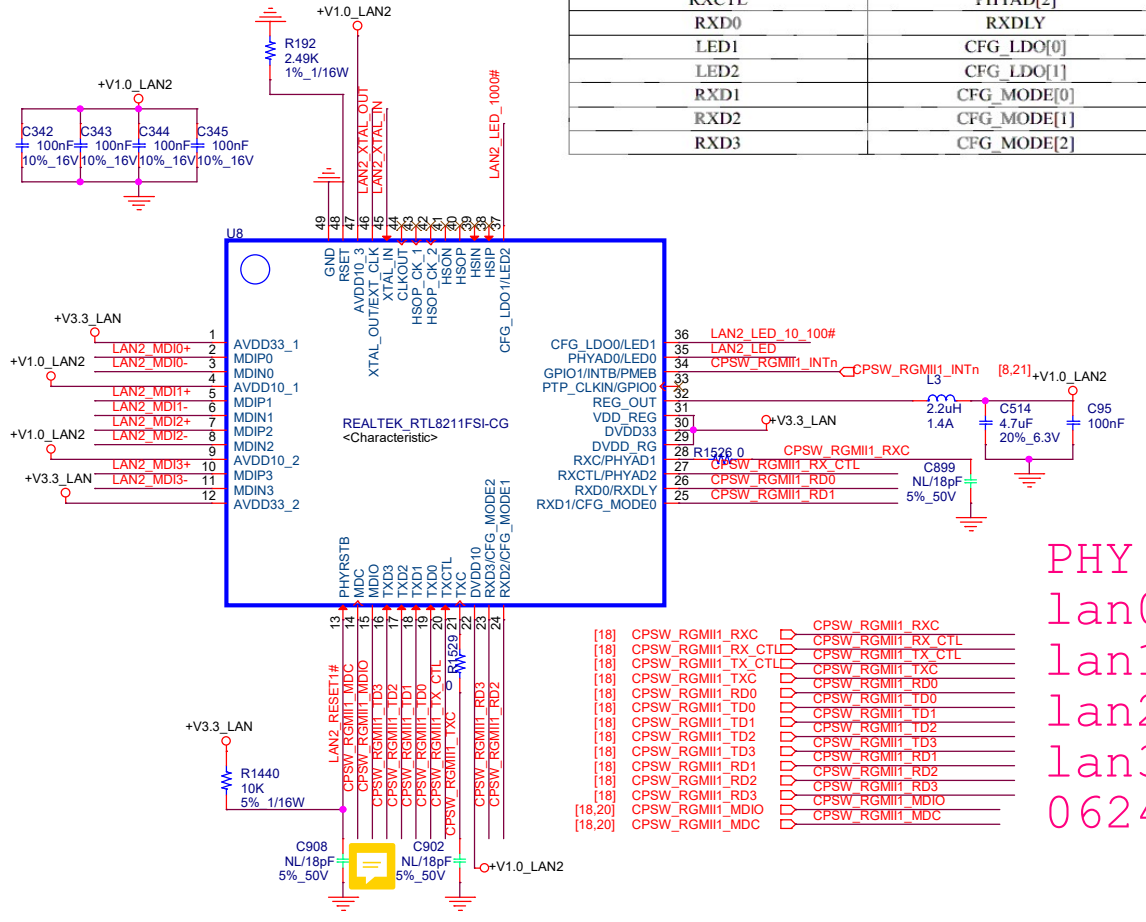


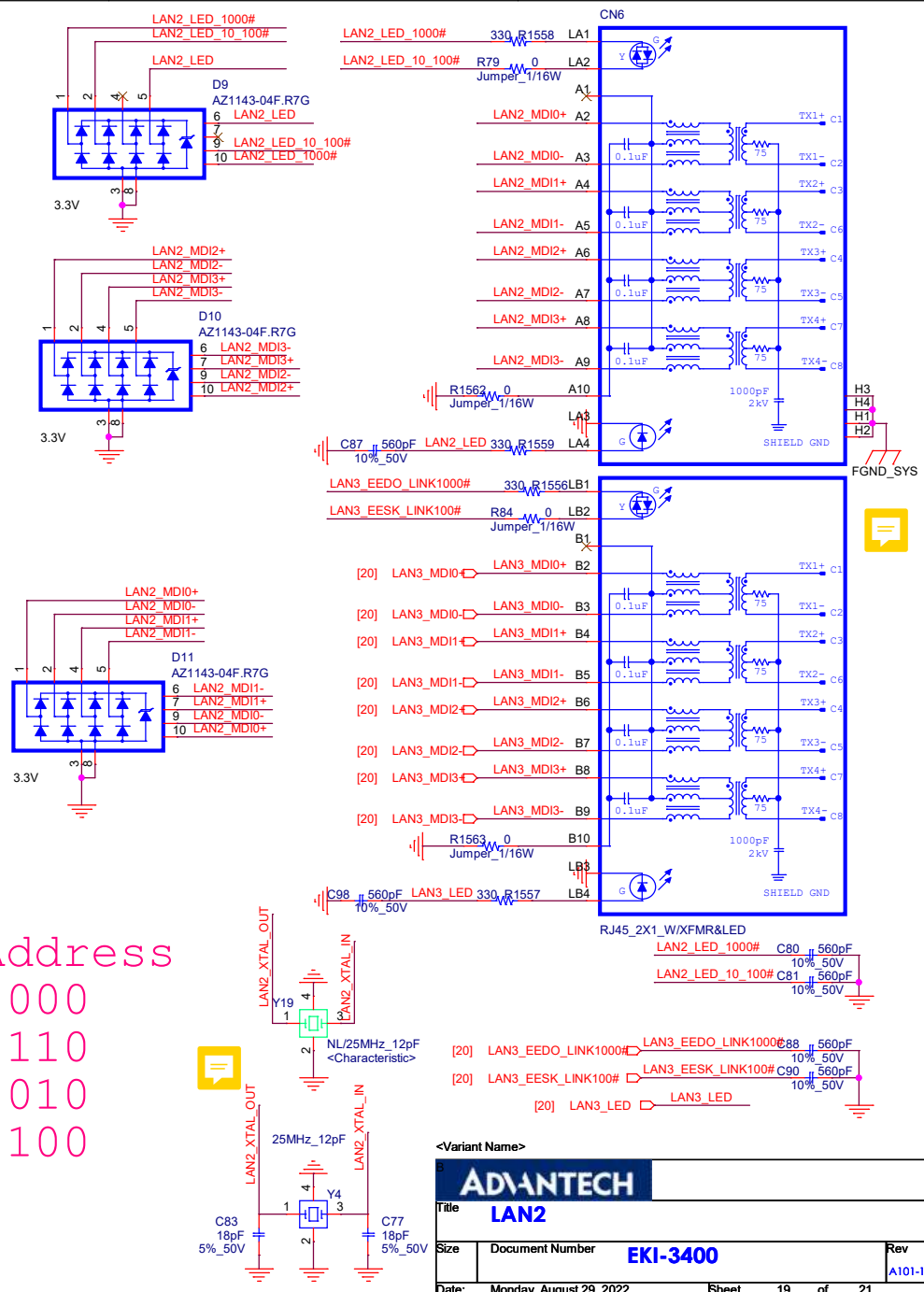
Table 11. CONFIG Pins vs. Configuration Register

CONFIG Pin	Configuration
LED0	PHYAD[0]
RXC	PHYAD[1]
RXCTL	PHYAD[2]
RXD0	RXDLY
LED1	CFG_LDO[0]
LED2	CFG_LDO[1]
RXD1	CFG_MODE[0]
RXD2	CFG_MODE[1]
RXD3	CFG_MODE[2]



PHY Address

lan0	000
lan1	110
lan2	010
lan3	100
	0624

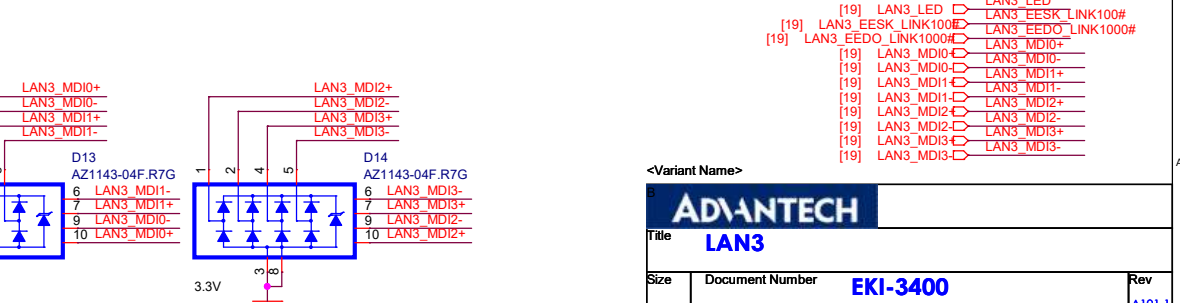
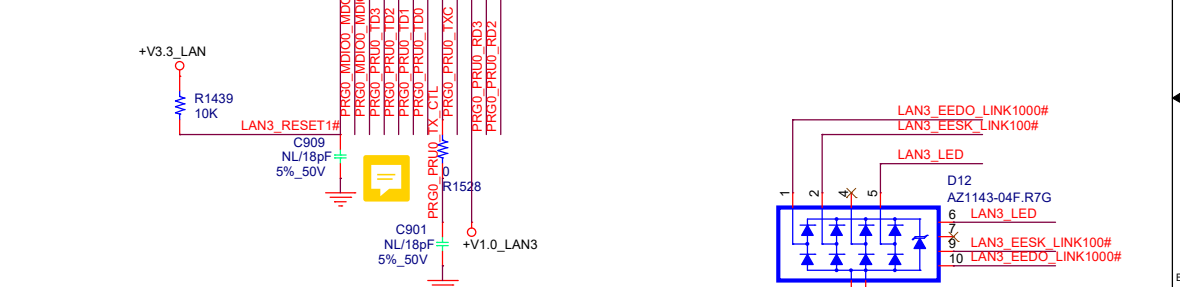
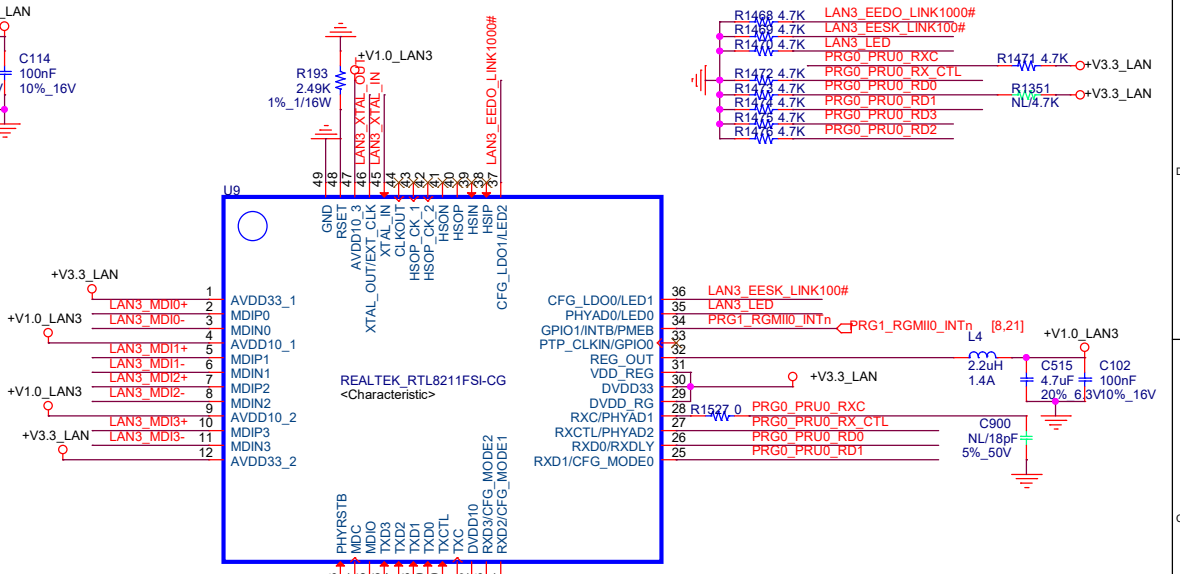
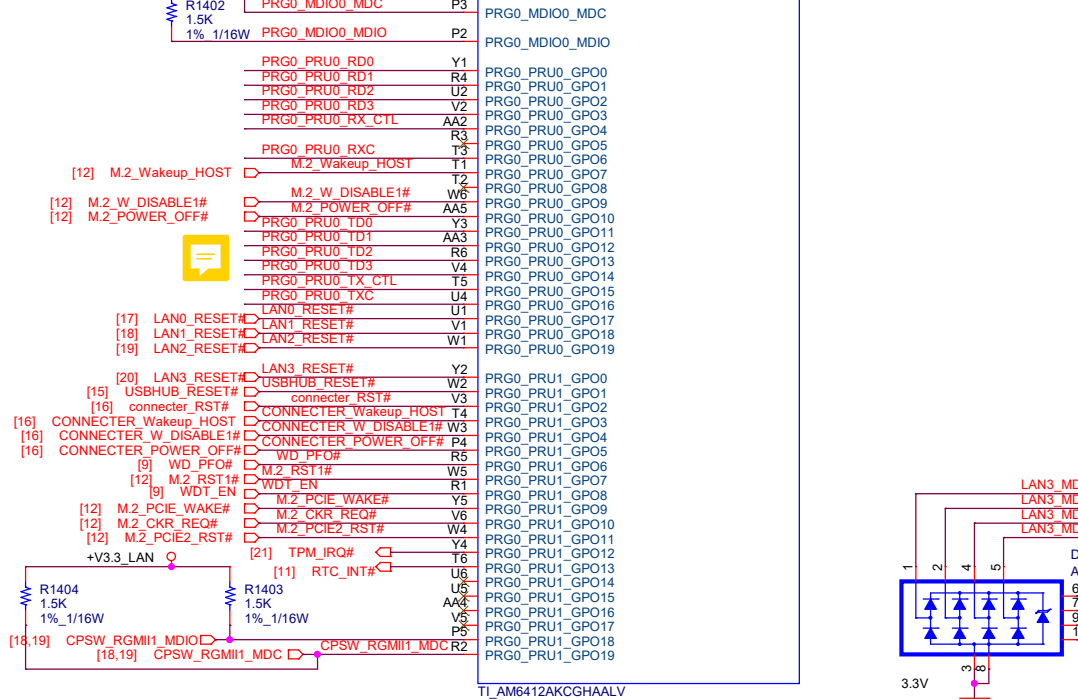
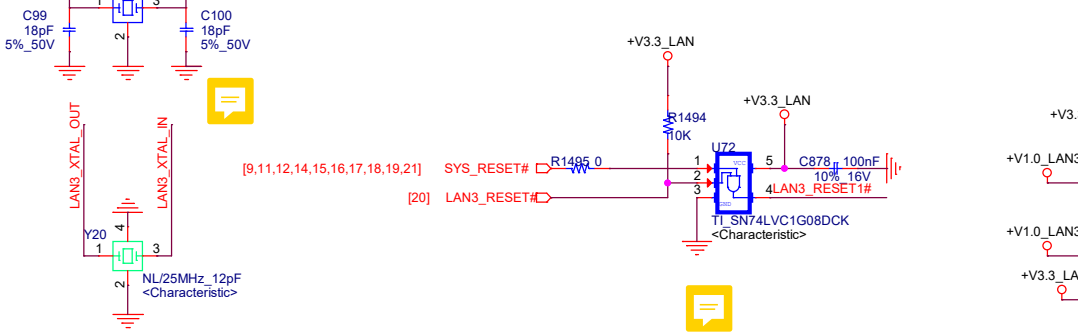
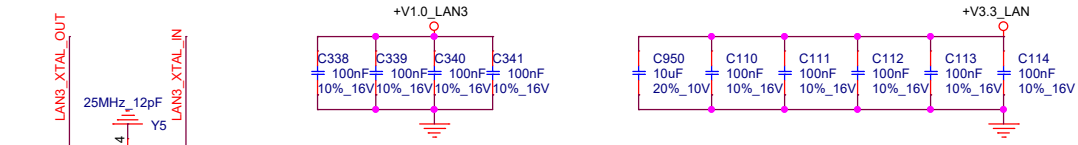


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LAN2

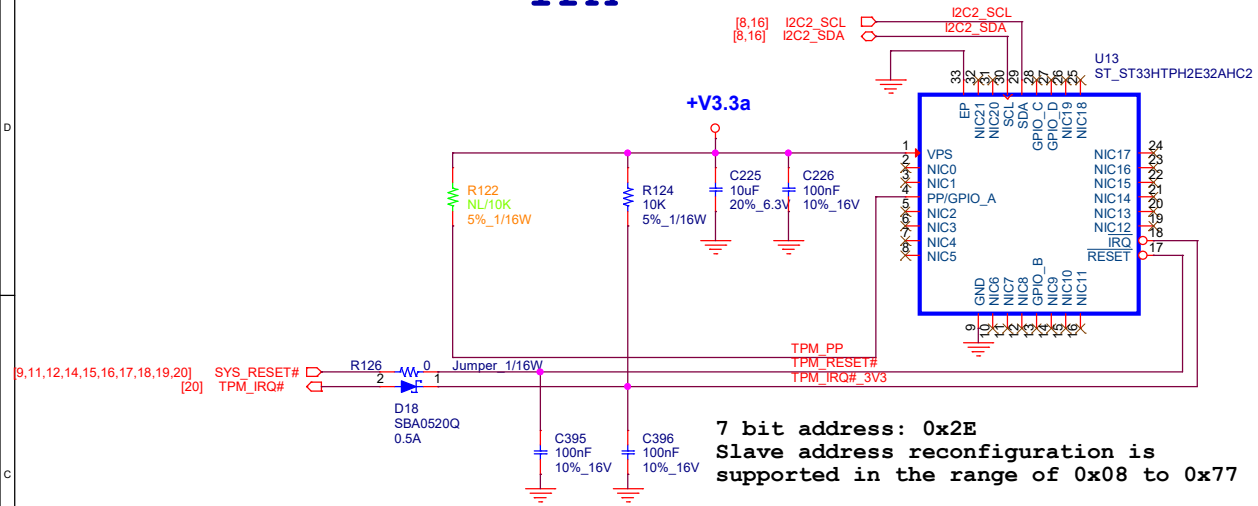
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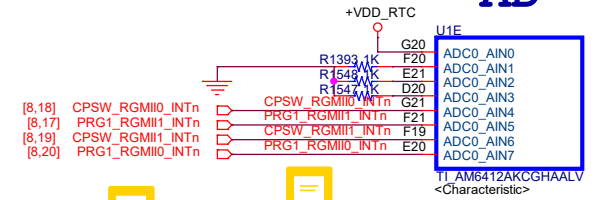
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TPM

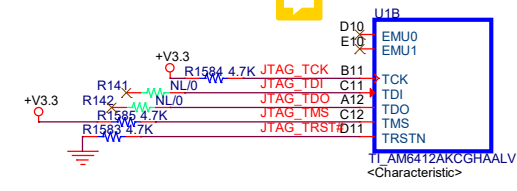


7 bit address: 0x2E
 Slave address reconfiguration is supported in the range of 0x08 to 0x77

AD



JTAG



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