SAMSUNG

Samsung 1xnm LPDDR4 4GB Validation Issue on TDA4 with CBT Enable

Dec. 10th, 2021 | Samsung Electronics

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TI TDA4 & 1xnm LPDDR4 4GB CBT Fail Issue

Issue Description

During 1xnm LPDDR4(Multi-Rank product) validation on TDA4 system, Samsung has found booting fail when CBT is enabled at all speed.

(*validation condition for TDA4 : CBT enable, 4266Mbps + 5% O/C)

Analysis Result

- During SI test with Samsung & other vendor's DRAM, unterminated section was found with Samsung DRAM after finishing Rank0 training
- Through the MR13 value checking for each step of CBT, Samsung found one missing sequence before Rank1 Training on TDA4

> 9. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the high frequency operating point.

→ Turning on termination(ODT) for high frequency operation is missing before Rank1(after Rank0) training.

(*CBT training is performed in a high frequency environment.)

- Samsung has tried TI's suggestion and turned out issue was resolved in case of turning on termination(ODT) in the entire CBT training process

→ Memtester Test Passed on CBT Enable at 4266Mbps + 5% O/C, each Temp.(-40℃/ 25 ℃/ 125 ℃), each VDD(LVDD/ NVDD/ HVDD)

Conclusion & Suggestion

- Samsung concluded that this issue occurred because TDA4 did not follow the LP4 CBT sequence in a specific part.
- There are two options for resolving the issue.

Option1. To apply LP4 CBT sequence of JEDEC on TDA4 (by TI) and change the Frequency set condition at DDRSS file.

Option2. To change the Frequency Set condition to operate Samsung DRAM without changing CBT sequence.

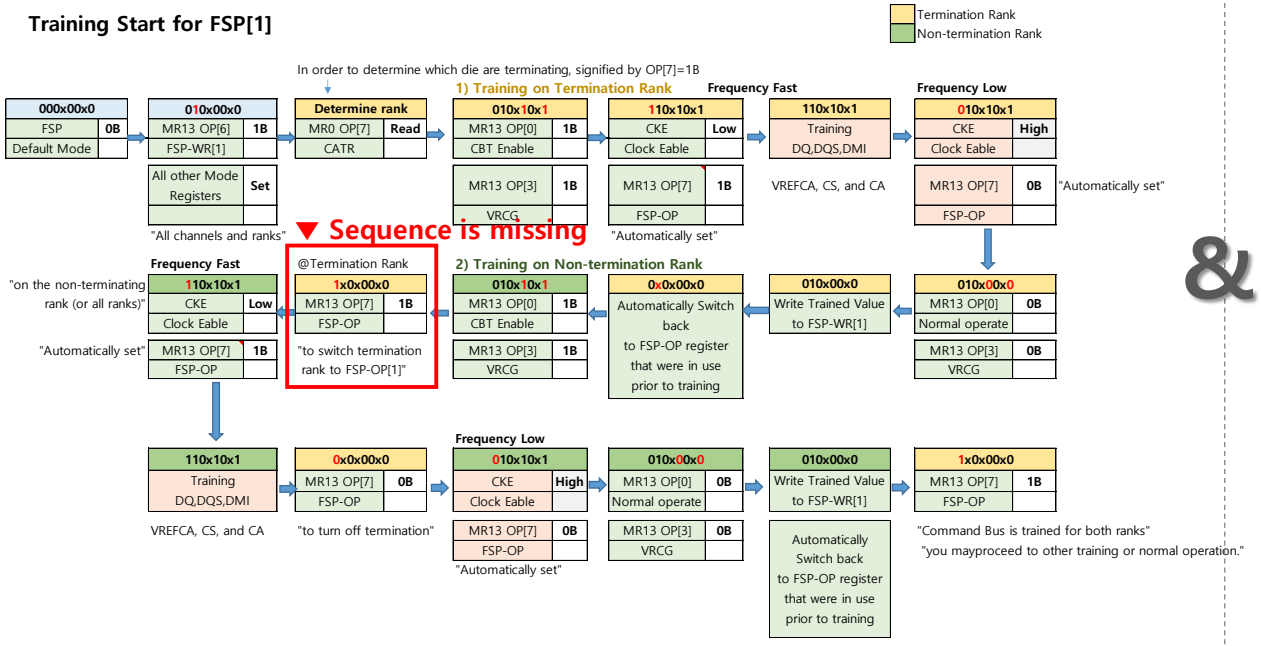
: This option has been proposed by TI and optimized by Samsung and can be applied immediately. However, the CBT sequence still does not follow the JEDEC Spec.

#Option1. CBT Sequence & Frequency Set Condition Change

① To apply LP4 CBT sequence of JEDEC on TDA4 (by TI)

(JEDEC Spec. No. 209-4D Page 191.)

: Need to add the missing sequence.



② To change the Frequency Set condition for Samsung DRAM on XLS Tool(DDRSS File)

: Need to find the appropriate condition after changing CBT sequence.

&

Parameter Group	Parameter	Frequency Set 0	Frequency Set 1	Frequency Set 2	Units	Notes
VREF Control	DQ VREF Range	Range 0	Range 0	Range 0	-	2
	DQ VREF	16	16	16	% of VDDQ	2
	CA VREF Range	Range 0	Range 0	Range 0	-	2
	CA VREF	25.6	25.6	25.6	% of VDDQ	2
Drive Strength	Pull-Down (PDDS)	RZQ/5	RZQ/5	RZQ/5	Ohms	2, 3
	Pull Up Calibration	VDDQ / 3	VDDQ / 3	VDDQ / 3	-	2
Termination	CA ODT Disable	ODT_CA Bond Pad	ODT_CA Bond Pad	ODT_CA Bond Pad	-	2
	CK ODT Override	Disable	Enable	Enable	-	2
	CS ODT Override	Enable	Enable	Enable	-	2
	CA ODT	Disable	RZQ/4	RZQ/4	Ohms	2, 3
	DQ ODT	Disable	RZQ/5	RZQ/5	Ohms	2, 3
	SOC ODT	RZQ/5	RZQ/5	RZQ/5	Ohms	1, 2, 3

Example

※ Please refer to slide 10 (JEDEC Spec. No.10 209-4D Page 191)

#Option2. Frequency Set Condition Change (Nov.4th '2021)

To change the Frequency Set condition to operate Samsung DRAM without changing CBT sequence

Parameter Group	Parameter	Frequency Set 0	Frequency Set 1	Frequency Set 2	Units	Notes
VREF Control	DQ VREF Range	Range 0	Range 0	Range 0	-	2
	DQ VREF	~~10~~ → 16	16	16	% of VDDQ	2
	CA VREF Range	Range 0	Range 0	Range 0	-	2
	CA VREF	~~10~~ → 25.6	25.6	25.6	% of VDDQ	2
Drive Strength	Pull-Down (PDDS)	RZQ/6	RZQ/6	RZQ/6	Ohms	2, 3
	Pull Up Calibration	VDDQ / 3	VDDQ / 3	VDDQ / 3	-	2
Termination	CA ODT Disable	ODT_CA Bond Pad	ODT_CA Bond Pad	ODT_CA Bond Pad	-	2
	CK ODT Override	~~Disable~~ → Enable	~~Disable~~ → Enable	~~Disable~~ → Enable	-	2
	CS ODT Override	Enable	Enable	Enable	-	2
	CA ODT	~~Disable~~ → RZQ/4	~~RZQ/5~~ → RZQ/4	~~RZQ/5~~ → RZQ/4	Ohms	2, 3
	DQ ODT	~~Disable~~ → RZQ/6	RZQ/6	RZQ/6	Ohms	2, 3
	SOC ODT	RZQ/6	RZQ/6	RZQ/6	Ohms	1, 2, 3

#Option2. Frequency Set Condition Change (Updated on Dec.10th '2021)

It is necessary that additional modifications (in orange colored cell) being applied to optimize the performance under temp.(-40~125'c) and various VDD conditions.

A) Processor / DDR Controller IO Configuration

Parameter Group	Parameter	Data Lane 0		Data Lane 1		Data Lane 2		Data Lane 3		Address / Command				
		DQ / DM	DQS	DQ / DM	DQS	DQ / DM	DQS	DQ / DM	DQS	CA[5:0]	Clock	CKE	RST	CS
VREF Control	Range	Range 0	Range 0	Range 0	Range 0	Range 0	Range 0	Range 0	Range 0	Range 0	Range 0	Range 0	Range 0	Range 0
	% of VDDQ	16.7	16.7	16.7	16.7	16.7	16.7	16.7	16.7	16.7	16.7	16.7	16.7	16.7
Drive Strength	Driver Pull-Up	~~40~~ → 48 Ohm	~~40~~ → 48 Ohm	40 Ohm	40 Ohm	40 Ohm	40 Ohm	40 Ohm	40 Ohm	34.3 Ohm	34.3 Ohm	34.3 Ohm	34.3 Ohm	34.3 Ohm
	Driver Pull-Down	~~40~~ → 48 Ohm	~~40~~ → 48 Ohm	40 Ohm	40 Ohm	40 Ohm	40 Ohm	40 Ohm	40 Ohm	34.3 Ohm	34.3 Ohm	34.3 Ohm	34.3 Ohm	34.3 Ohm
Termination	ODT Pull-Up	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z					
	ODT Pull-Down	~~40~~ → 48 Ohm	~~40~~ → 48 Ohm	40 Ohm	40 Ohm	40 Ohm	40 Ohm	40 Ohm	40 Ohm					

B) DRAM IO Configuration

Parameter Group	Parameter	Frequency Set 0	Frequency Set 1	Frequency Set 2	Units	Notes
VREF Control	DQ VREF Range	Range 0	Range 0	Range 0	-	2
	DQ VREF	16	16	16	% of VDDQ	2
	CA VREF Range	Range 0	Range 0	Range 0	-	2
	CA VREF	25.6	25.6	25.6	% of VDDQ	2
Drive Strength	Pull-Down (PDDS)	~~RZQ/6~~ → RZQ/5	~~RZQ/6~~ → RZQ/5	~~RZQ/6~~ → RZQ/5	Ohms	2, 3
	Pull Up Calibration	VDDQ / 3	VDDQ / 3	VDDQ / 3	-	2
Termination	CA ODT Disable	ODT_CA Bond Pad	ODT_CA Bond Pad	ODT_CA Bond Pad	-	2
	CK ODT Override	Enable	Enable	Enable	-	2
	CS ODT Override	Enable	Enable	Enable	-	2
	CA ODT	RZQ/4	RZQ/4	RZQ/4	Ohms	2, 3
	DQ ODT	~~RZQ/6~~ → RZQ/5	~~RZQ/6~~ → RZQ/5	~~RZQ/6~~ → RZQ/5	Ohms	2, 3
	SOC ODT	~~RZQ/6~~ → RZQ/5	~~RZQ/6~~ → RZQ/5	~~RZQ/6~~ → RZQ/5	Ohms	1, 2, 3

* Yellow colored Cell : Initial modification.
* Orange colored Cell : Additional modification.

* In addition to suggested solution by TI, Samsung has modified some freq. set conditions and IO config. Additionally.

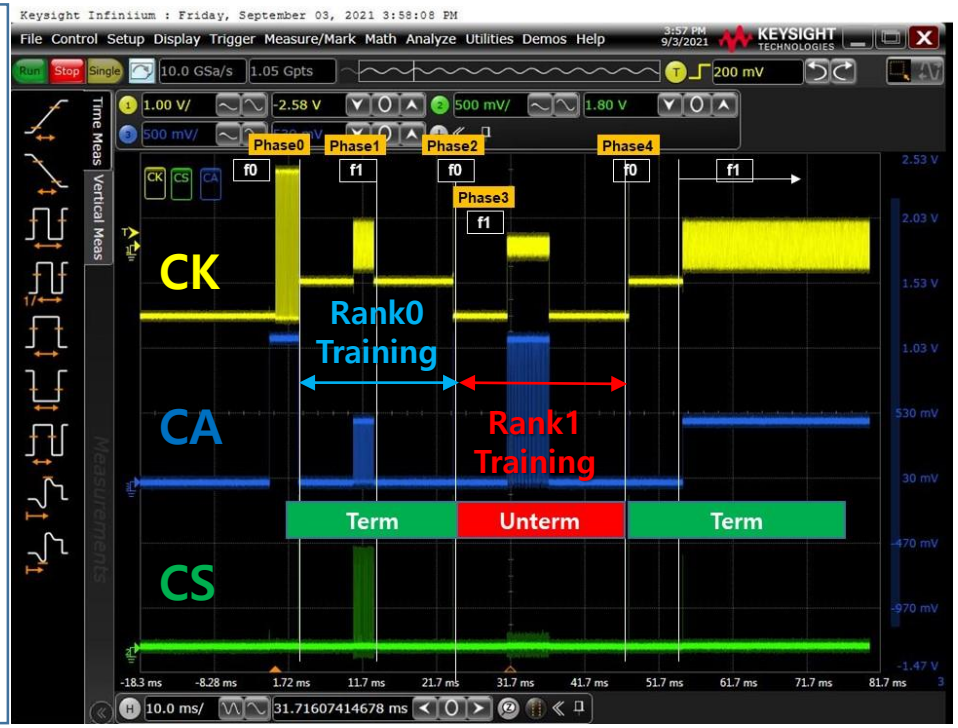
* In case of Option#2, the CBT sequence still does not follow JEDEC spec.

A journey shared takes us beyond

<Appendix> SI_Booting SI Comparison @Default Setting

1. Unterminated section was found with Samsung DRAM

Samsung



Log

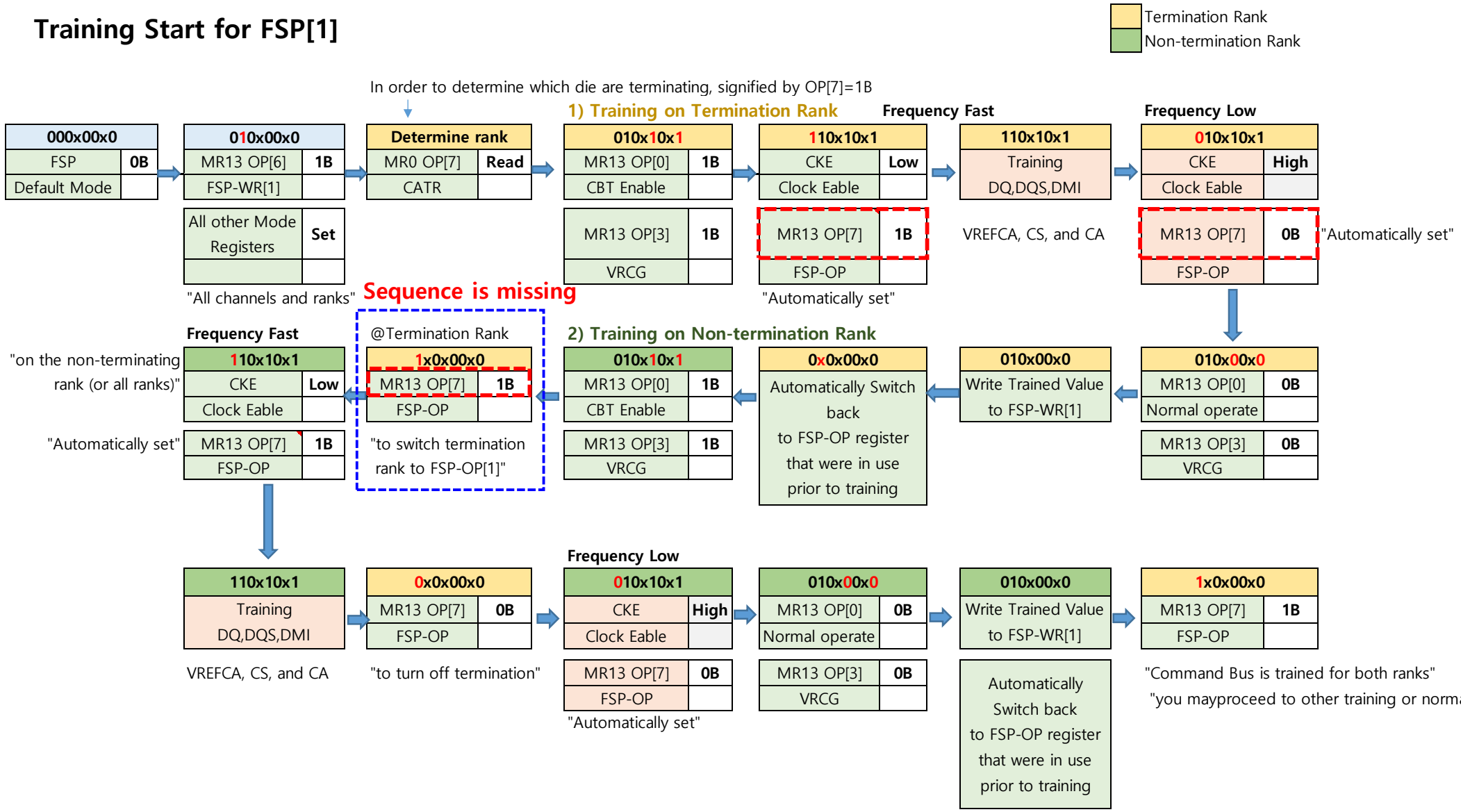
```
--->>> LPDDR4 Initialization is in progress ... <<<---
j721e_lpddr4_ack_freq_upd_req: received freq change req: req type = 1, req no. = 0
j721e_lpddr4_ack_freq_upd_req: received freq change req: req type = 0, req no. = 1
j721e_lpddr4_ack_freq_upd_req: received freq change req: req type = 1, req no. = 2
j721e_lpddr4_ack_freq_upd_req: received freq change req: req type = 0, req no. = 3
j721e_lpddr4_ack_freq_upd_req: received freq change req: req type = 1, req no. = 4
wait_for_bit_le32: Timeout (reg=114080 mask=80 wait_set=)
Timeout during frequency handshake
### ERROR ### Please RESET the board ###
```

Other DRAM Vendor

Log

```
j721e_lpddr4_ack_freq_upd_req: received freq change req: req type = 1, req no. = 0
j721e_lpddr4_ack_freq_upd_req: received freq change req: req type = 0, req no. = 1
j721e_lpddr4_ack_freq_upd_req: received freq change req: req type = 1, req no. = 2
j721e_lpddr4_ack_freq_upd_req: received freq change req: req type = 0, req no. = 3
j721e_lpddr4_ack_freq_upd_req: received freq change req: req type = 1, req no. = 4
j721e_lpddr4_ack_freq_upd_req: received freq change req: req type = 2, req no. = 5
j721e_lpddr4_ack_freq_upd_req: received freq change req: req type = 1, req no. = 6
j721e_lpddr4_ack_freq_upd_req: received freq change req: req type = 2, req no. = 7
j721e_lpddr4_ack_freq_upd_req: received freq change req: req type = 1, req no. = 8
j721e_lpddr4_ack_freq_upd_req: received freq change req: req type = 2, req no. = 9
LPDDR4_Start: PASS
```

<Appendix> CBT Sequence Analysis



<Appendix> JEDEC Spec for LP4 CBT Sequence

4.28.1.2 Training Sequence for multi-rank systems

Note that the example shown here assumes an initial low-frequency operating point, training a high frequency operating point. The green text is low-frequency, magenta text is high-frequency. Any operating
point may be trained from any known good operating point.

1. Set MR13 OP[6]=1B to enable writing to Frequency Set Point 'y' (FSP-WR[y]) (or FSP-WR[x], See Note).
2. Write FSP-WR[y] (or FSP-WR[x]) registers for all channels and ranks to set up high frequency operating parameters.
3. Read MR0 OP[7] on all channels and ranks to determine which die are terminating, signified by MR0 OP[7]=1B.
4. Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode on the terminating rank.
5. Drive CKE LOW on the terminating rank (or all ranks), and change CK frequency to the high frequency operating point.
6. Perform Command Bus Training on the terminating rank (VREFCA, CS, and CA).
7. Exit training by driving CKE HIGH, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands to write the trained values to FSP-WR[y] (or FSP-WR[x]). When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e. trained values are not retained by the SDRAM).
8. Issue MRW-1 and MRW-2 command to enter training mode on the non-terminating rank (but keep CKE HIGH)
9. **Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the high frequency operating point.**
10. Drive CKE LOW on the non-terminating (or all) ranks. The non-terminating rank(s) will now be using FSP-OP[y] (or FSP-OP[x]).
11. Perform Command Bus Training on the non-terminating rank (VREFCA, CS, and CA).
12. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[x] (or FSP-OP[y]) to turn off termination.
13. Exit training by driving CKE HIGH on the non-terminating rank, change CK frequency to the low frequency operating point, and issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e.
trained values are not retained by the SDRAM).
14. Write the trained values to FSP-WR[y] (or FSP-WR[x]) by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
15. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the high frequency operating point. At this point the Command Bus is trained for both ranks and you may proceed to other training or normal operation.

<Appendix> TI's Guide for unterm issue

1. CA ODT / DQ ODT Enable @ Frequency Set 0

1) CA ODT : RZQ/5
2) DQ ODT : RZQ/6

From: Scholz, Kevin
Sent: Tuesday, October 19, 2021 6:47 PM
To: jinho21.jang@samsung.com
Cc: jace.jung@samsung.com; Kenneth Kang Wang <ken.wang@samsung.com>; hj0601.choi@samsung.com; by.oh@samsung.com; junho12.lim@samsung.com; jylove.jeong@samsung.com; sh98.kim@samsung.com; sungoh.huh@samsung.com; dhee029.kim@samsung.com; sj47.kim@samsung.com; dongminkim@samsung.com; Scholz, Kevin <k-scholz@ti.com>
Subject: RE: RE: RE: RE:(6) (Reminder)(Inquiries) [EXTERNAL] TI Validation with Samsung part

Hi Jinho,

Looking at this more, have you already tried enabling termination in F0 of the XLS tool (set the cells boxed in red below to "RZQ/5" and "RZQ/6" respectively)? If I understand the issue correctly, I think this ***may*** (not certain) help resolve the issue / enable termination during rank 1 CBT.

B) DRAM IO Configuration

Parameter Group	Parameter	Frequency Set 0	Frequency Set 1	Frequency Set 2	Units	Notes
VREF Control	DQ VREF Range	Range 0	Range 0	Range 0	-	2
	DQ VREF	10	16	16	% of VDDQ	2
	CA VREF Range	Range 0	Range 0	Range 0	-	2
	CA VREF	10	25.6	25.6	% of VDDQ	2
Drive Strength	Pull-Down (PDDS)	RZQ/6	RZQ/6	RZQ/6	Ohms	2, 3
	Pull Up Calibration	VDDQ / 3	VDDQ / 3	VDDQ / 3	-	2
Termination	CA ODT Disable	ODT_CA Bond Pad	ODT_CA Bond Pad	ODT_CA Bond Pad	-	2
	CK ODT Override	Disable	Disable	Disable	-	2
	CS ODT Override	Enable	Enable	Enable	-	2
	CA ODT	Disable	RZQ/5	RZQ/5	Ohms	2, 3
	DQ ODT	Disable	RZQ/6	RZQ/6	Ohms	2, 3
	SOC ODT	RZQ/6	RZQ/6	RZQ/6	Ohms	1, 2, 3

NOTES:
1) This parameter should be set to match the ODT setting configured under "Processor / DDR Controller IO Configuration".
2) Default settings are recommended.

Title-README | Config | DRAMTiming | IOControl | R-Boot | GEL | RTOS | CMM | Revision